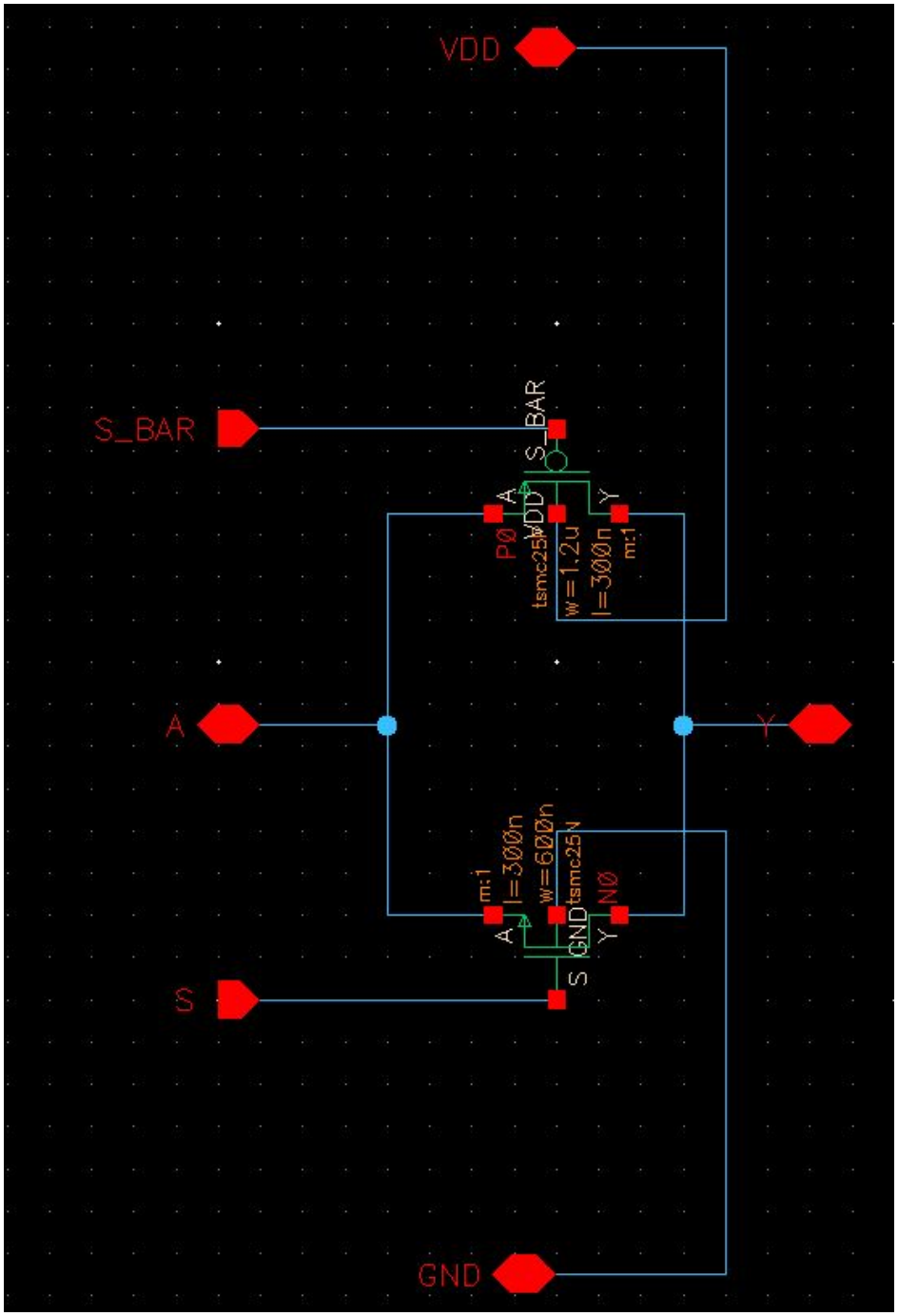
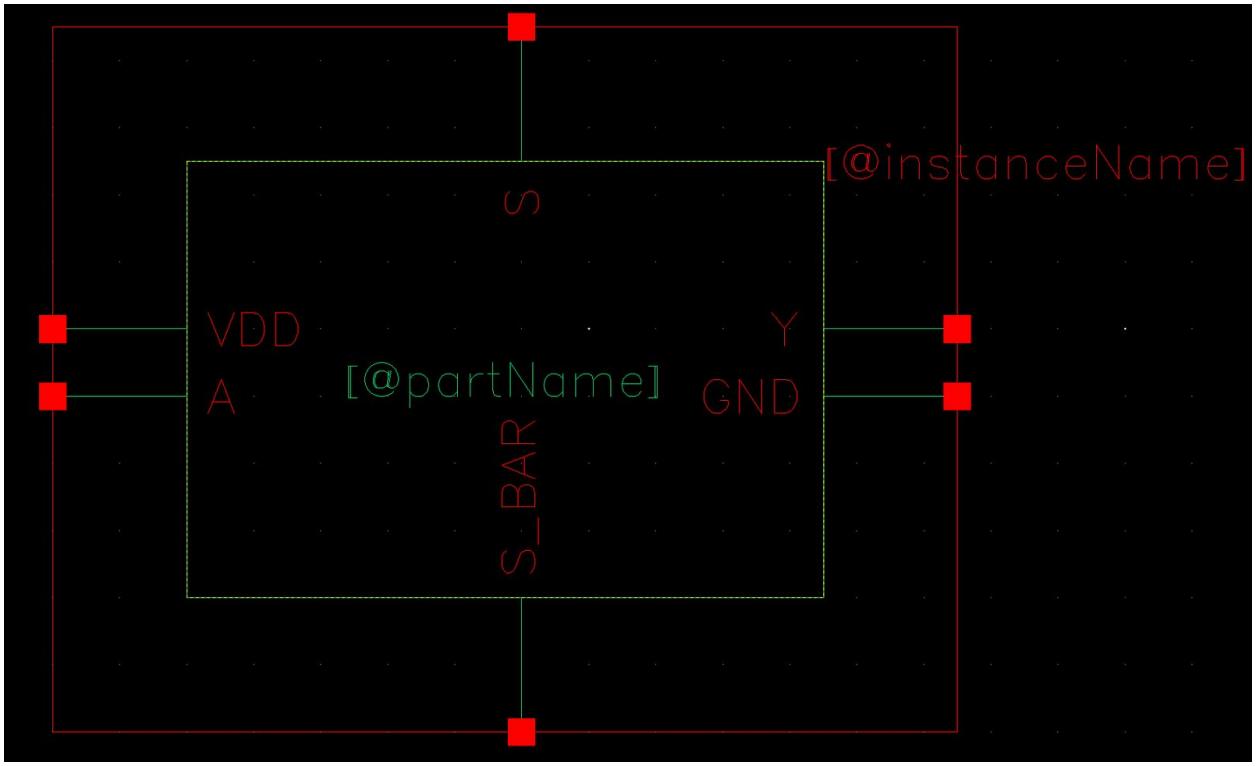
Raphaelle Marcial
Lab 3
RUID: [redacted]

Transmission Gate
Schematic

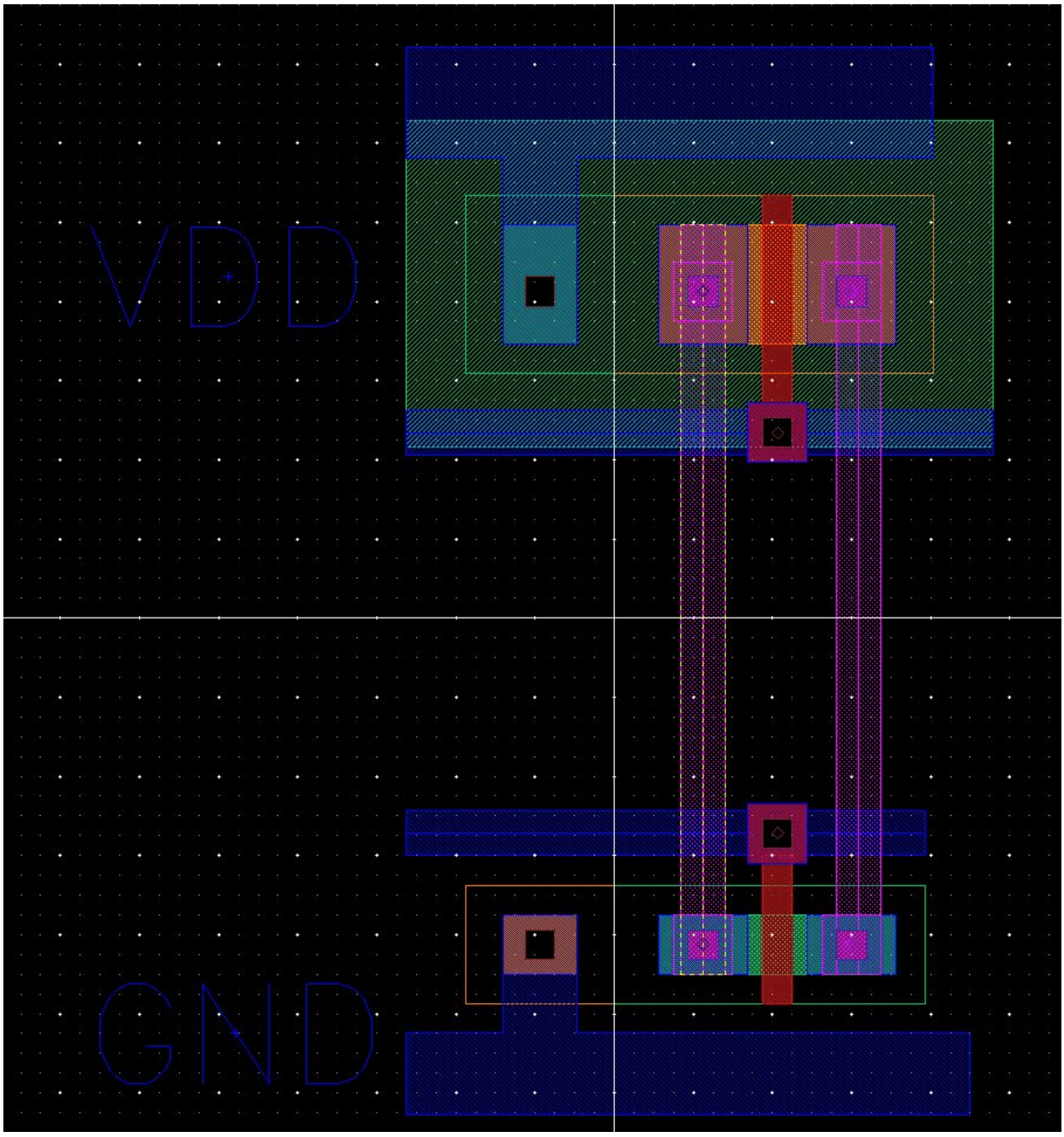


nMOS width = 600nM, pMOS width = 1.2 uM

Symbol

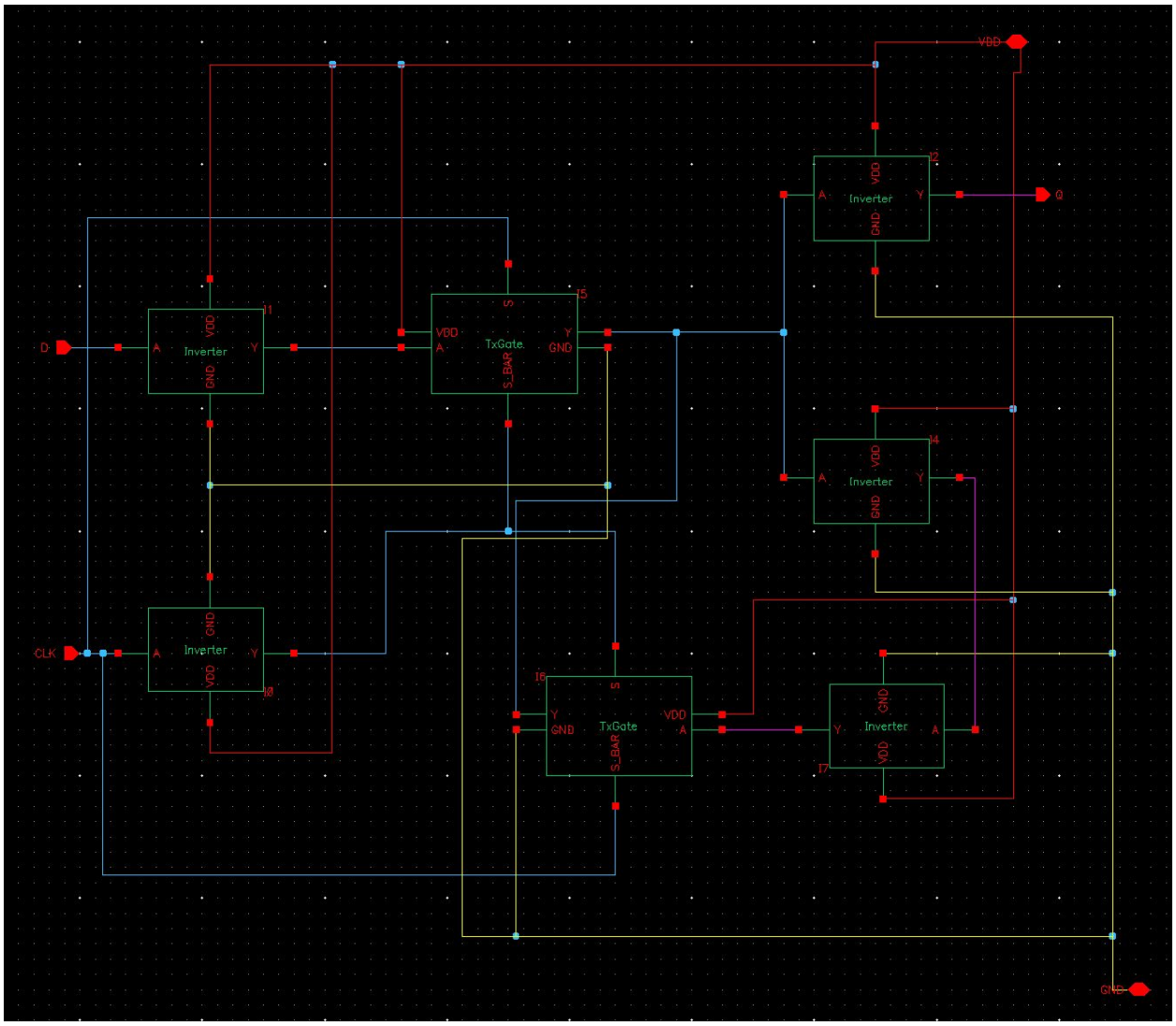


Layout

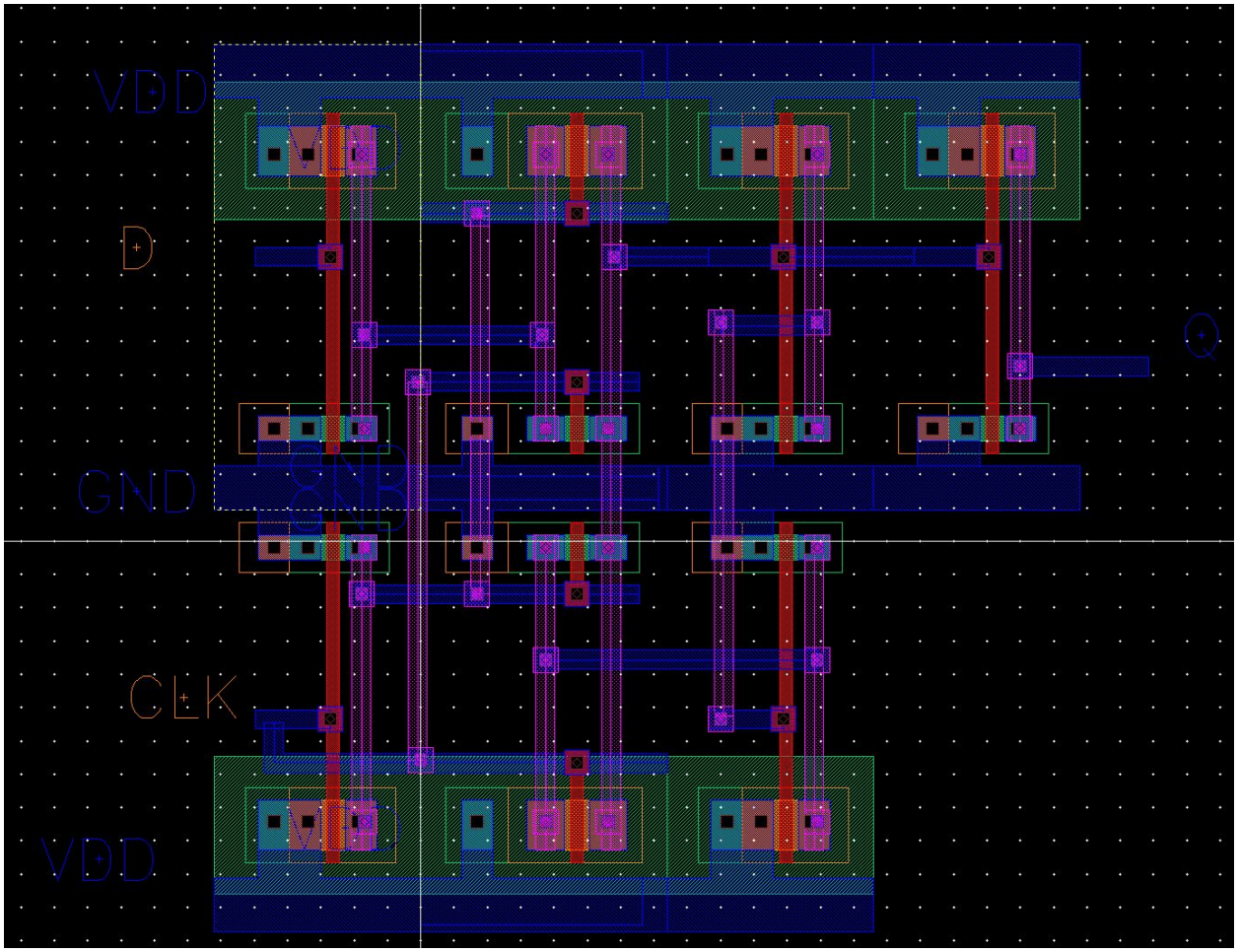


D-Latch

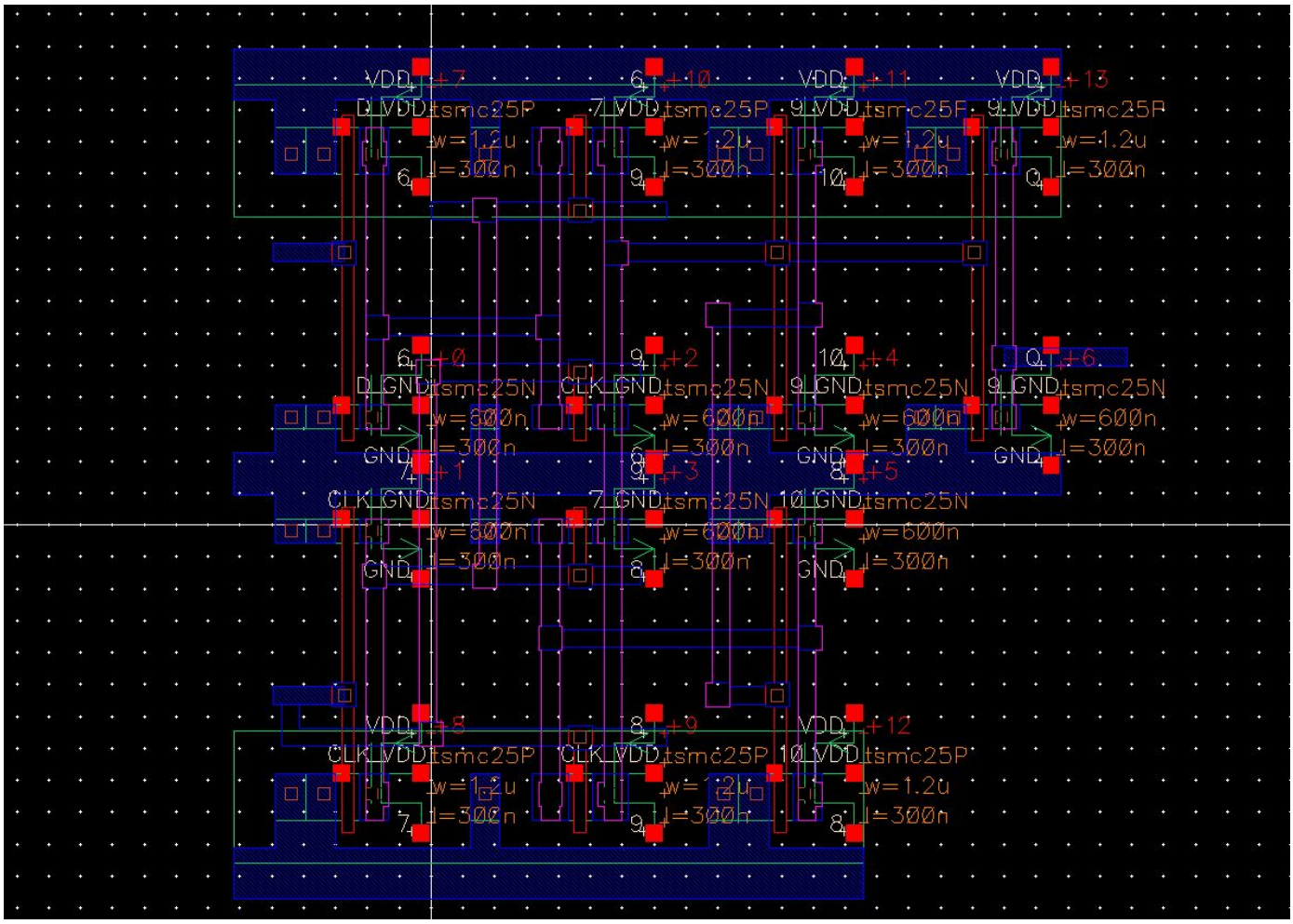
Schematic



Layout



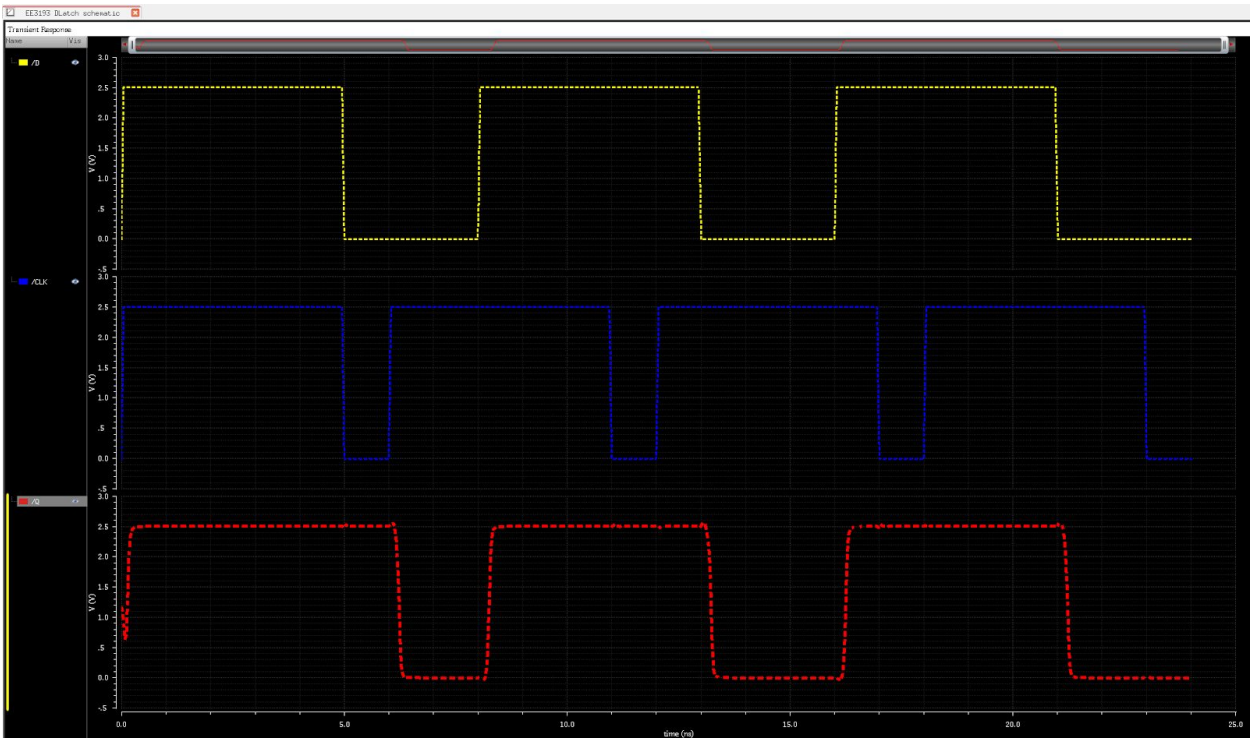
Extracted


VDD
D_VDD tsmc25P
w=1.2u
l=300n
CLK_VDD tsmc25P
GND
D_GND tsmc25N
CLK_GND tsmc25N
9_GND tsmc25N
Q_GND tsmc25N
w=600n
l=300n

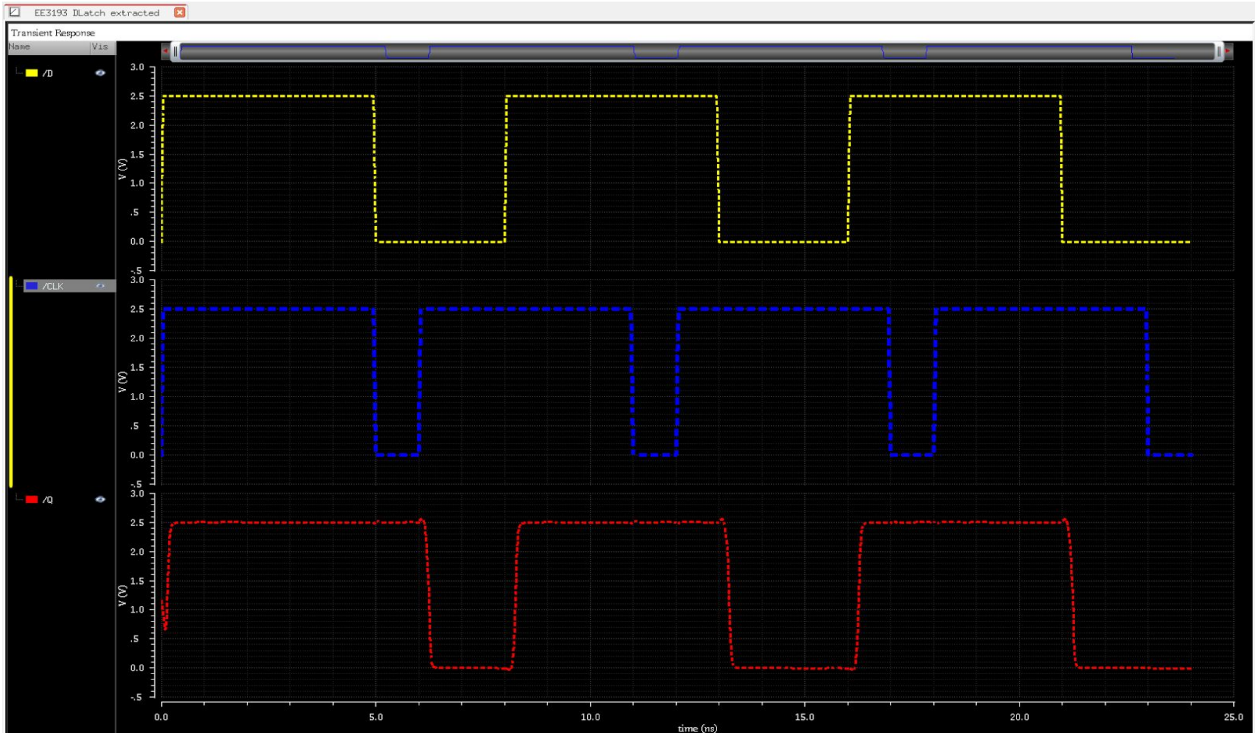
D-Latch

Clk_{period} = 6ns D_{period} = 8ns Rise/Fall = 50ps Pulse Width = 4.9ns Legend: D Clk Q

Schematic Simulation: 24ns



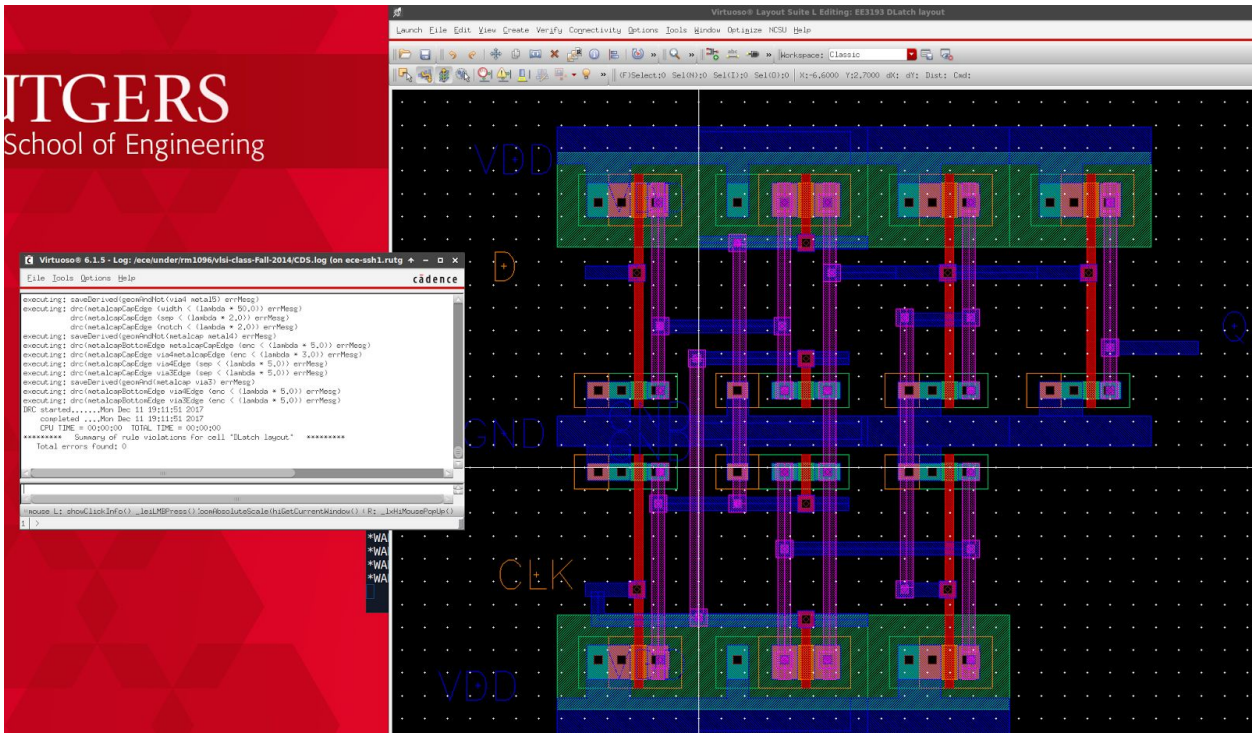
Extracted Simulation: 24ns



The simulation results are basically mirror images of each other (as they should be).

Verification

DRC



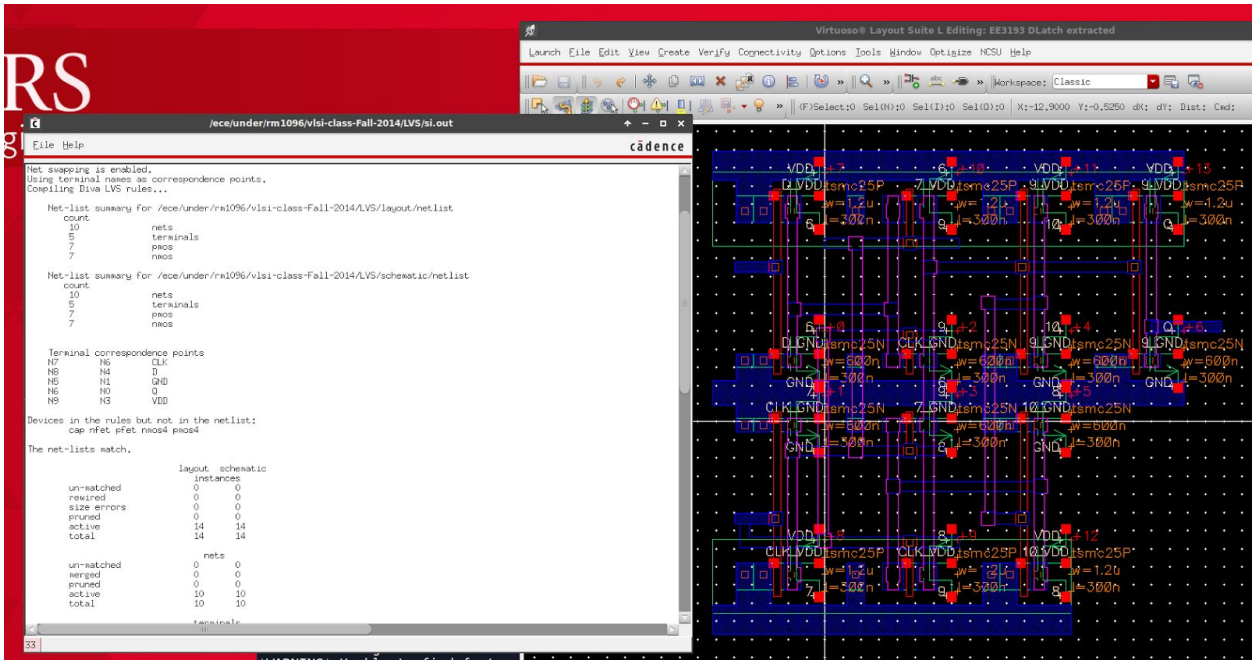
Virtuoso® 6.1.5 - Log: /ece/under/rm1096/vlsi-class-Fall-2014/CDS.log (on ece-ssh1.rutg

File Tools Options Help cadence

```
executing: drc(metalcapCapEdge (width < (lambda * 50.0)) errMesg)
           drc(metalcapCapEdge (sep < (lambda * 2.0)) errMesg)
           drc(metalcapCapEdge (notch < (lambda * 2.0)) errMesg)
executing: saveDerived(geomAndNot(metalcap metal4) errMesg)
executing: drc(metalcapBottomEdge metalcapCapEdge (enc < (lambda * 5.0)) errMesg)
executing: drc(metalcapCapEdge via4metalcapEdge (enc < (lambda * 3.0)) errMesg)
executing: drc(metalcapCapEdge via4Edge (sep < (lambda * 5.0)) errMesg)
executing: drc(metalcapCapEdge via3Edge (sep < (lambda * 5.0)) errMesg)
executing: saveDerived(geomAnd(metalcap via3) errMesg)
executing: drc(metalcapBottomEdge via4Edge (enc < (lambda * 5.0)) errMesg)
executing: drc(metalcapBottomEdge via3Edge (enc < (lambda * 5.0)) errMesg)
DRC started.......Mon Dec 11 19:55:52 2017
    completed ....Mon Dec 11 19:55:52 2017
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
**********   Summary of rule violations for cell "DLatch layout"   **********
   Total errors found: 0

Getting layout propert bag
```

LVS



/ece/under/rm1096/vlsi-class-Fall-2014/LVS/si.out

File Help cadence

```
@(#)$CDS: LVS version 6.1.5 11/28/2011 22:18 (sjfd1238) $

Command line: /ece/vlsitools/cadence/6.15.508/tools.lnx86/dfII/bin/32bit/LVS -dir /ece/under/rm1096/vlsi-class-Fall-2014/LVS
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /ece/under/rm1096/vlsi-class-Fall-2014/LVS/layout/netlist
       count
         10              nets
         5               terminals
         7               pmos
         7               nmos

    Net-list summary for /ece/under/rm1096/vlsi-class-Fall-2014/LVS/schematic/netlist
       count
         10              nets
         5               terminals
         7               pmos
         7               nmos


    Terminal correspondence points
    N7          N6          CLK
    N8          N4          D
    N5          N1          GND
    N6          N0          Q
    N9          N3          VDD

Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                              layout  schematic
                                 instances
        un-matched               0       0
        rewired                  0       0
        size errors              0       0
        pruned                   0       0
        active                   14      14
        total                    14      14

                                   nets
        un-matched               0       0
        merged                   0       0
        pruned                   0       0
        active                   10      10
        total                    10      10

                                 terminals
        un-matched               0       0
        matched but
        different type           0       0
        total                    5       5
```