Heaven's Light is Our Guide
Rajshahi University of Engineering & Technology
B.Sc. Engineering 3rd Year 6th Semester Examination, 2015

Department of Computer Science & Engineering
Course No. CSE 607   Course Title: Peripherals & Interfacings
Full Marks: 70   Time: THREE (03) hours

N.B:
Answer SIX questions taking THREE from each section.
The questions are of equal value.
Use separate answer script for each section.

SECTION A

		Marks
Q.1(a)	Describe the operation performed by the instruction OUT(47h)AL.	02
(b)	How is 8255A PPI configured if its control register contains 9Bh?	03½
(c)	For higher speed data transfer, why is simple strobe I/O data transfer not used?	02
(d)	What is the purpose of TEST pin on 8086 microprocessor? Write the differences between 8086 and 8088 microprocessor.	04
Q.2(a)	Why does 8086 need two memory banks? Explain with example.	03
(b)	Draw a circuit that uses 2732 EPROMs for a 16K x 8 section of memory in an 8086 microprocessor based system using 74LS138 decoder.	04½
(c)	Write down the bit format for sending asynchronous serial data.	02
(d)	What is the meaning of the statement "The 8251A USART is double-buffered"?	02
Q.3(a)	A 74LS138 decoder has its three SELECT inputs, connected to A_{11}, A_{12}, A_{13} of the system address bus. It has $\overline{G2B}$ connected to A_{14}, $\overline{G2A}$ connected to ground and G1 connected to A_{15}. Use an address decoder worksheet to determine, what eight 1KB RAMs address blocks the decoder output will select? Also determine, what address ranges will the block-2/RAM1 select?	06
(b)	Describe the purposes of address decoding in micro-computer system.	02½
(c)	Describe the response that an 8259A will make if it receives an interrupt signal on its IR1 and IR2 inputs at the same time.	03
Q.4(a)	Is it possible to select PORT C as an input port and output port at the same time using the command byte of the command register in the 82C55 PPI? Briefly explain.	04
(b)	How many 8259A are required to have 25 interrupt inputs? Why?	02
(c)	Find out the bit sequence of command byte A for the following arrangement: port A input, port B output and port C input.	03
(d)	Distinguish between transducer and actuator.	02½

SECTION B

Q.5(a)	What is the advantage of a smaller resolution?	02
(b)	Draw the basic R/2R ladder DAC and prove that $V_{OUT} = (-V_{REF}/16) \times B$, where B is the value of binary input.	04
(c)	Why does conversion time increase with the value of analog input voltage?	02
(d)	Write down the working principle of counter type ADC.	03½
Q.6(a)	A certain memory has a capacity of 32K x 16. Calculate (i) How many bits are in each word? (ii) How many words are being stored? and (iii) How many memory cells does this memory contain?	03
(b)	Design Mask-Programmed ROM to store the function $y = x^3 + 5$, where input address supplies the value for x and the value of the output data is y.	04½
(c)	Draw the timing diagram of write cycle for static RAM.	02
(d)	What do you mean by quantization error?	02
Q.7(a)	Why does DRAM need refresh operation?	02½
(b)	A static RAM iC has a capacity of 16 x 4, one active low chip select input and common data input and output line. Now show how to combine several RAM ICs to form a 16 x 16 module.	05
(c)	Write down the differences between PROM, PAL and PLA. What is programming or burning in a ROM?	04
Q.8(a)	Draw the simplified architecture of a 32 x 4 RAM. Also draw a structure of a MROM which can be used to store the function, $y = 2x^2$.	07
(b)	Explain and draw the block diagram of 8251A USART.	04½

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Rajshahi University of Engineering & Technology
B.Sc. Engineering 3rd Year Even Semester Examination, 2016
Department of Computer Science & Engineering
Course No. CSE 3207   Course Title: **Peripherals & Interfacings**
Full Marks: 72   Time: THREE (03) hours

N.B:

Answer **SIX** questions taking **THREE** from each section.
The questions are of equal value.
Use separate answer script for each section.

SECTION A

		Marks
Q.1(a)	If you want to transfer data between I/O and microprocessor using IN, INS, OUT, OUTS instructions, then which interfacing technique will you choose and why?	03
(b)	Is it possible to access 32-bit I/O port using 8-bit I/O ports?	02
(c)	Many I/O devices accept or release information at a much slower rate than the microprocessor. How can you synchronize these I/O devices with microprocessor? Explain with example.	04
(d)	Can 82C55 interface any TTL-compatible I/O device to the microprocessor? How many ports are there in 82C55? What are the purposes of these ports?	03
Q.2(a)	What do you mean by programmable peripheral device? Why are the port lines of programmable port devices automatically put in the input mode when the device is first powered up or reset?	04
(b)	In mode 2 operation of 8255A which pins are used as input pin and output pin?	02
(c)	Write down the Mode-Set control word format for 8255A.	04
(d)	Write the instruction to send the control word 8Eh. Explain.	02
Q.3(a)	Explain why is a modem required to send digital data over standard switched phone lines?	04
(b)	What logic levels on BHE and A_0 is required to write a word to address 04300H?	02
(c)	Draw the block diagram of 8086 memory banks.	03
(d)	Explain the working of a hand shake input port and output port.	03
Q.4(a)	Draw a circuit that uses 2764 EPROMs for a 64k x 8 section of memory in an 8086 microprocessor system using 74LS138 decoder.	04
(b)	What are functions of A_0, A_1, and GATE input in 8254 programmable timer?	03
(c)	How does the main processor distinguish its instruction from those for 8087 as it fetches instruction from memory?	02
(d)	Convert the decimal number 178.25 to 8087 short real data format.	03

SECTION B

Q.5(a)	What is resolution of a five-bit D/A converter that produces $V_{out} = 0.2V$ for a digital input of 00001? Describe the staircase signal out of this DAC.	03
(b)	Describe the operation of a DAC using an OP-AMP summing amplifier with binary weighted registers.	04
(c)	Write down the application of DAC in signal reconstruction.	02
(d)	What is the problem of using a high-resolution DAC that has large difference in registor values between the LSB and MSB? What is the solution of this problem?	03
Q.6(a)	Draw the architecture of a 32 x 8 ROM.	04
(b)	What is mask-program ROM? MROMs can be used to store tables of mathematical function. Show how MROM can be used to store the function, $y = x^2+3$, where the input address supplies the value for x and the value of the output data is y.	05
(c)	Draw the architecture of PAL for the following functions: $O_0 = A + B\bar{D} + C\bar{D}$ $O_1 = AB\bar{C}\bar{D} + \bar{A}\bar{B}CD$ $O_2 = A\bar{B}C$ $O_3 = AB + \bar{C}\bar{D}$	03
Q.7(a)	How many 8259As are required to have 64 interrupt inputs and why?	03
(b)	Assume that IR inputs in 8259A are in fixed priority. If it receives interrupt signal on IR2 and IR4 inputs at the same time, then how will it response?	03
(c)	How can you configure 8255A PPI if its control register contains 8Ch? Explain with necessary figure.	04
(d)	What is the purpose of using in-service register in 8259A?	02
Q.8(a)	What is DMA operation? Write the advantages and applications of DMA operation.	03
(b)	How can you interface a 4 x 4 keyboard with 8086 microprocessor using 8255A PPI? Explain with necessary diagram and assembly instructions.	05
(c)	Write the differences between synchronous and asynchronous data communication.	02
(d)	How can you perform interfacing through memory mapped I/O technique? Write with example.	02

RAJSHAHI UNIVERSITY OF ENGINEERING & TECHNOLOGY
DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING
3rd Year Even Semester Examination 2017
COURSE NO: CSE 3207   COURSE TITLE: Peripherals and Interfacing
FULL MARKS: 72   TIME: 3 HRS

N.B.   (i) Answer any SIX questions taking any THREE from each section.
        (ii) Figures in the right margin indicate full marks.
        (iii) Use separate answer script for each section.

SECTION : A

Q.1.   (a) State any three features of intel 8086 microprocessor. What is the main difference   4
             between the 8086 and 8088 microprocessor?

        (b) In isolated I/O methods different memory location is used for I/O address space,   3
             why?

        (c) Draw control word format for Bit set/reset for 8255A IC. Describe it briefly.   5

Q.2.   (a) Describe the 8088/86 hardware interrupt pins   3

        (b) List and describe in general terms the steps an 8086 will take when it responds to an   3
             interrupt.

        (c) Show only memory map for the 8085 microprocessor such that it should contain 8k   4
             byte of EPROM and 8k byte of RAM.

        (d) Why we use 8259A with 8086 microprocessor?   2

Q.3.   (a) Outline the major difference between isolated and memory mapped I/O techniques.   4

        (b) What two methods are used to select the memory in 8086 microprocessor? What is   4
             the purpose of $\overline{BHE}$ and A_0 pins in 8086?

        (c) How can you configure 8255A PPI if its control register contains 90h? Explain with   4
             necessary figure.

Q.4.   (a) What are the differences between synchronous and asynchronous data transmission?   7
             Which device is used to do either synchronous or asynchronous communication?
             Explain with block diagram.

        (b) Why is DMA data transfer faster than doing the same data transfer with program   5
             instructions? Describe the series of action that a DMA controller will perform after it
             peripheral device to memory data transfer.

Q.4. (a) What are the differences between synchronous and asynchronous data transmission? Which device is used to do either synchronous or asynchronous communication? Explain with block diagram.   7

(b) Why is DMA data transfer faster than doing the same data transfer with program instructions? Describe the series of action that a DMA controller will perform after it receives a request from peripheral device to memory data transfer.   5

SECTION - B

Q.5. (a) What is the advantage of a smaller or finer resolution? An eight-bit DAC has an output of 3.92 mA for an input of 01100010. What are the DAC's resolution and full scale output?   5

(b) What is the advantage of R/2R ladder DACs over those that use binary weighted registers?   2

(c) Why does conversion time increase with the value of analog input voltage in digital ramp ADC? What is quantization error?   5

Q.6. (a) Address decoding is needed for a 4k byte memory. This memory is built from 256×8 chips.   6
   i) How many 256×8 RAM chips are needed?
   ii) What size decoder is needed to fully address all 4k of memory?
   iii) Assuming the least significant address bit is A_0, which address lines must be connected to the select lines on the decoder?

(b) A RAM chip has a capacity of 1024 words of 8 bits each (1k×8). Draw the circuit diagram to construct a 16k×16 RAM from 1k×8 RAM in where 2×4 decoder are available with enable line.   4

(c) What are the differences between PAL and PLA?   2

Q.7. (a) What are the advantages and disadvantages of DRAM compared with SRAM? Which one would you expect to find on the main memory modules of your PC?   5

(b) What would you need to expand the memory of 8k×8 to 32k×8? Describe what address lines are used.   4

(c) What is the problem of using a high resolution DAC that has large difference in register values between the LSB and MSB? What is the solution of this problem?   3

Q.8. (a) Which group of pin is used during bidirectional operation of the 82C55?   2

(b) Explain the term handshaking as it applies to computer I/O systems.   3

(c) A 74LS138 decoder has it's three SELECT inputs connected to three address pins of the system address bus. It has $\overline{G2A}$ connected to A_{15}, $\overline{G2B}$ connected to $\overline{RD}$ and G_1 6

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3rd Year Even Semester Examination 2018
COURSE NO: CSE 3207   COURSE TITLE: Peripherals and Interfacing
FULL MARKS: 72   TIME: 3 HRS

N.B. (i) Answer any SIX questions taking any THREE from each section.
(ii) Figures in the right margin indicate full marks.
(iii) Use separate answer script for each section.

SECTION : A

Q.1. (a) What is port? What are the differences between fixed port addressing and variable port addressing? — 3

(b) Describe the purposes of decoding in microcomputer system. — 2

(c) In isolated I/O method, different memory location is used for I/O address space, why? — 3

(d) Draw the interface diagram of an 8-digit LED display interfaced to the 8088 microprocessor through an 82C55 PPI. — 4

Q.2. (a) Why we use 82C55 with 8086 microprocessor? — 2

(b) Find out the bit sequence of command byte A for the following arrangement: Port A input, Port B output and Port C input. — 3

(c) Draw control word format for bit set/reset for 82C55A IC. Describe briefly. — 3

(d) Draw the timing diagram of 82C55 mode 2 bidirectional operation. — 4

Q.3. (a) Which device is used to handle the multiple interrupts? — 2

(b) With a neat diagram, discuss the operation of the USART 8251. — 6

(c) If an 8259A is already servicing IR_1 interrupt input and in the mean time an interrupt request comes on IR_2 input PIN, how will it response to that interrupt input? — 4

Q.4. (a) What are the differences between 8283 and 8284 timer? — 2

(b) What is the importance of synchronization between microprocessor and peripheral devices? Which method is used for this synchronization? Explain with real life example. — 5

(c) With a neat diagram, show how the 8287 DMA controller can be interfaced in an 8086 based system. — 5

SECTION : B

Q.5. (a) Design a 5-bit DAC uses binary-weighted registors. Assume the MSB resistor is 10KΩ. What is the disadvantage of using binary weighted registor DAC? — 4

(b) What are the advantages of R/2R ladder DACs? Draw the basic R/2R ladder DAC and prove that $V_{ out } = \dfrac{-V_{ ref }}{16} \times B$, where B is the value of binary input. — 4

(c) In the following below figure, the waveform at V_{AX} for a six bit SAC (DAC) with a step size of 40mV during a complete conversion cycle. Examine this waveform and describe what is occurring at time t_0 to t_5. Then determine the resultant digital output. — 4
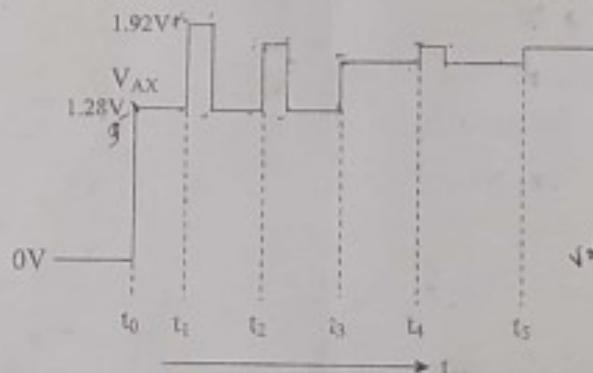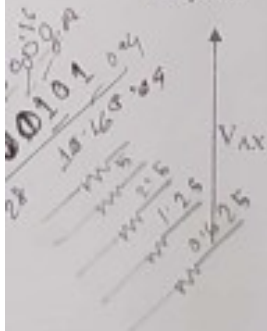
Q.6. (a) What will happen to the operation of a digital ramp ADC if the analog input V_A is greater than the full-scale value? — 2

(b) What will be the conversion time of a 10 bit flash ADC? Explain the operation of a 5-bit SAC for analog input $V_A=20.4V$ with proper steps. — 5

(c) What is multiplexing? Explain the conversion of four analog inputs by multiplexing through one ADC. — 5

Q.7.   (a) How does 8086 microprocessor interrupt the instructions of a math co-processor?   4

      (b) What is addressing mode? Give an example that demonstrates the use of based   4
index addressing mode.

      (c) What is cascaded 8259A? What is the function of CAS_{0p}, CAS1, and CAS_2 for master   4
and slave selection? How many master and slave are required to have 74 interrupts
inputs in 8259A?

Q.8.   (a) Explain why we use co-processor? What are the purposes of NEU of 80×87?   2

      (b) Draw the internal structure of the 80×87 arithmetic co-processor and explain the   4
co-processor status register.

      (c) Why we use 8254 chip? Draw the block diagram of 8254 IC.   4

      (d) Write the modes of operation of 8254 IC.   2