Physical Design Flow

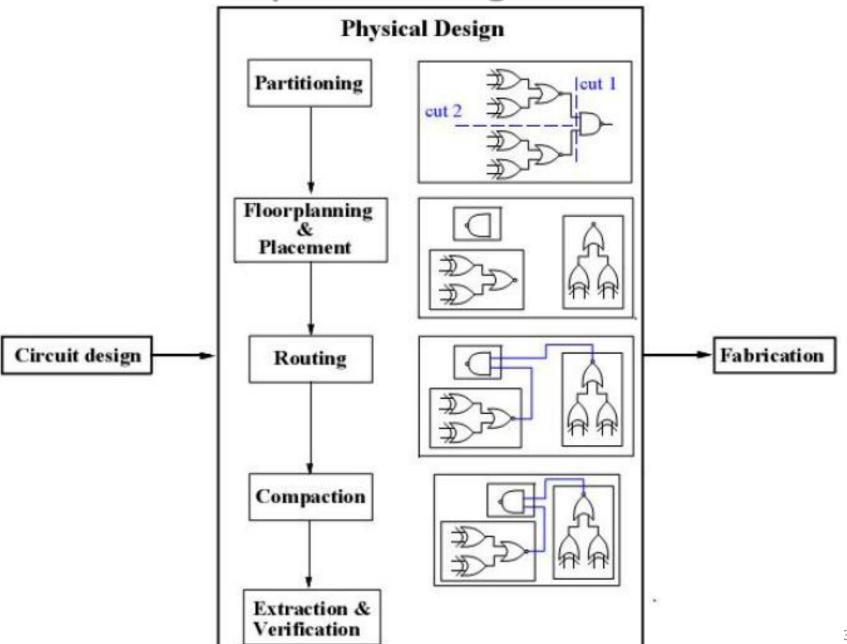
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Physical Design

- Physical design converts a circuit description into a geometric description.
- The description is used to manufacture a chip. also for cost effectiveness
- Physical design cycle:
 - Logic partitioning
 - 2. Floorplanning, placement, and pin assignment
 - Routing (global and detailed)
 - 4. Compaction
 - 5. Extraction and Verification

Physical Design Flow



What is Partitioning?

System Design

- Decomposition of a complex system into smaller subsystems.
- Each subsystem can be designed independently.
- Decomposition scheme has to minimize the interconnections between the subsystems.
- Decomposition is carried out hierarchically until each subsystem is of manageable size.

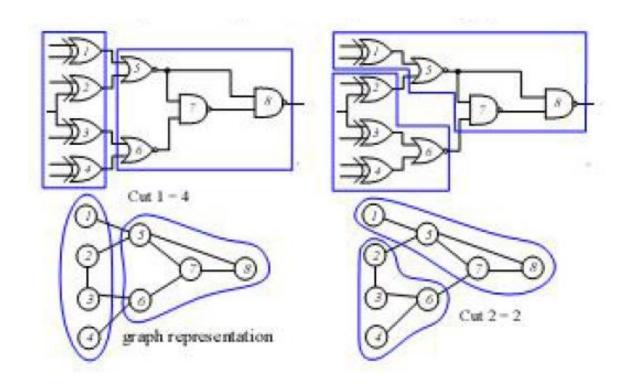
Module 1

Module 2

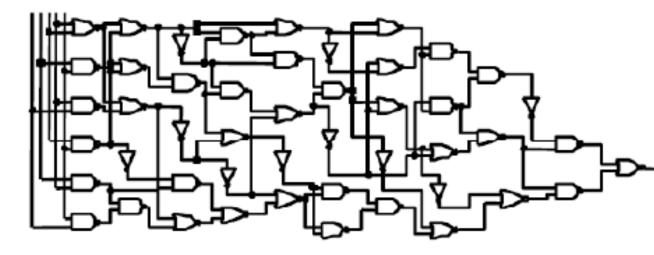
Modulen

Interface Information

- Objective: Partition a circuit into parts such that every component is within a prescribed range and the # of connections (cut size) among the components is minimized.
 - More constraints are possible for some applications.



Input size: 48



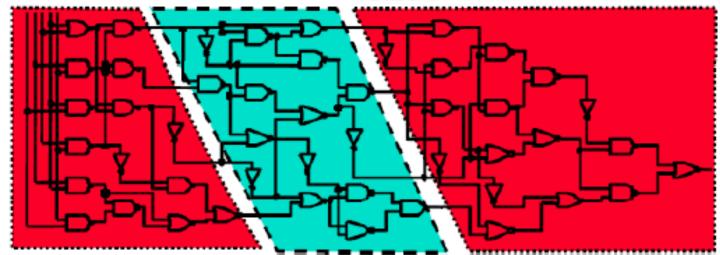
Cut 1=4

Cut 2=4

Size 1=15 Size 2=16

Size 3=17

Courtesy: Andrew Kahng, UCSD



- Partitioning leads to
 - Blocks with well-defined areas and shapes (hard blocks).
 - Blocks with well-defined areas and flexible shapes (soft blocks).
 - A netlist specifying connections between the blocks.

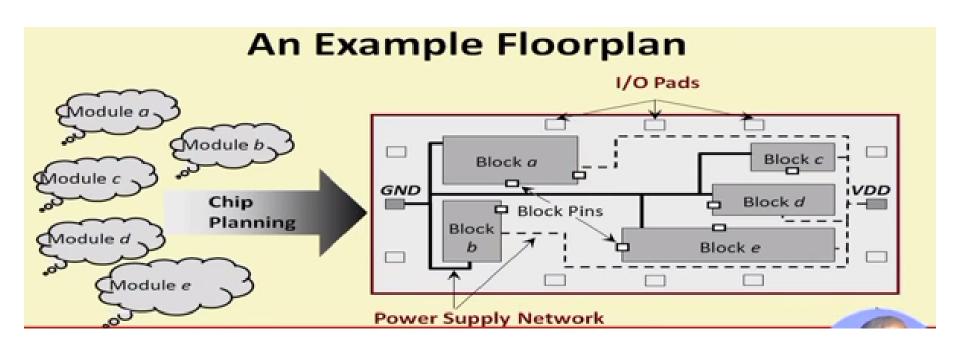
Problem Formulation

- Partition a given netlist into smaller netlists such that:
 - Interconnection between partitions is minimized.
 - Delay due to partitioning is minimized.
 - Number of terminals is less than a predetermined maximum value.
 - The area of each partition remains within specified bounds.
 - The number of partitions also remains within specified bounds.

- Broadly two classes of algorithms:
 - Constructive
 - Random selection
 - Cluster growth
 - Hierarchical clustering
 - Iterative-improvement
 - Min-cut
 - Simulated annealing

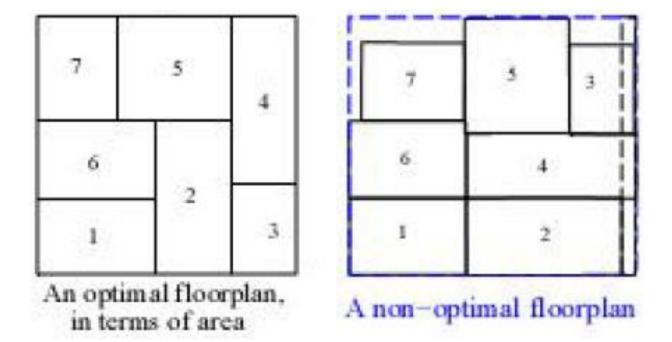
Floor Planning

- Find approximate locations of a set of modules that need to be placed on a layout surface.
 - Available region typically considered rectangular.
 - Modules are also typically rectangular in shape, but there can be exceptions (e.g. L-shaped modules).

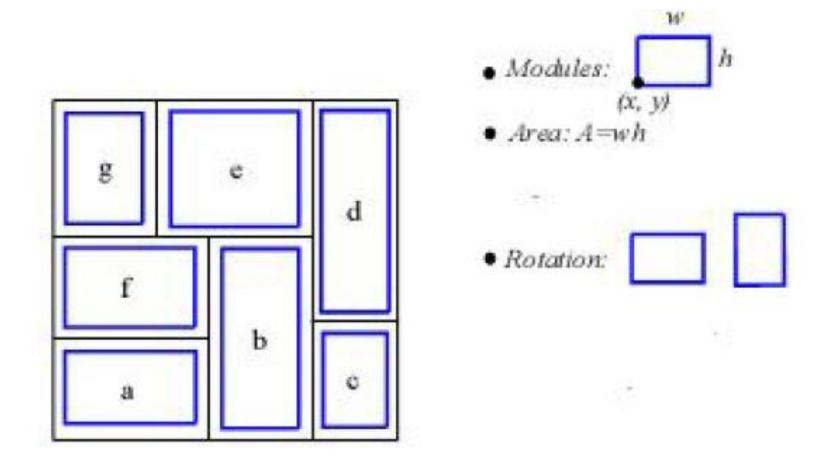


Floor Planning...

- Objectives: Minimize area, reduce wirelength for (critical) nets, and determine shapes of soft blocks, etc.
- Inputs to the floorplanning problem:
 - A set of blocks, hard or soft.
 - Pin locations of hard blocks.
 - A netlist.



Floor Plan Specification

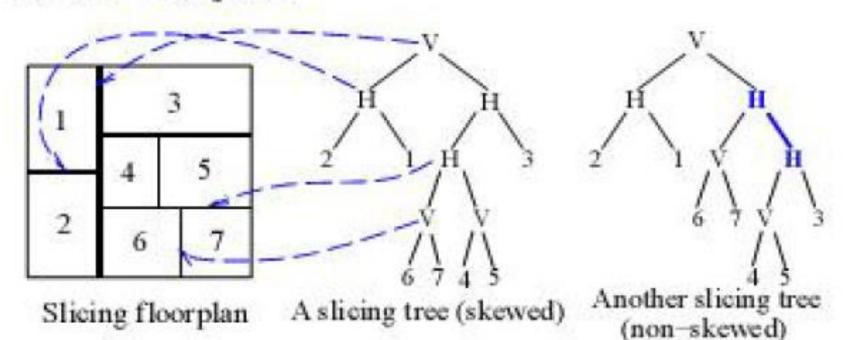


Slicing Structure

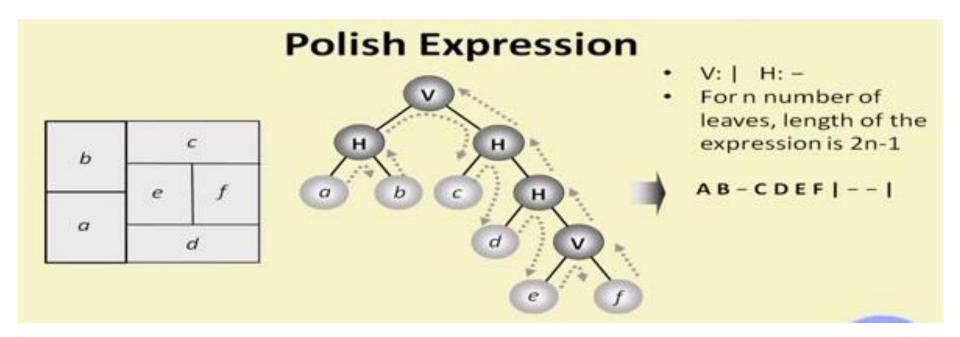
- A rectangular dissection that can be obtained by repeatedly splitting rectangles by horizontal and vertical lines into smaller rectangles.
- Slicing Tree:
 - A binary tree that models a slicing structure.
 - Each node represents a vertical cut line (V), or a horizontal cut line (H).
 - A third kind of node called Wheel (W) appears for non-sliceable floorplans (discussed later).
 - Each leaf is a basic block (rectangle).

Slicing Floor Plan Representation: Slicing Trees

- A slicing floorplan can be represented by a slicing tree.
- Slicing tree: A binary tree, where each internal node represents a vertical cut line or horizontal cut line, and each leaf a basic rectangle.
- Skewed slicing tree: One in which no node and its right child are the same.
- There is a 1-to-1 correspondence between a slicing floorplan and a skewed slicing tree.

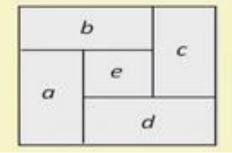


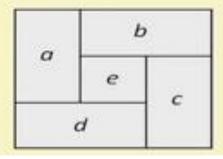
Slicing Floor Plan Representation: Slicing Trees...



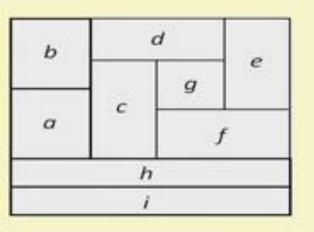
A Non-Slicing Floorplan

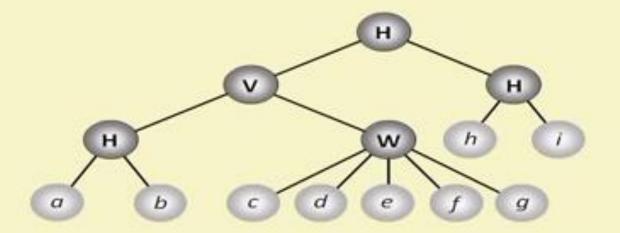
- One that may not be obtained by repetitively subdividing alone.
 - Also called a WHEEL.





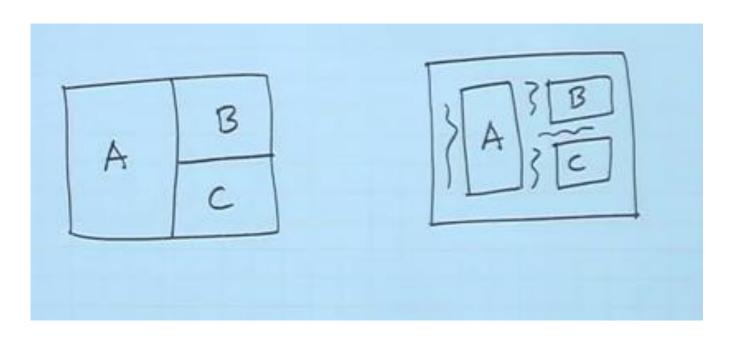
A Hierarchical Floorplan





Floorplanning and Placement: Differences

- The problems are similar in nature.
- Main differences:
 - Floorplanning:- Some of the blocks may be flexible, and the exact locations of the pins are not yet fixed.
 - Placement: All blocks have well-defined geometrical shapes, with defined pin locations. We keep separate space for routing.

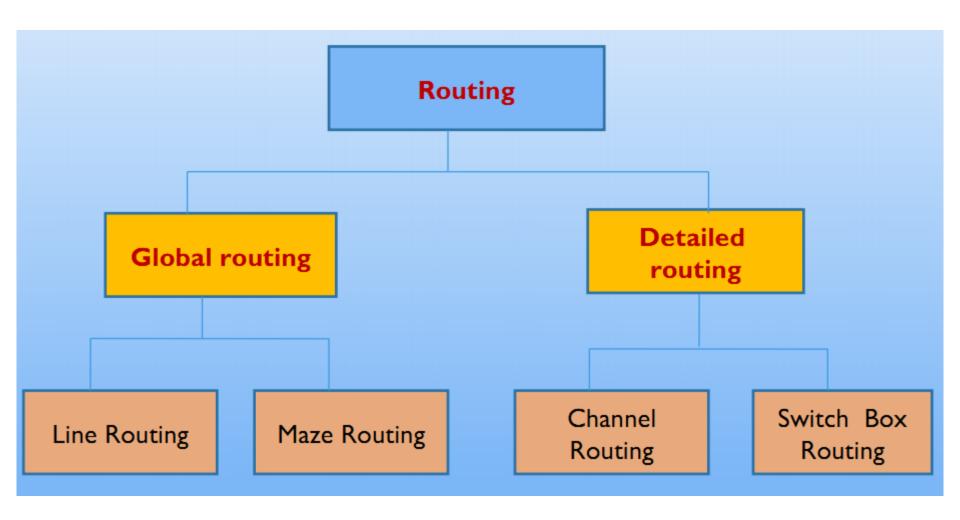


Routing

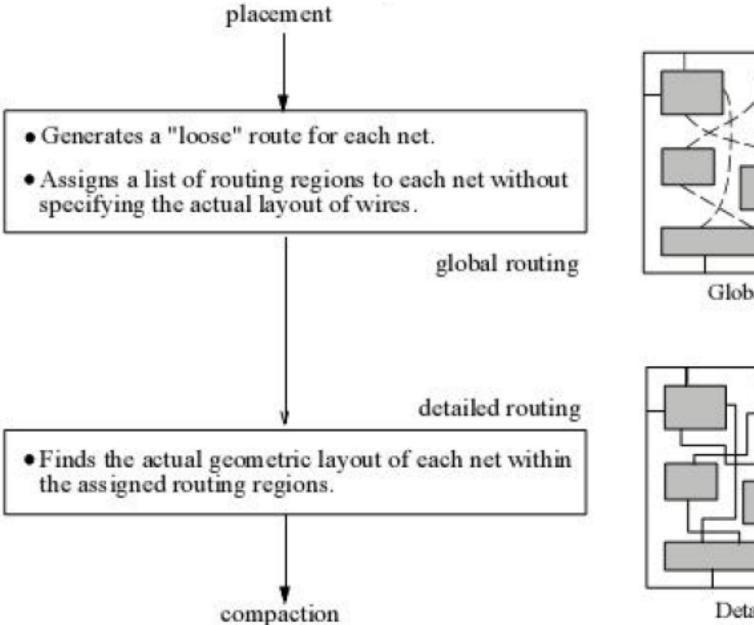
 Routing involves generating metal wires to connect the pins of same signal while obeying manufacturing design rules.

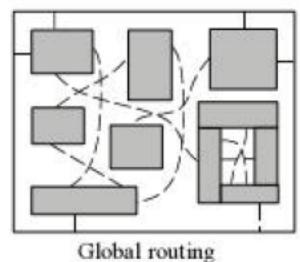
Before routing is performed on the design, cell placement
has to be carried out wherein cells used in the design are
placed.

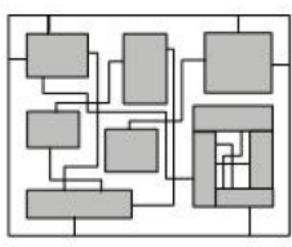
Types of Routing



Types of Routing...







Detailed routing 20

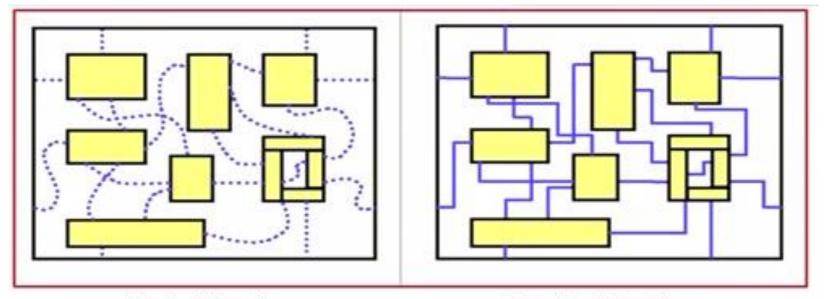
Types of Routing...

Global Routing

- Define the routing regions.
- Generate a tentative route for each net.
- Each net is assigned to a set of routing regions.
- Does not specify the actual layout of wires.

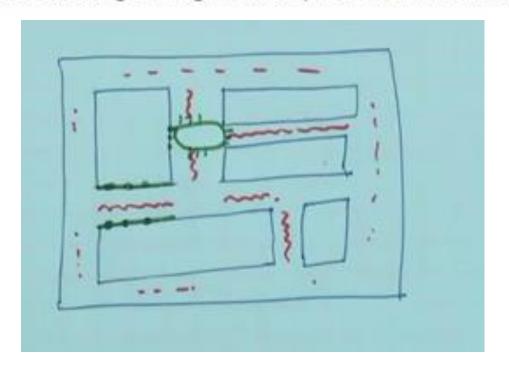
Detailed Routing

- For each routing region, each net passing through that region is assigned particular routing tracks.
- · Actual layout of wires gets fixed (channel routing and switchbox routing).

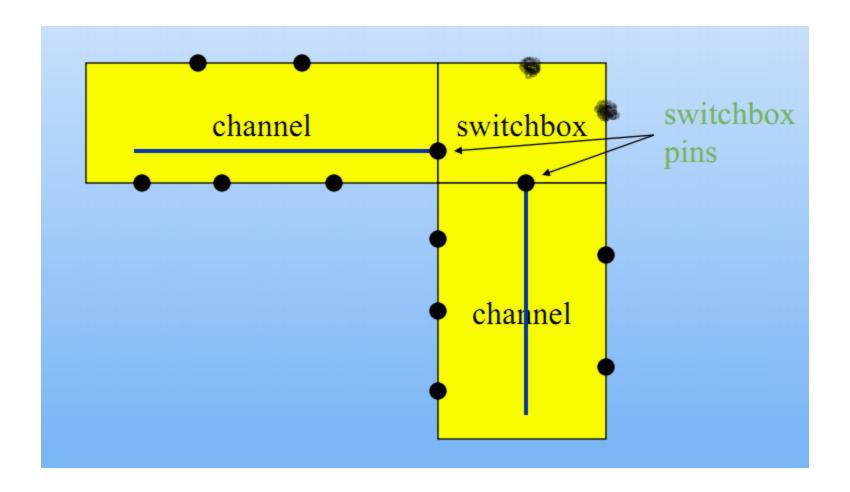


Routing Regions

- Regions through which interconnecting wires are laid out.
- How to define these regions?
 - Partition the routing area into a set of non-intersecting rectangular regions.
 - Types of routing regions:
 - Horizontal channel: parallel to the x-axis with pins at their top and bottom boundaries.
 - Vertical channel: parallel to the y-axis with pins at their left and right boundaries.
 - Switchbox: rectangular regions with pins on all four sides.



Routing Regions...



Routing Regions...

Points to note:

- Identification of routing regions is a crucial first step to global routing.
- Routing regions often do not have pre-fixed capacities.
- The order in which the routing regions are considered during detailed routing plays a vital part in determining overall routing quality.

Types of Channel Junctions

Three types of channel junctions may occur:

L-type:

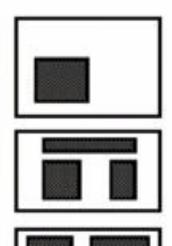
- Occurs at the corners of the layout surface.
- Ordering is not important during detailed routing.
- Can be routed using channel routers.

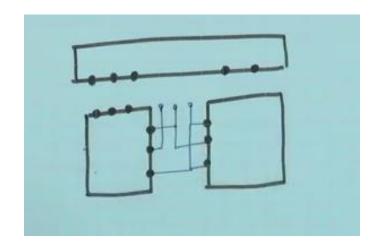
T-type:

- · The leg of the "T" must be routed before the shoulder.
- · Can be routed using channel routers.

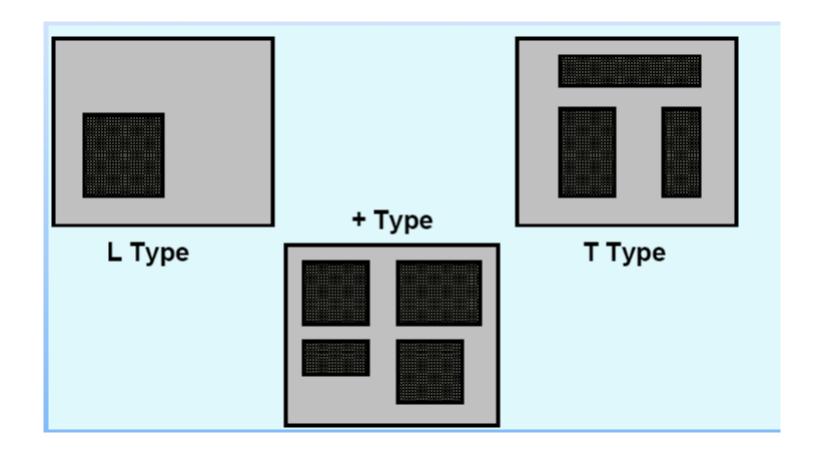
+-type:

- More complex and requires switchbox routers.
- Advantageous to convert +-junctions to T-junctions.





Leg of T must be routed before shoulder



Graph Models used in Global Routing

- Global routing is typically studied as a graph problem.
 - Routing regions and their relationships modeled as graphs.
- Three important graph models:
 - Grid Graph Model
 - Most suitable for area routing
 - Checker Board Model
 - 3. Channel Intersection Graph Model
 - Most suitable for global routing

After Global Routing

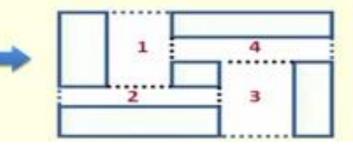
- The two-stage routing method is a powerful technique for routing.
- During the global routing stage:
 - The routing region is partitioned into a collection of rectangular regions.
 - To interconnect each net, a sequence of sub-regions to be used is determined.
 - All nets crossing a given boundary of a routing region are called floating terminals.
 - Once the sub-region is routed, these floating terminals become fixed terminals for subsequent regions.

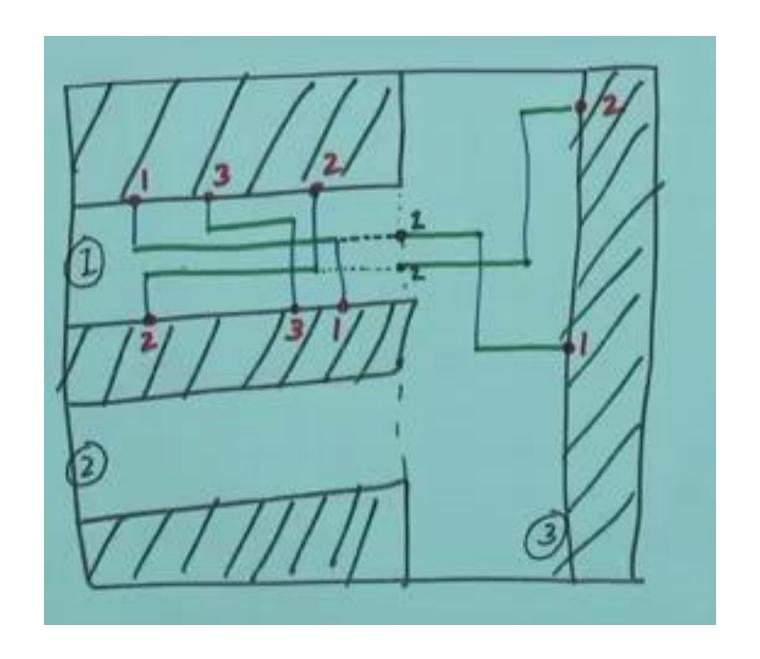
Order of Routing Regions

- Slicing placement topology.
 - Nets can be routed by considering channels 1, 2 and 3 in order.



- Non-slicing placement topology.
 - Channels with cyclic constraints.
 - Some of the routing regions are to be considered as switchboxes.



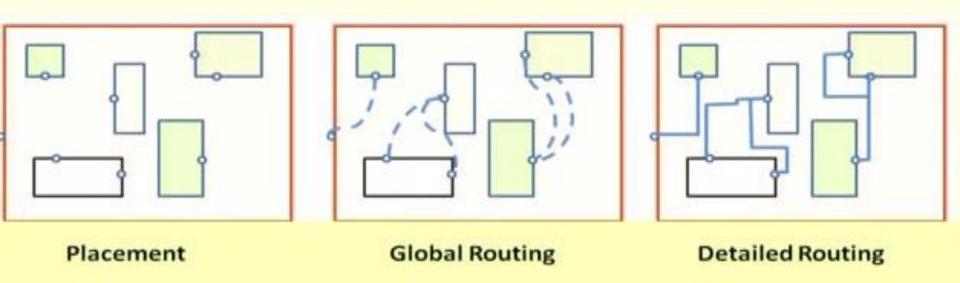


Detailed Routing

- Find actual geometric layout of each net within assigned routing regions.
- No layouts of two different nets should intersect on the same layer.
- Problem is solved incrementally, one region at a time in a predefined order.



A Routing Example



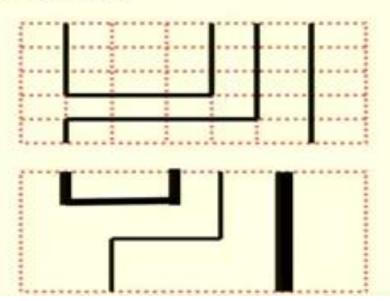
Routing Models

Grid-based model

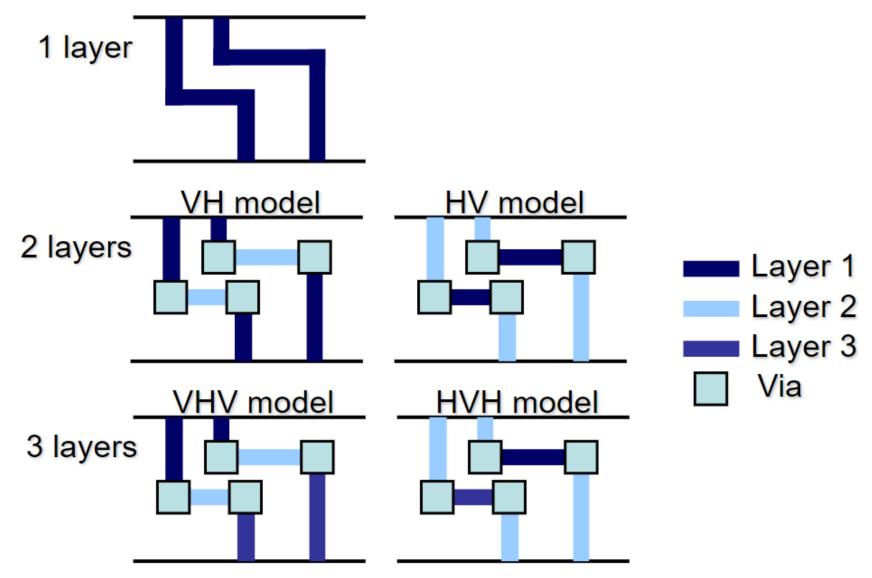
- A grid is super-imposed on the routing region.
- Wires follow paths along the grid lines.

Gridless model

Does not follow the gridded approach.

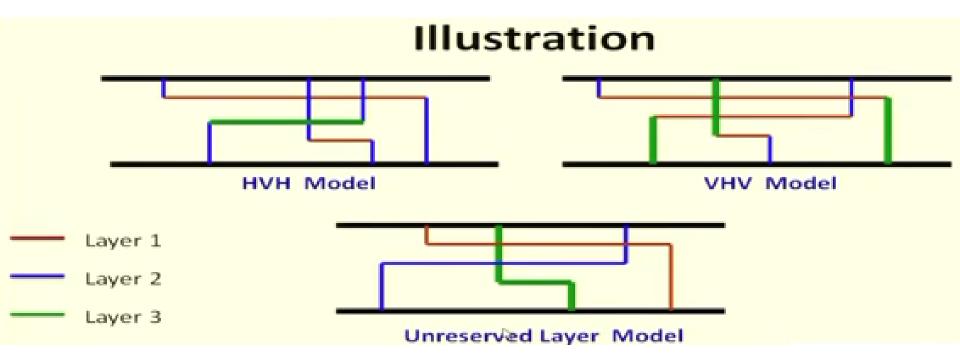


Routing Layer Models



Models for Multi-Layer Routing

- Unreserved layer model
 - Any net segment is allowed to be placed in any layer.
- Reserved layer model
 - Certain types of segments are restricted to particular layer(s).
 - Two-layer (HV, VH)
 - Three-layer (VHV, HVH)



Acknowledgement

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