CT#2 CSE 3207 Time: 20min Marks: 20(10+10)

Q1. A 74LS138 decoder has its three SELECT inputs connected to A12, A13 and A14 of the system address bus. It has G2A connected to A15. G2B connected to RD, and G1 connected to +5V. Use an address decoder worksheet to determine what eight ROM address blocks the decoder outputs will select. Find out the starting and ending address of 5^{th} and 7^{th} ROM.

Q2. Why is the 8086 memory set up as 2-byte-wide? Describe the 8086 bus operation a word to address 04373H.

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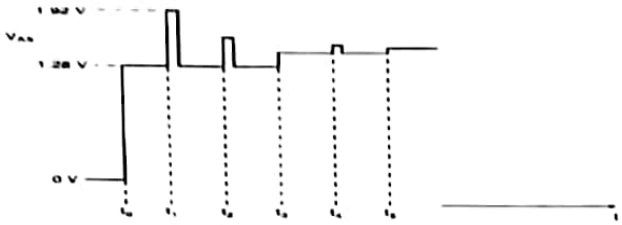
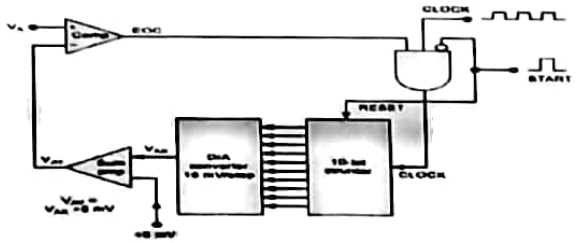
CT#3 CSE 3207 Time: 20min Marks: 20(6+7+7)

Q1. Figure 1 shows the waveform at V_{ax} for a six bit SAC with a step size of 40mV during a complete conversion cycle. Examine this wave form and describe what is occurring at time t0 to t5. Then determine the resultant digital output.



Q2.For the ADC of below figure, determine the range of analog input values that will produce a digital output of 0100011100



Q3. What are the advantages of R/2R ladder? Deduce the equation, $V_{out}=(-V_{REF}/16)xB$ where the Op-Amp reference resistance R and B is the digital representation of binary value.

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