Testing of VLSI Circuits

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Why Do We Need Testing

- Possibility of errors during the design process.
- There can even be bugs in the translation process (viz. the CAD tools used).
- Possibility of faults during fabrication / packaging.
- Necessary to test each and every chip before they can be used.
- Billions of transistors is present-day VLSI chips.
  - Chances of faults creeping in is also quite significant.

Basic Objectives of Testing

- We use testing to determine the presence of faults in a given circuit / chip.
  - ***Fallacy***: *Testing is used to guarantee that a circuit / chip is fault-free.*
  - No amount of testing can give this guarantee.
  - Using testing, we can increase out confidence in the correct working of the circuit / chip.
- We usually use verification along with testing.
  - Distinctly different objectives.

Verification VS Testing

- Verification guarantees the correctness of the design.
- Performed *once* before the actual manufacturing of the circuits / chips.
- Primarily responsible for the quality of the design.
- Uses formal methods, simulation, etc.

- Testing *tries to* guarantee the correctness of the manufactured circuits / chips.
- Has to be performed on *every* manufactured device.
- Primary responsible for the quality of the devices that go to the market.
- Two steps involved: (a) Test Generation, (b) Test Application.

When to Do Testing

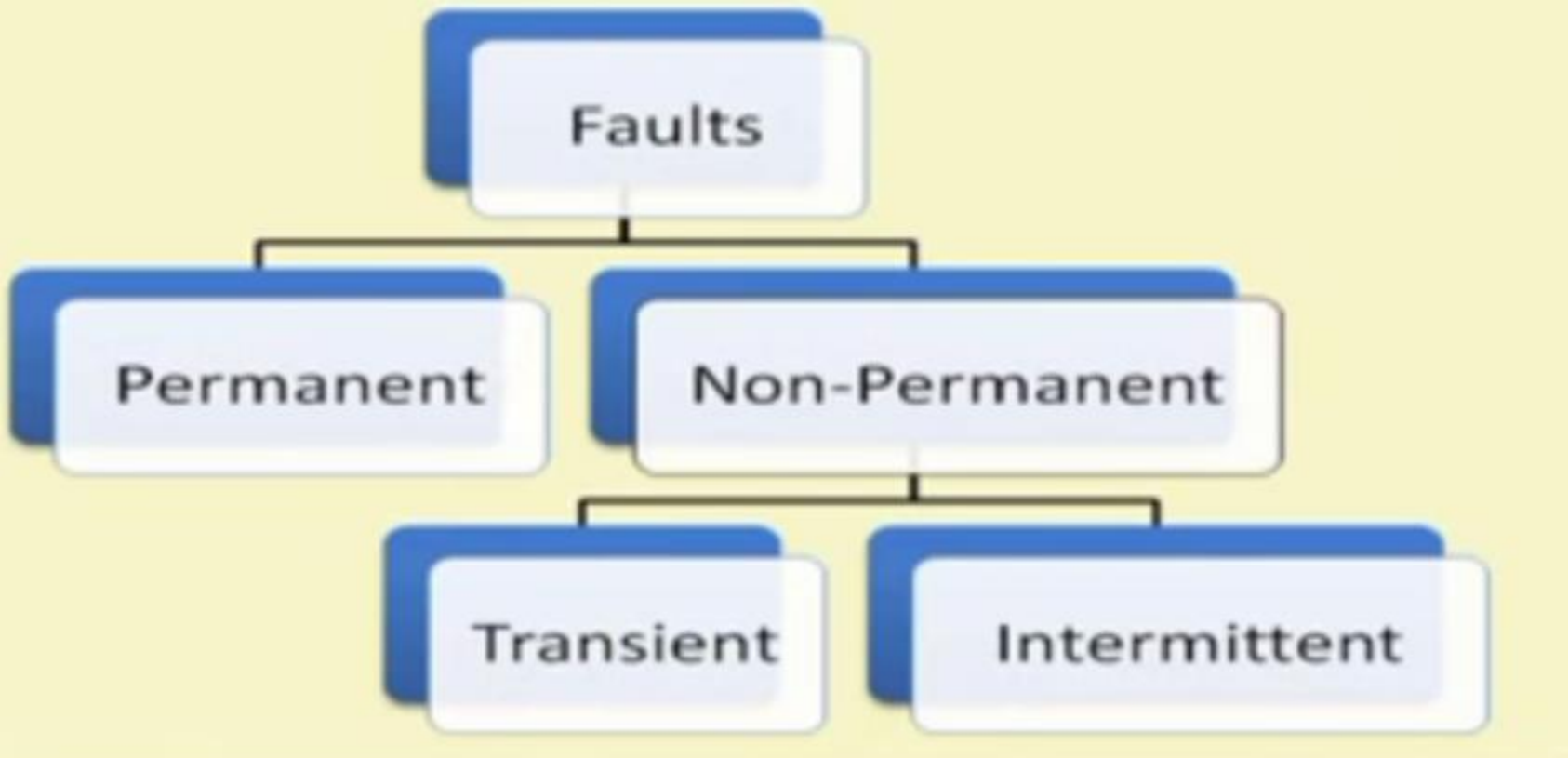
- Can be carried out at various levels:
  - At the chip-level, when chips are manufactured.
  - At the board-level, when chips are integrated on the boards.
  - At the system-level, when several boards are assembled together.
- Rule of thumb:
  - Detecting a fault early reduces the cost of testing.
  - *Empirical Rule*: It is 10 times more expensive to test a device as we move to the next higher level (*chip* → *board* → *system*).

Sources of Faults

- Because of errors during the fabrication process.
  - Missing contact window, parasitic transistors, etc.
- Because of defects in the material(s).
  - Cracks or imperfections in the substrate, surface impurities, etc.
- Because of ageing.
  - Dielectric breakdown, electron migration, etc.
- Because of defects during packaging.
  - Contact degradation, disconnection, etc.

Parasitic Transistor: Unwanted transistor formation in an integrated circuit structure.

Types of Faults



Types of Faults…

- *Permanent Faults* change the functional behavior of a chip in a time-independent (permanent) way.
  - Design errors, incorrect connections, etc.
  - Easier to detect.

- *Non-Permanent Faults* occur randomly and at unpredictable times and for unpredictable time durations.
  - Difficult to detect.
  - The fault may not show up during testing.
  - On-line testing is a popular method.

Types of Faults…

- *Transient Faults* are caused due to environmental conditions.
  - Charged particles, variations in pressure, vibration, temperature, etc.
  - Example: Bit changes in RAMs caused by α-radiation (called *soft errors*; no permanent damage).

- *Intermittent Faults* are caused by non-environmental conditions, and behave like permanent faults during the duration of the failure.
  - Loose connections, critical timing, changes in parameter values, etc.
  - May require repeated testing for detection.

Some Terminologies

- *Fault Coverage*: Percentage of the total number of logical faults that can be tested using a given test set *T*.

$$FC = \frac{\text{Number of detected faults}}{\text{Total number of faults}}$$

Defect Level: Fraction of shipped parts that are defective.

$$DL = 1 - Y^{(1-FC)}$$

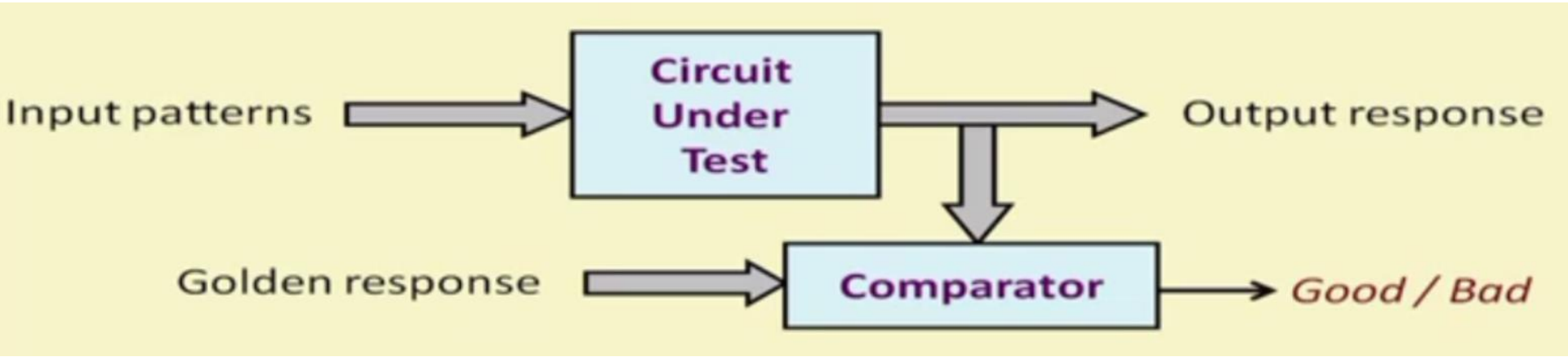
Where Y is the yield. Yield says what is the fraction of the chips that are fabricated which are good.

Processes of Testing

- Fault Modeling
  - Abstract the physical defects and define a suitable logical fault model.
  - Limits / simplifies the scope of test generation.
- Test Generation
  - Given a circuit and a set of faults *F*, determine a set of test vectors *T* that detects all faults in *F*.
- Fault Simulation
  - Given a circuit, a set of faults *F*, and a set of test vectors *T*, determine the faults in *F* that are tested by the vectors in *T*.

- Design for Testability (DFT)
  - Formulate a set of design rules that, if followed, results in a circuit that will be *easily testable*.
  - Typically introduces both area overhead and performance degradation.
- Built-in Self-Test (BIST)
  - Test generation and response evaluation of the circuits are performed on-chip.
  - The chip can test itself.
  - Additional area overhead.

Basic Testing Principle



References

1. Lectures by: Prof. Indranil Sengupta, Department of Computer Science and Engineering,
IIT Kharagpur, India.

Thanks