

08-06-14

2-A

Logic low $0 = 0 \text{ V} \sim 3 \text{ V}$ } typical value
High $1 = 2.4 \text{ V} \sim 5 \text{ V}$ } for experiment

for bidden range / hidden range

$$\begin{array}{r} 2 | 29 \\ 2 | 14 - 1 \\ 2 | 7 - 0 \\ 2 | 3 - 1 \\ 2 | 1 - 1 \\ 0 - 1 \end{array} \quad (29)_{10} = (11101)_2$$

Number System Conversion:

Digit Range (0-6) (Position number system).
 $(+0)_2 = (\dots)_{10}$

$$(23)_7 = (\dots)_{10}$$

$$2 \times 7^1 + 3 \times 7^0 = 14 + 3 = (17)_{10}$$

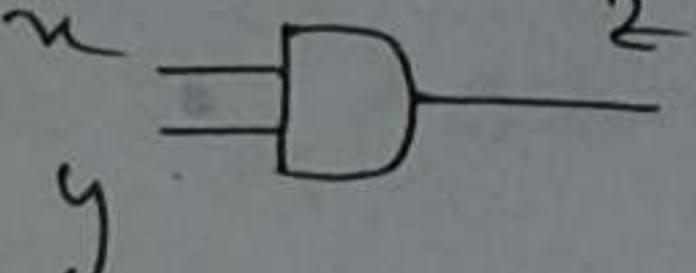
10.6.14

2-c

Basic Gate

Basic gate which are the basic component in our digital system.

1. And gate
2. OR gate
3. NOT gate

1. AND gate:  $Z = x \cdot y$ (nancy)

2 input & 1 output

Properties: if all inputs are logic 1 then output is logic 1 otherwise o/p is low.

Truth table for AND gate:

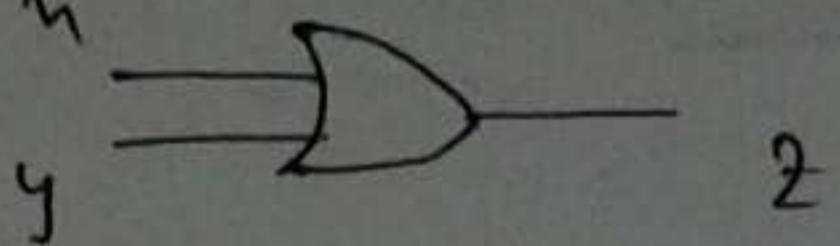
Input	O/P	
x	y	Z
0	0	0
0	1	0
1	0	0
1	1	1

$$Z = a \cdot b \cdot c \cdot d$$

$$\underline{Z = a \cdot b \cdot c \cdot d}$$

boolean equation,

2 OR gate:



$$z = n + y \quad (n \text{ or } y)$$

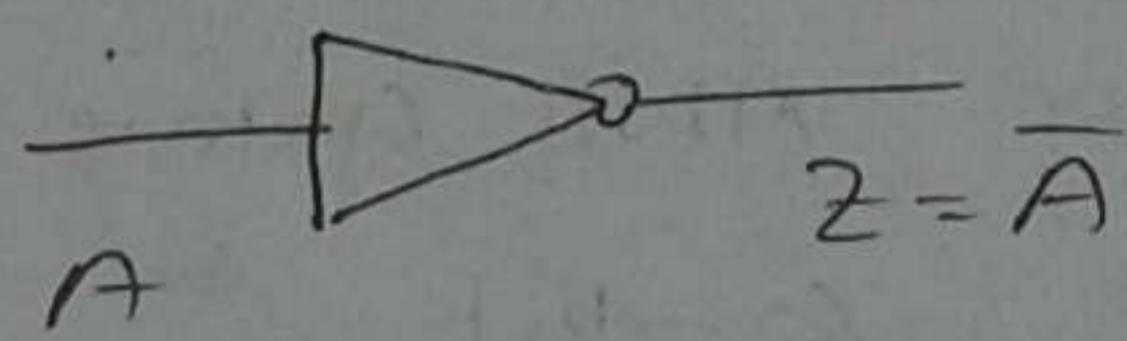
Property: Output will be high when at least one input is high otherwise low.

Truth table for OR gate:

Input		O/P
n	y	z
0	0	0
0	1	1
1	0	1
1	1	1

3. NOT gate:

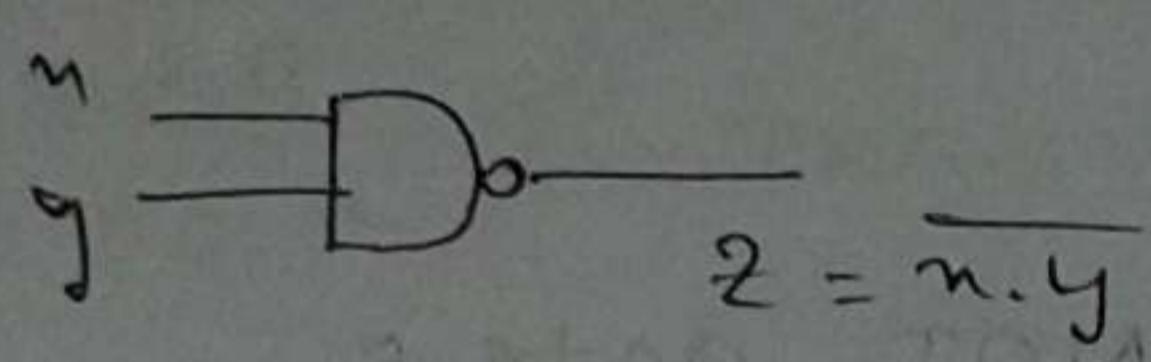
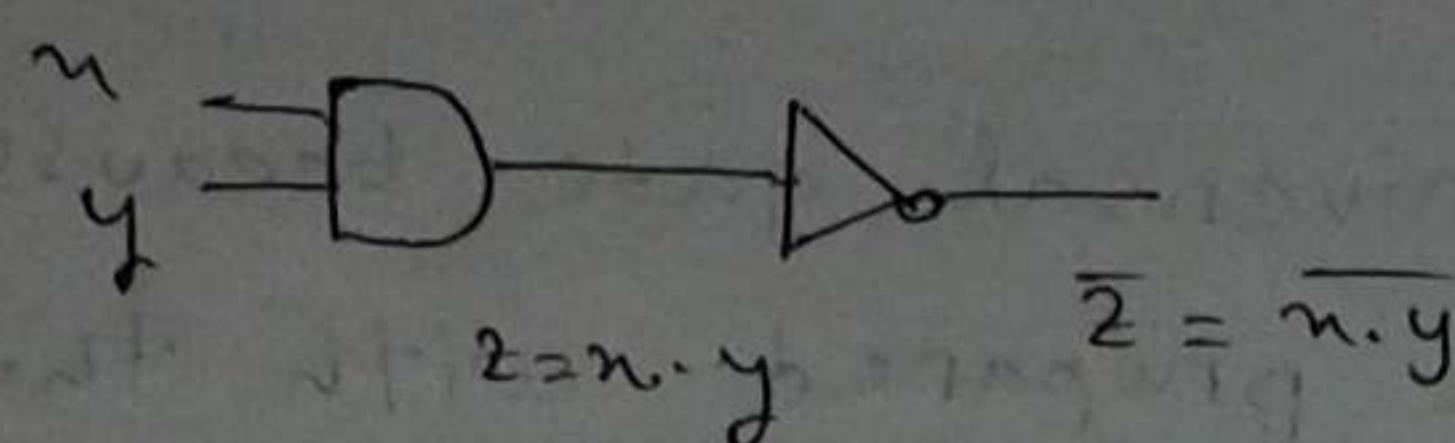
Complementary form of regular expression,



It reverse the input value.

Input	Output
A	A-bar
0	1
1	0

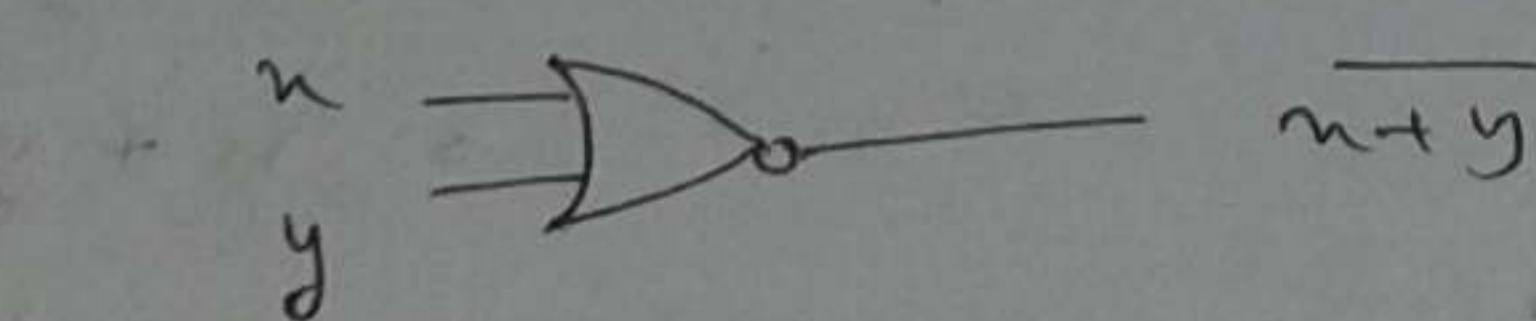
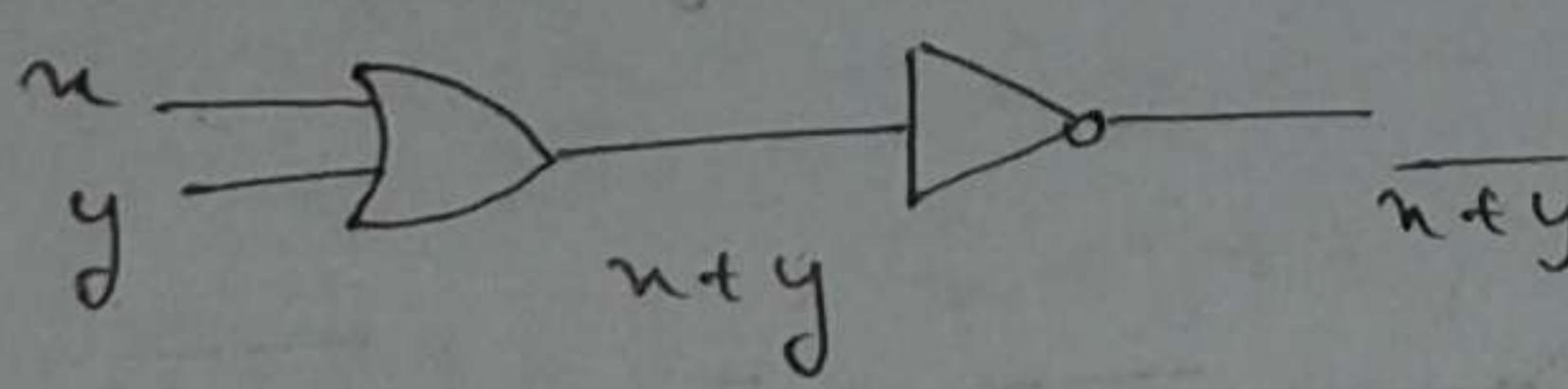
4. NAND gate : (AND + NOT)



Input		O/P
x	y	z
0	0	1
0	1	1
1	0	1
1	1	0

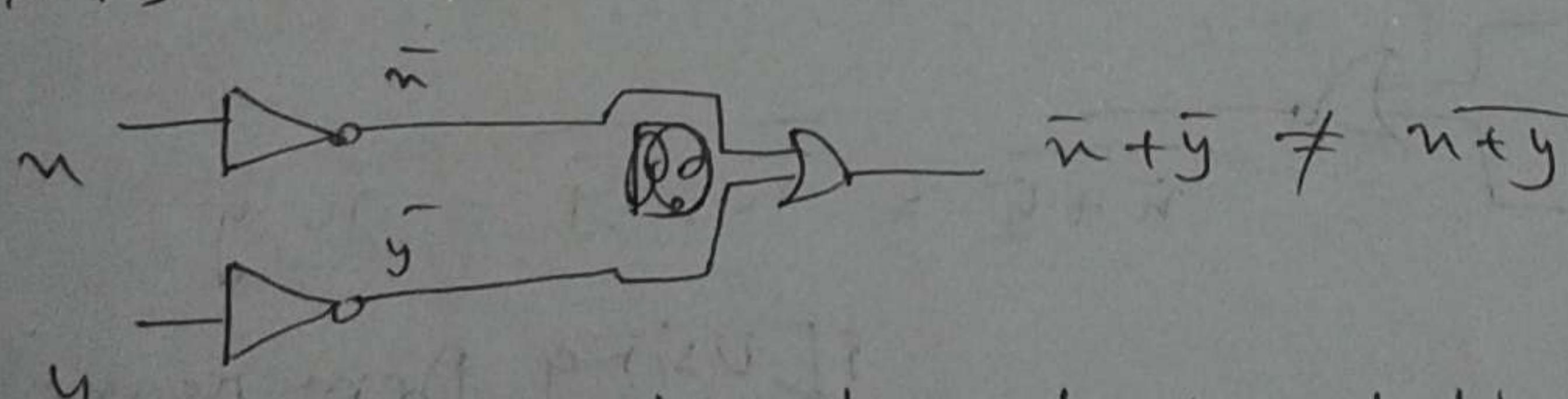
If all the inputs are logic 1 then output is logic zero otherwise high.

5. NOR gate : (OR + NOT)



Input		O/P
x	y	z
0	0	1
0	1	0
1	0	0
1	1	0

Is not possible



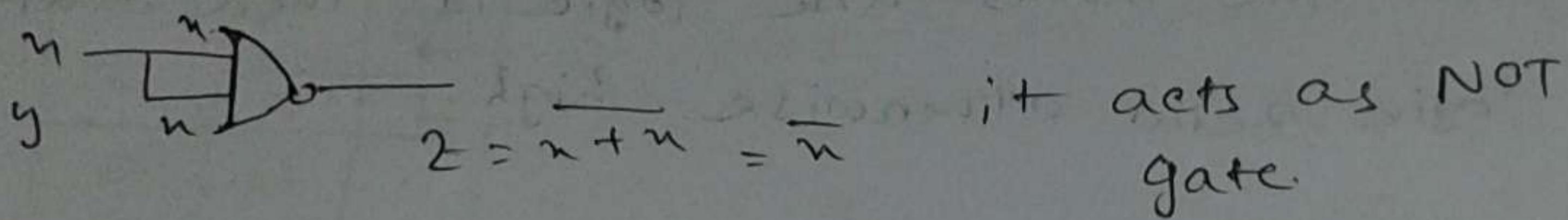
By using the truth table we can prove it.

Universal Gate:

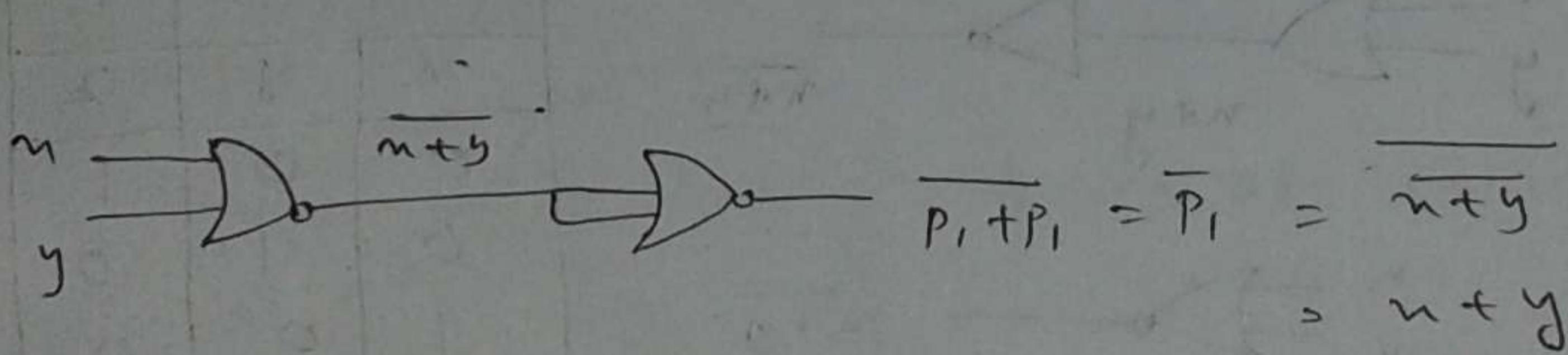
NOR, NAND

This are called universal gate because all basic gates are prepared with the help of these gate

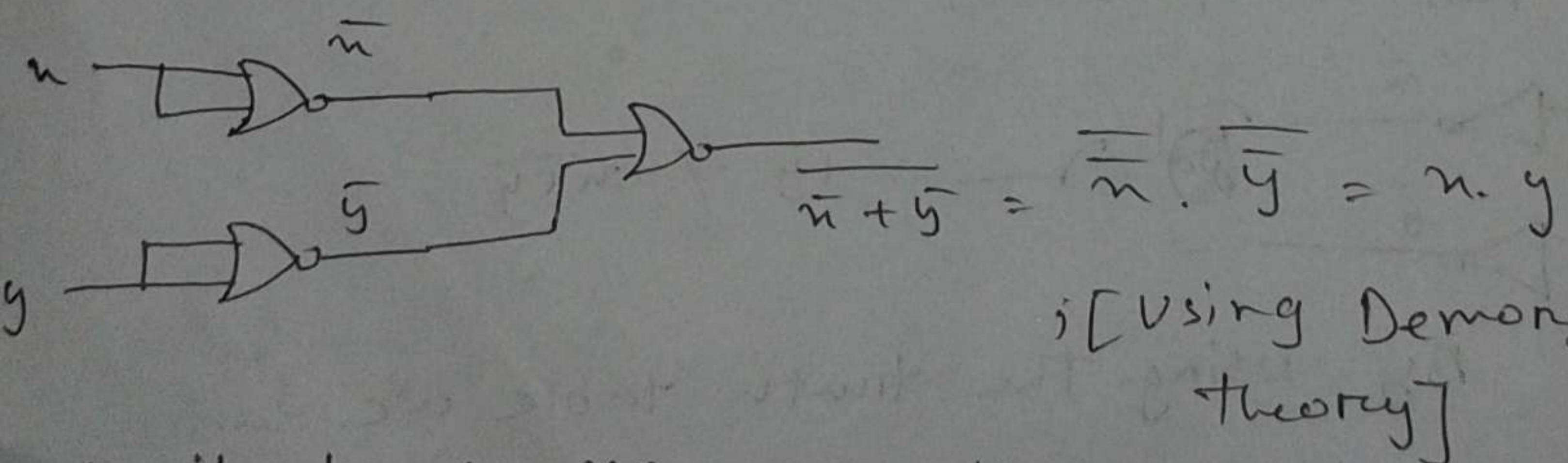
1. NOR gate acts as NOT gate:



2. NOR gate acts as OR gate



3. NOR gate acts as AND gate.

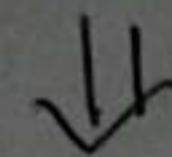


Similarly we can prove all by NAND gate - self study.

23.06.14

3-B

$$x+0 = x$$



$$x=0, 1$$

$$\boxed{1} + 0 = 1$$

$$\boxed{0} + 0 = 0$$

$$x + 0 = x \Rightarrow \text{Zero Axiom}$$

$$x + \bar{x} = 1$$

$$1 + 0 = 1$$

$$0 + 1 = 1$$

$$x \cdot \bar{x} = 0$$

De Morgan's:

$$\overline{x+y} = \bar{x} \cdot \bar{y}$$

$$\overline{x+y+z} = \bar{x} \cdot \bar{y} \cdot \bar{z}$$

Boolean algebra properties:

The duality principle:

Duality: $\bar{x}^* \bar{y} \bar{z} + \bar{x} \bar{y} z$
 $(\bar{x}+y+\bar{z}), (\bar{x}+\bar{y}+z)$

$$x+0 = x \Leftrightarrow x \cdot 1 = x$$

$$x+\bar{x} = 1 \quad x \cdot \bar{x} = 0 \quad P = x + x \cdot y$$

Absorption property

$$= x(1+y) \quad | \quad 1+y=1$$

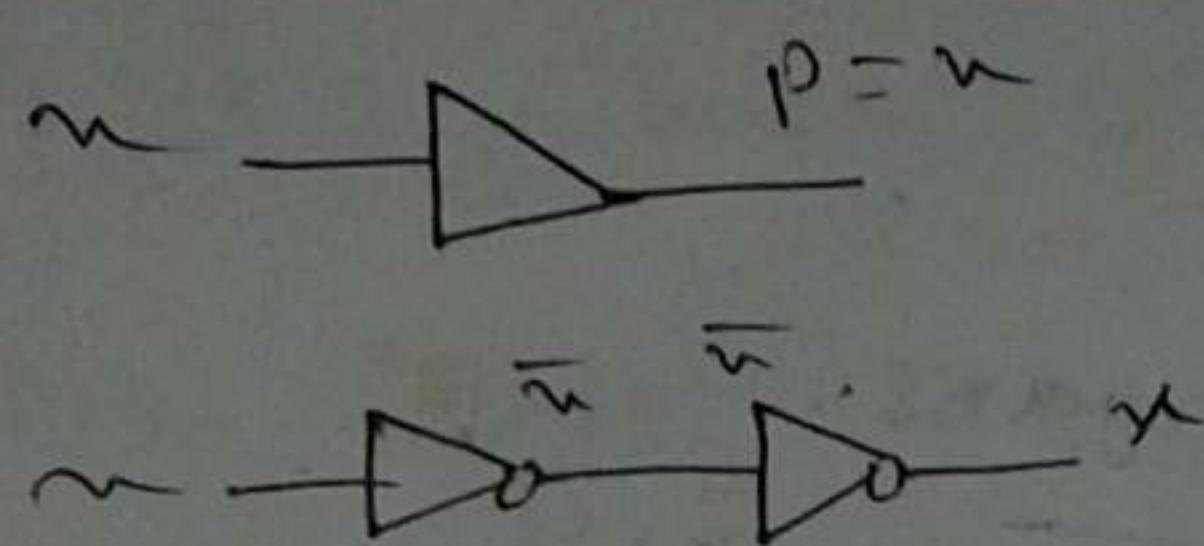
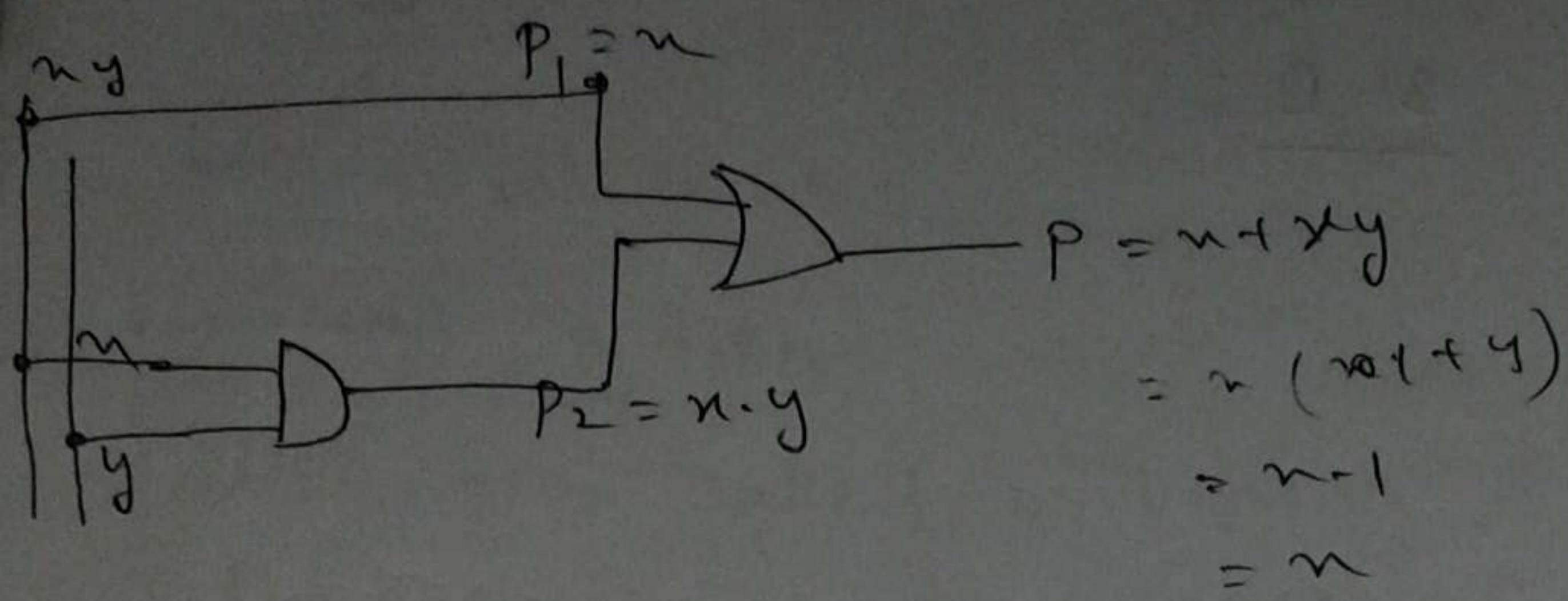
$$= x \cdot 1$$

$$x + x \cdot y = x$$

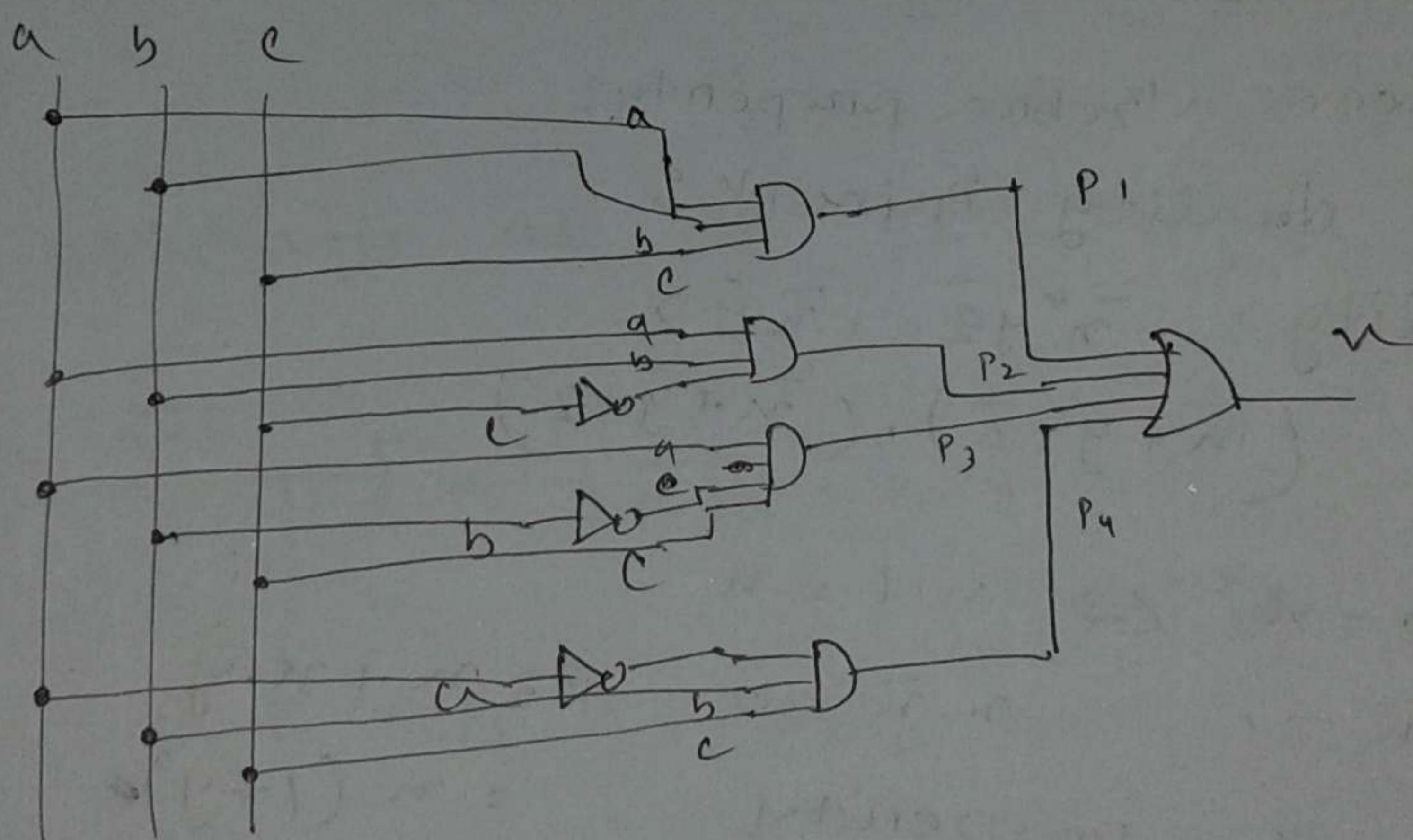
$$x \cdot (x+y) = \underline{x}$$

$$\frac{x+x \cdot y}{P_1 + P_2}$$

$$P = P_1 + P_2$$



$$\# n = \frac{abc}{P_1} + \frac{ab\bar{c}}{P_2} + \frac{a\bar{b}c}{P_3} + \frac{\bar{a}bc}{P_4}$$



$$[n + n = x]$$

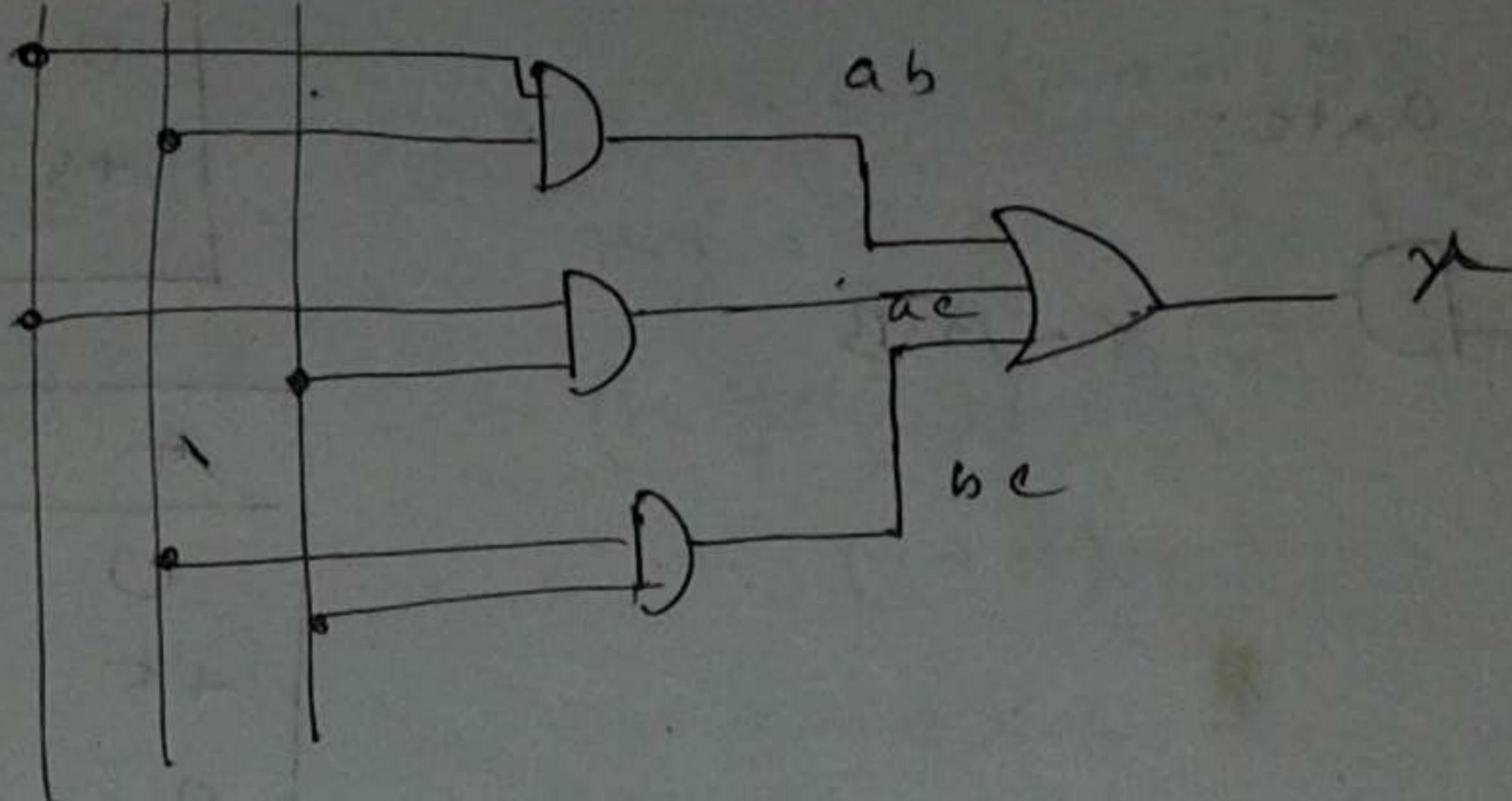
$$[n + n + x + \dots = n]$$

$$\begin{aligned}
 n &= abc + ab\bar{c} + a\bar{b}c + \bar{a}bc \\
 &= (abc + a\bar{b}\bar{c}) + (abc + \bar{a}bc) + (\bar{a}bc + a\bar{b}c) \\
 &= ab(c + \bar{c}) + ac(b + \bar{b}) + bc(a + \bar{a})
 \end{aligned}$$

$$c + \bar{c} = 1$$

$$= ab + ac + bc$$

a b c



Book Exercise

3-A
LAB -1

16.06.14

Exp: 1

Name of the experiment: Basic Logic function

Objectives:

Theory:

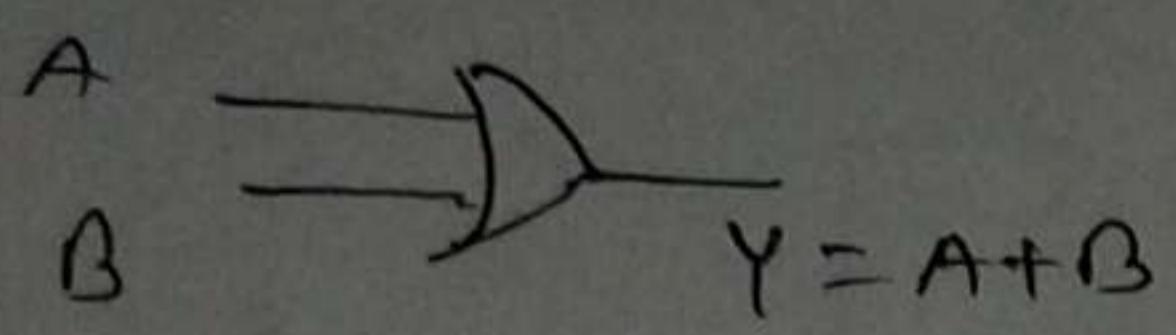
Apparatus:

Calculation / chart / Table:

Result:

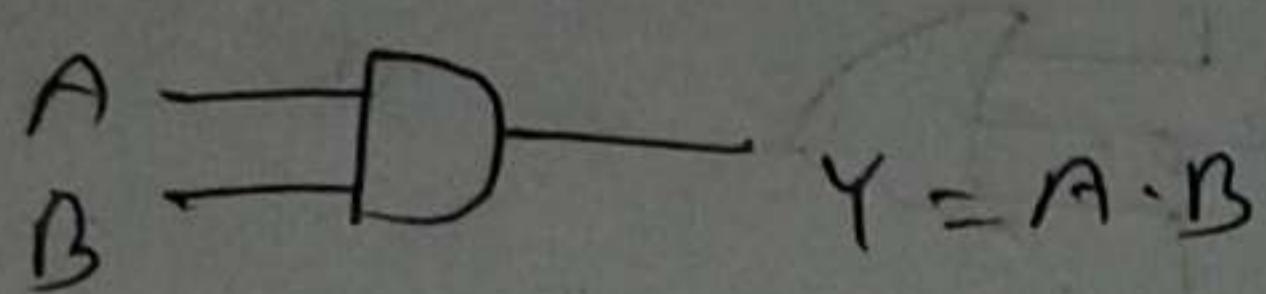
Conclusion and Discussion:

OR gate:



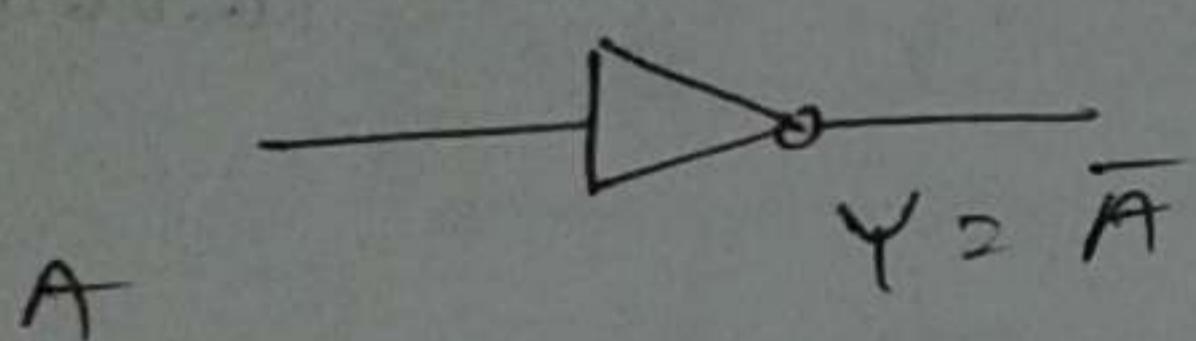
A	B	Y
0	0	0.14
+5	0	4.40
0	+5	4.40
+5	+5	4.40

AND gate:



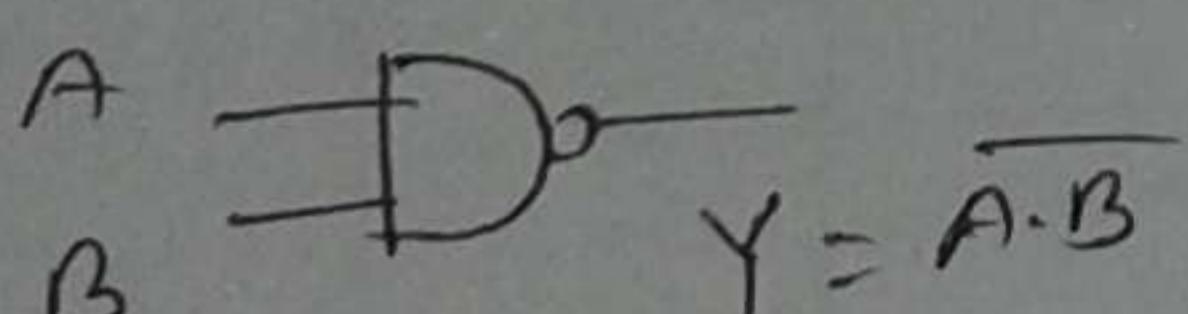
A	B	Y
0	0	0.16
+5	0	0.16
0	+5	0.16
+5	+5	4.38

NOT gate:



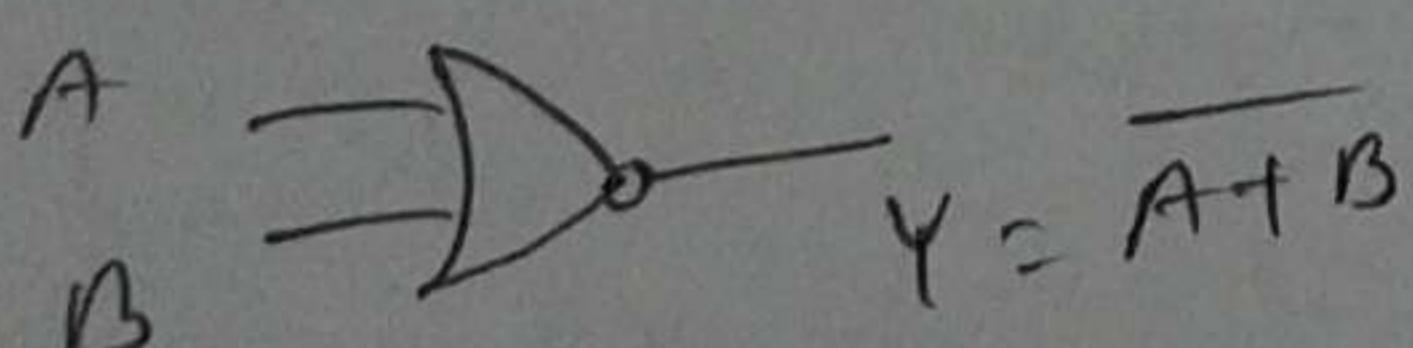
A	Y
0	4.42
+5	0.14

NAND gate:



A	B	Y
0	0	4.41
+5	0	4.41
0	+5	4.41
+5	+5	0.20

NOR gate:



A	B	Y
0	0	4.40
+5	0	0.18
0	+5	0.18
+5	+5	0.16

⑧ 4-A

24.06.14

$$\begin{aligned}
 & \# P = n + \bar{n} y \\
 & = n \cdot 1 + \bar{n} y \\
 & = n \cdot (n + \bar{n}) + \bar{n} y \\
 & = n \cdot n + n \cdot \bar{n} + \bar{n} y \\
 & = x
 \end{aligned}$$

$$\begin{aligned}
 P &= ny + \bar{n}^2 + y^2 \\
 &= ny + \bar{n}^2 + \underbrace{(n + \bar{n})}_{\perp} y^2 \\
 &= ny + \bar{n}^2 + ny^2 + \bar{n}y^2 \\
 &= (ny + ny^2) + (\bar{n}^2 + \bar{n}y^2) \\
 &= ny(1+z) + \bar{n}^2(1+y)
 \end{aligned}$$

$$\begin{aligned} \# P &= n + \bar{n} y \\ &= n(y + \bar{y}) + \bar{n} y \\ &= ny + \bar{n}\bar{y} + \bar{n} y \end{aligned}$$

Boolean Function:

$$\begin{aligned} P &= n + \cancel{n} y \\ &= n (n + \cancel{n}) + \cancel{n} y \\ &> n \cancel{n} + n \cdot \cancel{n} + \cancel{n} y \end{aligned}$$

$$P(n, y) = n + \bar{n} y$$

$$\overline{F}(a,b) = \overline{a + \overline{a}b} = a(b + \overline{b}) + \overline{a}b = a.b + \overline{a}\overline{b} + \overline{a}b$$

\downarrow \downarrow

(SOP)

ST and SOP = Sum of Product

POS = Product of Sum
= 1,1 + 1,0 + 0,1

$$\text{For } F(a,b) = (a+b)(a+\bar{b}) \cdot \underline{(a+\bar{b} \cdot b)}$$

Just one sign will

$$\bar{a} + b\bar{b} = (\bar{a} + b)(\bar{a} + \bar{b})$$

$$= (\bar{a} + b) (\bar{a} + \bar{b}) (\bar{a} + b), (\bar{a} + \bar{b})$$

$$= (a+b) \cdot (\overset{a}{\underset{0}{\downarrow}} + b) (\overset{a}{\underset{1}{\downarrow}} + 5)$$

Exercise:

Sir @ 20 Topics 20% exercise H.W.

Manishan and Tocci @ 02,

Ex: Design a three input combinational circuit whose output will be high when the majority no. of inputs are at ⁱⁿ high state, otherwise low.

$f = \text{Sum all the minterms}$

$$> \bar{A}BC + A\bar{B}C +$$

$$A\bar{B}\bar{C} + AB\bar{C}$$

\Downarrow Simplify

$$> AB + BC + CA$$

Expression Minterm	I/P			O/P F
	A	B	C	
0	0	0	0	0
0	0	0	1	0
01	01	01	0	0
0	0	1	1	1
01	01	1	0	0
1	0	1	1	1
1	1	1	0	1
1	1	1	1	1

5.08.14

4-C

Canonical Sum of Products

Input $\rightarrow 0 \rightarrow \bar{A}$

$1 \rightarrow A$

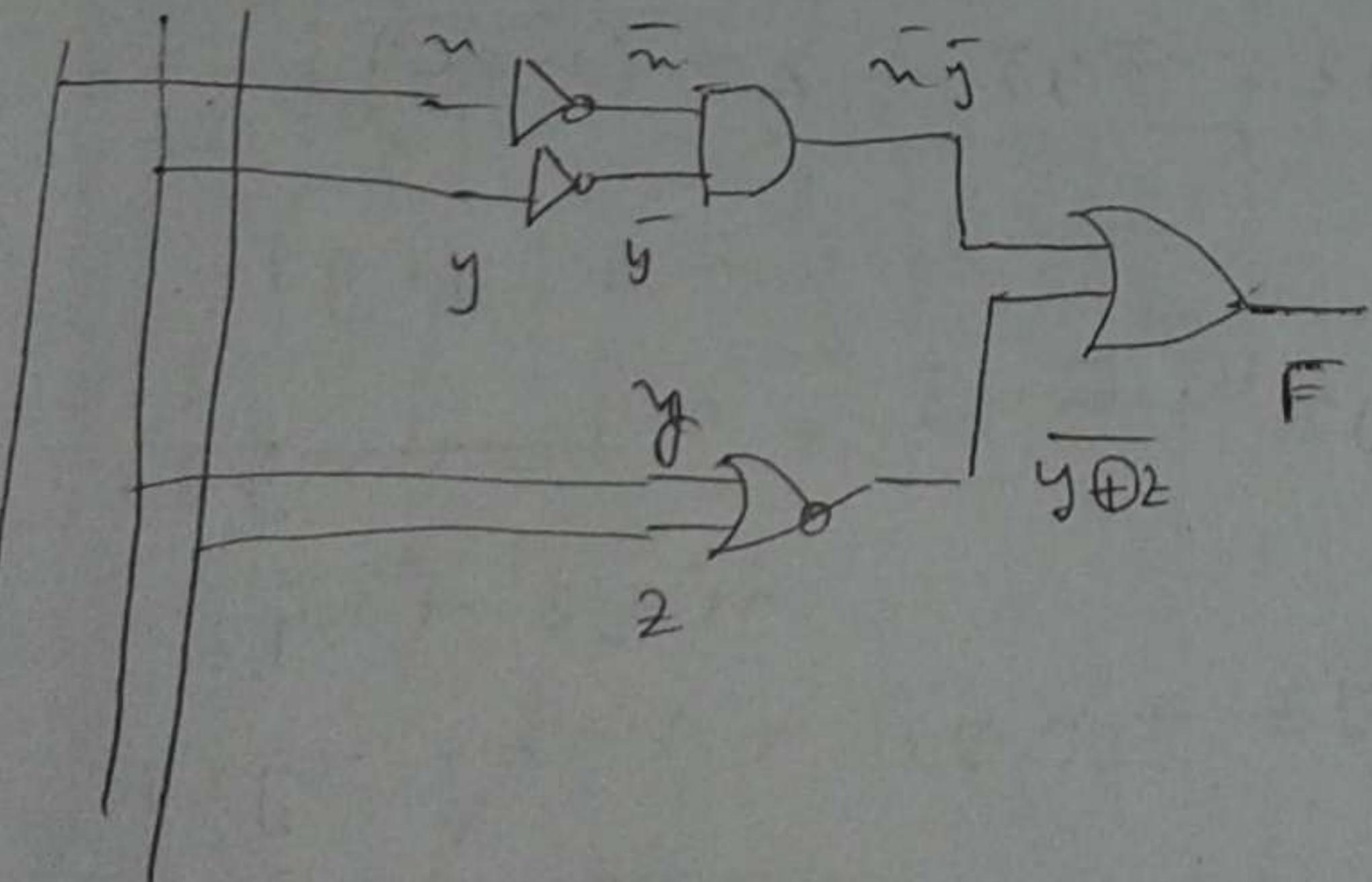
$$\begin{array}{ccccc}
 & \overline{n} & \overline{y} & \overline{z} & F \\
 0 & 0 & 0 & 0 & \oplus 1 \\
 & 0 & 0 & 1 & 1 \\
 0 & 1 & 0 & 0 & \\
 0 & 1 & 1 & 1 & \\
 1 & 0 & 0 & 1 & \\
 1 & 0 & 1 & 0 & \\
 1 & 1 & 0 & 0 & \\
 1 & 1 & 1 & 1 &
 \end{array}$$

$F = \bar{n}\bar{y}\bar{z} +$
 $\oplus \bar{n}\bar{y}z + \bar{n}yz$
 $\bar{n}\bar{y}z + nyz$
 $= \bar{n}\bar{y}(\bar{z} + z) +$
 $y_2(\bar{n} + n) +$
 $\bar{y}\bar{z}(n + \bar{n})$
 $= \bar{n}\bar{y}(\bar{z} + z) +$
 $y_2(\bar{n} + n) + \bar{n}\bar{y}\bar{z}$
 $+ \bar{n}\bar{y}\bar{z}$
 $= \bar{n}\bar{y} + y_2 + \bar{y}\bar{z}($
 $n + \bar{n})$

$$ny + \bar{ny} = n \oplus y$$

$$ny + \bar{ny} = \overline{n \oplus y}$$

ny_2



$$\begin{aligned}
 &= \bar{n}\bar{y} + y_2 + \bar{y}\bar{z} \\
 &\sim = \bar{n}\bar{y} + \overline{y \oplus z}
 \end{aligned}$$

Canonical Product of Sum:

$$F(x, y, z) = \sum_{(1, 2, 4, 7)}^{\text{Min term}} (\bar{x}\bar{y}z + \bar{x}y\bar{z} + x\bar{y}\bar{z})$$

In this combination
output 1

$$F(x, y, z) = \pi_{(0, 3, 5, 6)} \rightarrow \text{In this combination}$$

output 0

$$(x+y+z) \cdot (x+\bar{y}+\bar{z}) \cdot (\bar{x}+y+\bar{z}).$$

$$P(x, y, z) = m_1, m_2 + m_3 + m_4 + m_5 + m_6 \quad (\bar{x} + \bar{y} + \bar{z})$$

$$F(x, y, z) = M_0, M_1, M_2, M_3, M_4, M_5 \rightarrow \text{max}$$

conversion of canonical form

$$\nexists F(x, y, z) = \bar{x}y + z$$

$$= \bar{x}y(z+\bar{z}) + z(x+\bar{x})$$

$$= \bar{x}yz + \bar{x}y\bar{z} + zx + \bar{x}z$$

$$= \bar{x}yz + \bar{x}y\bar{z} + z(x+y) +$$

$$\bar{z}x(y+\bar{y})$$

$$= \bar{x}yz + \bar{x}y\bar{z} + xy\bar{z} + x\bar{y}z +$$

$$\bar{x}y\bar{z} + \bar{x}\bar{y}z$$

$$= \bar{x}yz + \bar{x}y\bar{z} + xy\bar{z} + x\bar{y}z +$$

$$= \sum (3, 2, 7, 5, 4) \bar{x}\bar{y}z$$

$$= \sum (1, 2, 3, 5, 7).$$

$$\text{Function} = \pi_{(0, 4, 6)}$$

$$\text{Expression} = (x+y+z) \cdot (x+\bar{y}+\bar{z}) \cdot (\bar{x}+y+\bar{z})$$

$$abc + a\bar{b}\bar{c} + \bar{a}bc$$

$$\begin{aligned} &= ab + ac \\ &= a(b+c) \end{aligned} \quad \left. \begin{array}{l} \text{Both may be correct} \\ \text{But canonical form always same.} \end{array} \right. \quad \begin{array}{l} \checkmark \\ \checkmark \end{array}$$

But canonical form always same. \checkmark

Y-E

09.08.14

Karnaugh Maps (K.-Map)

$$\begin{aligned} Y &= ab + \bar{a}\bar{b} \\ &= b(a + \bar{a}) \end{aligned}$$

2 variable:

$f(n,y)$

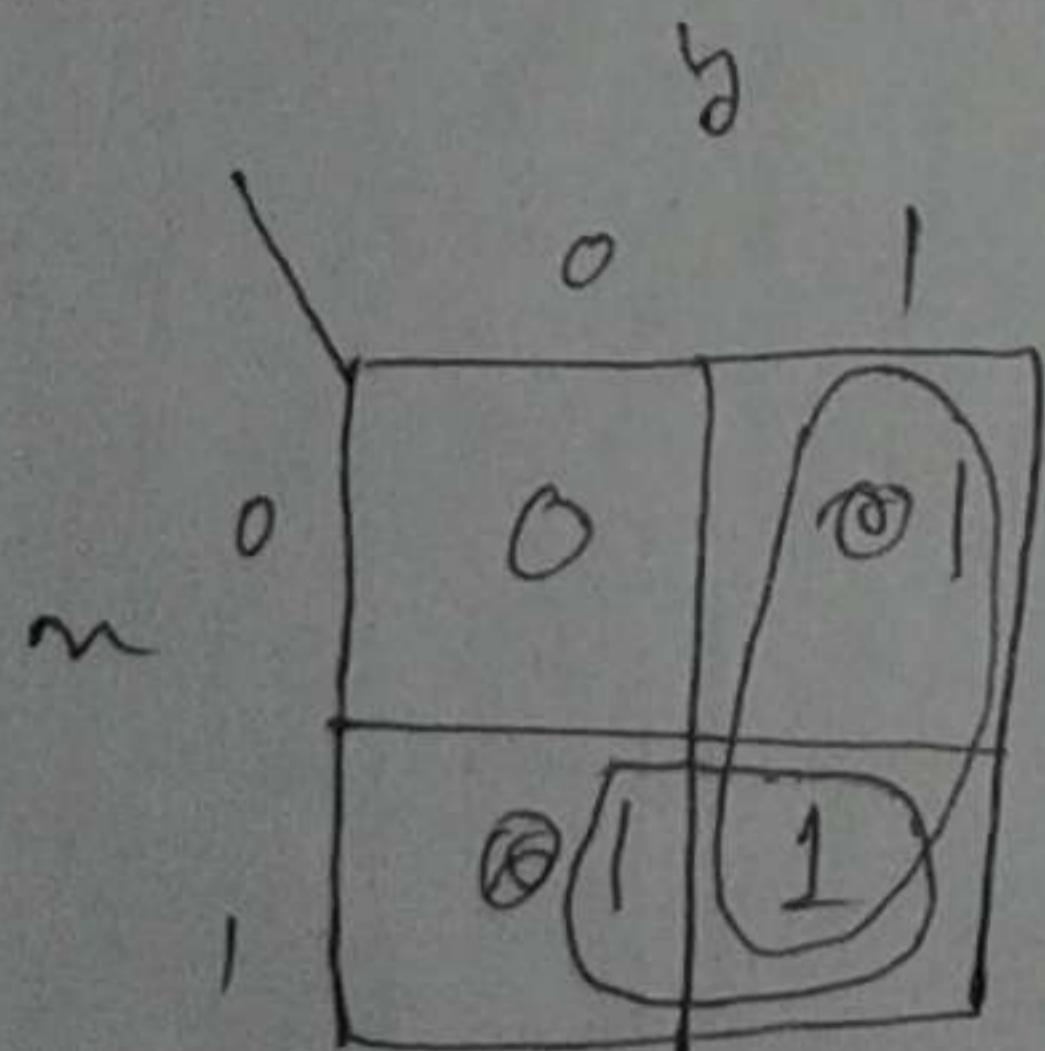
	n	y	P
0	0	0	0
1	0	1	1
2	1	0	1
3	1	1	1

$$2^{\text{nd}} = 2^2 = 4$$

$\neg n'y$	$\neg ny$
ny_2'	ny_3

n	n'
0	0
1	1

K-map



$$1. \quad 2^2 = 4 \quad \times$$

$$2^1 = 2 \quad \checkmark$$

$$2^0 = 1 \quad \checkmark$$

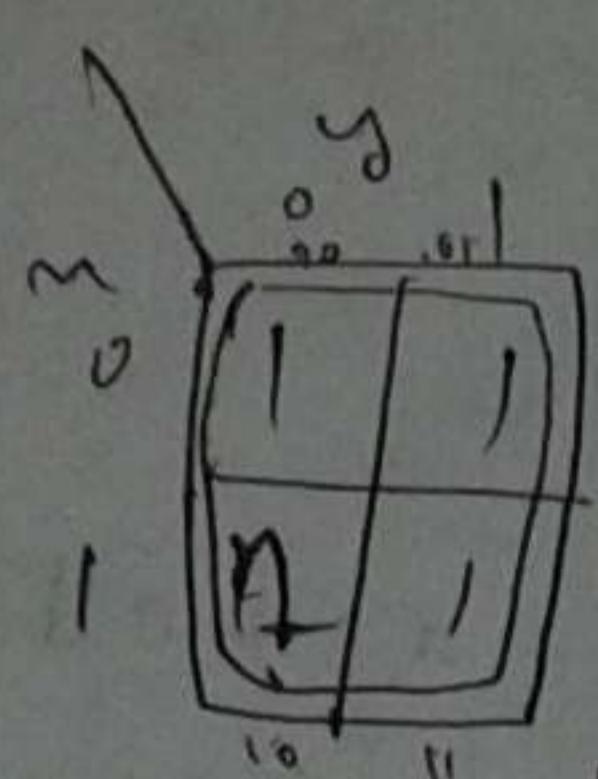
2. All 1 should be adjacent

$$ny' + ny = n(y' + y) = n$$

$$F(n, y) = n + y \quad (\text{loop } 1 \text{ is ready } 2\pi \text{ not fixed})$$

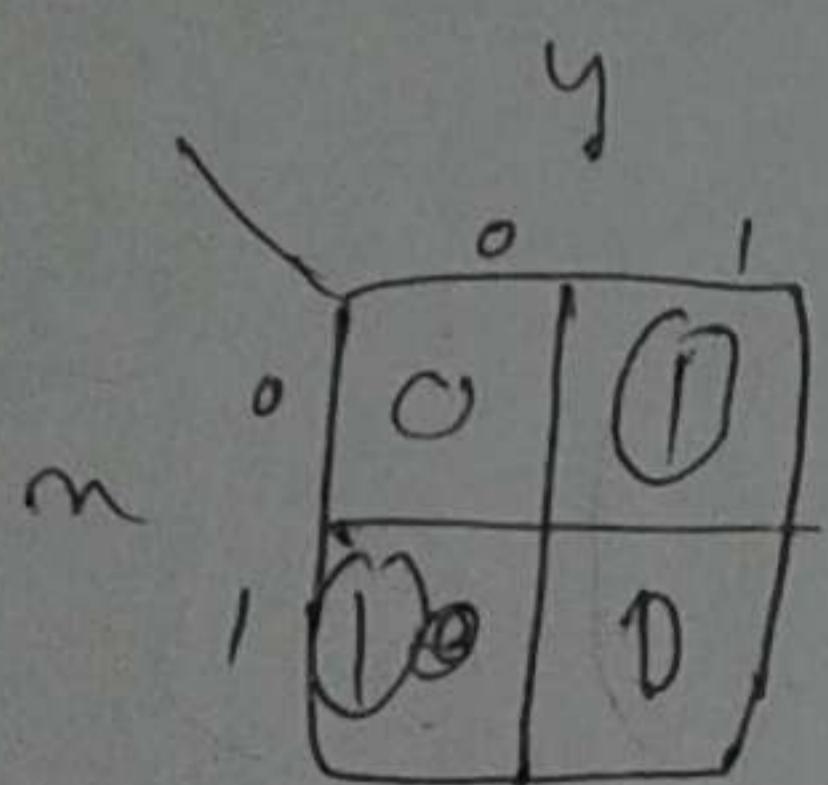
$$\begin{aligned} F &= \overbrace{n'y + ny' + ny}^{\text{overlap w.r.t } 2\pi \text{ to } 2\pi \text{ and } 1 \text{ to}} \\ &= y(n+x) + x(y'+y) \\ &\Rightarrow n + y \end{aligned}$$

overlap w.r.t 2π to 2π and 1 to
+ loop 2 to \oplus or Σ to 2π



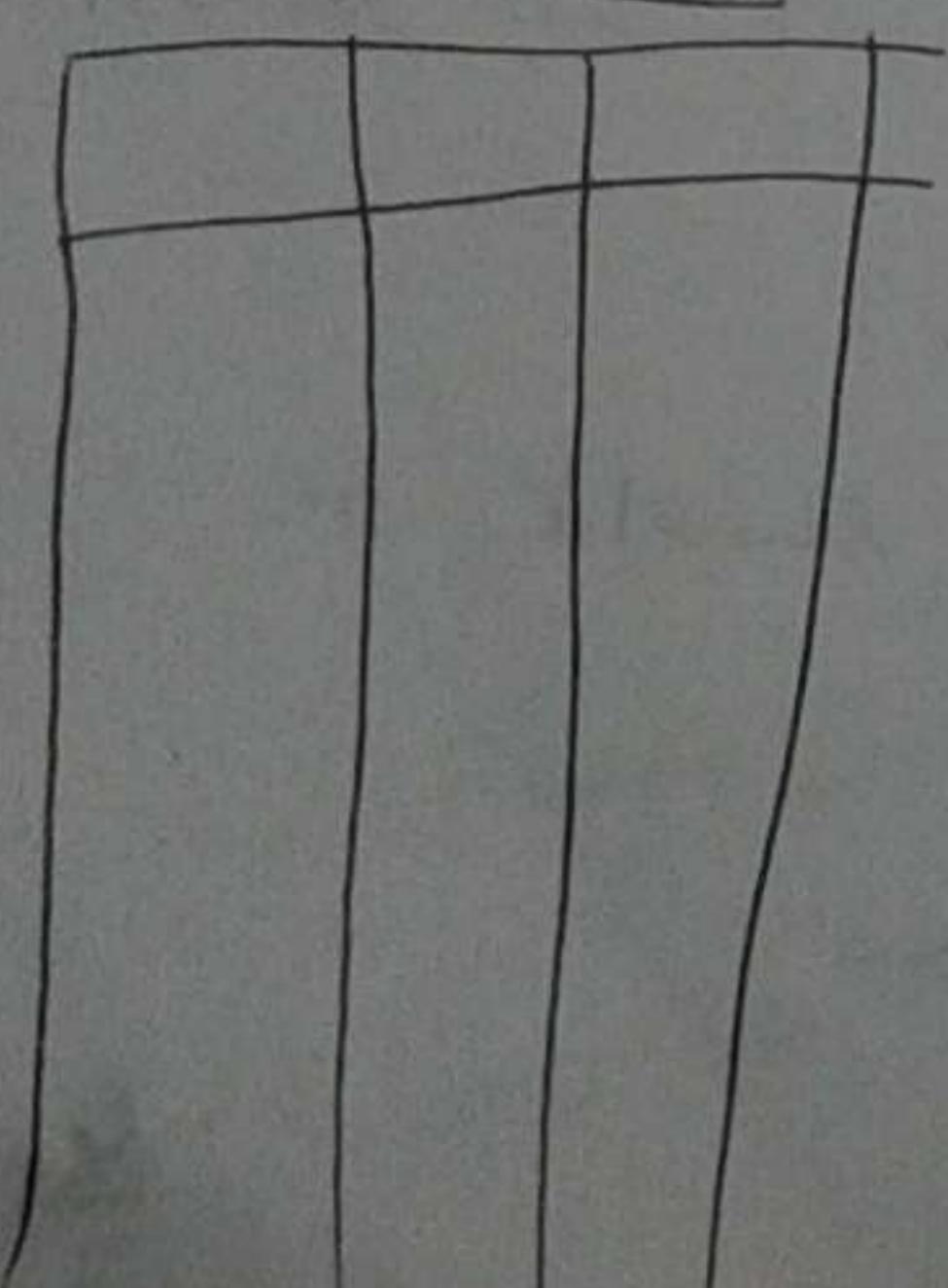
$$F(n, y) = 1$$

$$\begin{aligned} F &= \overbrace{n'y + ny' + ny + n'y'}^{\text{loop } 1 \text{ is ready}} \\ &= n'(y+y') + \end{aligned}$$



$$\begin{aligned} F(n, y) &= n'y + ny' \\ &\Rightarrow n \oplus y \end{aligned}$$

3 variable:



		0	1
		00	01
		10	11
	00	000-2	100-y
	01	001-1	101-z
m	10	011-2	111-x
	11	010-2	110-6

		00	01	11	10
		0	2	6	4
		01	3	7	5
	00	000	010	111	010
	01	000	011	111	010
	10	000	011	111	010
	11	000	011	111	010

$$F(m, y, z)$$

$$= \bar{y} + \bar{z}$$

$$\begin{aligned} F &= my' + ny \\ &= m(y' + y) \end{aligned}$$

10.08.14

S-A

Truth table

	m	y	z	F
-	0	0	0	1
-	0	0	1	1
-	0	1	0	0
-	0	1	1	1
-	1	0	0	1
-	1	0	1	1
-	1	1	0	0
-	1	1	1	0

n

		0	1
		00	01
		10	11
	00	1	1
	01	01	01
	10	1	0
	11	3	7

$$F = \bar{y} + \bar{m}z$$

$$F = \bar{u} + \bar{z}$$

$$\begin{aligned} X \quad F &= \bar{u} + \bar{y}\bar{z} + y\bar{z} \\ &= \bar{u} + \bar{z}(y + \bar{y}) \\ &= \bar{u} + \bar{z} \end{aligned}$$

$$F = \bar{u}\bar{y}\bar{z} + \bar{u}\bar{y}z + \bar{u}yz + u\bar{y}\bar{z}$$

How can you

K-map for optimal soln (Q4)

$\bar{u}\bar{y}\bar{z}$	F
1	1
0	0
1	0
0	1

$$F = \bar{u}\bar{y}\bar{z} + \bar{u}\bar{y}z + \bar{u}yz + u\bar{y}\bar{z}$$

$\bar{u}\bar{y}\bar{z}$	$\bar{u}\bar{y}z$	$\bar{u}yz$	$u\bar{y}\bar{z}$
00	1	0	0
01	1	0	0
11	1	0	0
10	1	1	0

$\bar{u}\bar{y}\bar{z}$	$\bar{u}\bar{y}z$	$\bar{u}yz$	$u\bar{y}\bar{z}$
00	1	0	0
01	0	1	0
11	1	0	0
10	0	1	0

$$F = \underline{\hspace{2cm}}$$

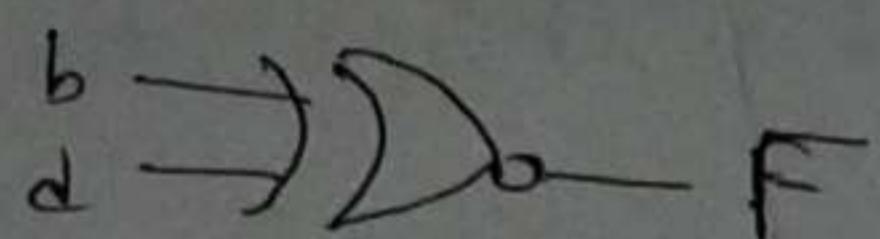
$$F = (a, b, c, d)$$

$$F = d + \bar{b}$$

a	b	c	d	
00	00	001	11	10
01	0	1	1	0
11	0	1	1	0
10	1	1	1	1

$$F = bd + \overline{b}\overline{d}$$

$$\therefore F = b \oplus d$$



ab	00	01	cd	11	10
00	1	0	0	1	
01	0	1	1	0	
11	0	1	1	0	
10	1	0	0	1	

$$f(a, b, c, d) = \sum (0, 1, 2, 5, 8, 9, 15)$$

5-C

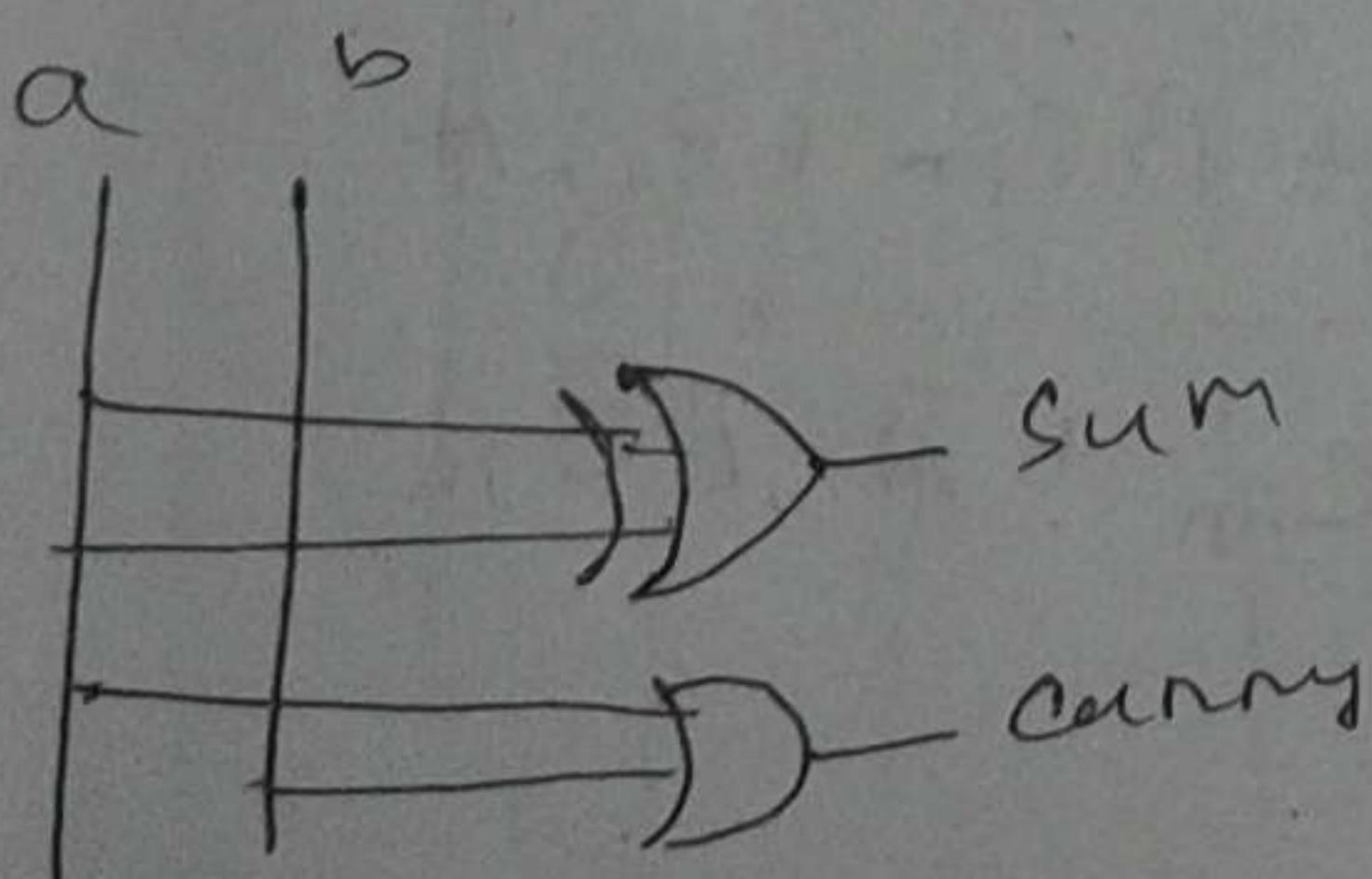
12.08.14

Design a half adder circuit

Adder \rightarrow Half Adder \rightarrow Add only two bit.

Full Adder $\frac{11}{11} = 3$ $\frac{11}{11} = 3$ $\frac{110}{110} = C$ } Can't solve by half adder

Input		Output	
A	B	C	S
0	0	0	0
0	1	0	1
1	1	1	0



sum:

A	B	S
0	0	0
0	1	1
1	0	1

Carry

A	B	C
0	0	0
0	1	1

$$S = A\overline{B} + \overline{A}B$$

$$C = A \oplus B$$

$$\Rightarrow A \oplus B$$

Input			Output	
A	B	Cin	Cout	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Sum: A

		Carry	
		A	\bar{A}
		0	1
$B C_{in}$	00	0	1
00	00	1	0
01	11	0	1
11	01	1	0
10	03	1	0
10	12	0	1
	6	2	6

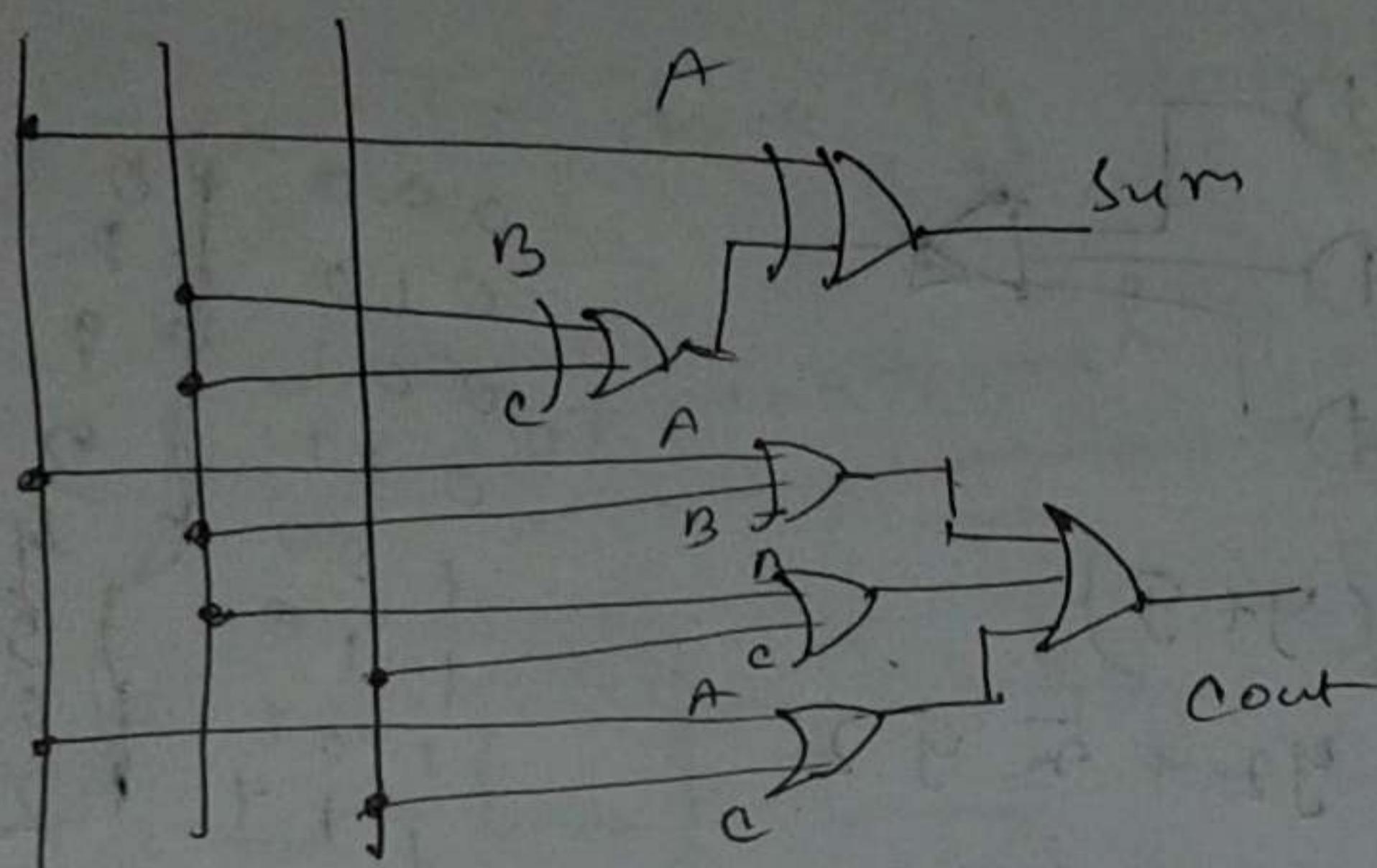
		Carry	
		A	\bar{A}
		0	1
$B C_{in}$	00	0	0
00	00	0	0
01	01	1	0
11	11	0	1
10	13	1	0
10	12	0	1
	7	3	7

$$Cout = AB + BC_{in} + C_{in}A$$

$$\text{Sum} = A \overline{B} \overline{C}_{in} + \overline{A} \overline{B} C_{in} + \overbrace{ABC_{in} + \overline{A} \cdot B \overline{C}_{in}}$$

$$\begin{aligned}
 &= A(\bar{B}\bar{C}_{in} + BC_{in}) + \bar{A}(\bar{B}C_{in} + B\bar{C}_{in}) \\
 &= A(\bar{B} \oplus C_{in}) + \bar{A}(B \oplus C_{in}) \\
 &= A \oplus (B \oplus C_{in})
 \end{aligned}$$

A B Cin



Design A full Subtractor circuit: } H.W
halt }

Five variable K-Map:

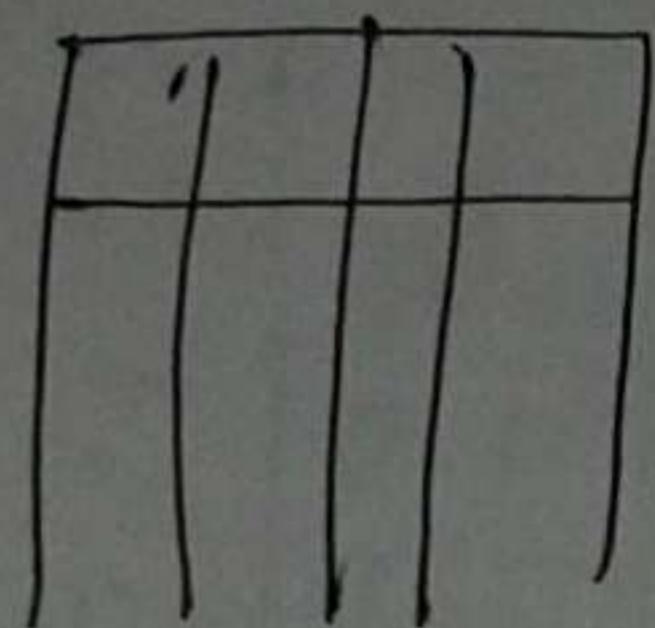
T	w	x	y	D2F
0	0	0	0	0
1	1	1	1	1
2	1	1	0	1
3	0	1	1	0
4	0	0	1	1
5	1	0	1	0
6	1	0	0	1
7	0	0	0	0

18.08.2014

C + solve

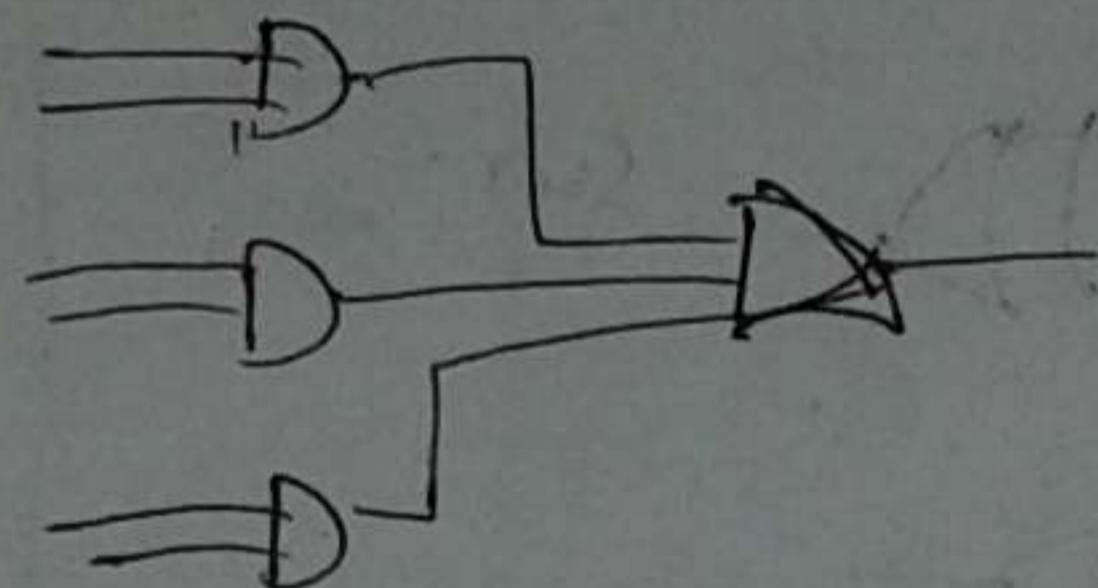
C - A

Q4



$$\bar{A}BC + AB\bar{C} + A\bar{B}\bar{C} + AB\bar{C}$$

$$\Rightarrow \bar{A}B + B\bar{C} + CA$$



Q3. $m_0 + m_1 + m_2$

0.0.0	0
0.1.0	1
0.0.1	2
0.1.1	3
1.0.0	4
1.1.0	5
1.0.1	6
1.1.1	7

$$\Rightarrow m_0(z + \bar{z}) + m_1(\bar{y} + y) + m_2(y + \bar{y})$$

$$= m_0 z + m_0 \bar{z} + m_1 \bar{y} + m_1 y + m_2 y + m_2 \bar{y}$$

$$= \sum (7, 6, 3, 1)$$

$$= \pi (0, 2, 4, 5)$$

$$= (x + y + z)(m + \bar{y} + z)(\bar{m} + y + \bar{z})(\bar{m} + y + \bar{z})$$

Q4. At $\begin{matrix} A \\ \bar{A} \end{matrix}$ $\begin{matrix} B \\ \bar{B} \end{matrix}$ $\begin{matrix} C \\ \bar{C} \end{matrix}$

=

$$= AB + B\bar{C} + CA + A + B + C$$

$$\Rightarrow A(B + 1) + B(C + 1) + C(A + 1)$$

$$\Rightarrow A + B + C$$

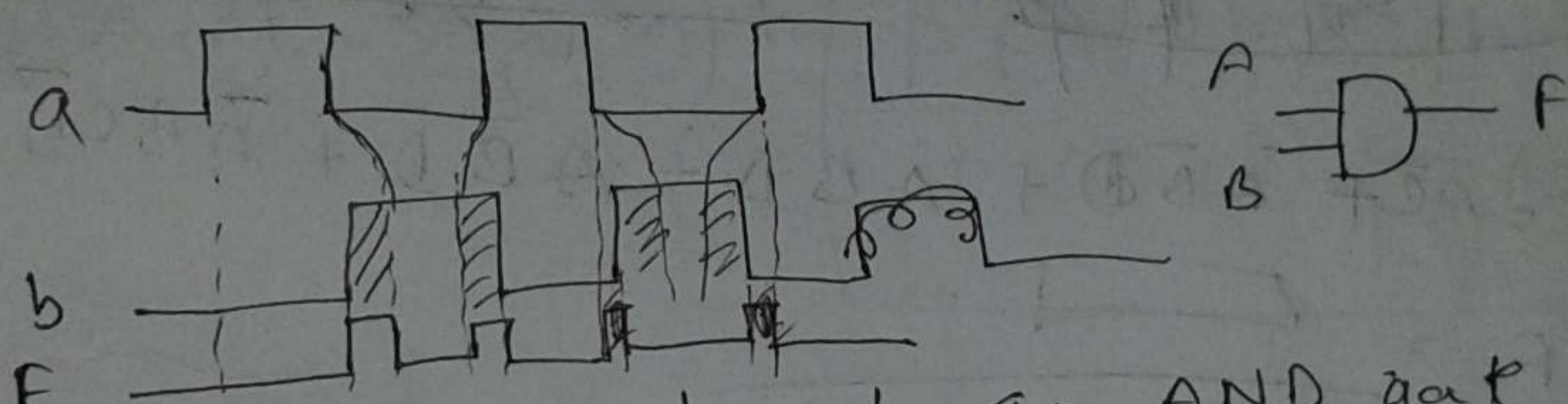
Complement of boolean function

$$\begin{aligned} F &= \overline{m y + \bar{n} z} \\ &= (\overline{m} y, \overline{\bar{n}} z) \\ &= (\bar{m} + y), (x + \bar{z}) \end{aligned}$$

It can be done by duality method

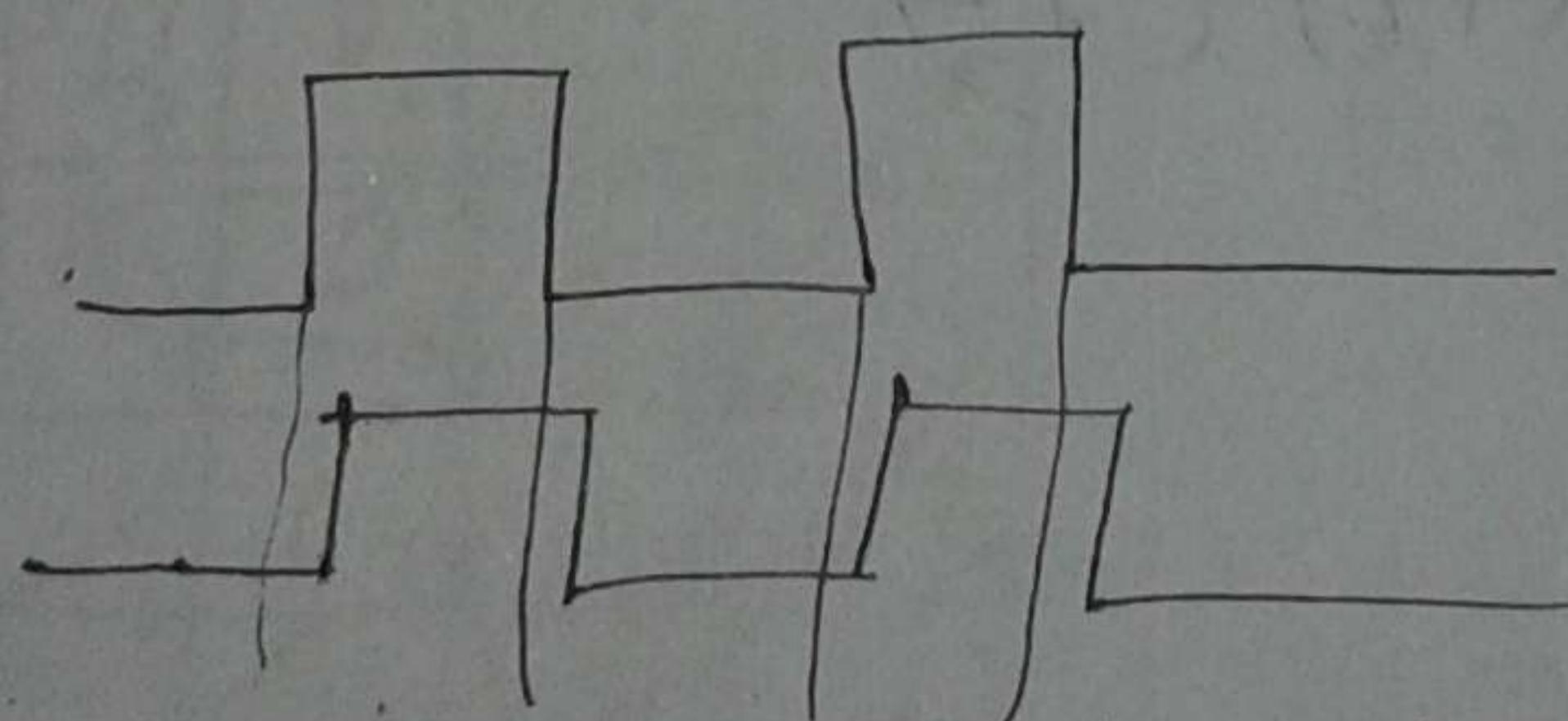
Combinational Logic Design

(Part II)



f is the output of an AND gate, Draw
the wave shape

[Tocci Book = Example]



ALU

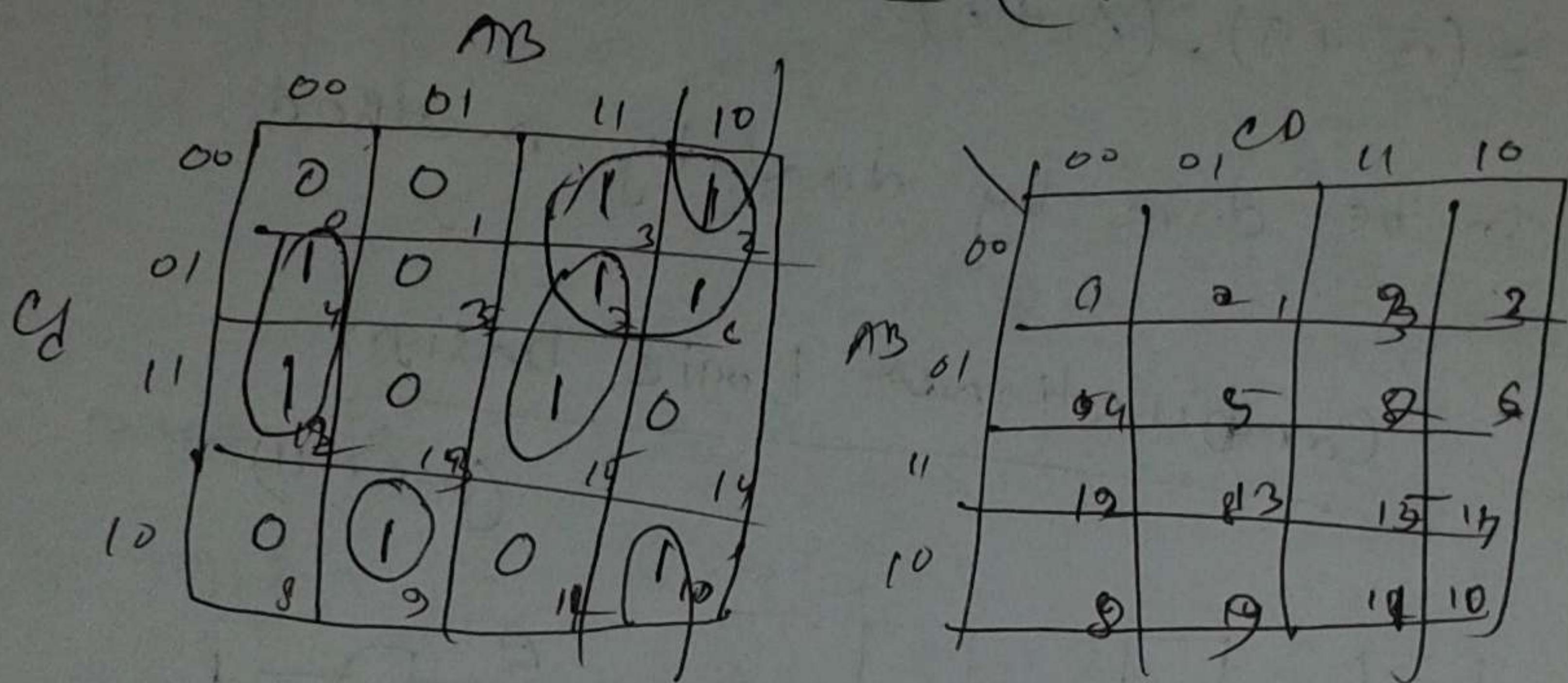
propagation Delay

29.08.14

G - E

CT# 2

Q1. $F(A, B, C, D) = \sum (1, 3, 6, 8, 9, 10, 12, 13, 15)$



$$F = A\bar{C} + \bar{A}\bar{B}\bar{D} + ABD + A\bar{B}\bar{D} + \bar{A}BC\bar{D}$$

Q2:

$$\begin{aligned} F &= \boxed{\quad} \\ F &= \overline{wz} + \overline{wz} + \overline{yz} \end{aligned}$$

$$z(\overline{wz}) \cdot (\overline{wz}) \cdot (\overline{yz})$$

$$= (\overline{w} + \overline{z}) \cdot (\overline{w} + \overline{z}) (yz)$$

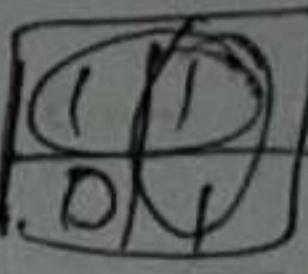
$$= (\overline{w} + \overline{z}) (w + \overline{z}) (yz)$$

K-Map with don't care functions:

		A		
		0	1	
B		0	1	X ← don't care
1		0	1	

$$F = A\bar{B} + \bar{A}\bar{B} \quad (\times \rightarrow 0 \Sigma(\bar{A}))$$

$$F = \bar{A}B + \bar{B} \quad (\times \rightarrow 1 \Sigma(\bar{B}))$$

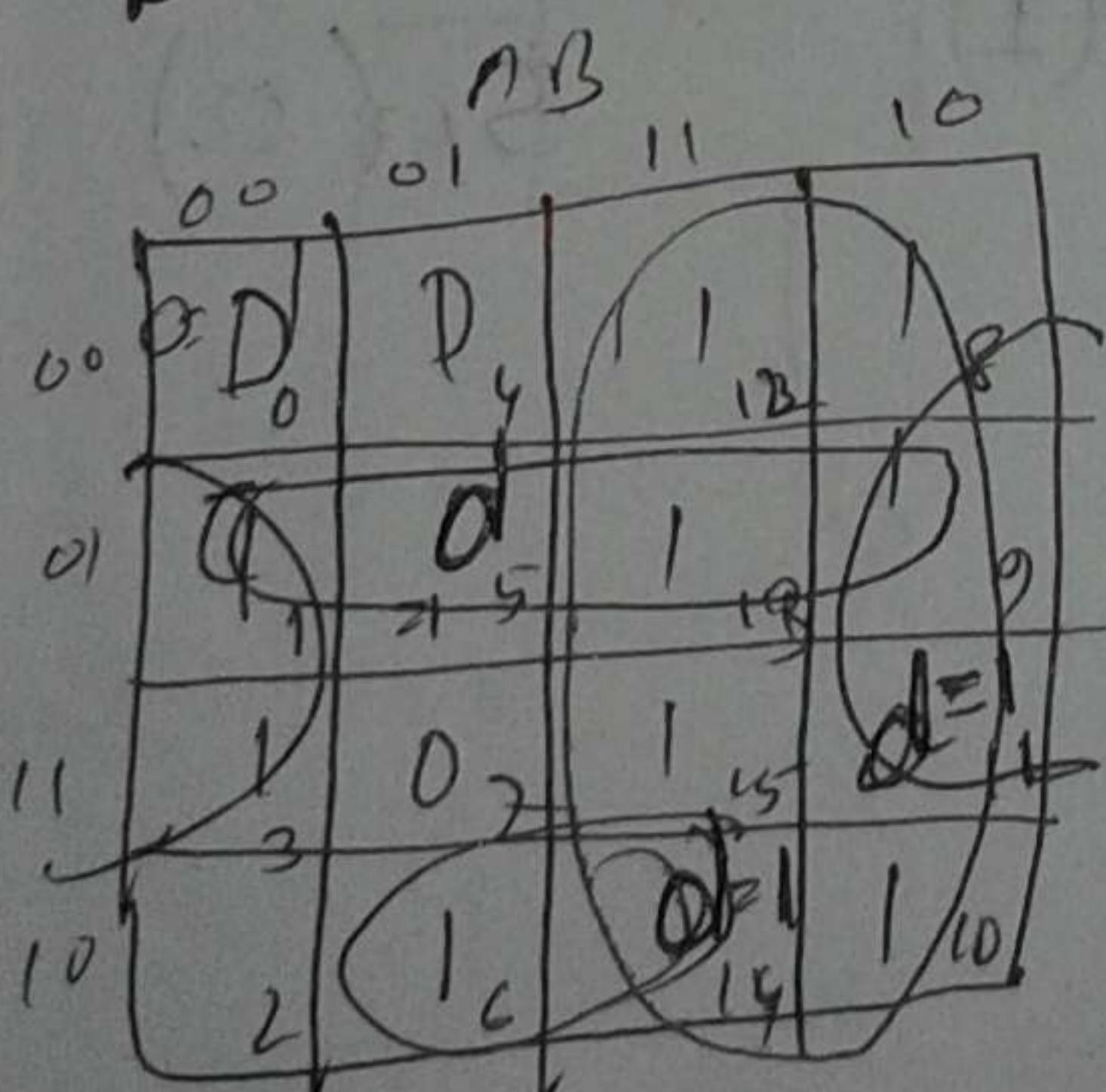


$$f(A, B) = \sum(0, 3)$$

$$\begin{aligned} P(A, 0) &= \sum(0, 3) \\ \& \& d(A, B) &= \sum(2) \end{aligned}$$

$$F(A, B, C, D) = \sum(0, 1, 3, 6, 8, 9, 10, 12, 13, 15)$$

$$D(A, B, C, D) = \sum(0, 5, 11, 14)$$



$$F = A + \bar{C}D + \bar{B}D + \bar{B}C\bar{D}$$

To get
minterms
Bⁿ

$$F(A, B, C, D) = \pi(0, 4, 8, 12) \Rightarrow \text{mean term}$$

(12010101)

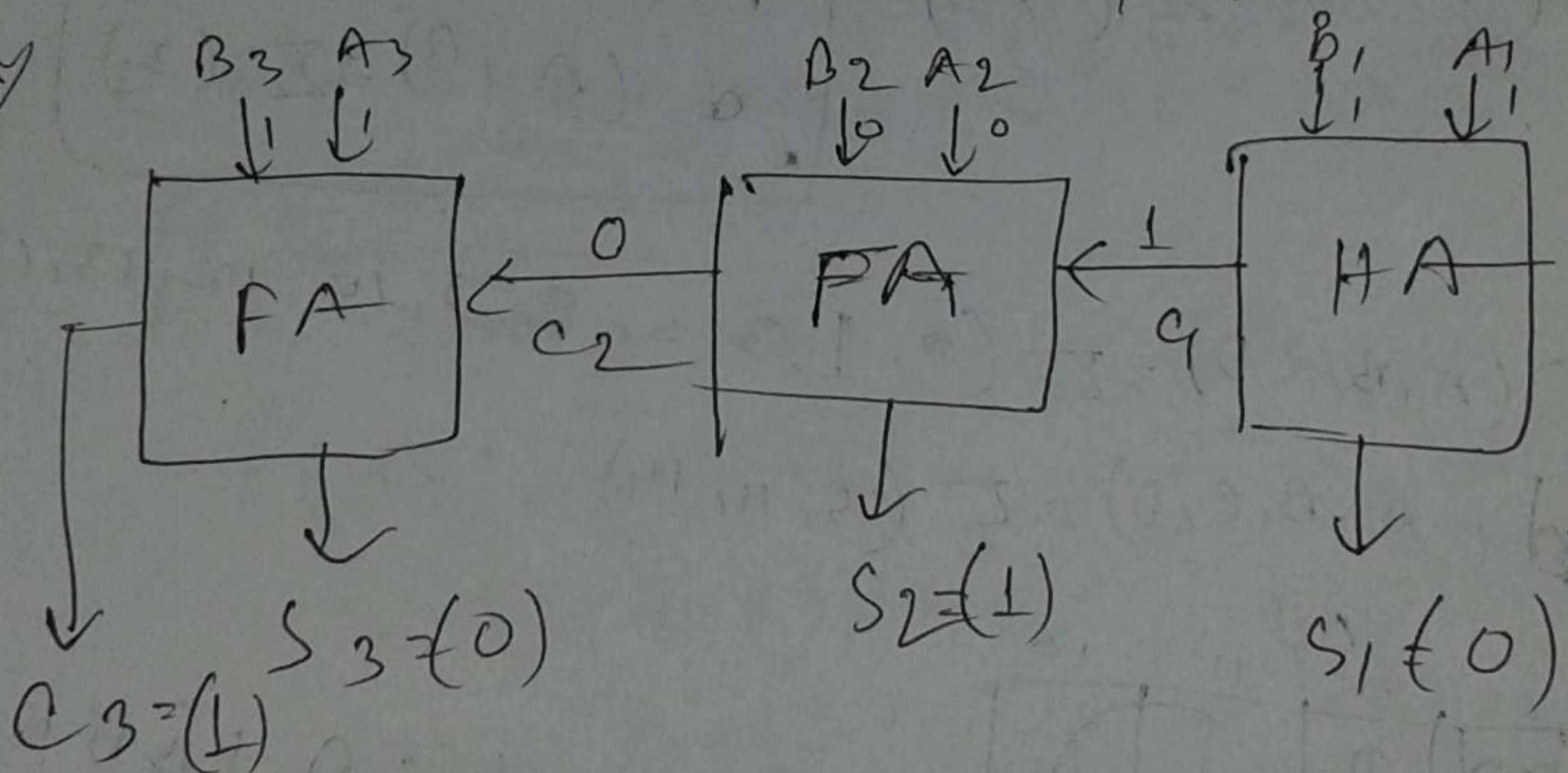
(10010101011111)

Design a parallel binary adder/Subtractor:

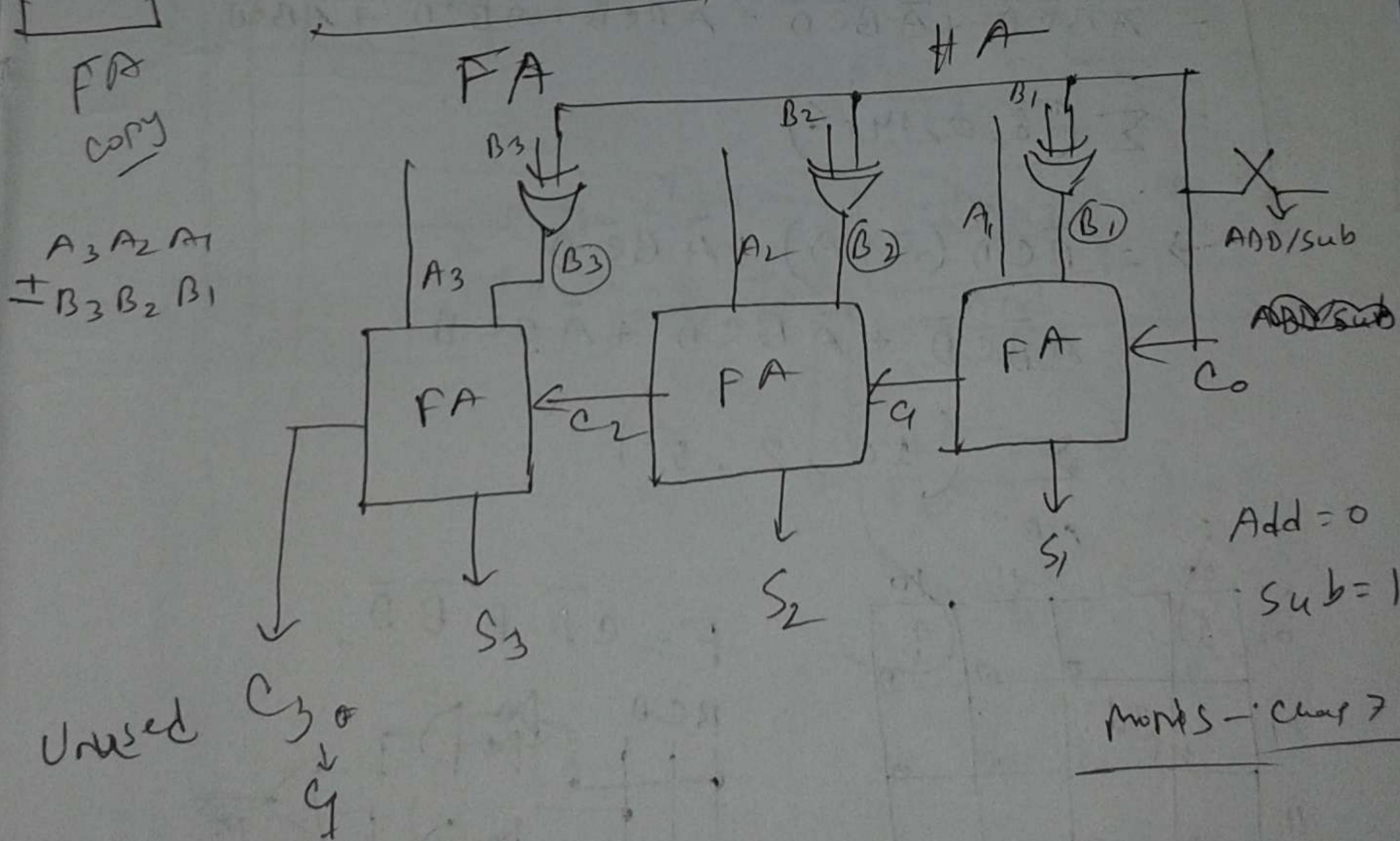
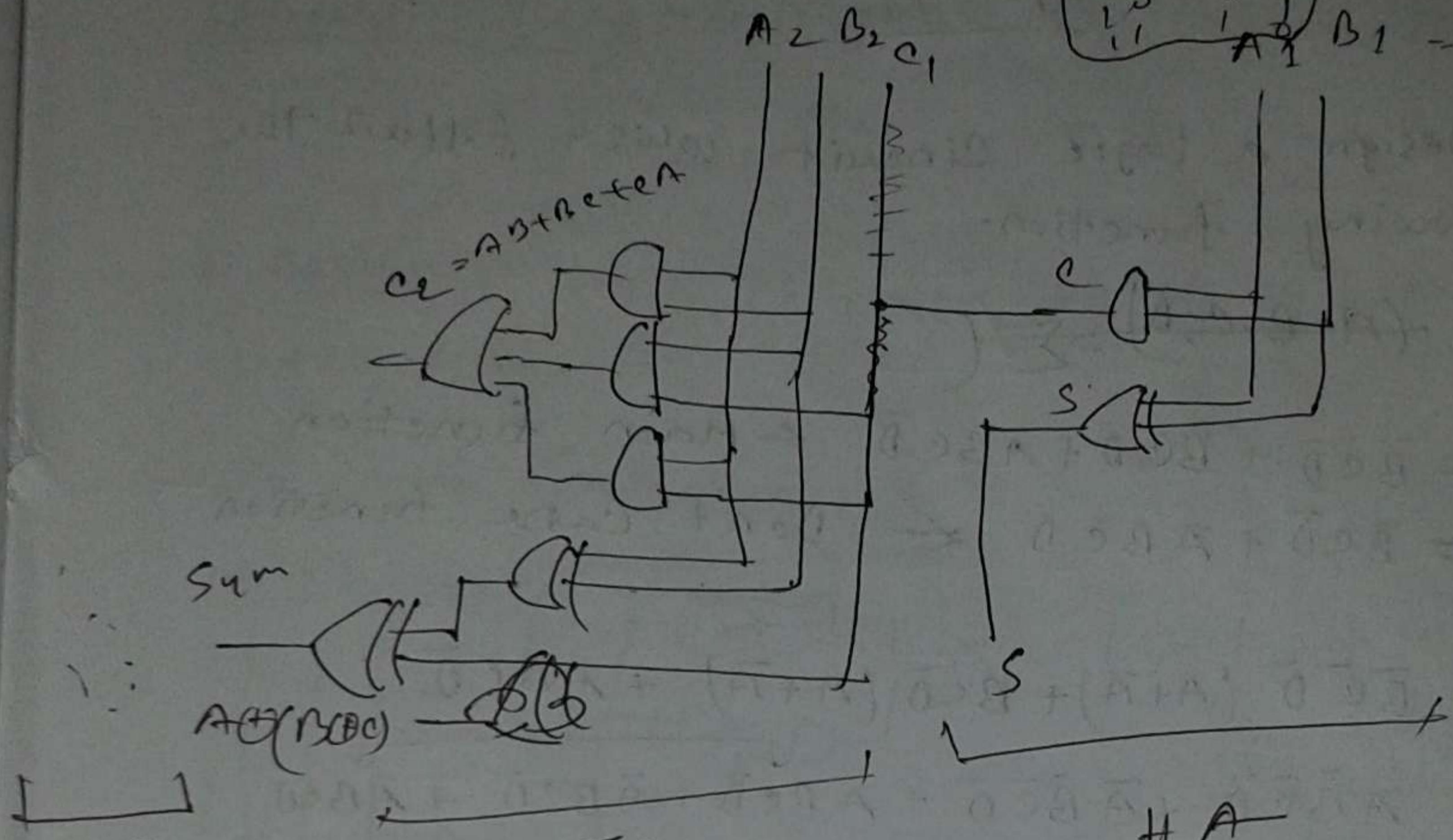
$$\begin{array}{r} A \rightarrow A_3 A_2 A_1 (101) \\ B \rightarrow B_3 B_2 B_1 (101) \\ \hline 1010 \end{array}$$

$$\begin{array}{r} 10 \\ 10 \\ \hline 1010 \end{array}$$

FA = Full Adder
HA = Half Adder



$$\begin{pmatrix} AB & C & S \\ 0 & 0 & 0 \\ 0 & 1 & 0 \\ 1 & 0 & 1 \\ 1 & 1 & 1 \end{pmatrix} \quad \begin{array}{l} AB + A\bar{B} \\ B_1 = AC \oplus B \end{array}$$



25.08.14

7-A

Design a logic circuit which follow the following function.

$$F(A, B, C, D) \rightarrow \sum($$

$$f = \bar{B}\bar{C}\bar{D} + BC\bar{D} + ABC\bar{D} \leftarrow \text{Main function}$$

$$d = \bar{B}\bar{C}\bar{D} + \bar{A}BC\bar{D} \leftarrow \text{Don't care function}$$

$$\Rightarrow = \bar{B}\bar{C}\bar{D}(A + \bar{A}) + BC\bar{D}(A + \bar{A}) + ABC\bar{D}$$

$$= A\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}\bar{D} + \underbrace{ABC\bar{D}}_{\bar{A}BC\bar{D}} + \underbrace{\bar{ABC}\bar{D}}_{\bar{A}BC\bar{D}}$$

$$= \sum(8, 0, 14, 6)$$

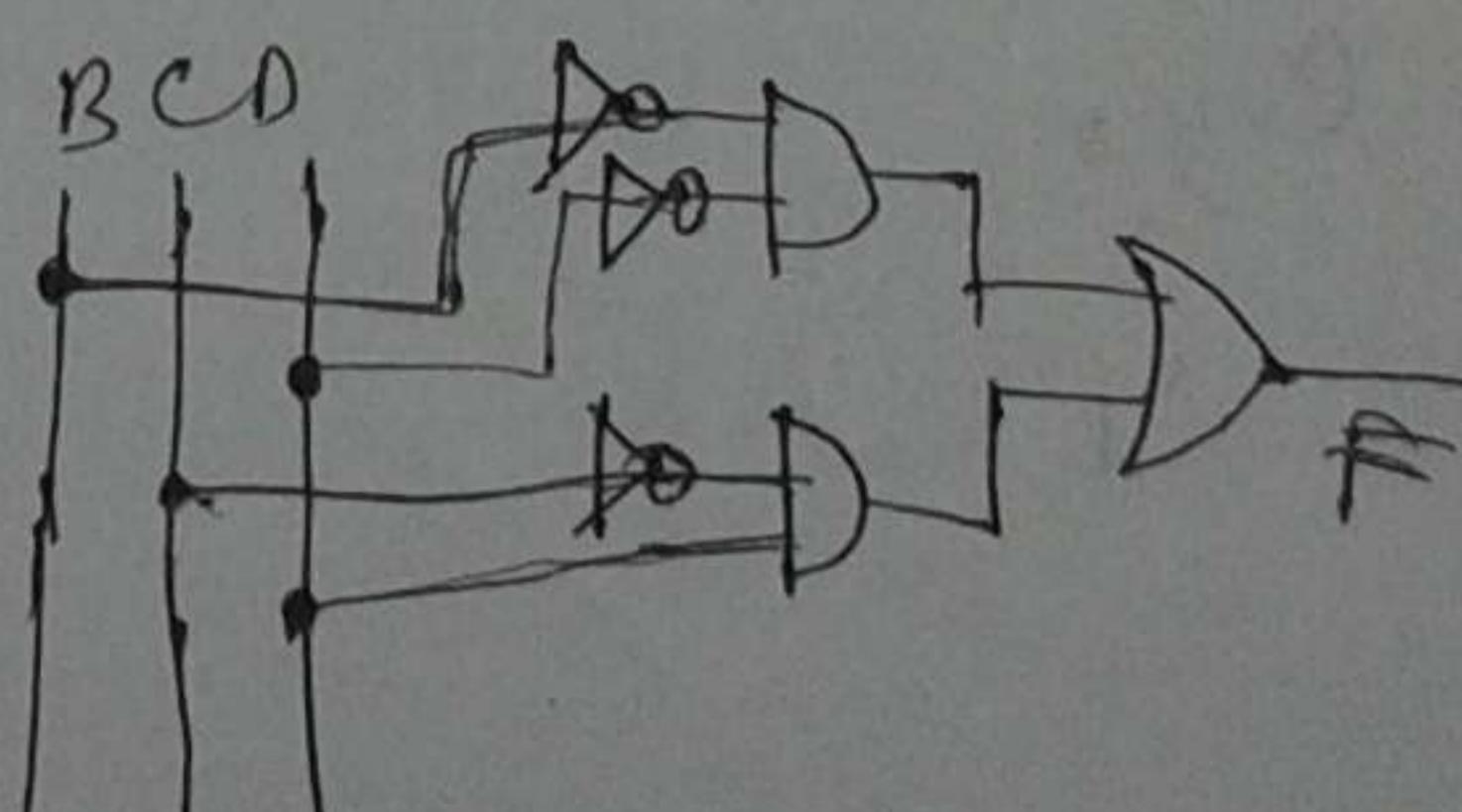
$$\Rightarrow = \bar{B}\bar{C}\bar{D}(A + \bar{A}) + \bar{A}\bar{B}\bar{C}\bar{D}$$

$$= A\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}B\bar{C}\bar{D}$$

$$= \sum(10, 2, 5)$$

		AB	CD		
		00	01	11	10
		00	1	0	1
		01	0	1	0
		11	0	0	0
		10	1	1	0

$$F = \bar{C}\bar{D} + \bar{B}\bar{D}$$



Chapter - 9 → Morris ~~notes~~

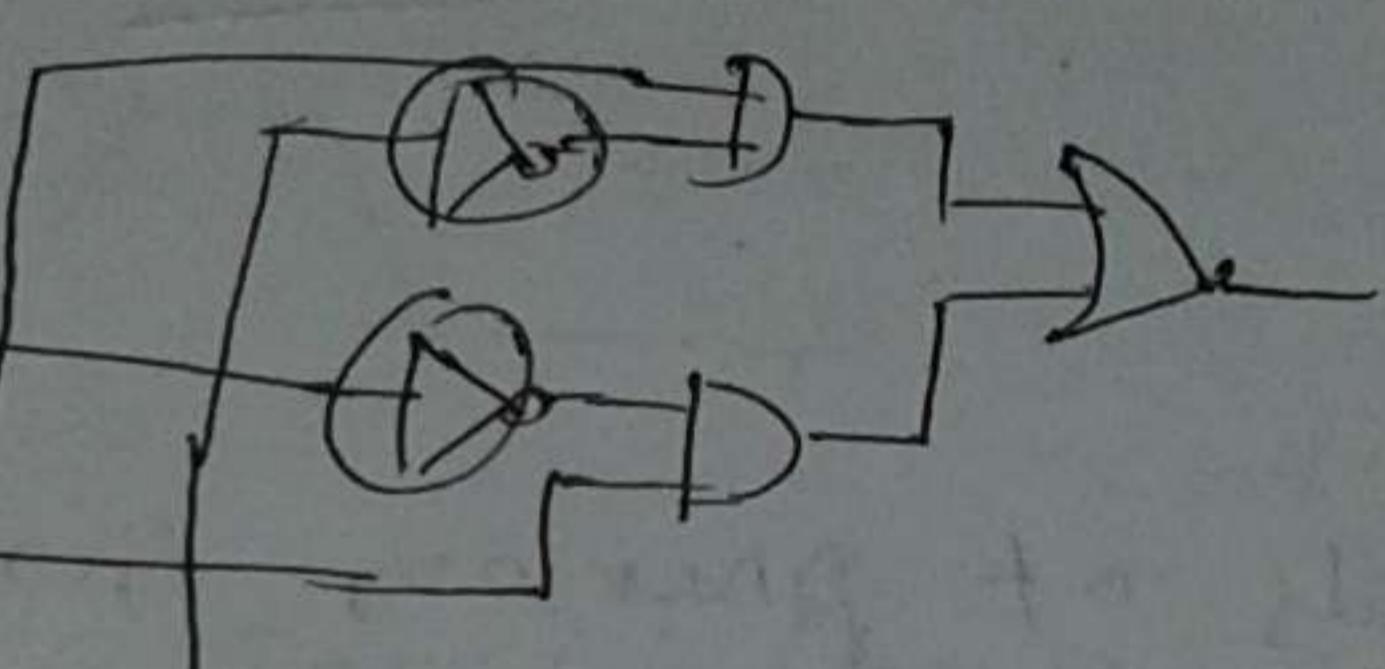
4.4

Design a logic circuit by using universal gates only.

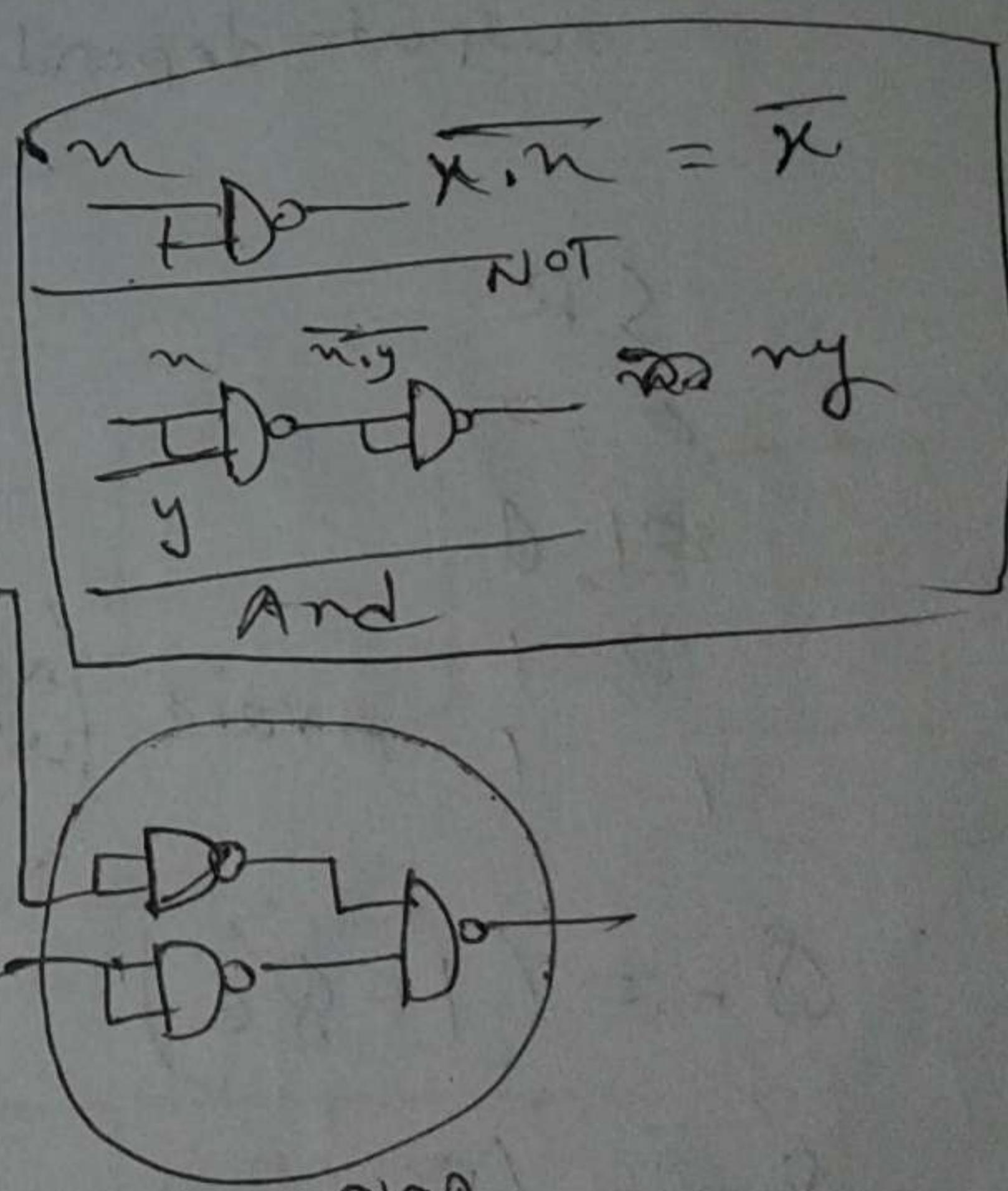
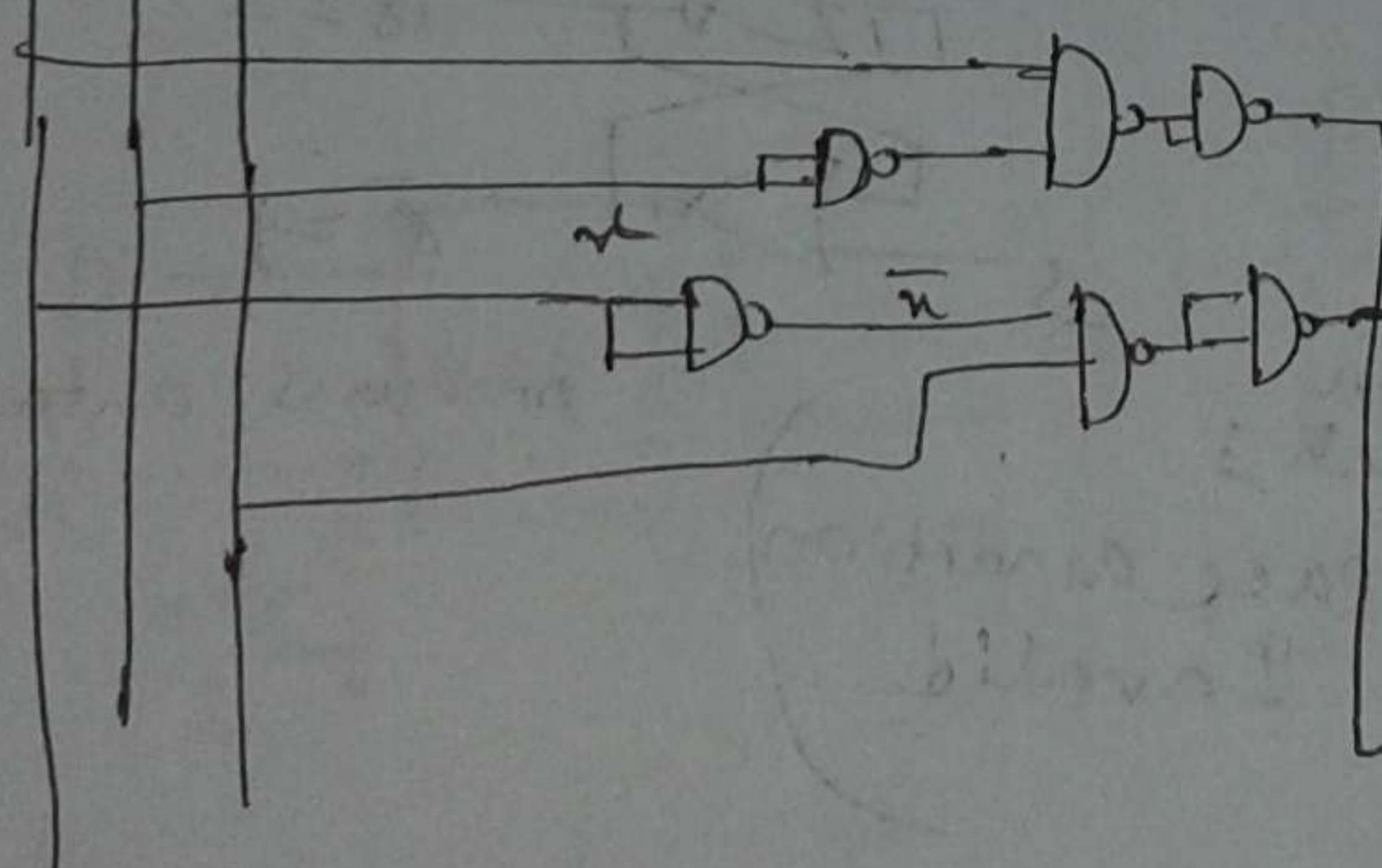
$$f = \bar{m}y + \bar{n}z$$

To see

$m \bar{y} z$



(without universal gate)



Design a BCD adder circuit (Self
study)

Hints: Follow chapter 6 of Toocci

7-C

27.08.14

Sequential logic circuit

Reset/Set

RS Non Latch

output depends of previous input

SR

0 0

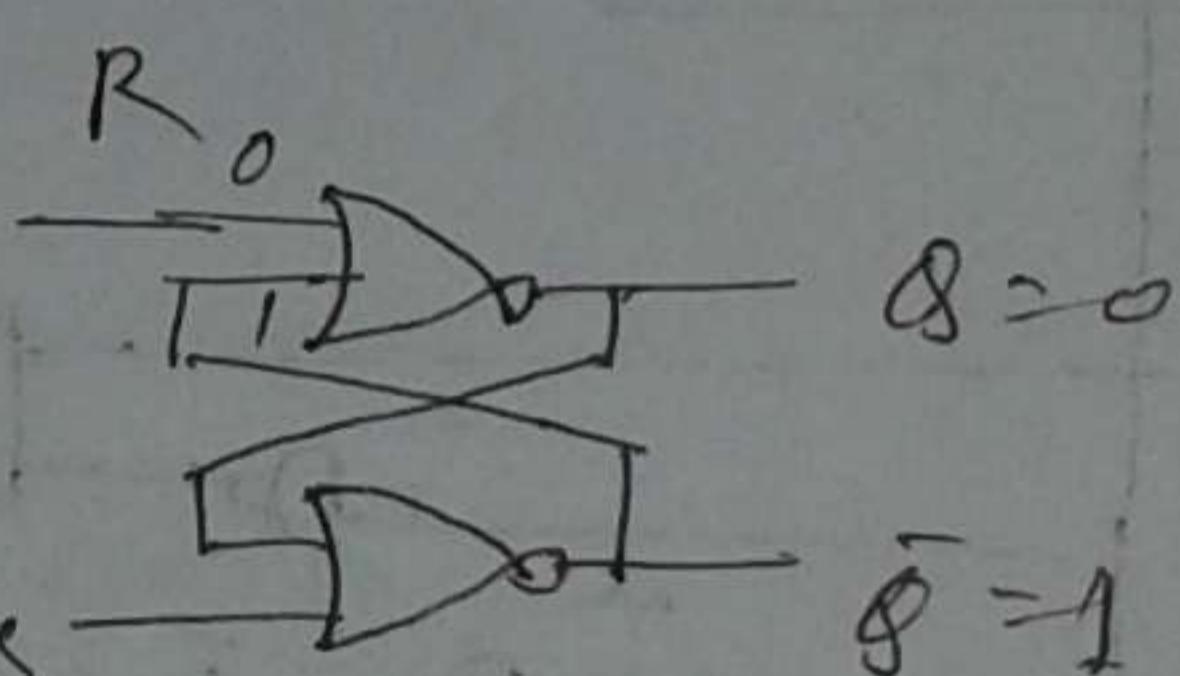
0 1

0 1

Avoid (Non
latching)
Race condition
Invalid

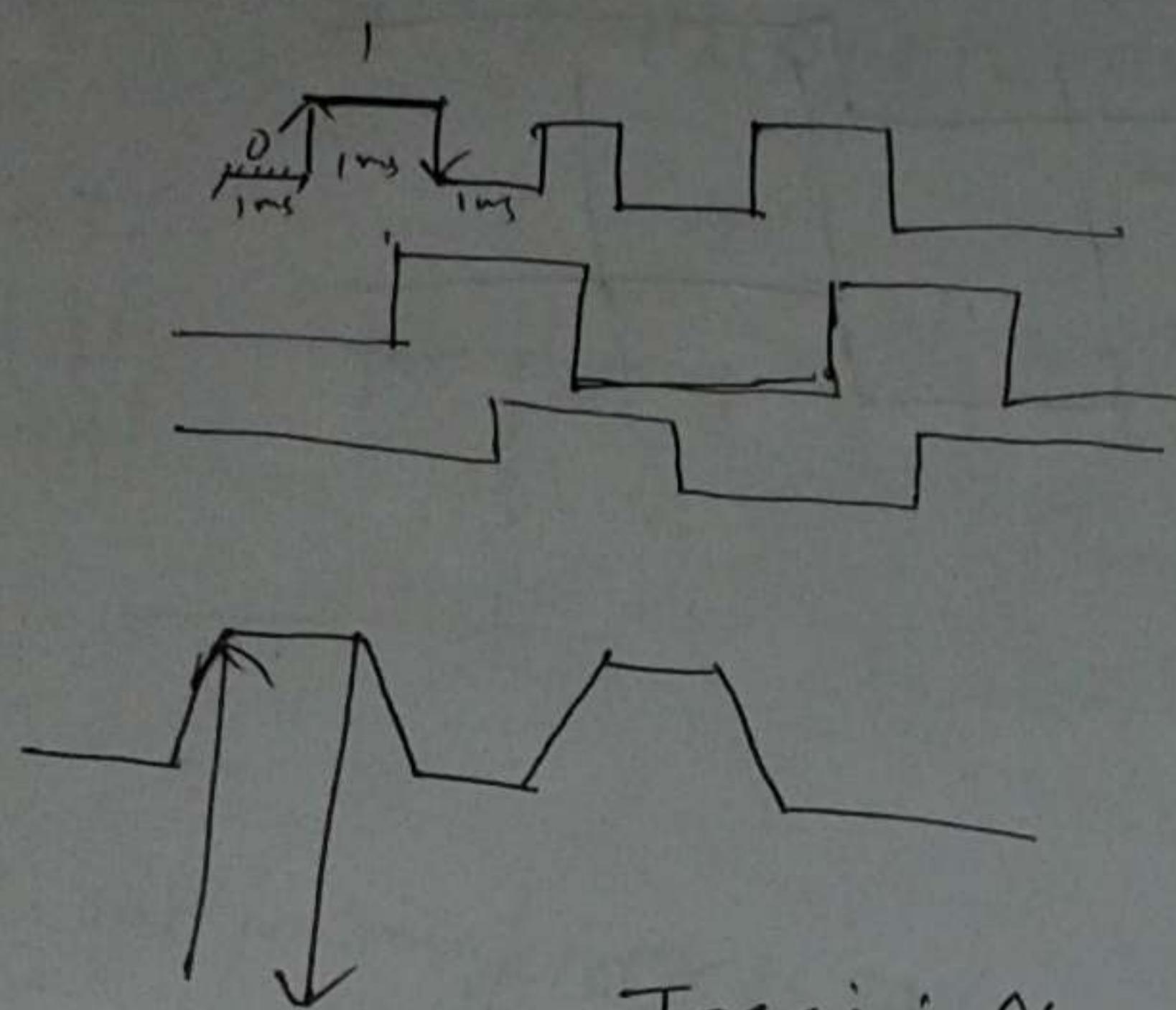
$$Q_n = (1 + \bar{Q}'_0)$$

$$\bar{Q}'_n = (1 + Q_0)$$



previous output

$\#$ Data
 \oplus D late & try to overcome limitation
 CLK = clock signal



Trigger

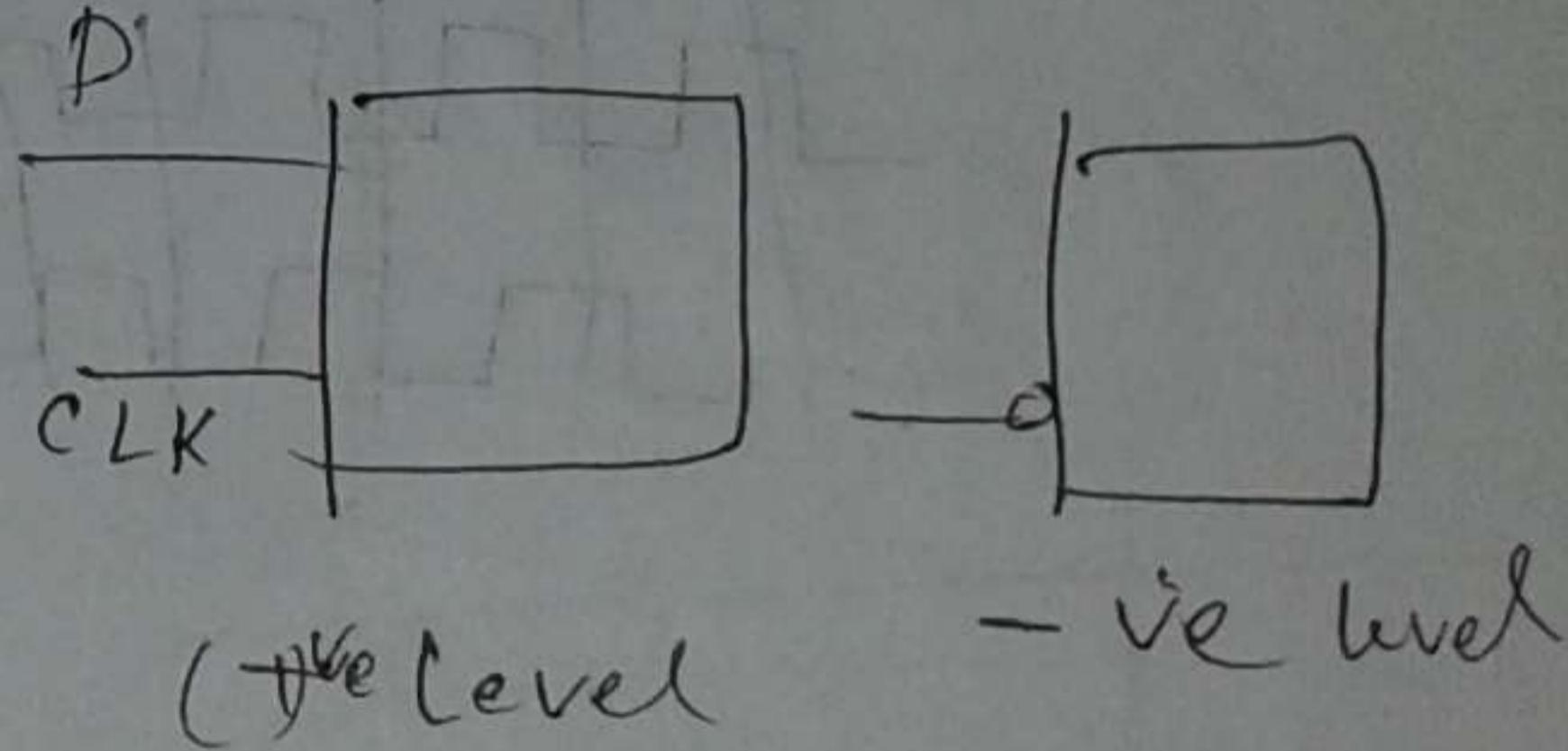
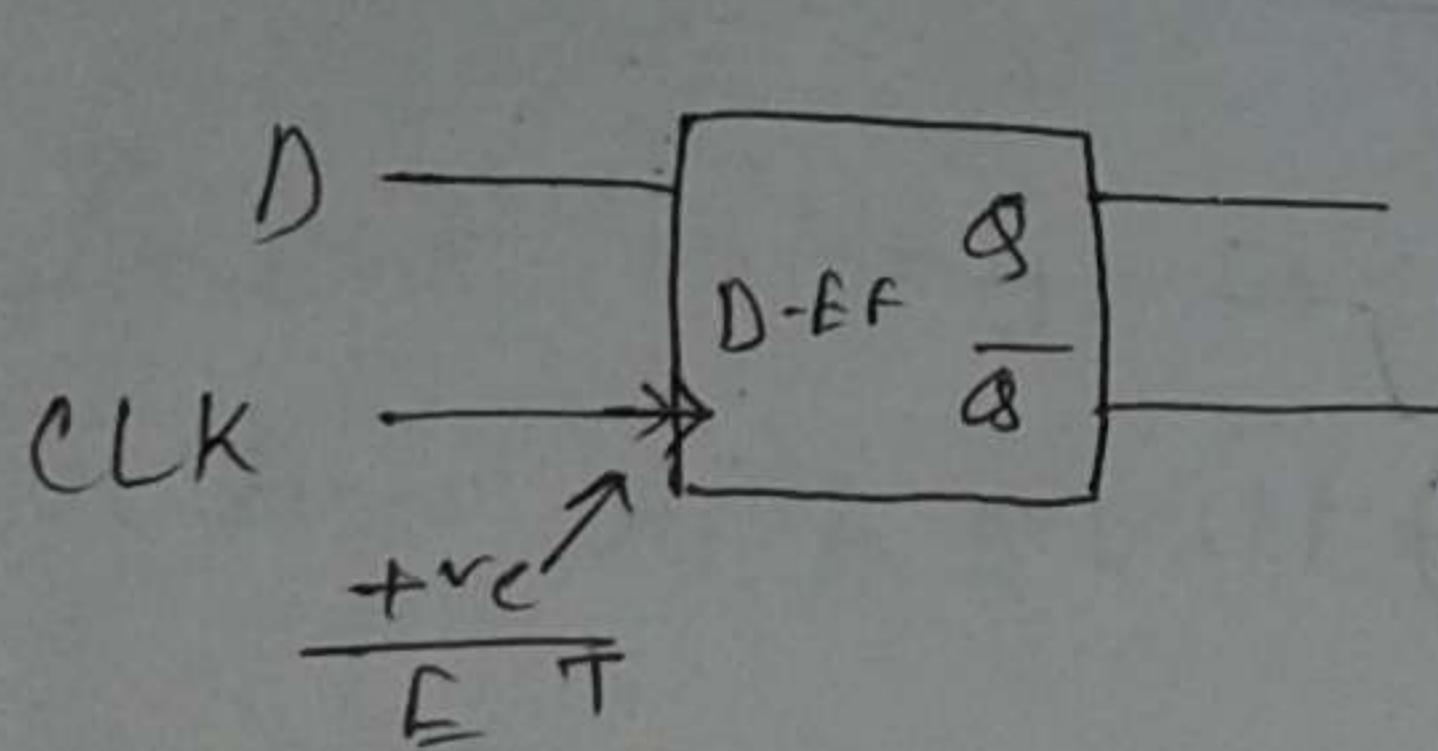
level triggering

- \rightarrow (+) ve level
- \leftarrow (-) ve level

Edge triggering

- \rightarrow (+) ve Edge
- \leftarrow (-) ve " "

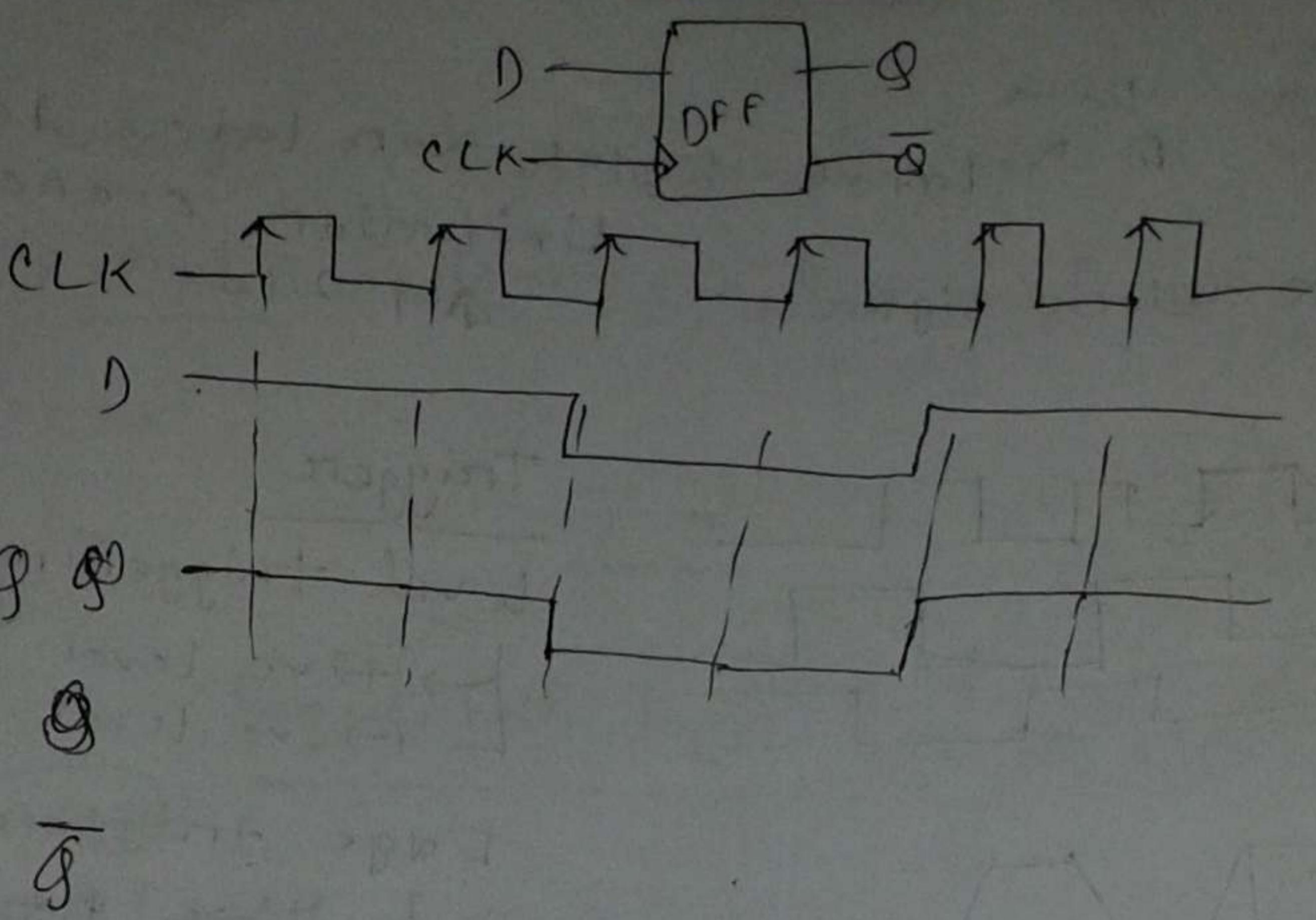
Tocci : Chap - 4/5



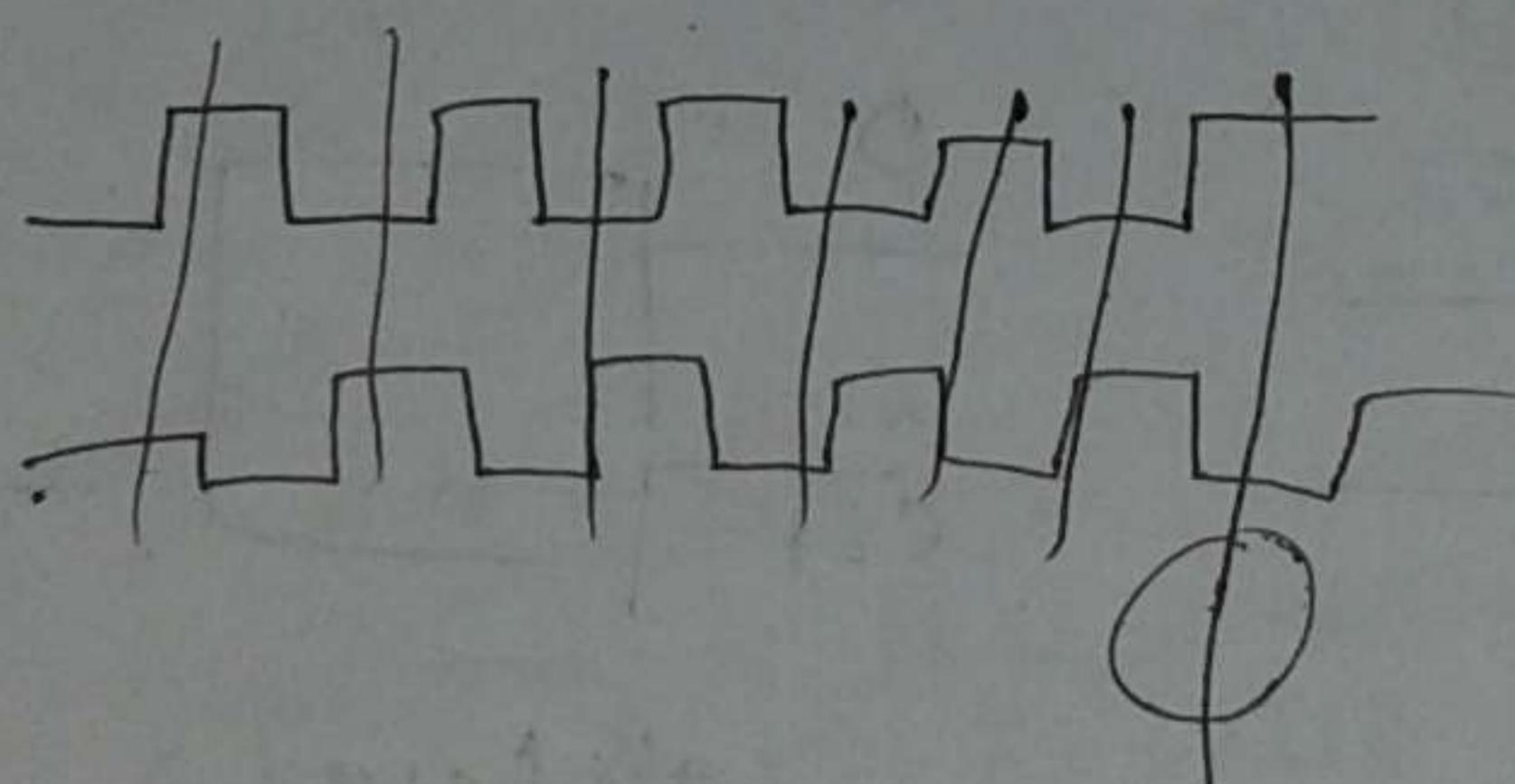
\rightarrow - ve Edge triggering

CLK	D	Q	\bar{Q}
\downarrow	X	NC	NC
\downarrow	X	NC	NC
\uparrow	0	0	1
\uparrow	1	1	0

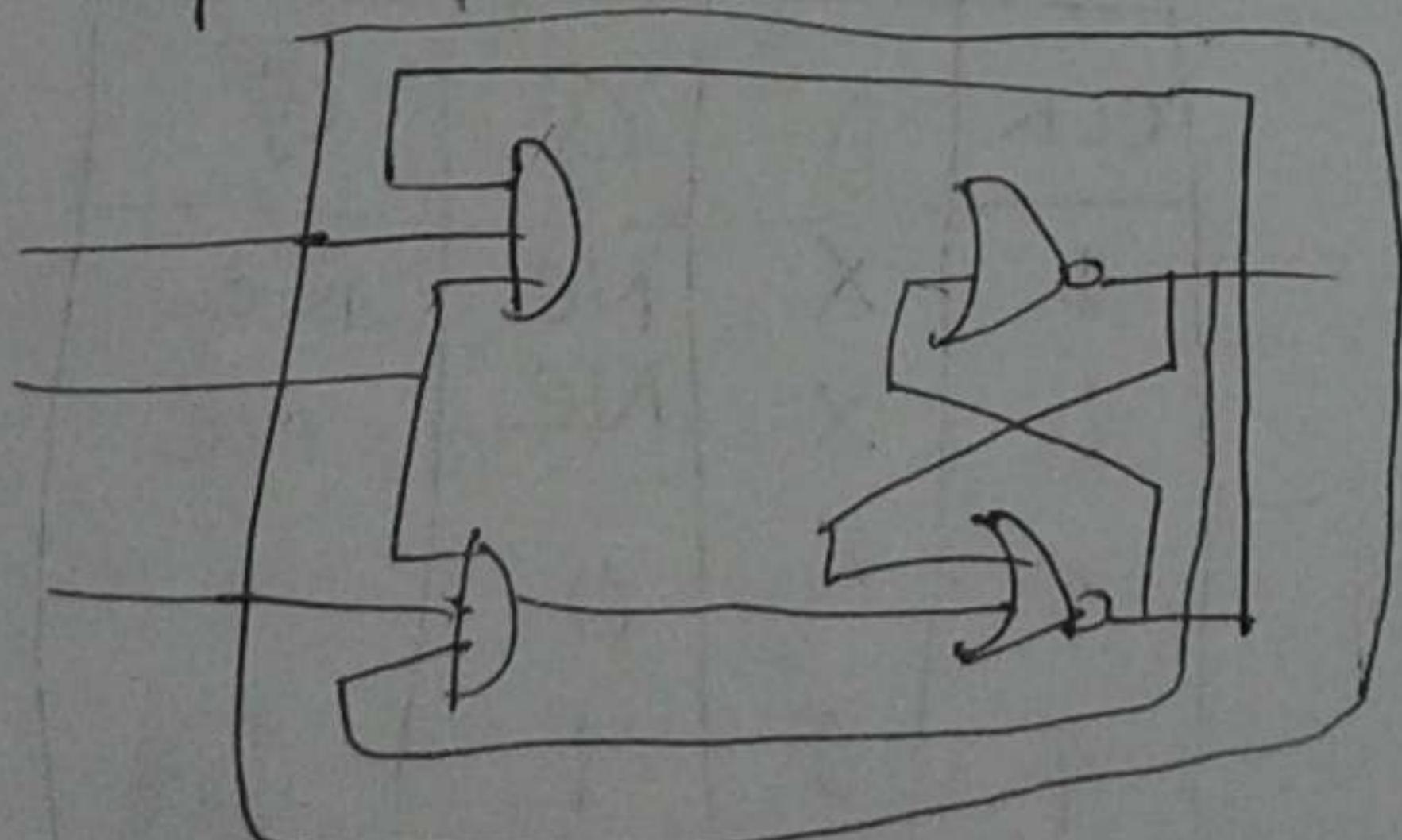
NC = No change



SR Flip Flop:



JK Flip Flop:

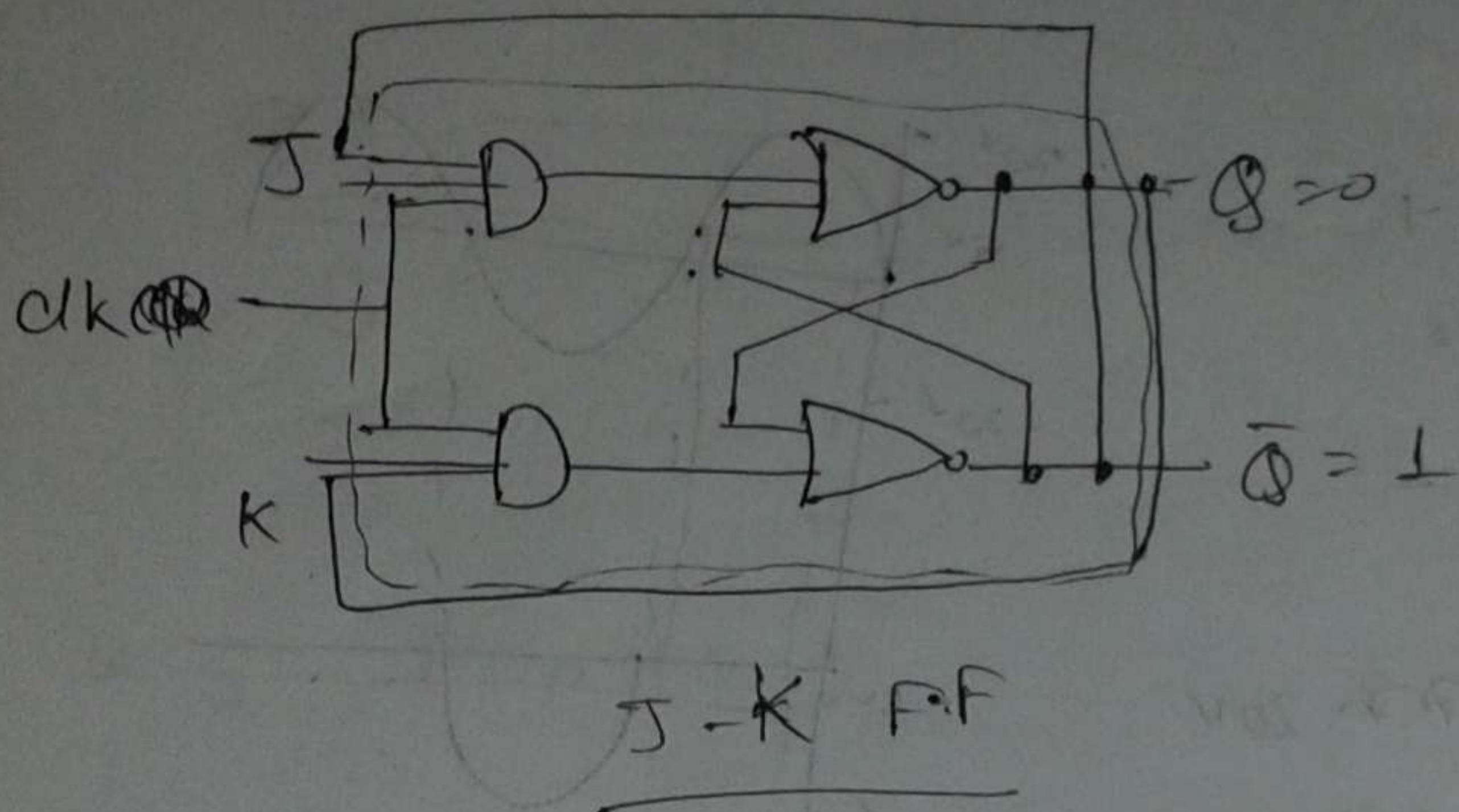


Morris Fig!
G.6

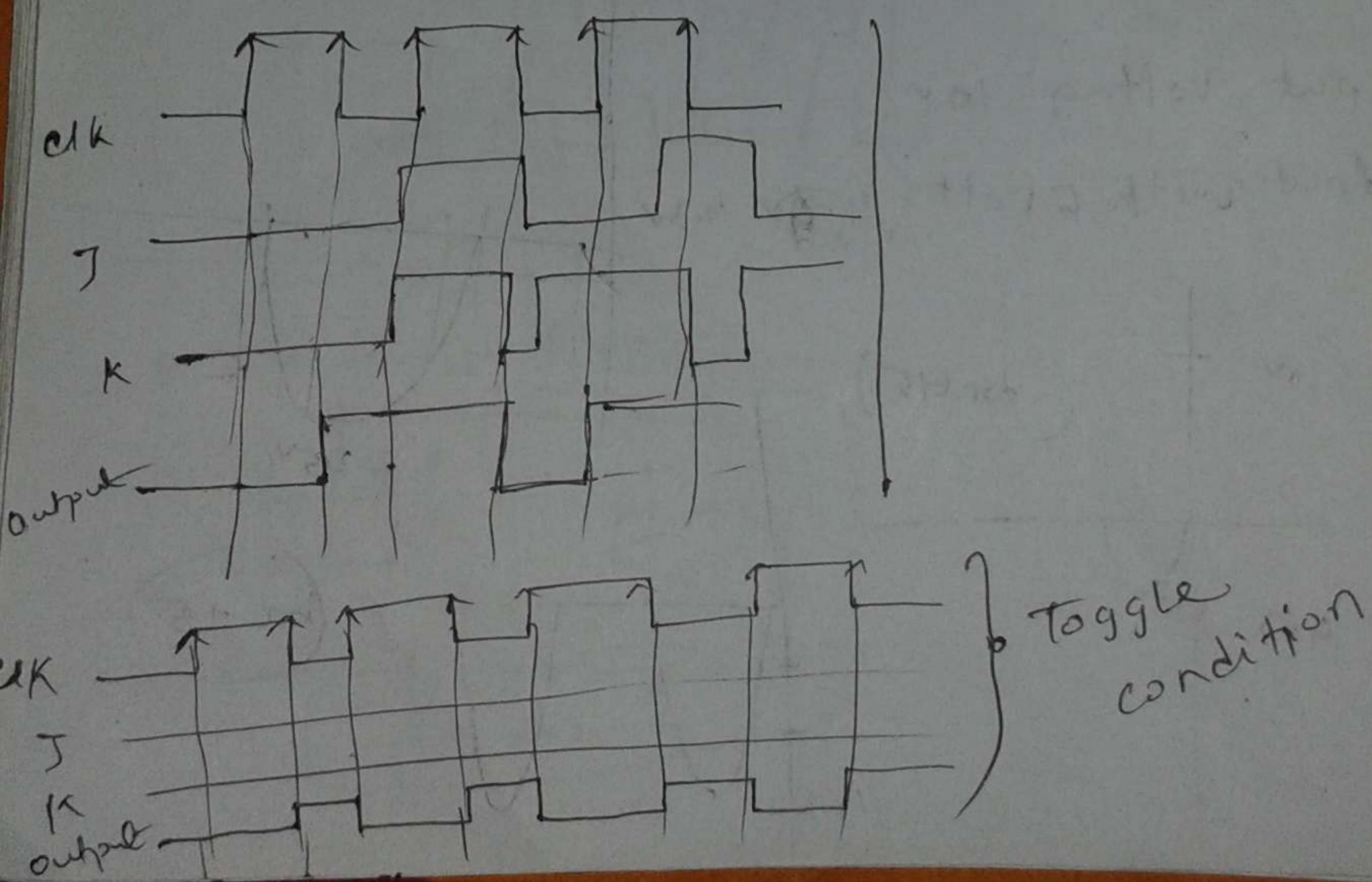
02.08.14

J - E

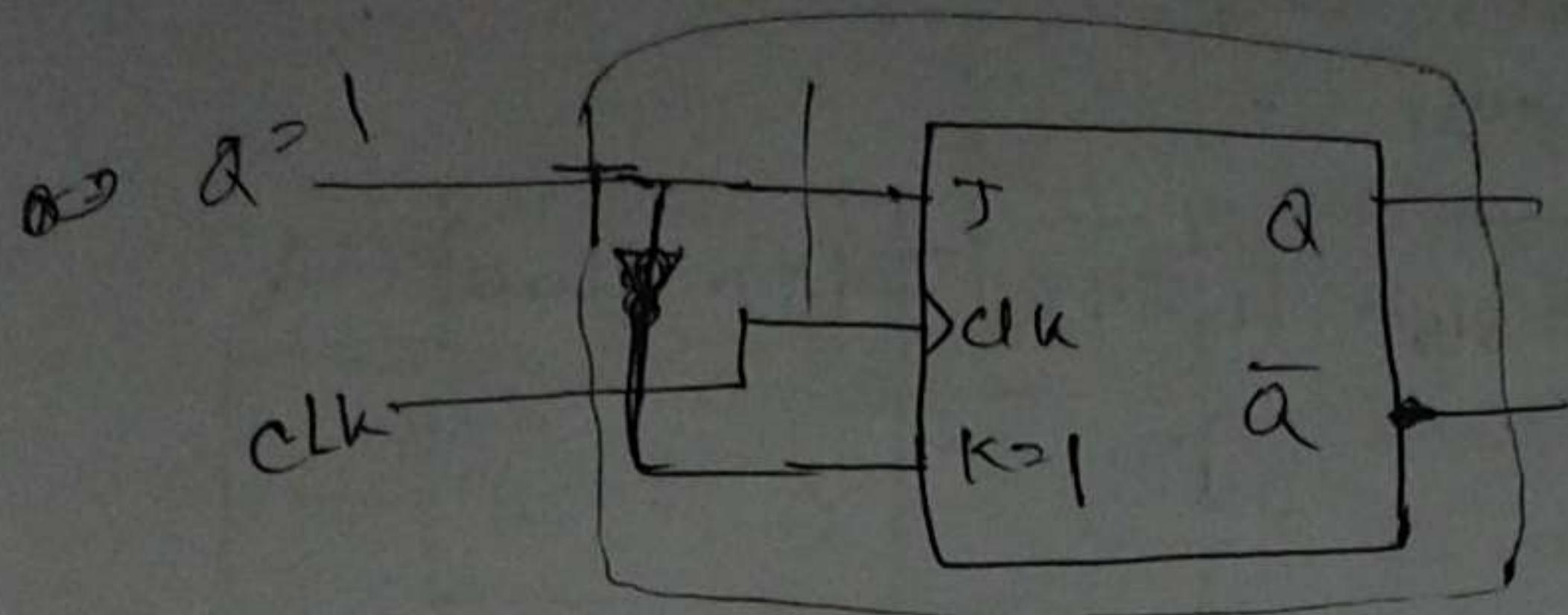
flip flop is the memory element, it's
a bistable device



J - K F.F



T - FlipFlop



$$\begin{array}{ll} 0 & 0 = 0 \\ 1 & 1 = 1 \end{array}$$

State diagram, State table
State mechanism.

03.09.14

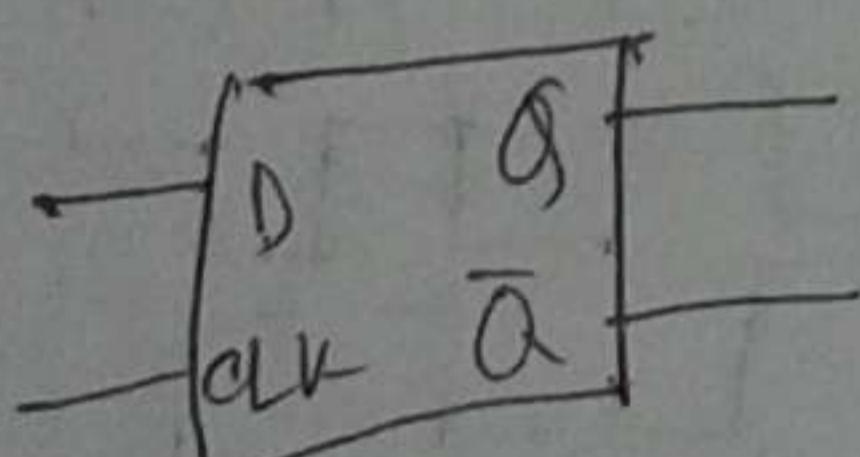
8-A

Derivation table for all FlipFlop:

flip flop conversions

Q	T	D	
0	0	0 - $\bar{Q}T$	$D = \bar{T}Q + Q'T^2$
0	1	1	$+ \Theta Q$
1	0	0	$+ \bar{Q}$

$$D = T \oplus Q$$

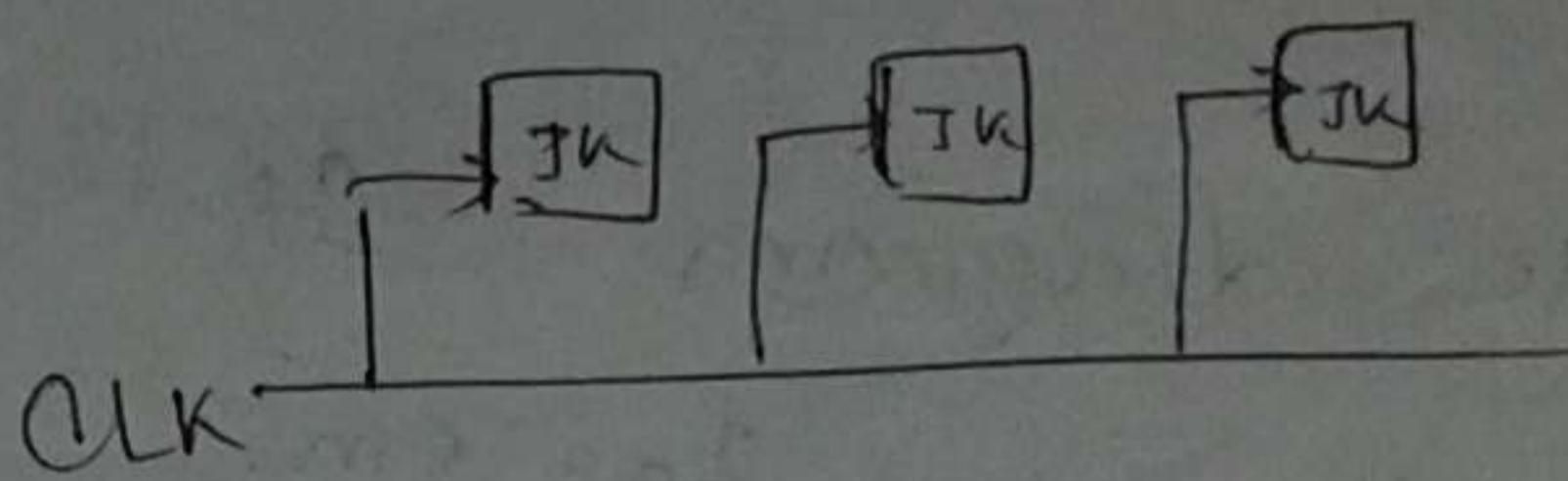


Assignment → see 2nd last

Counter: \rightarrow Synchronous Counter
Asynchronous

All counter are design with flip flop and basic gates.

Q) Synchronous:



Asynchronous/:

binary counter/

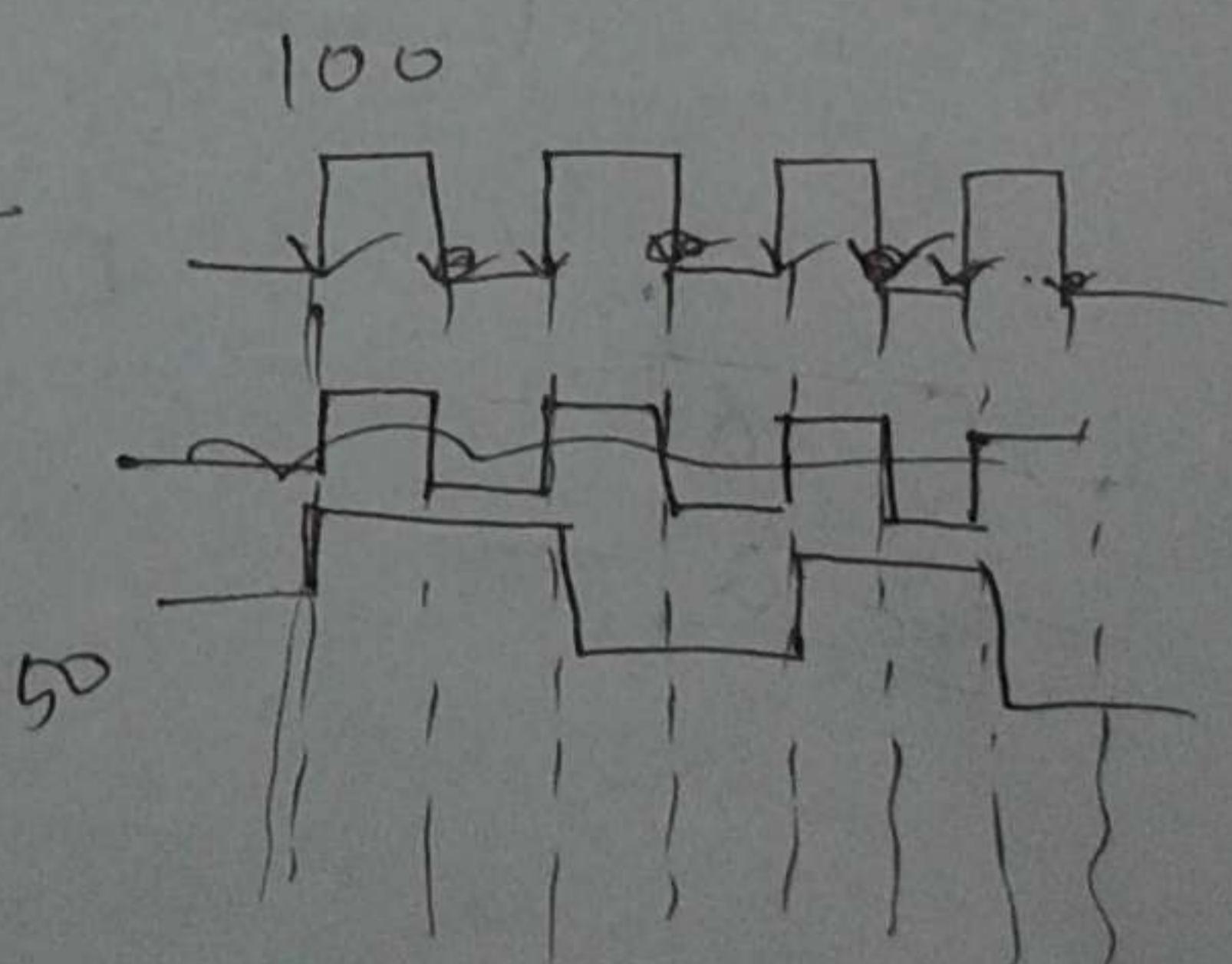
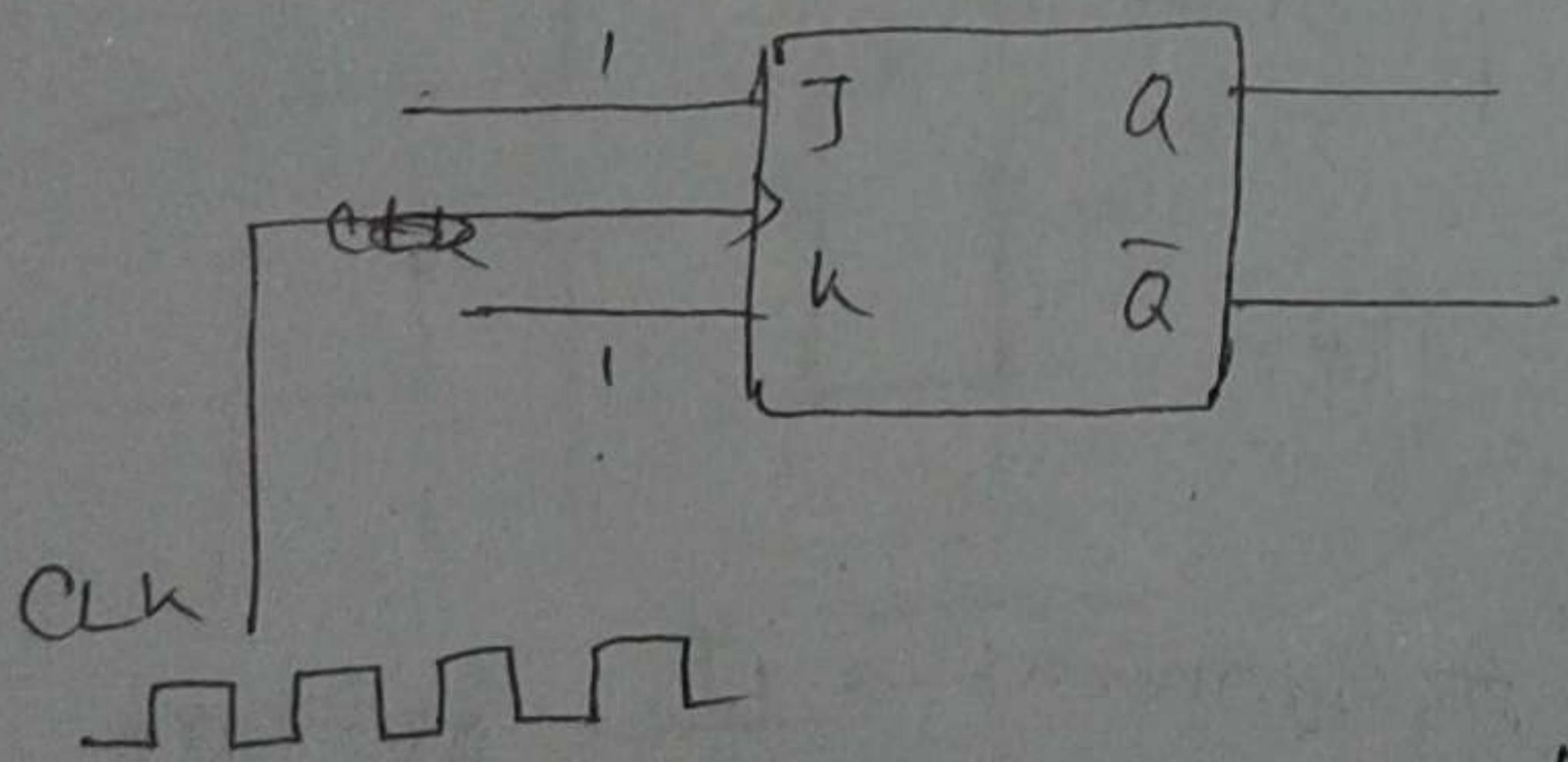
divided by two counter

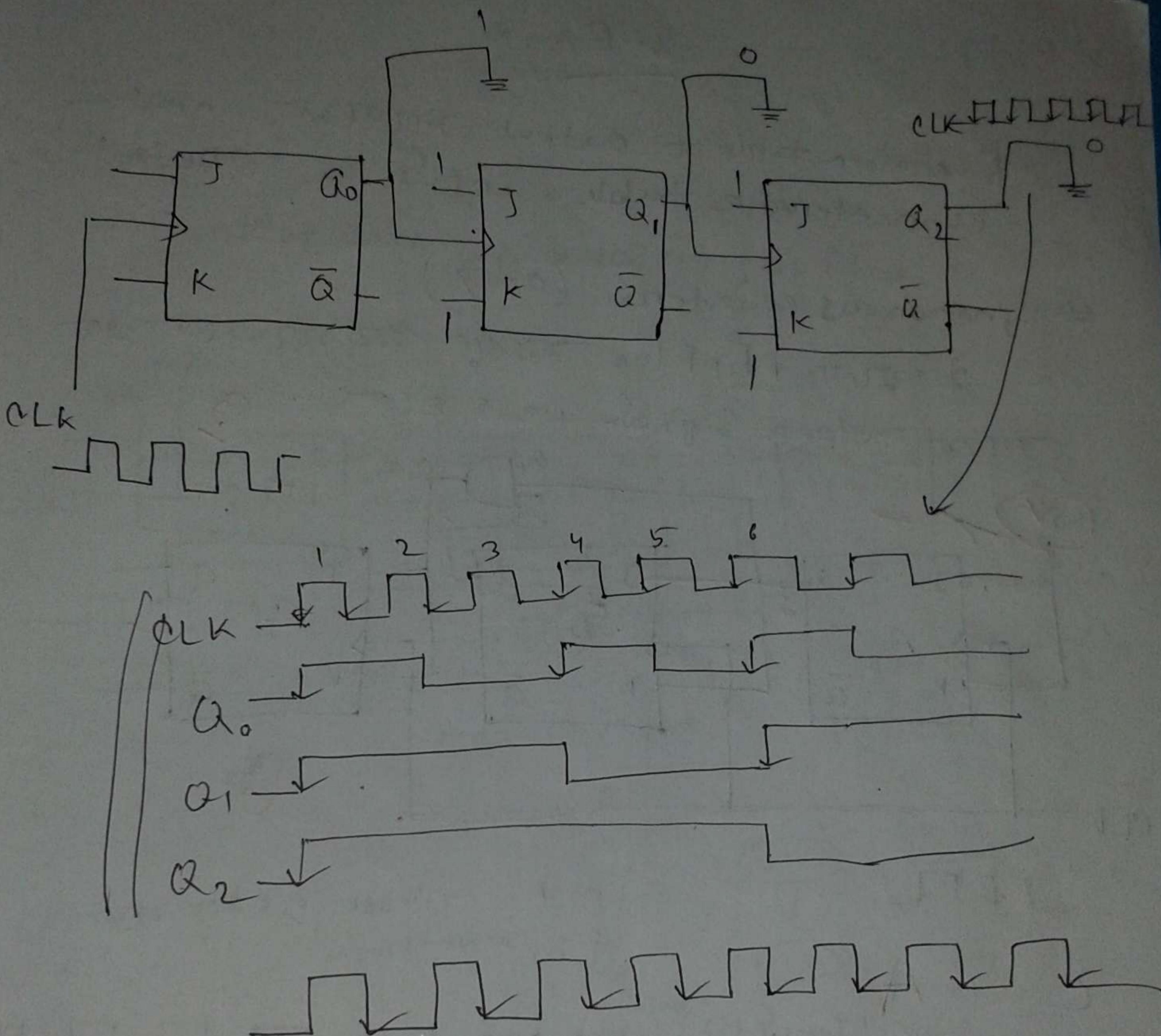
Design a binary counter

0 - 7

$000 \rightarrow 111$

it needs 3 flip flop (because of 3 bit)





16.09.14

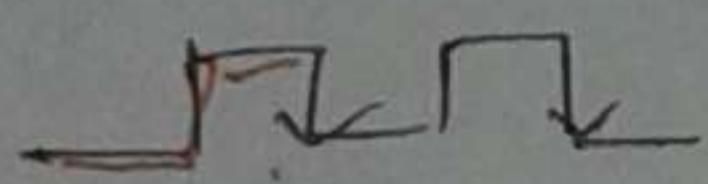
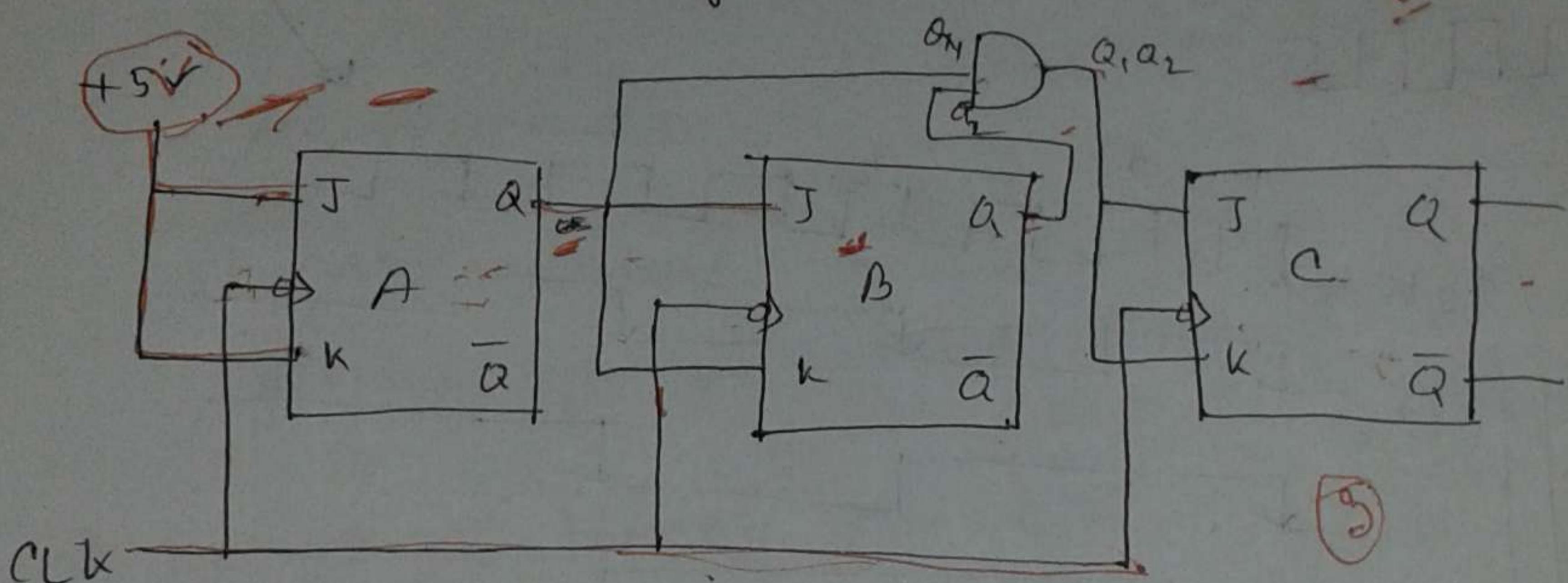
8-E

Excitation table = output ~~versus~~ input
Characteristic table = input \times output

Synchronous counter: (0-7)

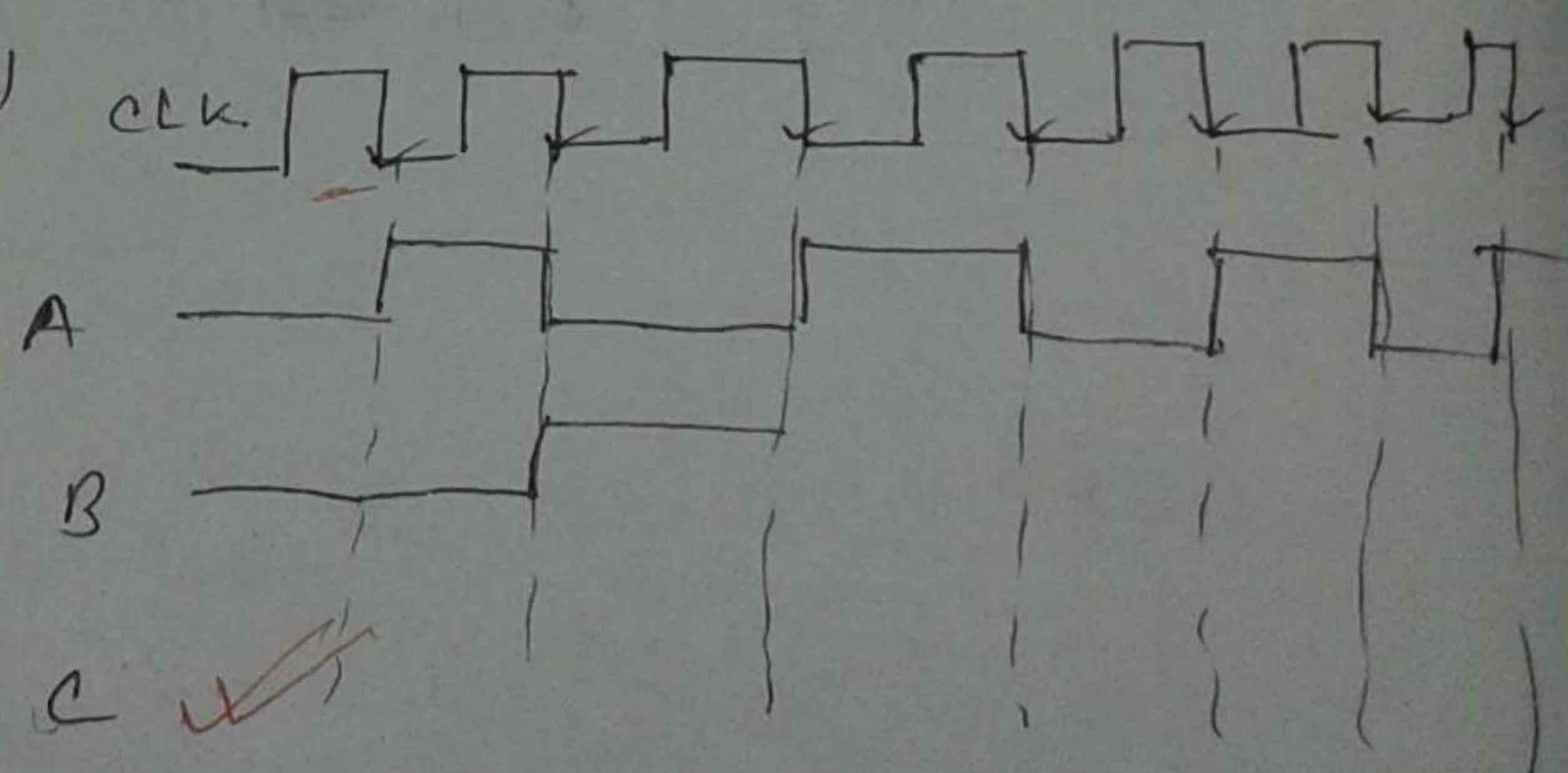
2-to-1 flip flop \rightarrow 3-to-2 counter \rightarrow

Inter clock signal pass etc



0' \rightarrow toggle 0, 1 \rightarrow 2nd. step
20' \rightarrow No change

	C	B	A
0	0	0	0 (Toggle)
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	0	1	0
7	0	0	1
8	0	0	0
9	1	0	0
10	0	1	0
11	0	0	1
12	0	0	0



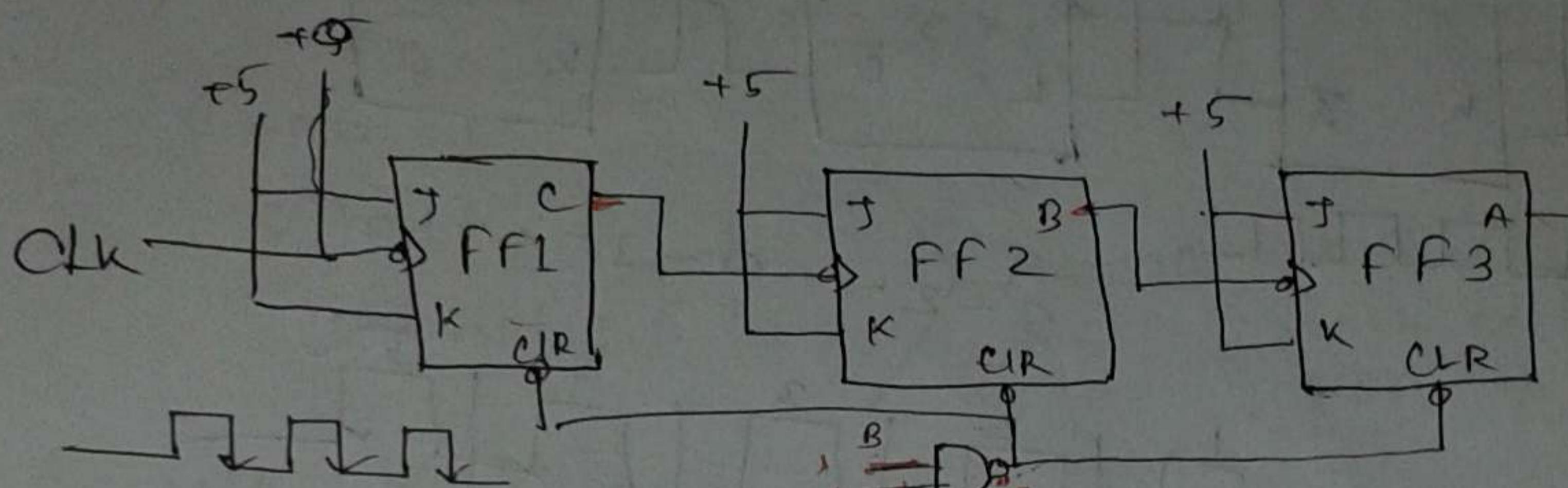
Toggling 0, 02
7. c

9-A

13.09.14

if $\cdot FF = 0-2$

\therefore Flip Flop Num: $2^n \rightarrow$ No. of flip flop



A B C

0 0 0

0 0 1

0 1 0

0 1 1

⋮ ⋮ ⋮

⋮ ⋮ ⋮

⋮ ⋮ ⋮

⋮ ⋮ ⋮

⋮ ⋮ ⋮

⋮ ⋮ ⋮

⋮ ⋮ ⋮

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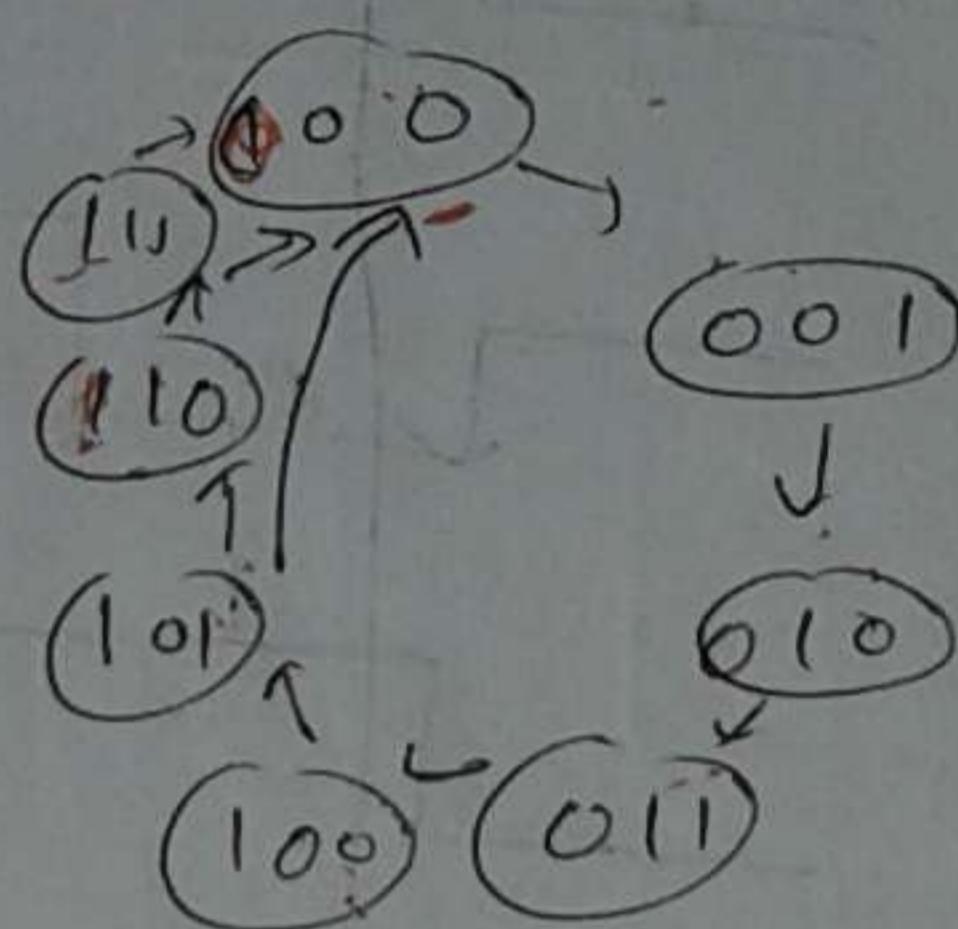
⋮ ⋮ ⋮

⋮ ⋮ ⋮

⋮ ⋮ ⋮

⋮ ⋮ ⋮

mod counter



Mod ⑤ A-D-

Mod ⑥ A-D-

Mod ⑦ A-D-

Mod ⑧ A-D-

Mod ⑨ A-D-

Mod ⑩ A-D-

Mod ⑪ A-D-

Mod ⑫ A-D-

Mod ⑬ A-D-

Mod ⑭ A-D-

Mod ⑮ A-D-

Mod ⑯ A-D-

Mod ⑰ A-D-

Mod ⑱ A-D-

Mod ⑲ A-D-

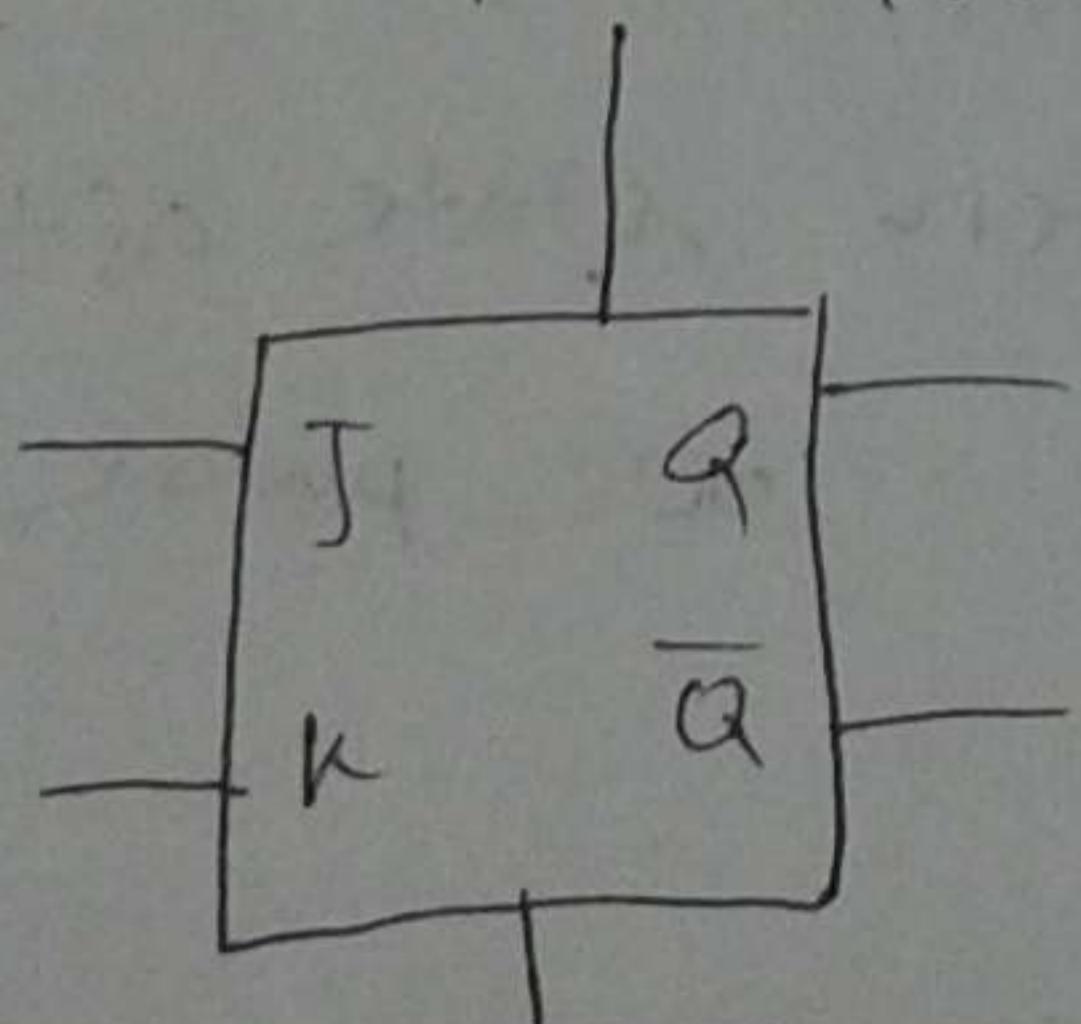
Mod ⑳ A-D-

Mod ㉑ A-D-

Mod ㉒ A-D-

MOD - 6 counter

Preset/Set. if Preset output should be 1

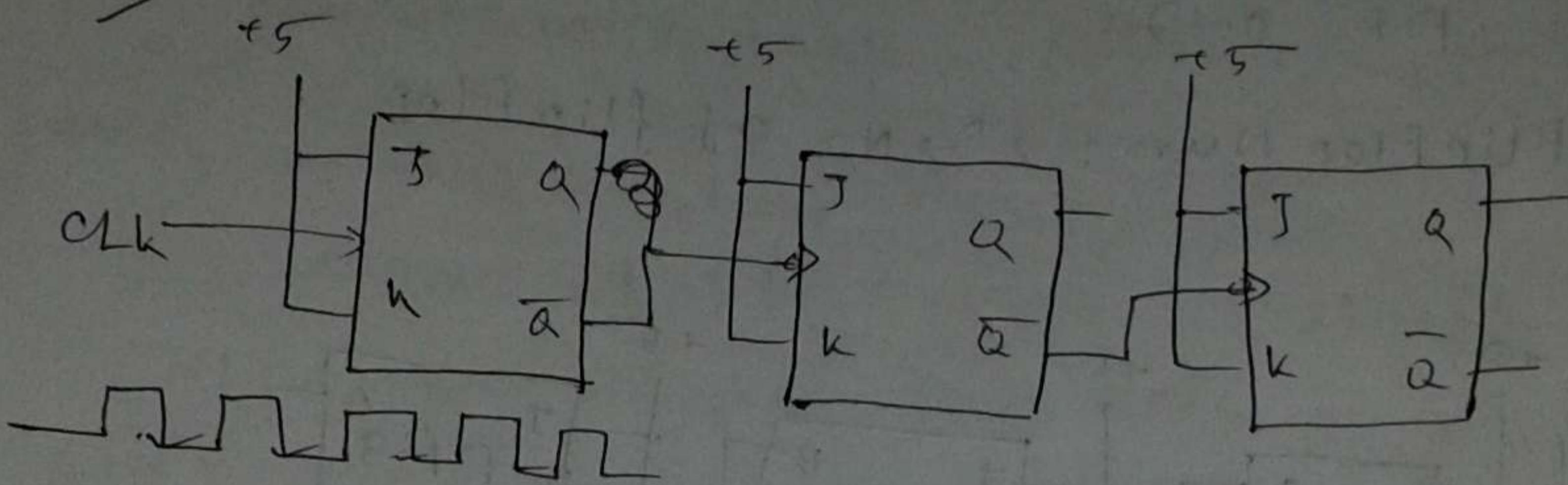


if Clear "

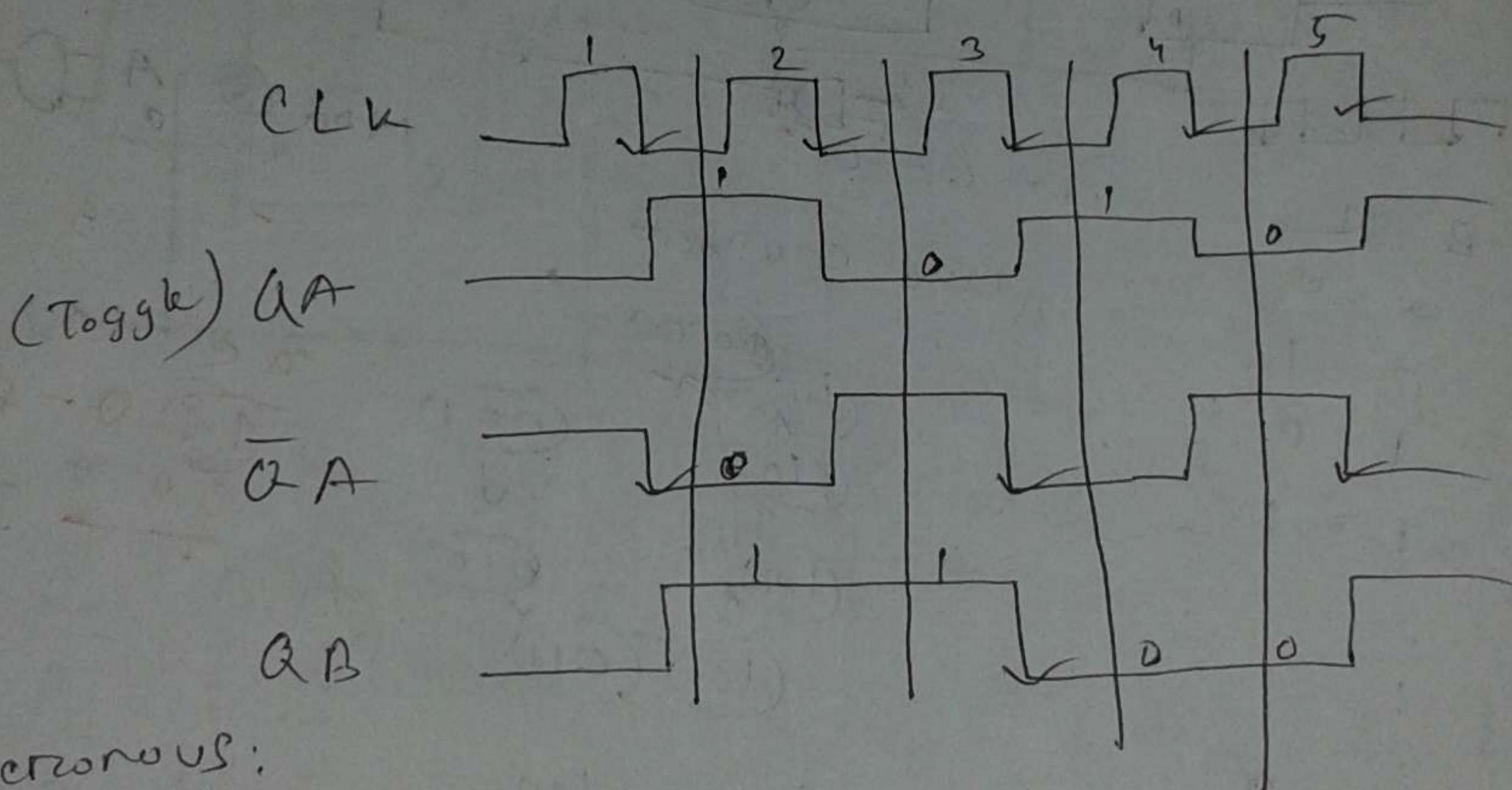
clear / Reset

Asynchronous counters down

7-6-5-4-3-2-1-0



3-2-1-0-3-2-1-0--



Asynchronous:

Counter has 5 FF $CLK = 100 \text{ MHz}$

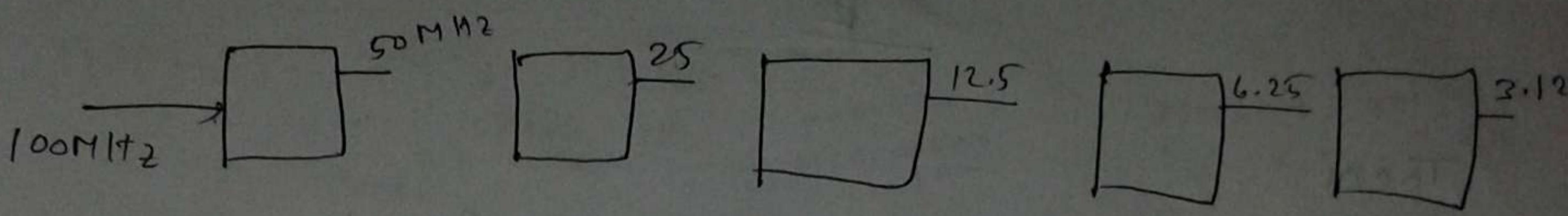
i) what are the O/P freq. of last FF

ii) what is the counter state after

1001 pulse

29

Q



Generate a formula: ~

~~Tocci~~ → Chap: 7 expl

Chap: 5

Antcl: 5.23

Expl: 5.16

Asynchronous Analysis
ninth edition
206

74LS293 (IC Asynchronous counter)

0-7
0-15
Antcl: 7.3

21.10.14

9-E

Tocci

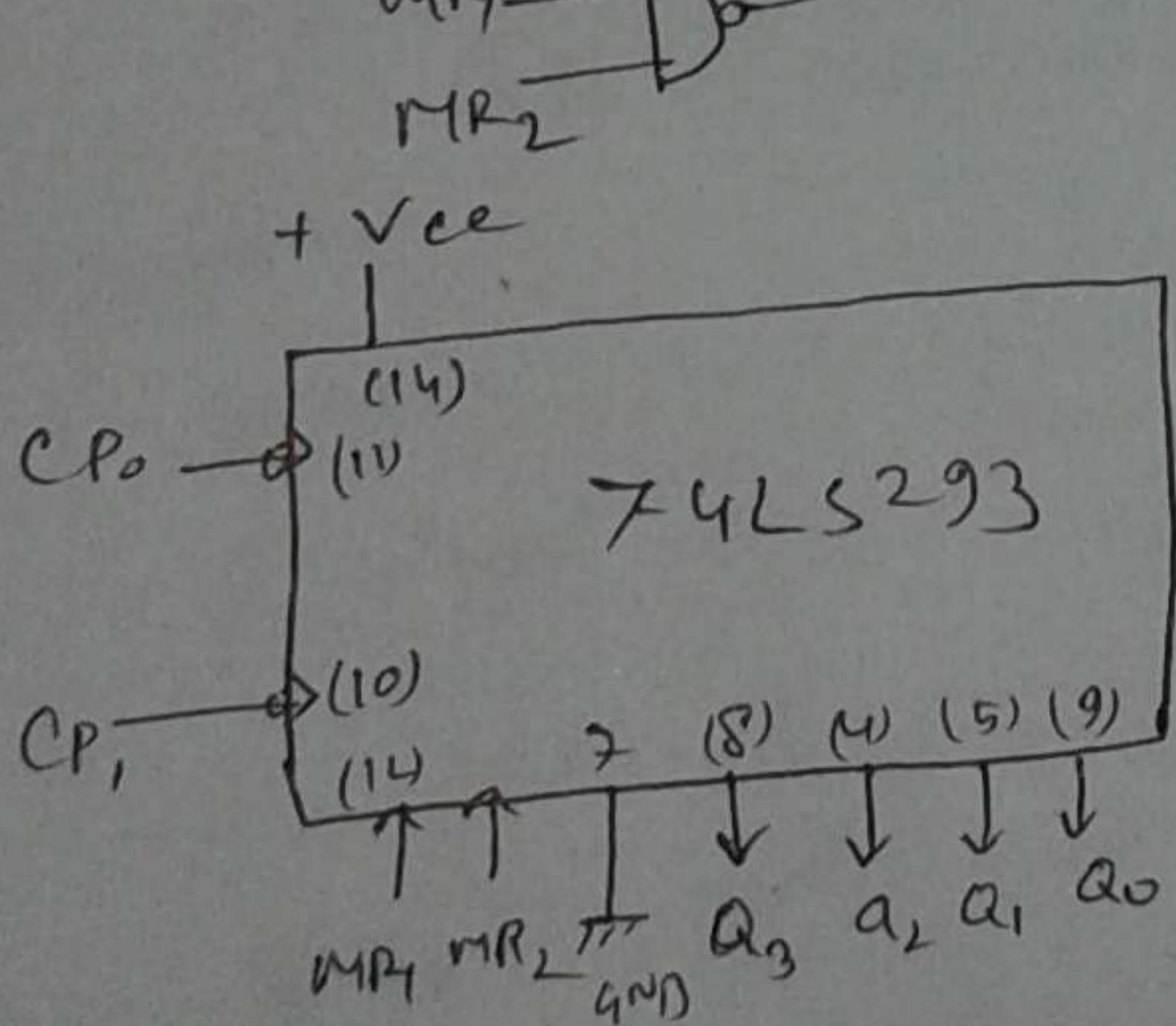
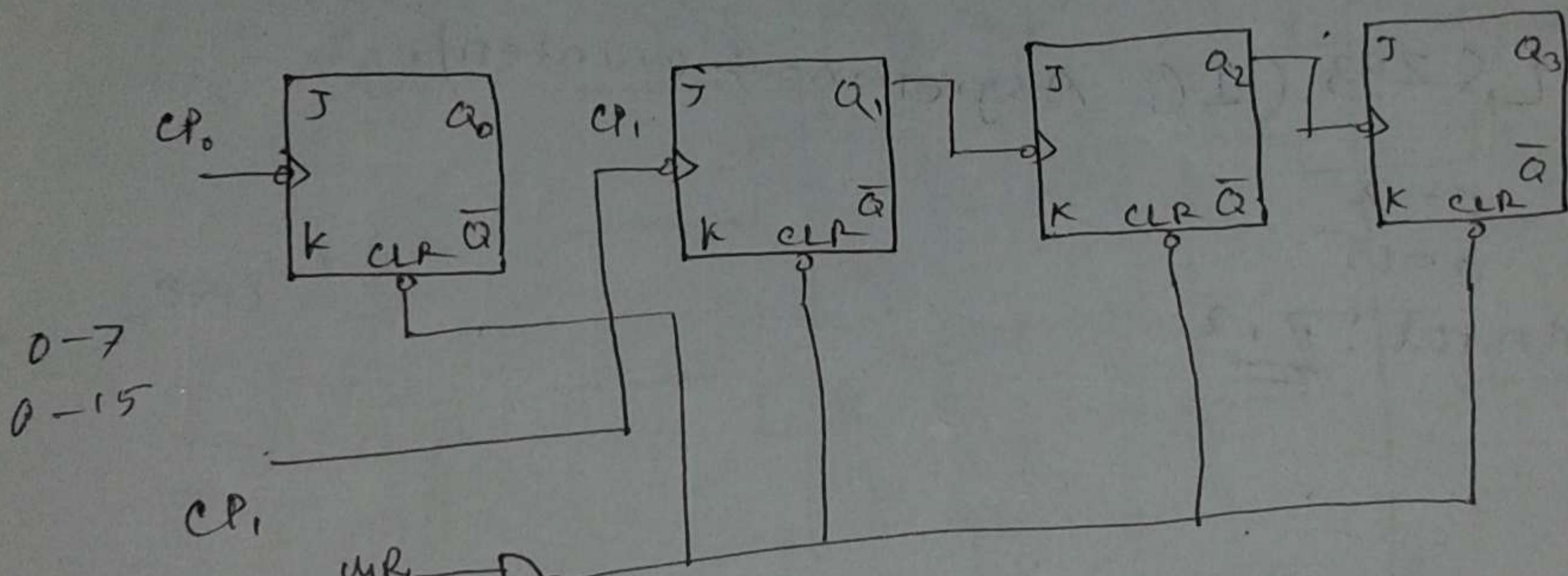
Ans : 7.3 : IC Asynchronous Counter

→ 74LS293 (Asy)

→ 74LS193 (synchronous Counter)

0-15 0-9
CP = clock Pulse

$V_{DD} = V_{SS} = +5V$



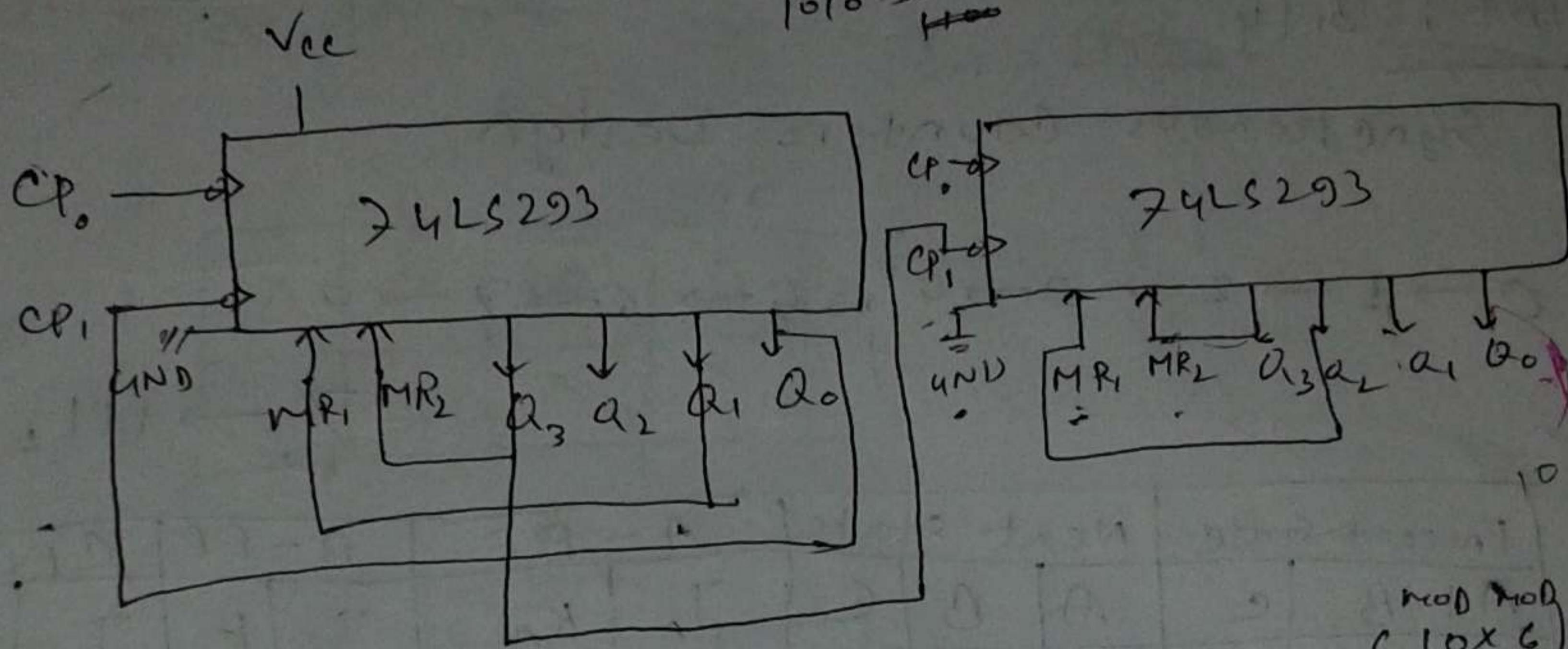
0000
:
1001
1010 → 0000

MOD-60 using 74LS293

MOD-10

0000
 $1010 \rightarrow 0000$

000
 101
MOD-6 $000 \rightarrow 110$
 $a_3 a_2 a_1$



MOD - 60

MOD-36

mod-6 x mod-6

$\sqrt{A_{NT}} = 7.3$

Ant: 7.7, 7.8, 7.9 (Sdf Study) Tocei

$0 \rightarrow 000$
$1 \rightarrow 001$
$2 \rightarrow 010$
$3 \rightarrow 011$
$4 \rightarrow 100$
$5 \rightarrow 101$
$6 \rightarrow 110$
$7 \rightarrow 111$

22.10.14

QD 10-A

Ans: 3.14

Synchronous Counter Design

$0 \rightarrow 1 \rightarrow 2 \rightarrow 3 \rightarrow 4 \rightarrow 5 \rightarrow 6 \rightarrow 7 \rightarrow 0$

$7_{10} \rightarrow 111_2$

Present State			Next state			A - FF		B - FF		C - FF	
A	B	C	A	B	C	J _A	K _A	J _B	K _B	J _C	K _C
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	1	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	1	X
1	0	0	1	0	1	X	0	0	X	1	1
1	0	1	1	1	0	X	0	0	X	1	X
1	1	0	1	1	1	X	0	X	0	1	X
1	1	1	0	0	0	X	1	X	1	X	1

State	J	K
$0 \rightarrow 0$	0	X
$0 \rightarrow 1$	1	1
$1 \rightarrow 0$	X	1
$1 \rightarrow 1$	X	0

FF-A

$J_A = BC$

BC

		00	01	11	10
		00	01	10	10
A	0	00	01	10	02
	1	x4	x5	x7	x6

$J_A = BC$

		00	01	11	10
		00	01	11	10
A	0	x	x	x	x
	1	00	01	11	10

$K_A = BC$

C FF

$J_C = 1$

$K_C = 1$

B FF

BC

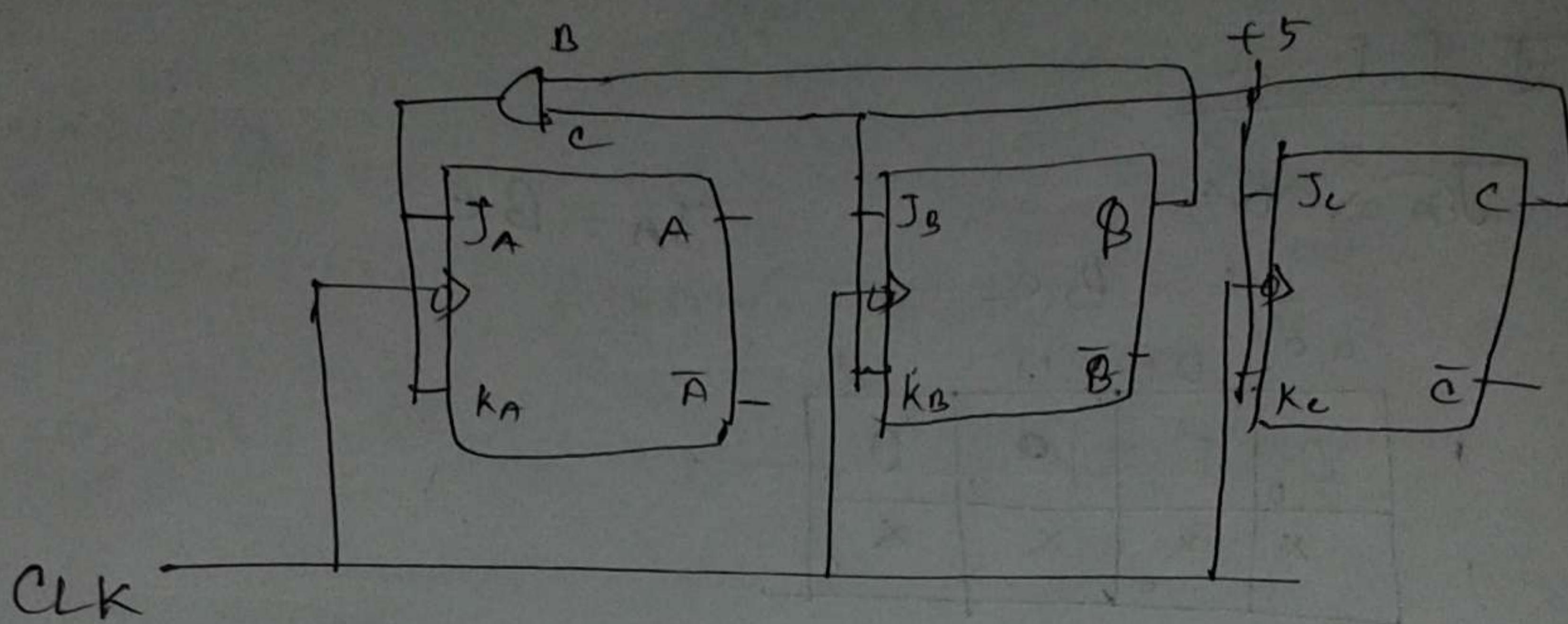
A

		00	01	11	10
		00	01	11	10
A	0	0	1	x	x
	1	0	1	x	x

$J_B = C$

x	x	1	0
x	x	1	0

$K_B = C$



Chapten: 7
 All empty } Self Study

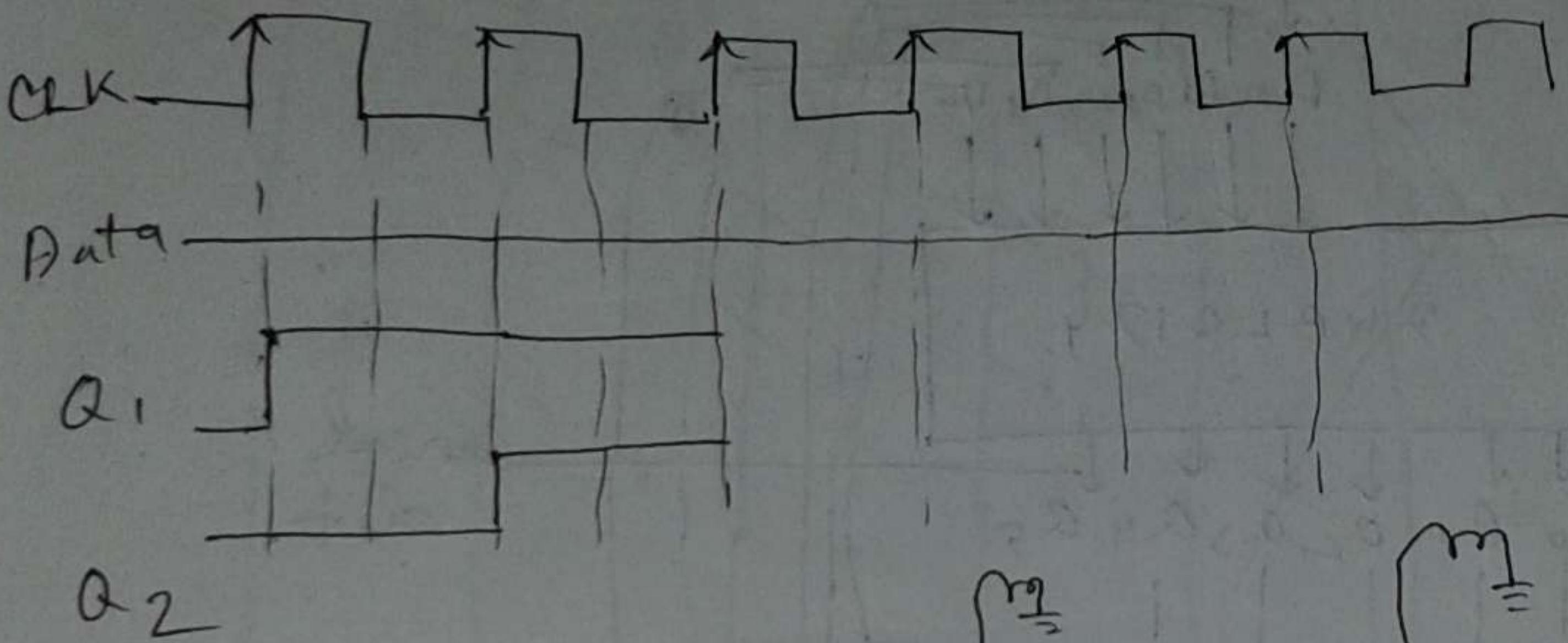
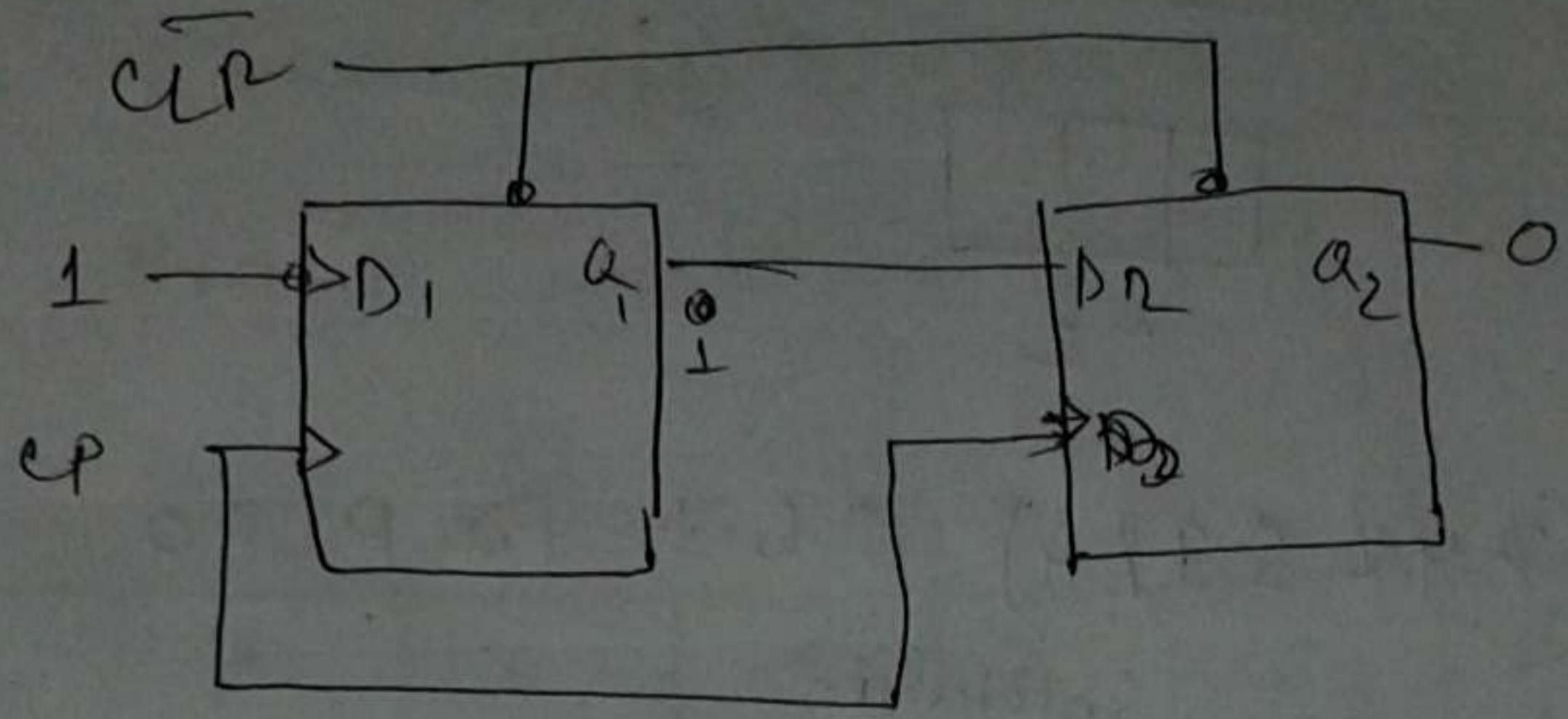
10 - E

29.10.14

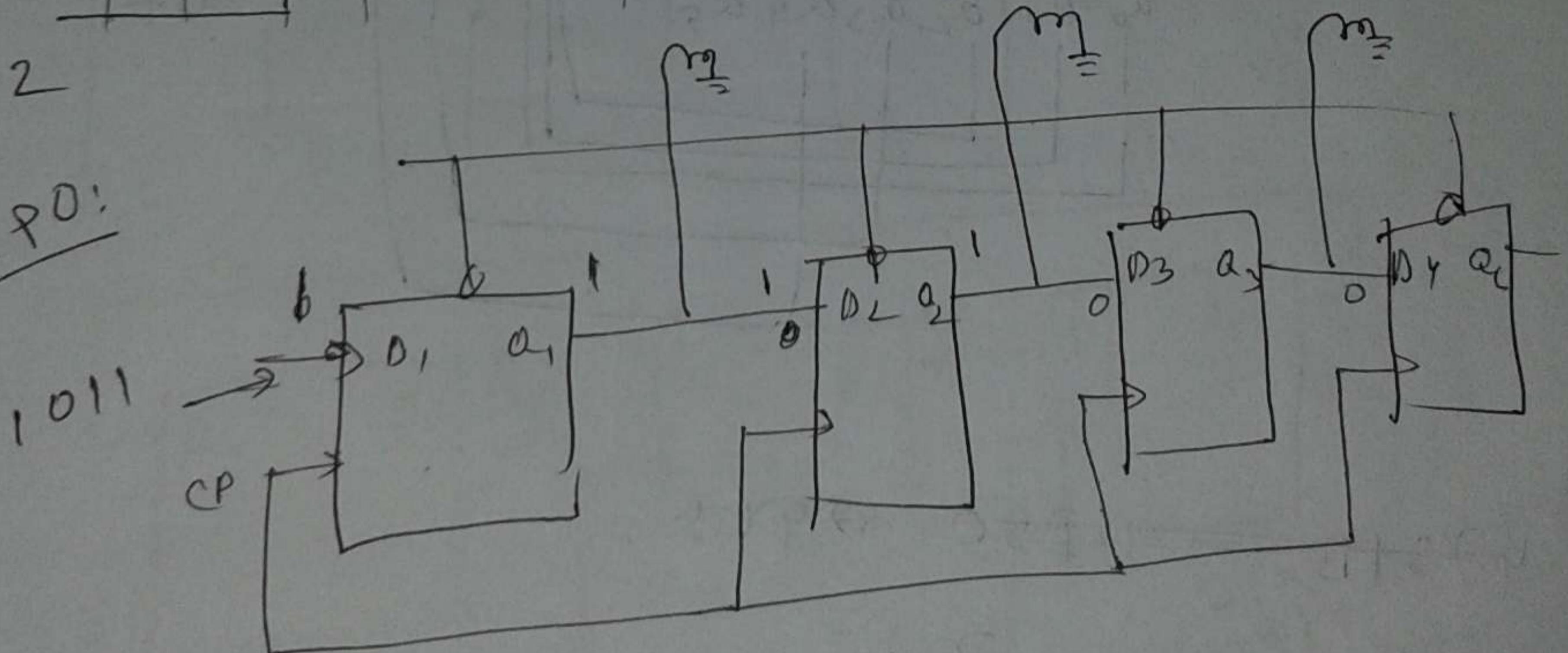
7.19: Integrated circuit Registers

- i) Serial in parallel out (SIPO)
- ii) Serial in serial out (SISO)
- iii) Parallel in serial out (PTSO)
- iv) Parallel in parallel out (PTPO)

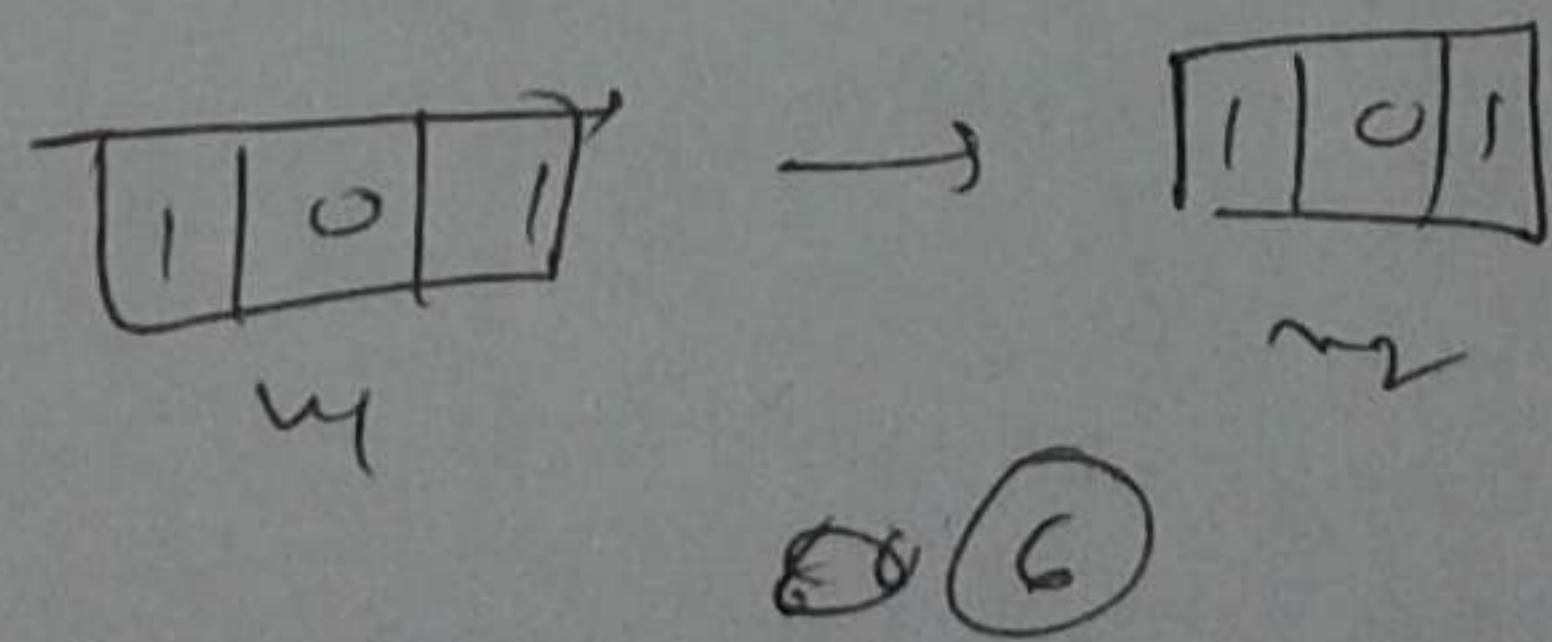
1) D flip flop



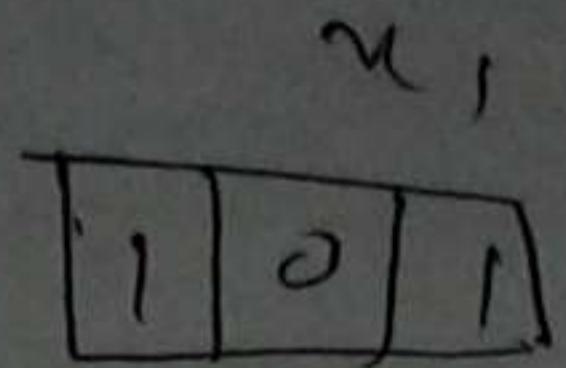
SISO:



SISO:



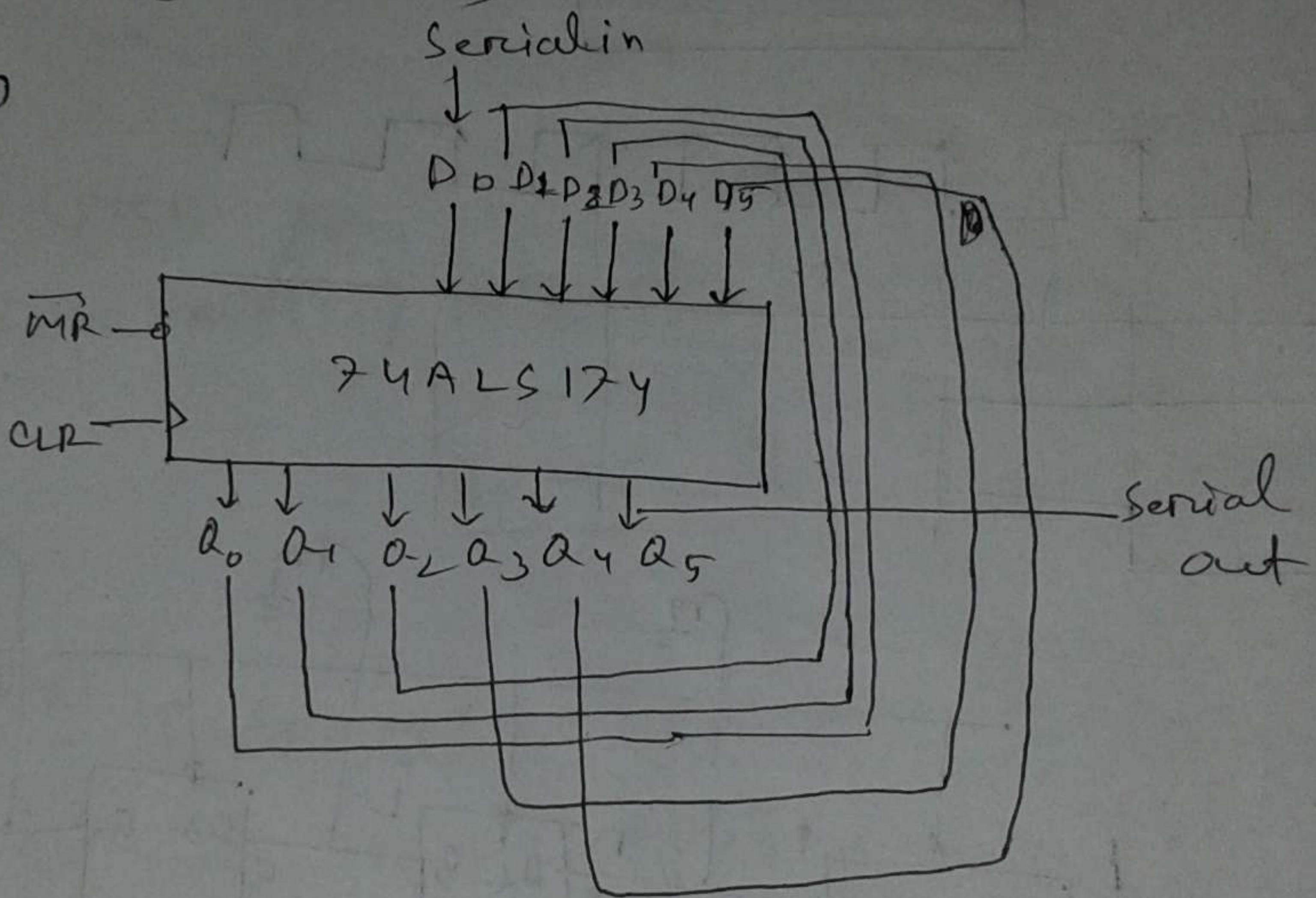
S1PO:



⑥

7.20:

PIPO: (74ALS174) 6 bit P&PIPO
Convert: ↓
SISO



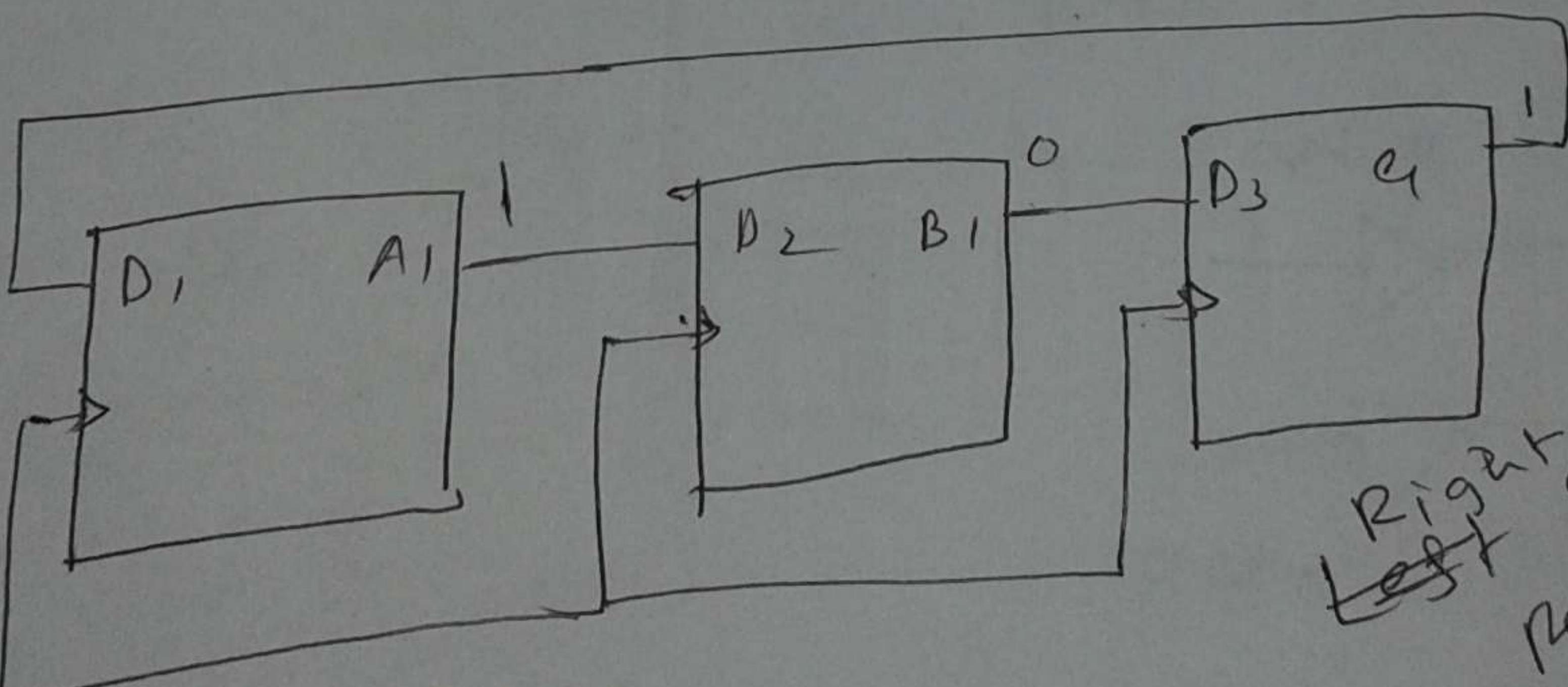
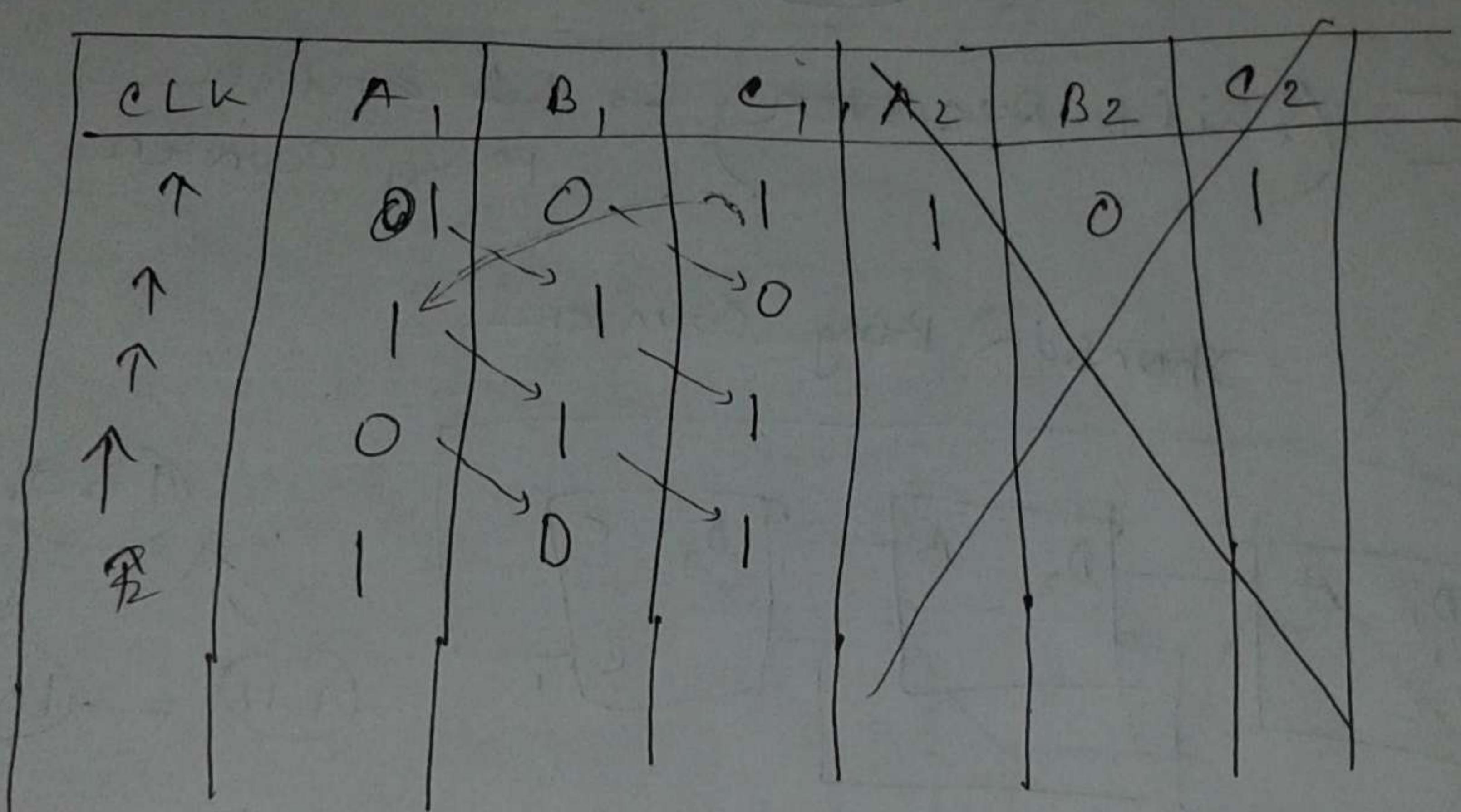
~~7.23+18~~ → PISO M95

7.21, 7.22, 7.23

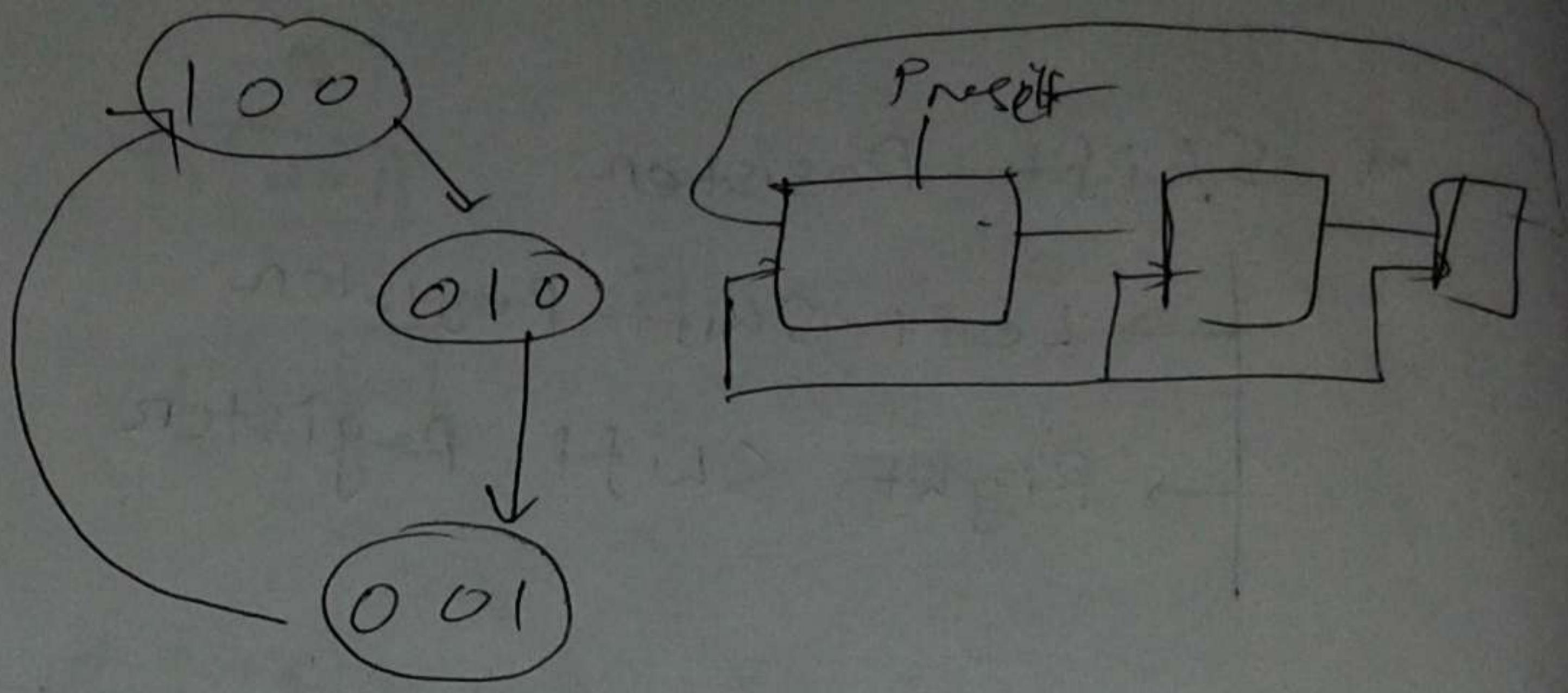
* Shift Register

→ Left Shift Register

→ Right Shift Register

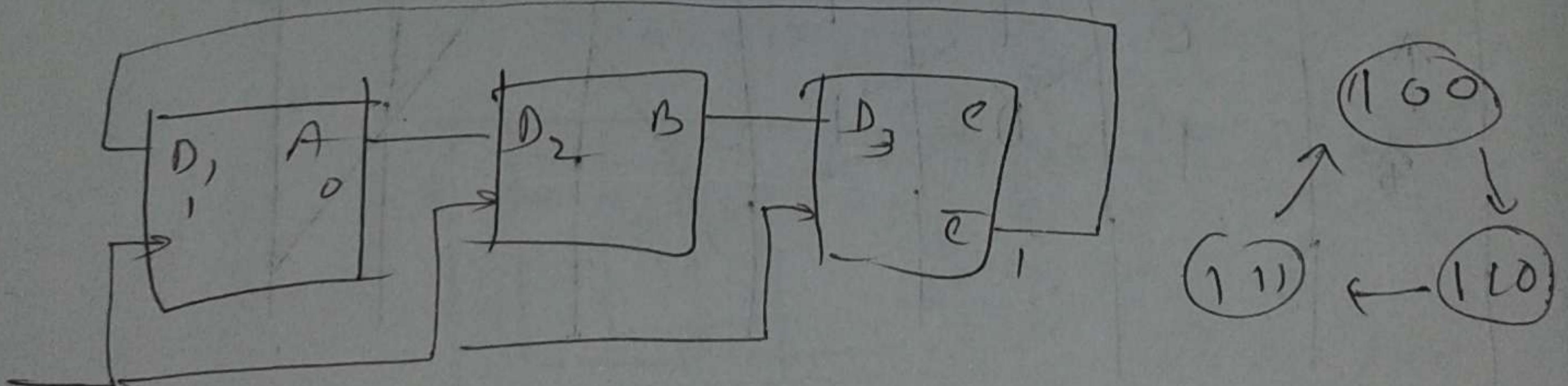


Shift Register



7.25 : (Shift Register) \rightarrow Sub article.
Ring counter

Johnson Ring Counter



1.11.14

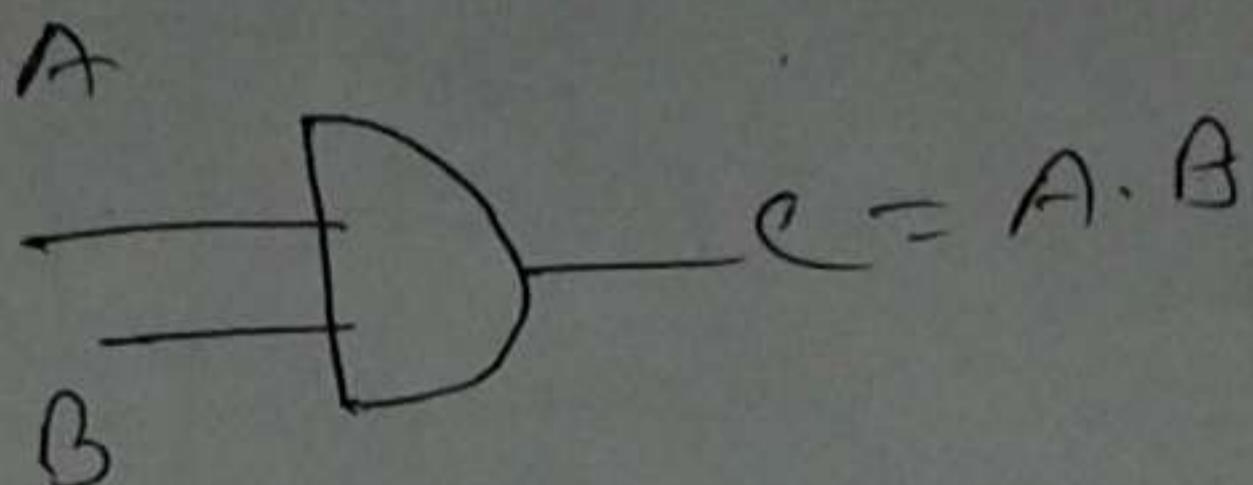
PD5.02

From
page 6

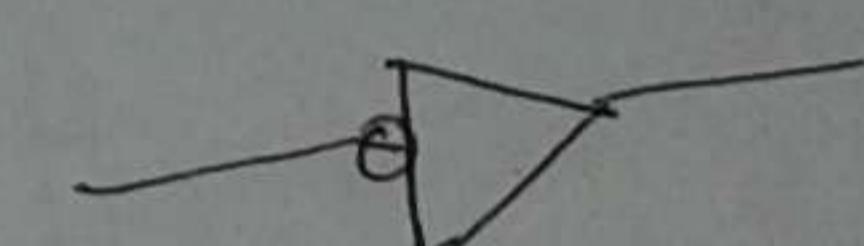
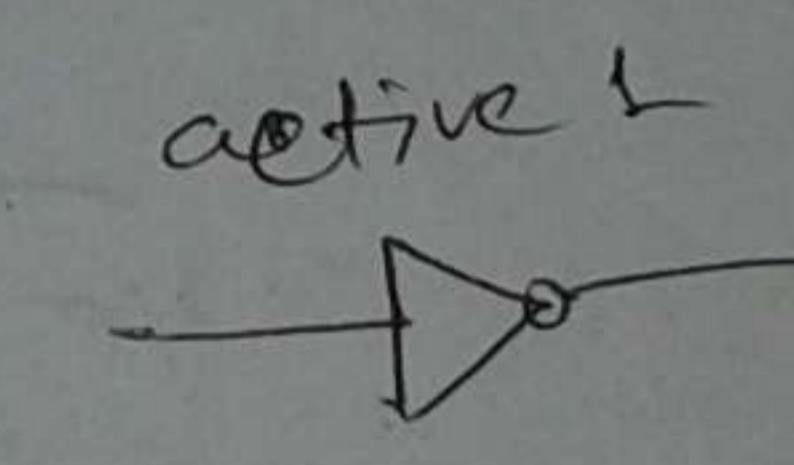
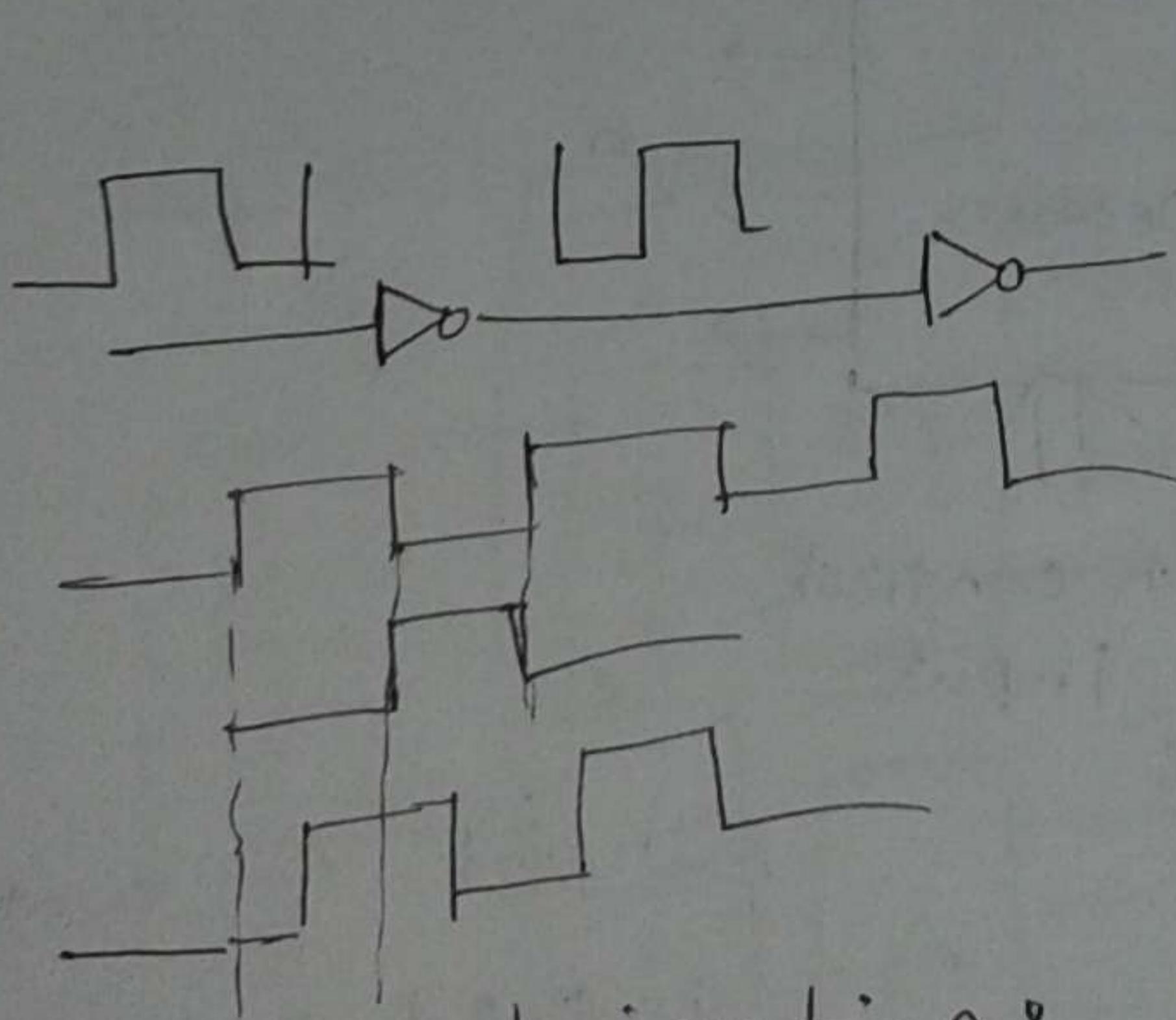
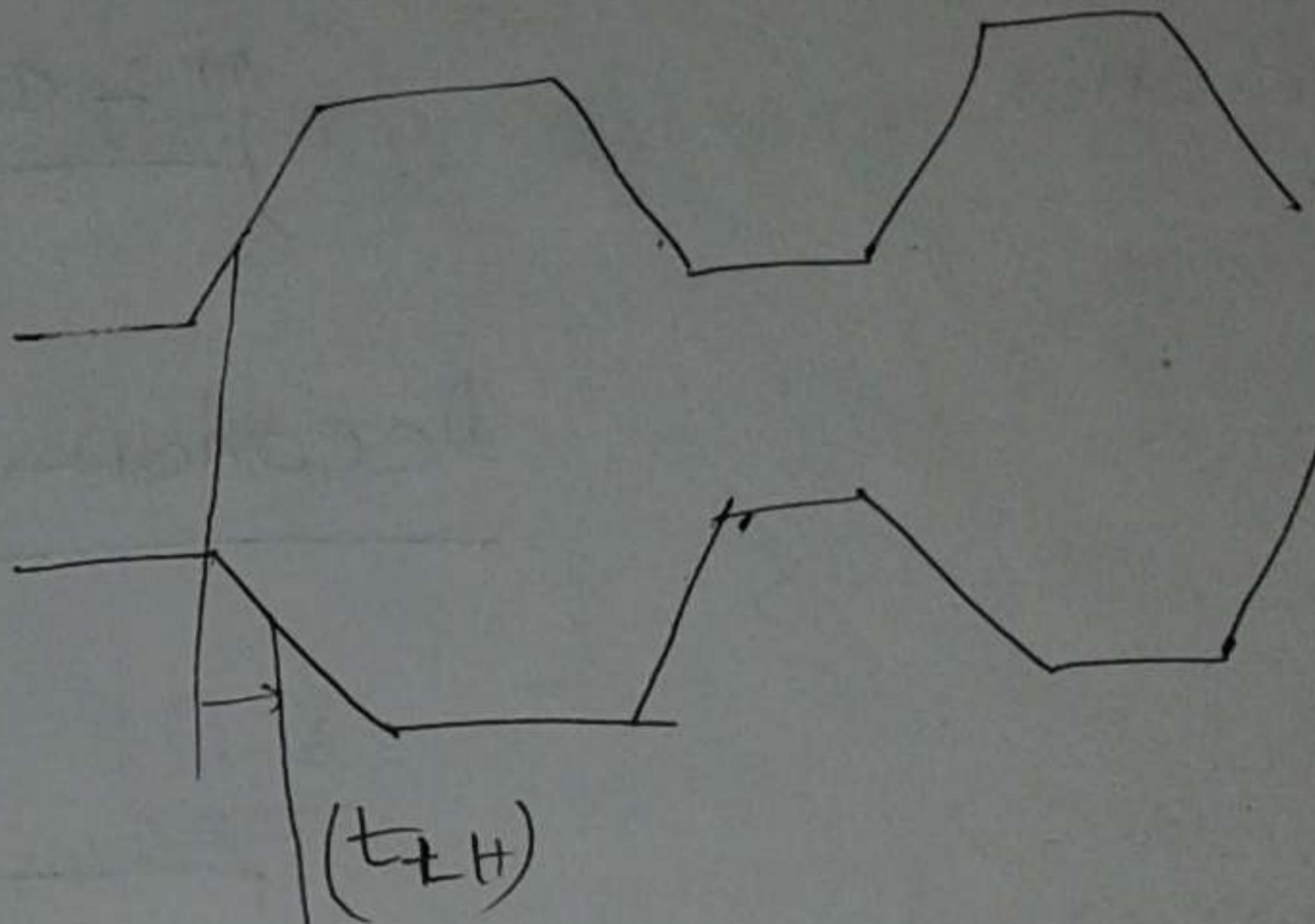
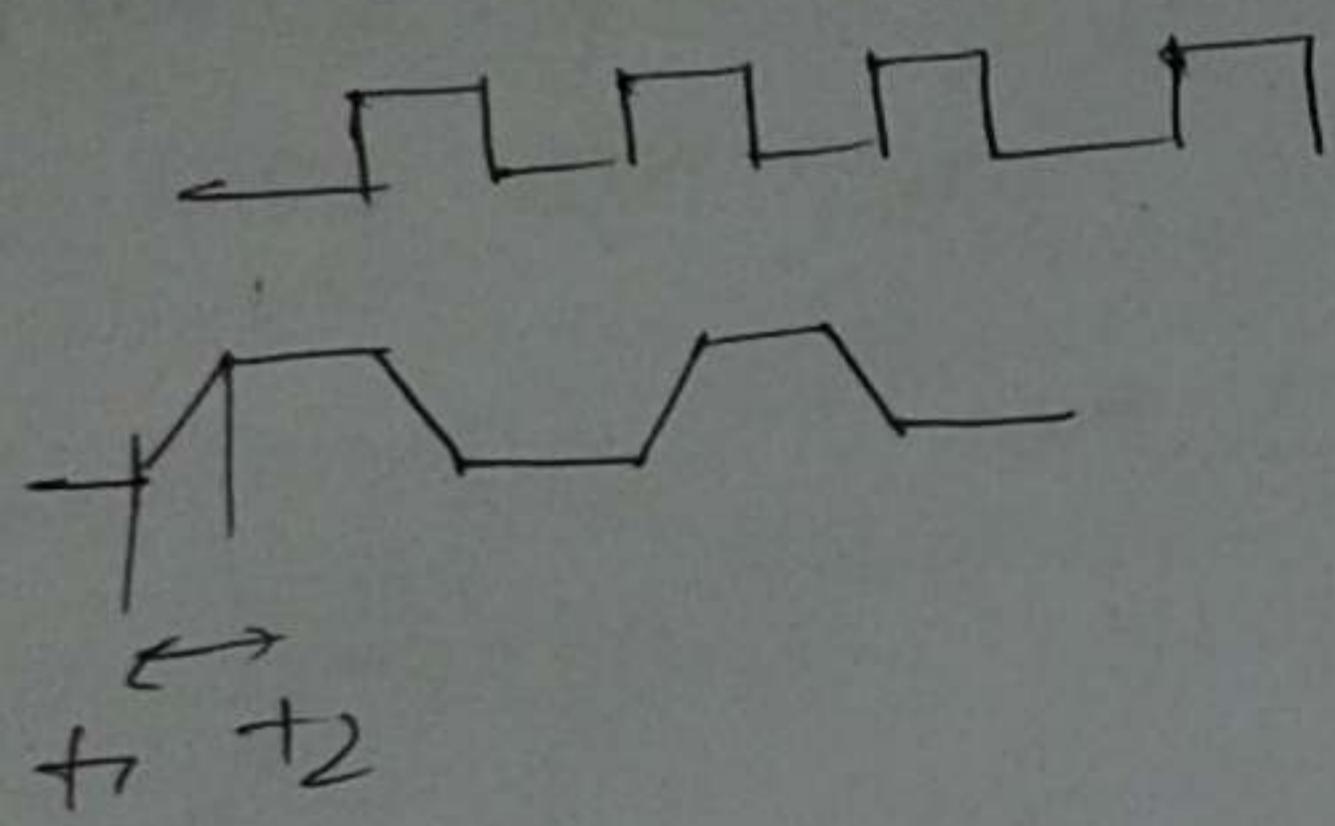
far In:

II - A

combinational logic circuit



Propagation delay:

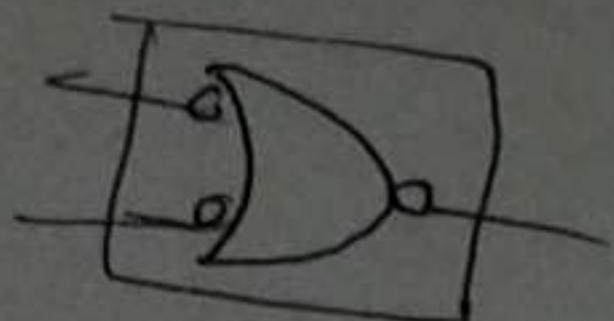


active 0

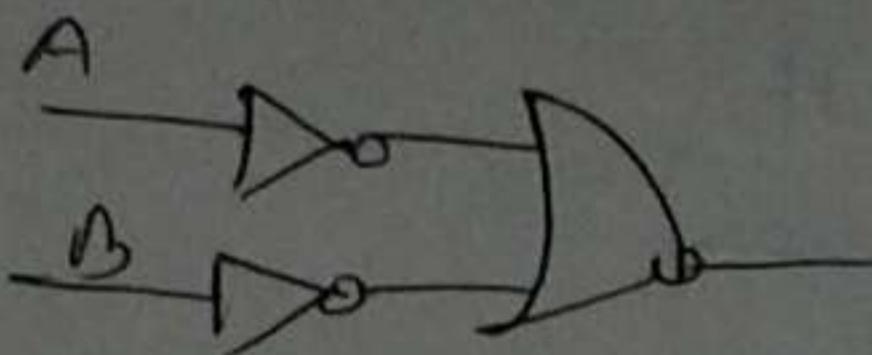


Power decipation:

AND



Active 0



$$\overline{\overline{A} + \overline{B}} = \overline{\overline{A}} \cdot \overline{\overline{B}} = \overline{A} \cdot \overline{B} = AB$$

Decodieren

Encoden

Multiplexen

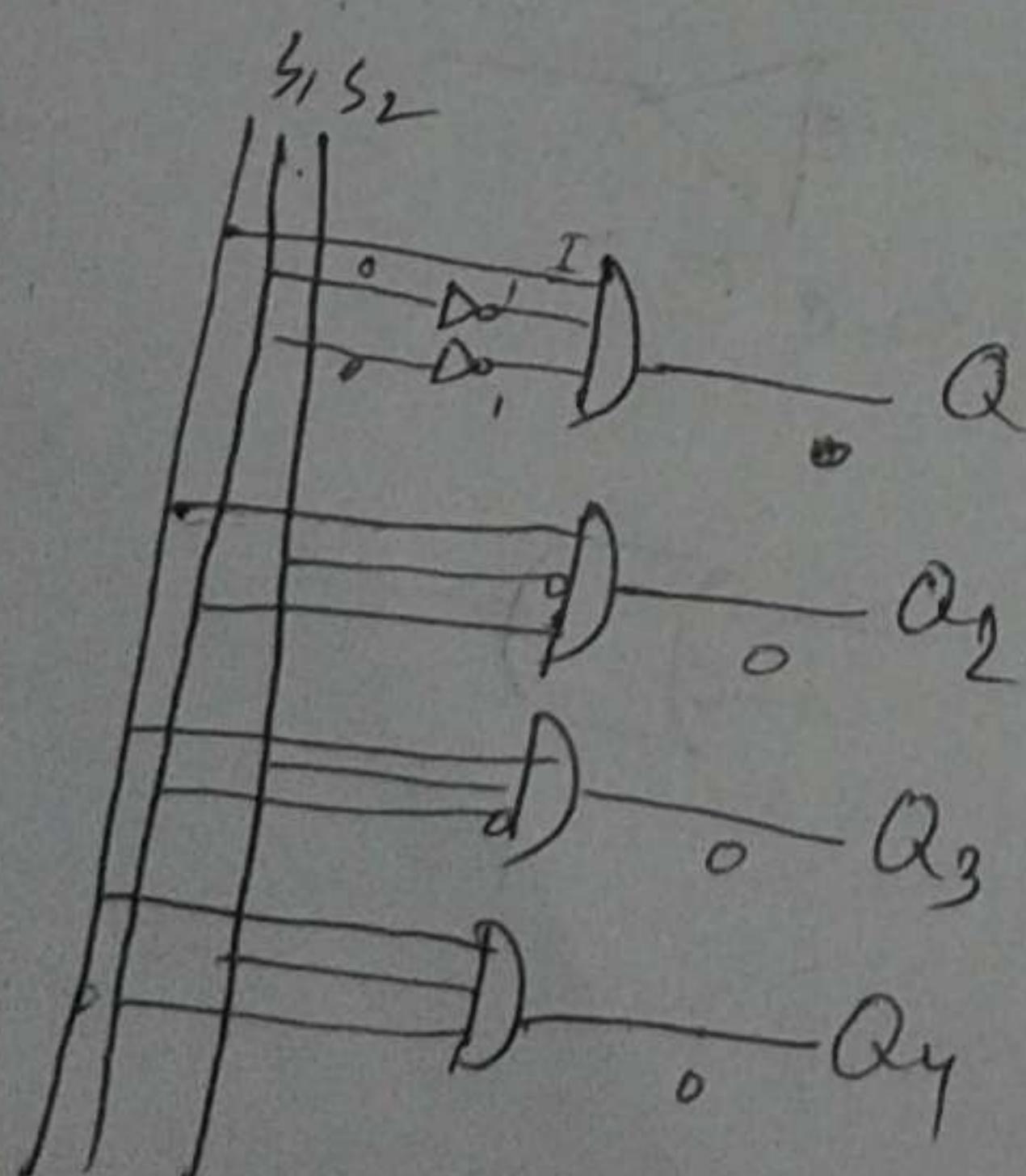
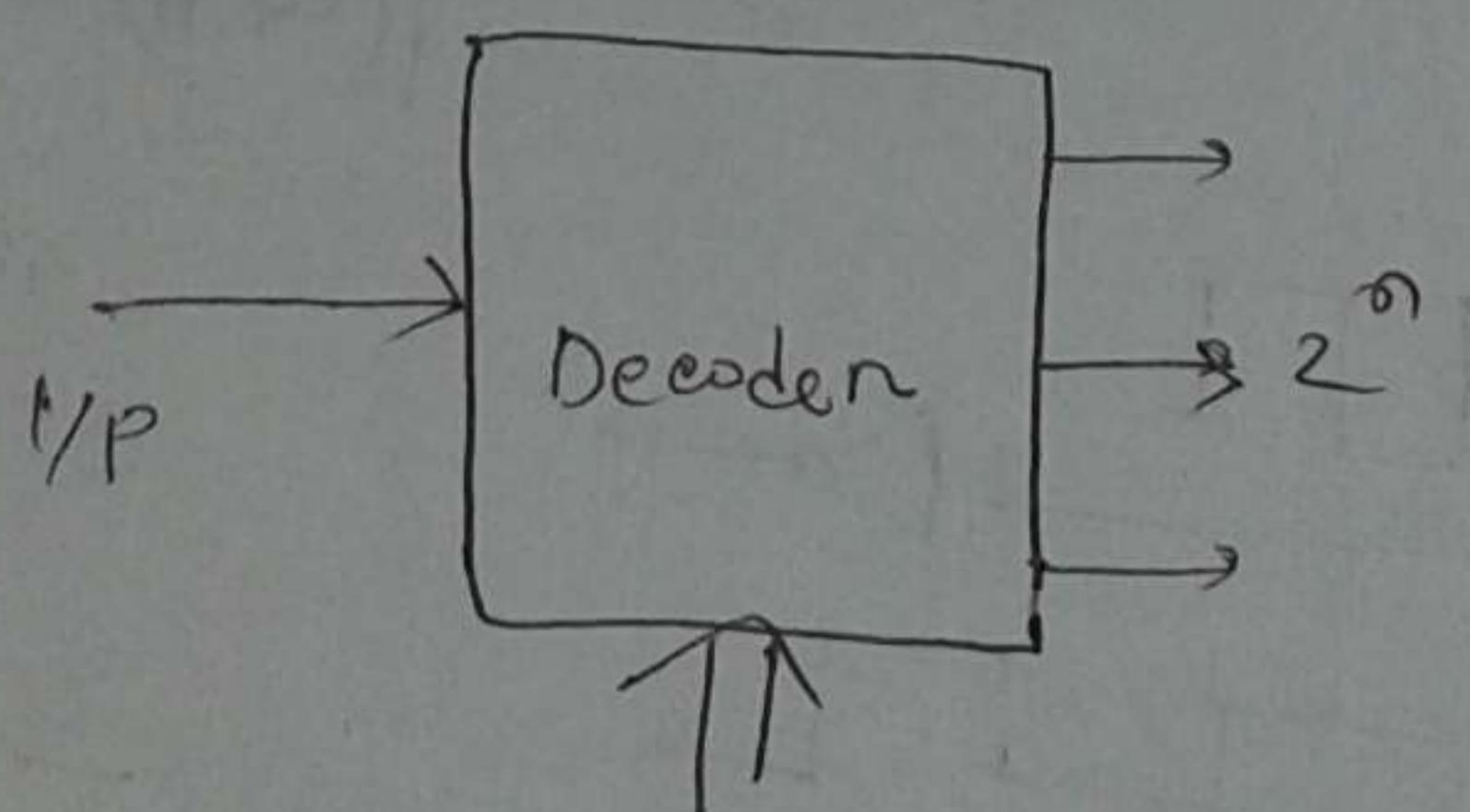
Demultiplexen

II - C

9.9 L.14

Decoder

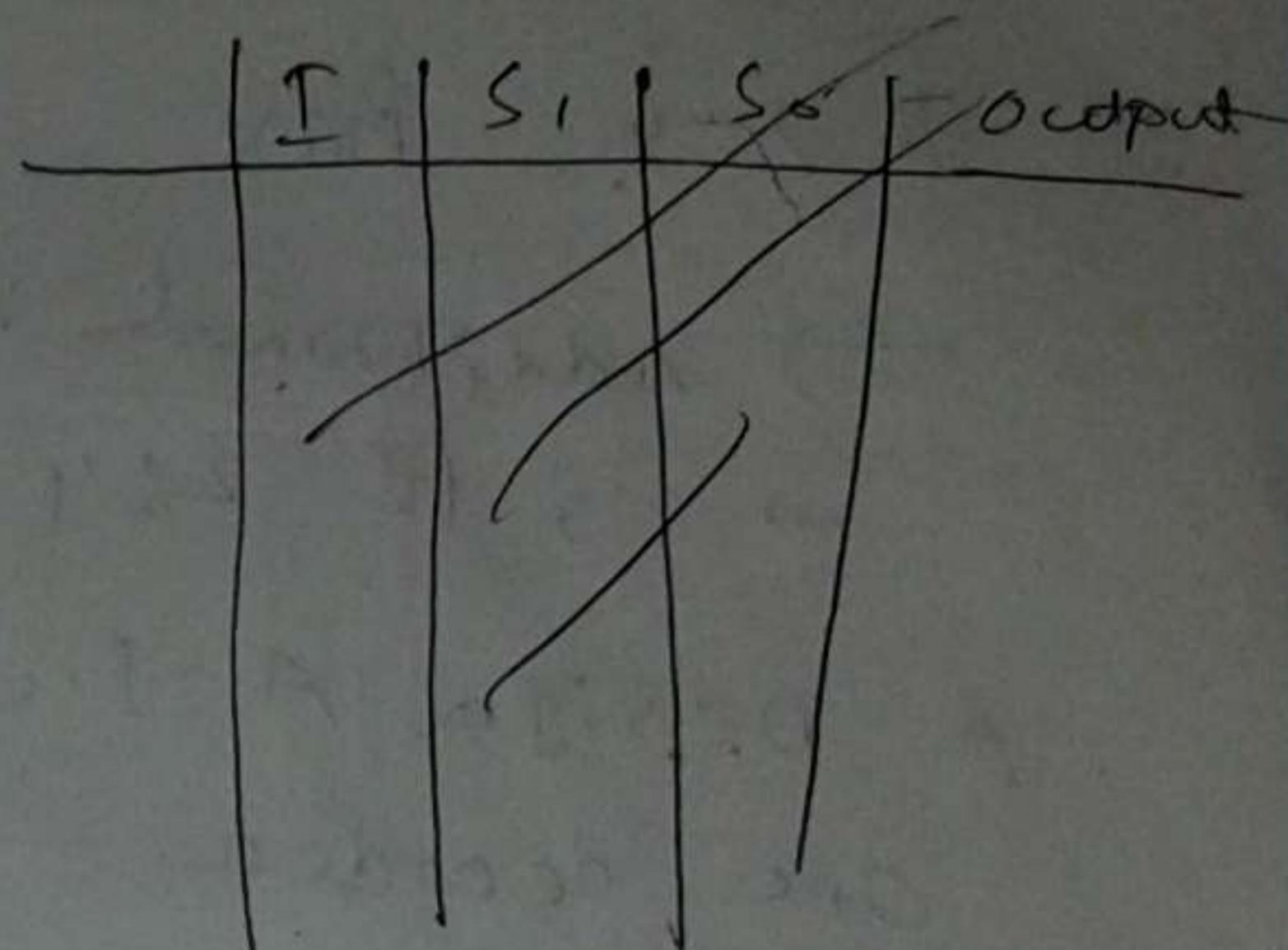
—————



n control
 $n = 2^4$ input

Output 2 control
 $input + = 2^4 L$

I	S_1	S_0	Output			
			O_1	O_2	O_3	O_4
I	0	0	I	I	I	I
I	0	1	I	I	I	I
I	1	0	I	I	I	I
I	1	1	I	I	I	I



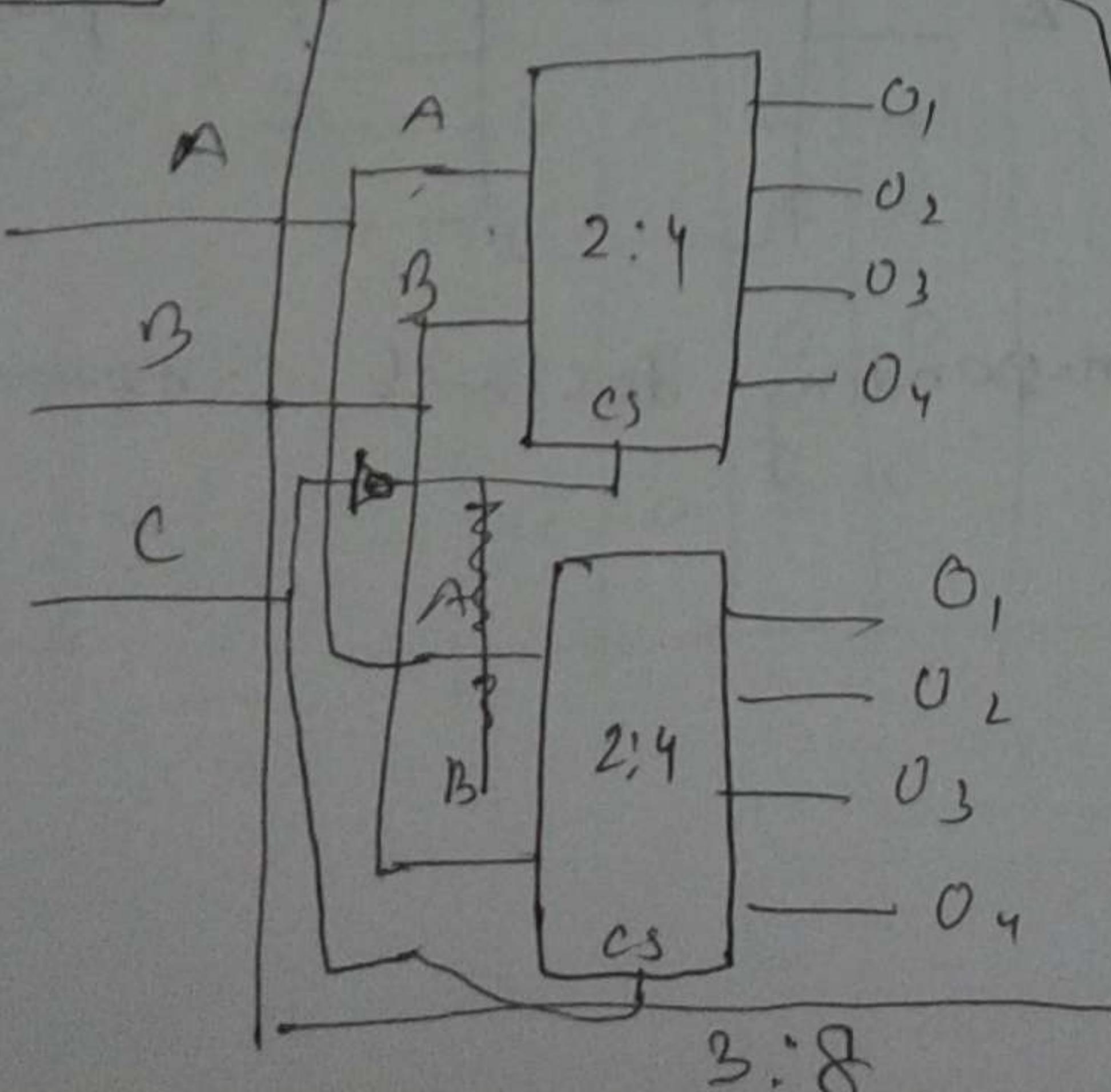
Memory management w/ 3-to-8 decoder circuit
use $\overline{A} \oplus \overline{B}$,

Morris : chapt 5 pArt 5.5

2:4

3:8

2:4



$CS = \overline{C} \oplus \overline{B}$
Select

C	A	B	CS	O8
0	0	0	0	0
0	0	1	1	1
0	1	0	1	0
0	1	1	0	1
1	0	0	0	0
1	0	1	1	0
1	1	0	1	0
1	1	1	0	1

2:4 FAN-IN 4:16 FAN-OUT 260

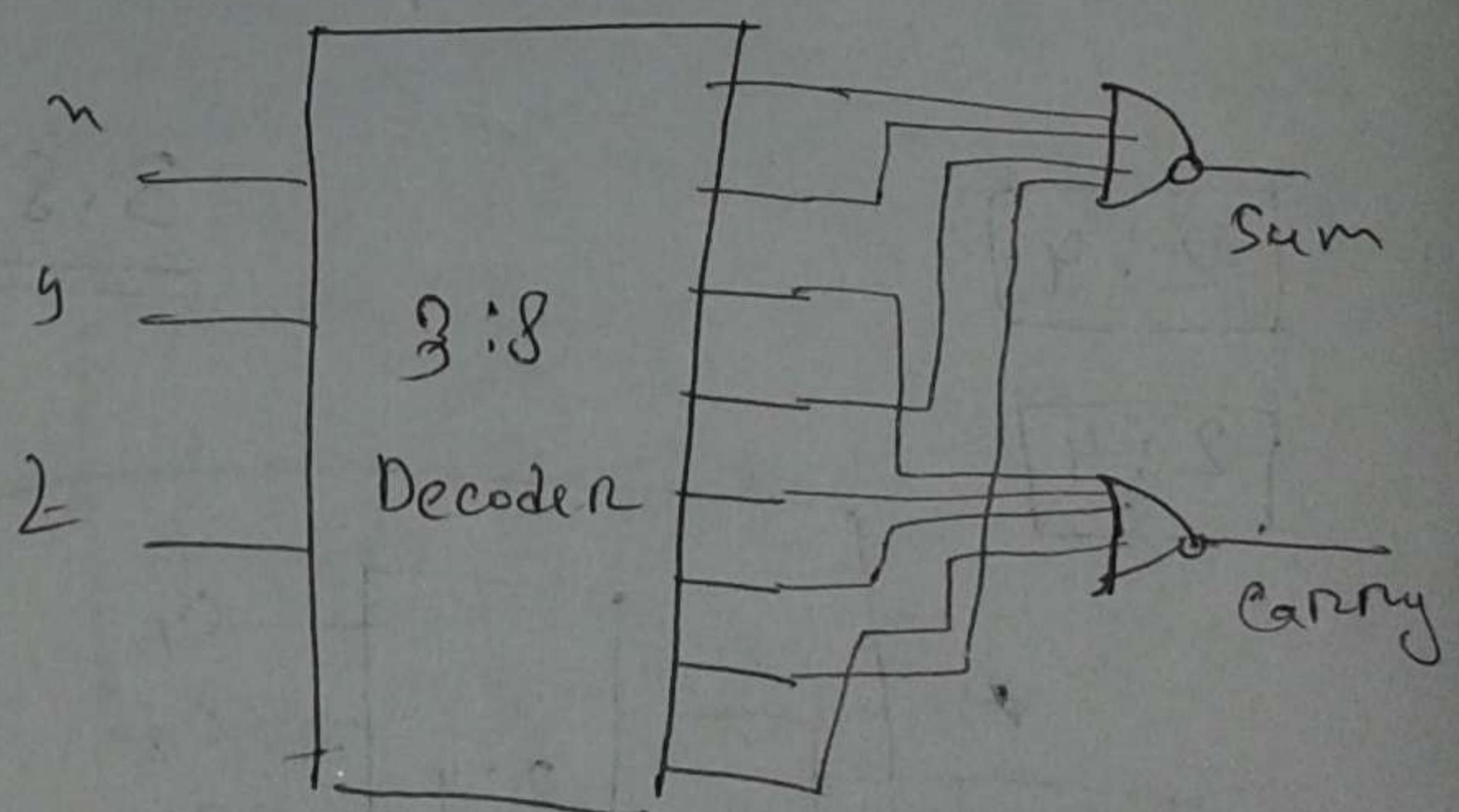
\Rightarrow Additional AND gate for

\Rightarrow 5 f² 2:4 fan-in

Design A full adder using at least one decoder

$$\text{Sum}, f_1(n, y, z) = \sum (1, 2, 4, 2)$$

A	B	C	S	CARRY	f ₂ (n, y, z) =
0	0	0	0	0	$\sum (3, 5, 6, 7)$
0	0	1	0	1	
0	1	0	0	1	
0	1	1	1	0	
1	0	0	0	01	
1	0	1	0	10	
1	1	0	0	10	
1	1	1	1	0	

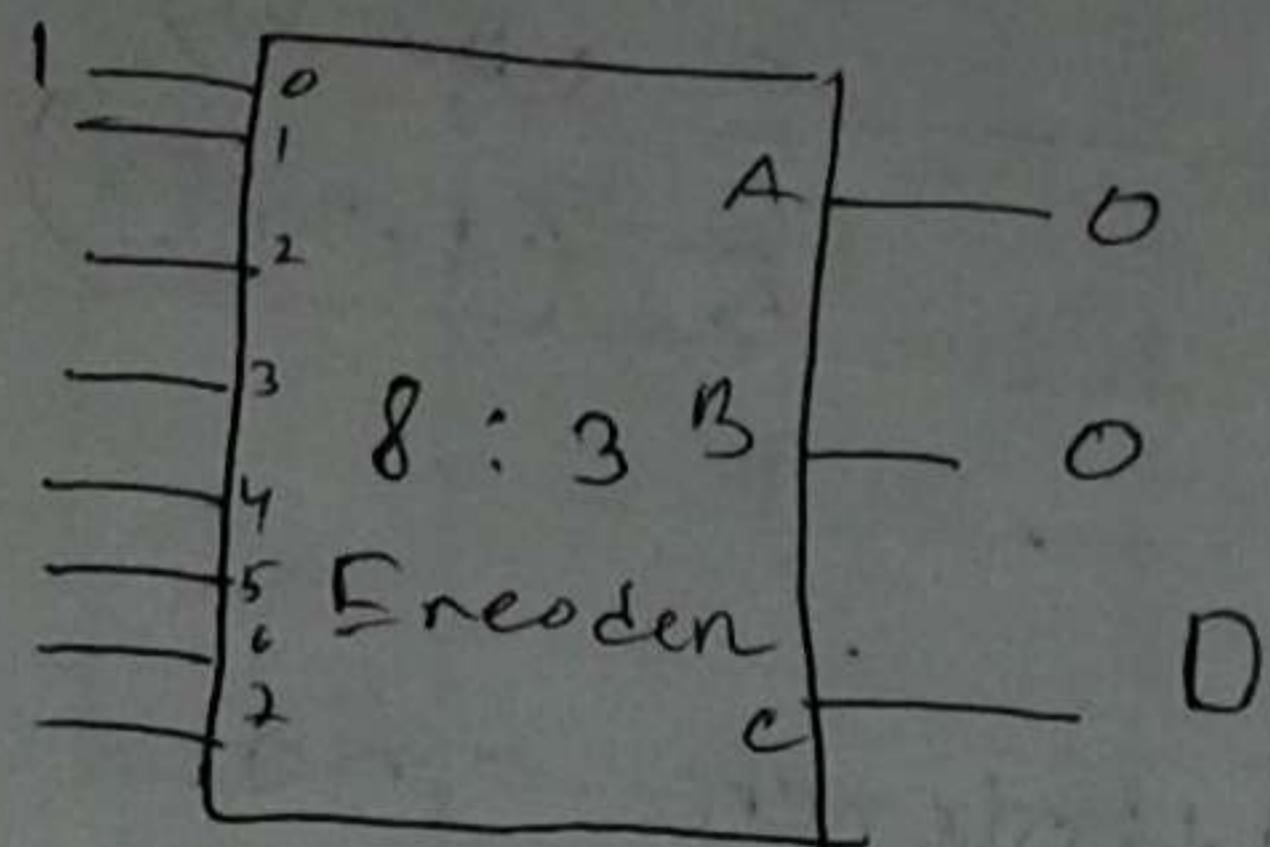


\rightarrow Binary & corresponding decimal output
Active 260,

11-E

11.11.14

Encoder



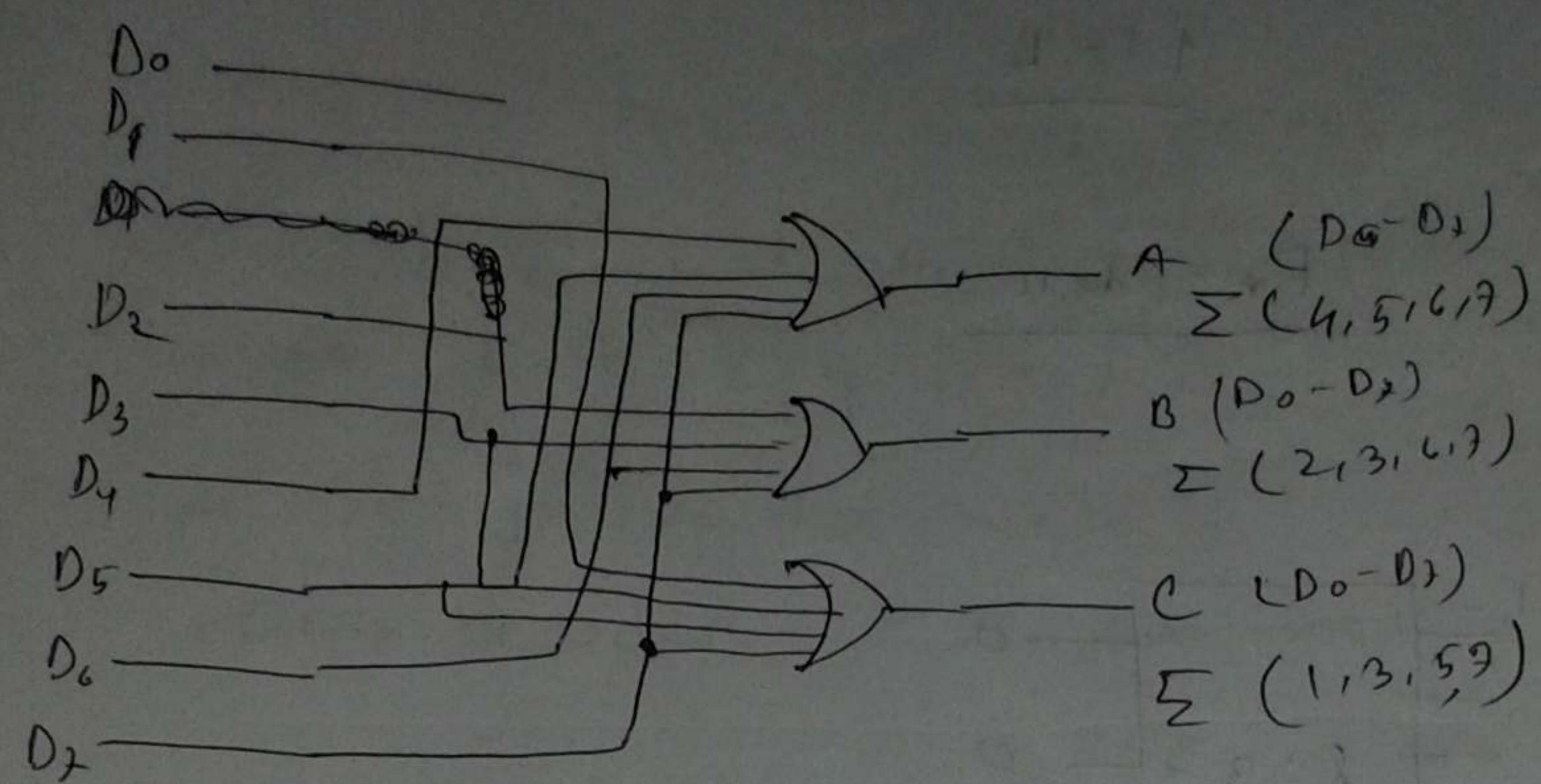
202³ 11122 5 to 3 input Active High 220 V.

Decimal Input Binary \Rightarrow Active High

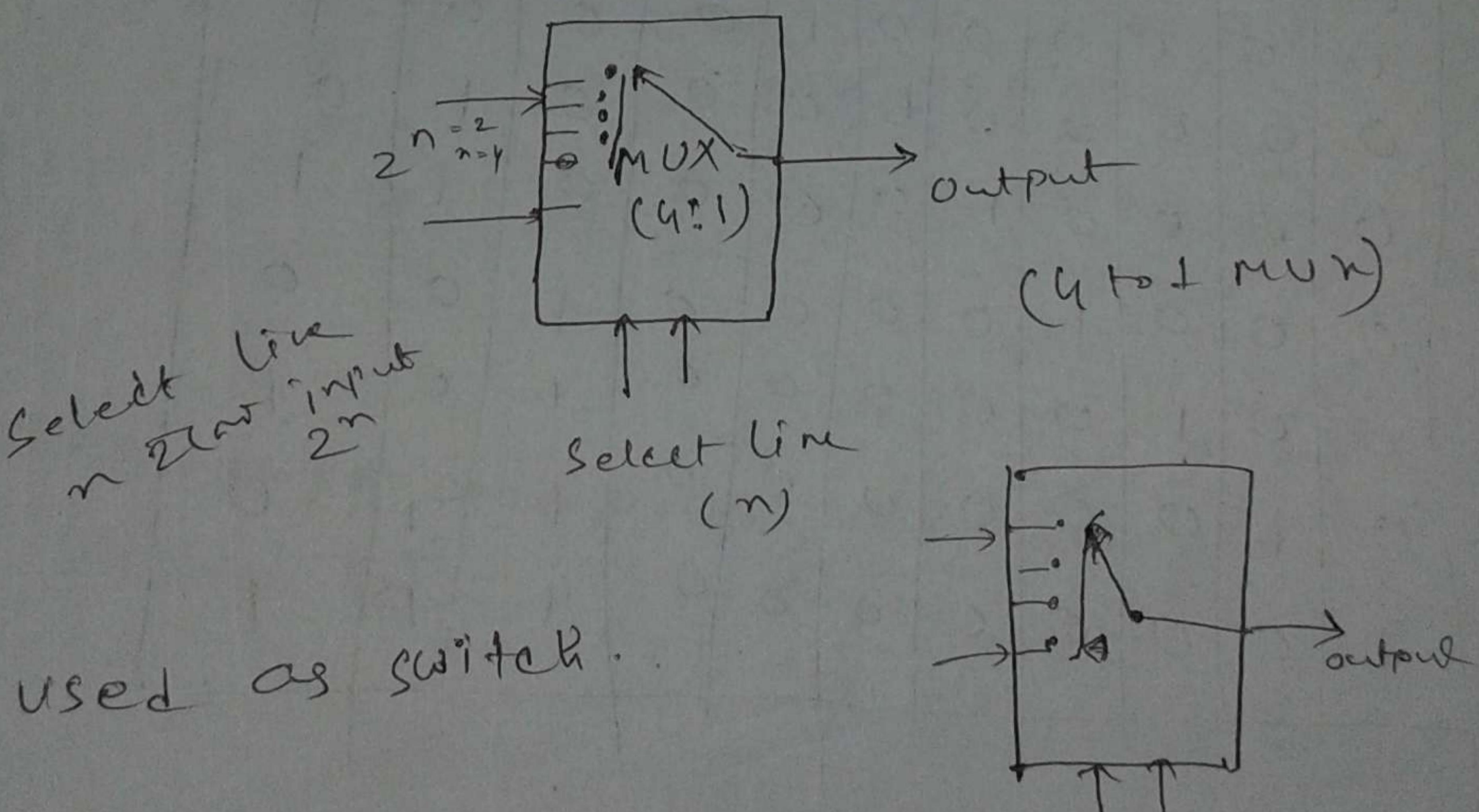
Input

Output

D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	A	B	C
0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	0	0	1
0	0	0	0	1	0	0	1	0
0	0	0	0	1	0	0	1	1
0	0	0	1	0	0	0	1	0
0	0	1	0	0	0	1	0	0
0	1	0	0	0	0	1	0	1
1	0	0	0	0	0	1	1	1

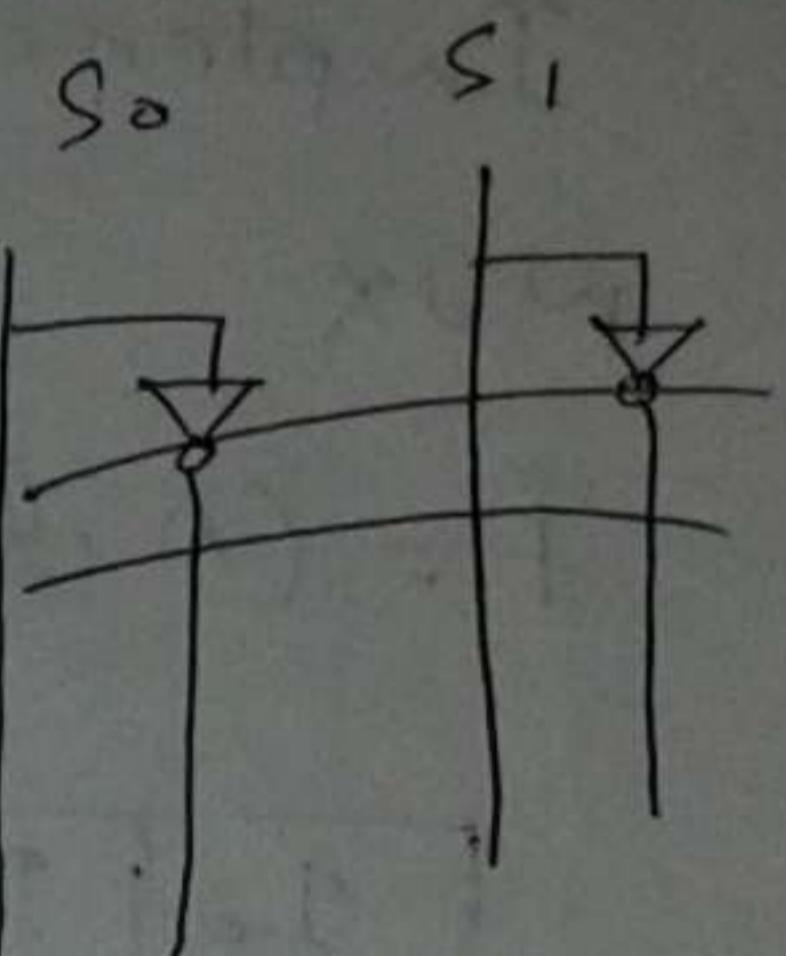


Multiplexers and Demultiplexers

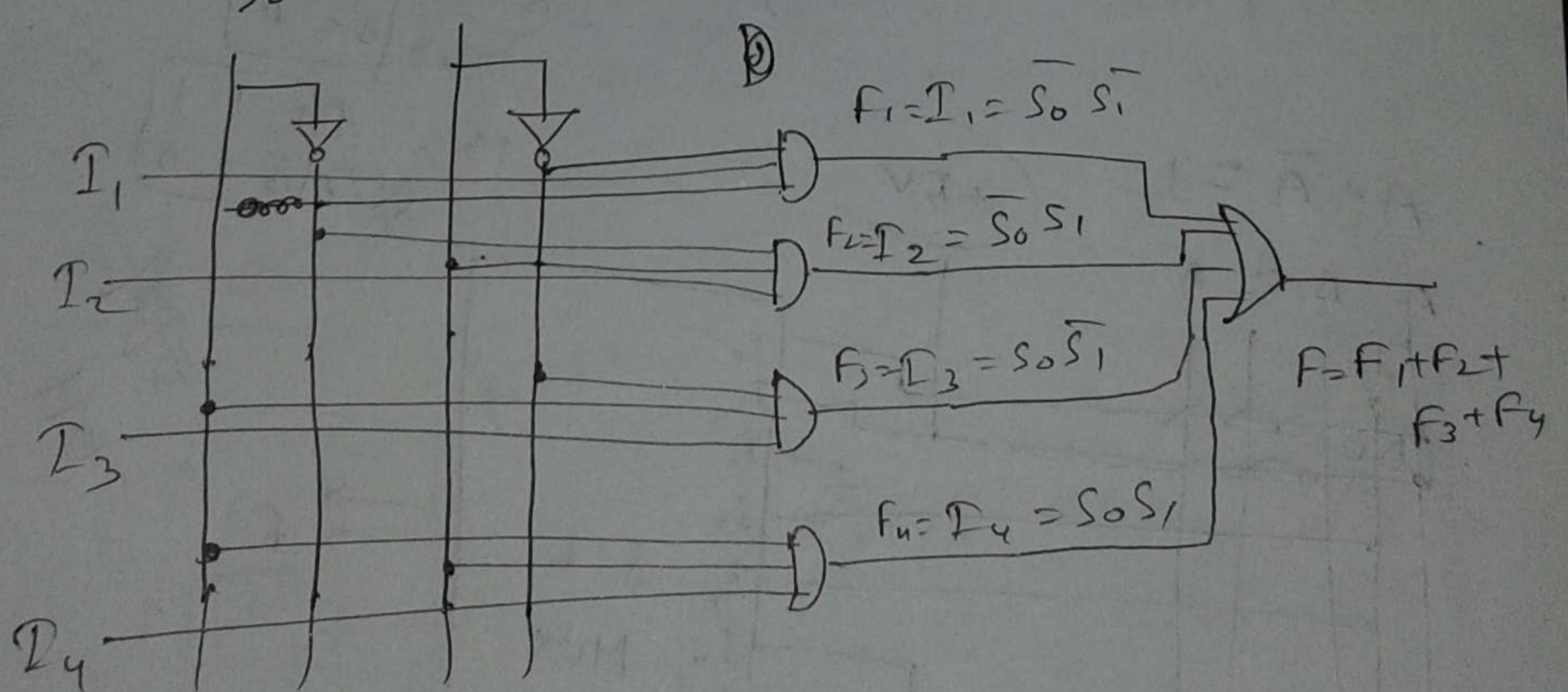


4:1 MUX

Input	Select line		Output
I	S_0	S_1	F
I_1	0	0	I_1
I_2	0	1	I_2
I_3	1	0	I_3
I_4	1	1	I_4



$$S_0 = 0, S_1 = 0$$



4:1 MUX

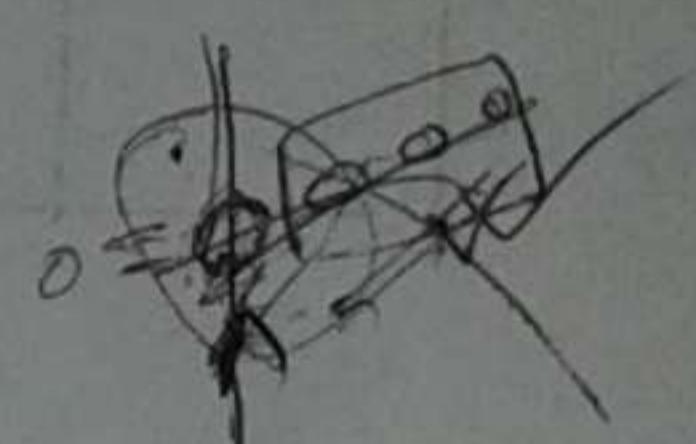
12.11.14

12-A

Implement the following function with MUX

$$F = (A, B, C, D) = \sum (0, 1, 3, 4, 8, 9, 15)$$

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
\bar{A}	0	0	2	3	4	5	6	2
A	8	9	10	11	12	13	14	15
	1	1	0	\bar{A}	\bar{A}	0	0	A

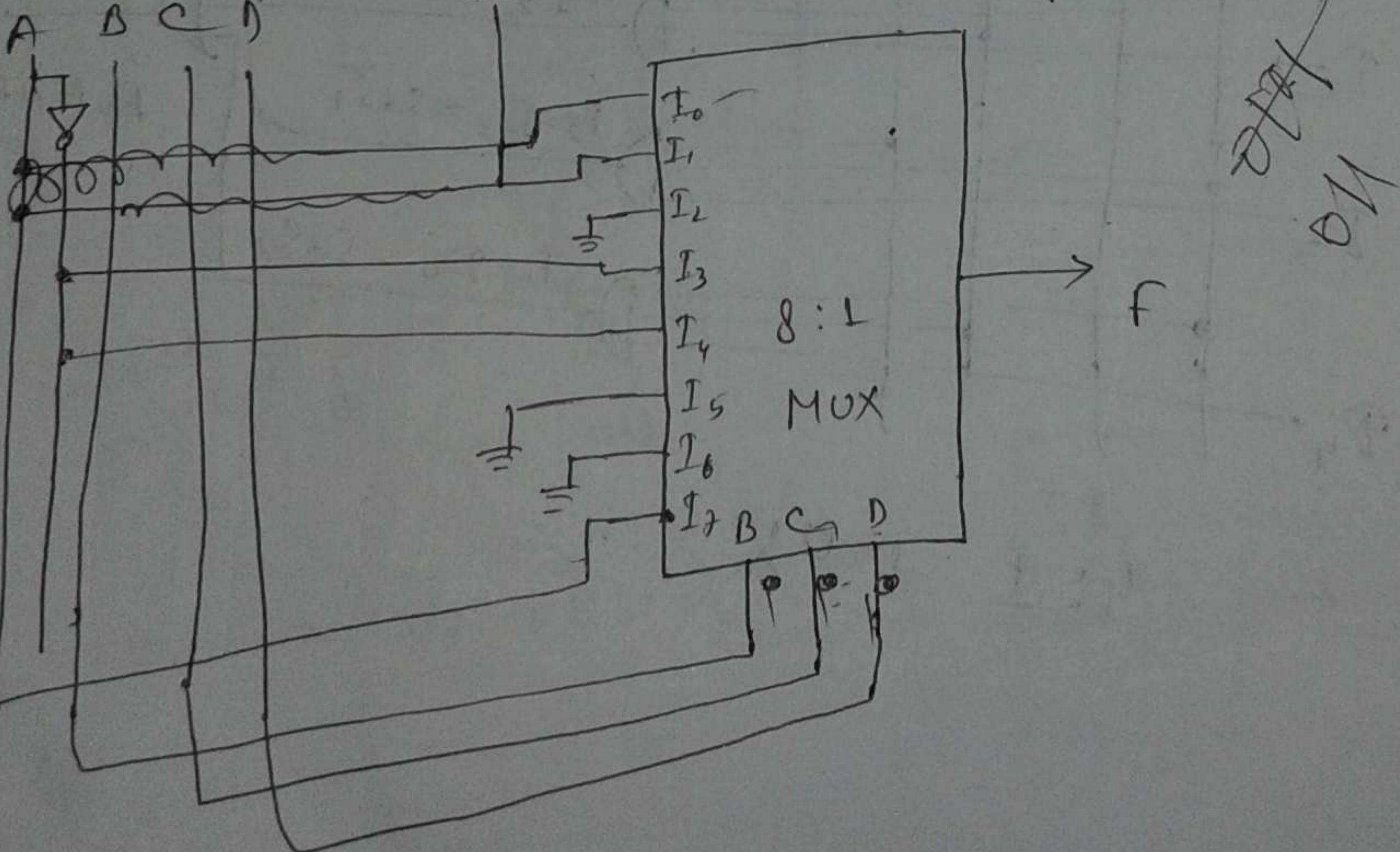


$$S = 1 \quad \begin{matrix} 0 & 0 & 0 \\ A & B & C & D \end{matrix}$$

$$15 - \quad \begin{matrix} 0 & 1 & 1 & 1 \\ A & B & C & D \end{matrix}$$

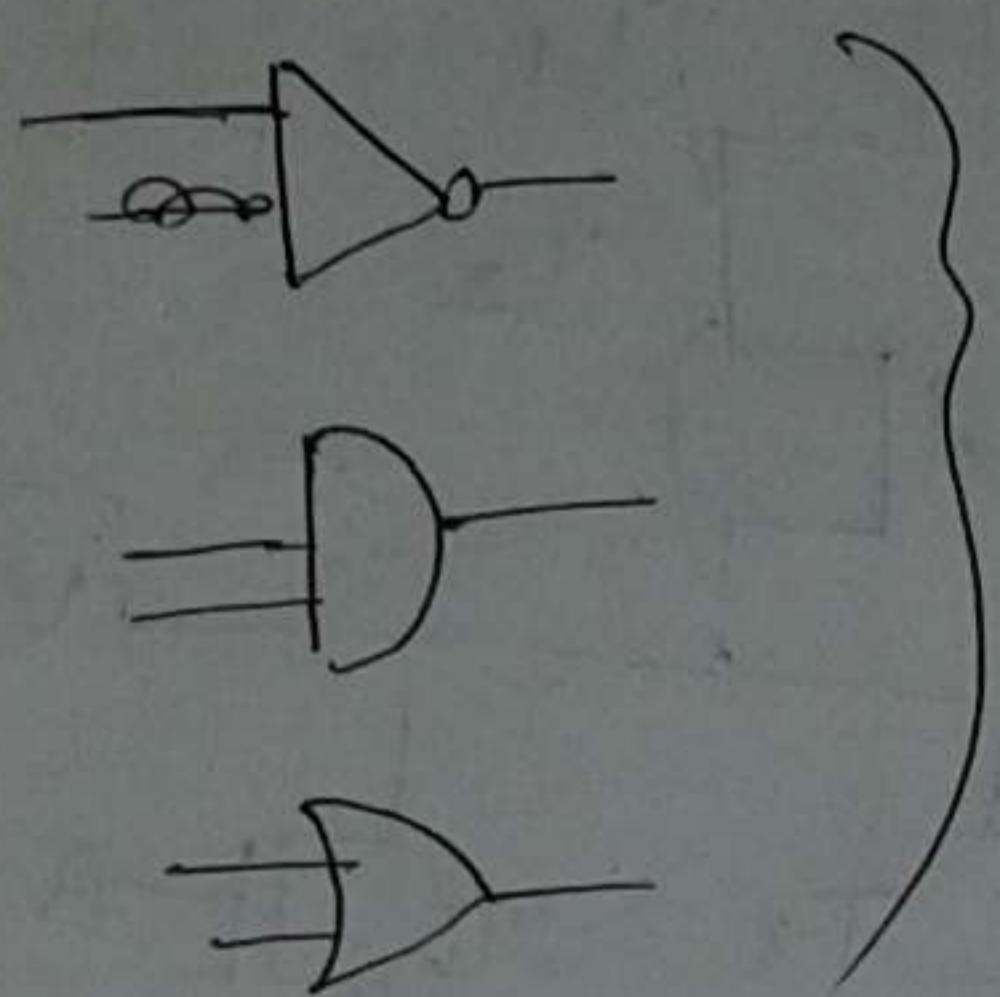
$$A + \bar{A} = 1$$

$$A \quad B \quad C \quad D$$



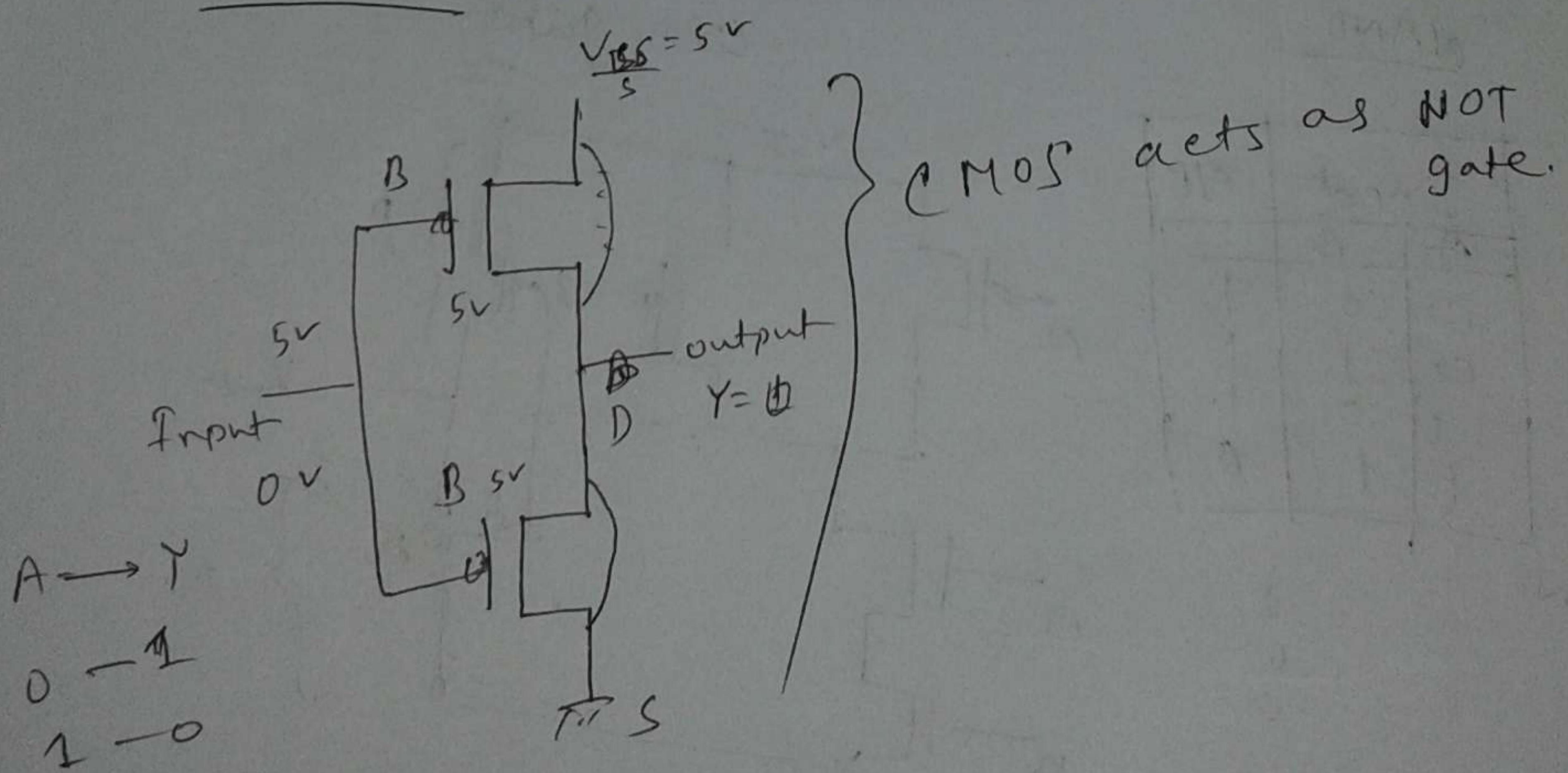
De Multiplexer (Self study)

Digital Logic Structures



All made by
CMOS, MOS (P,N)
↳ NMOS
↳ PMOS

CMOS

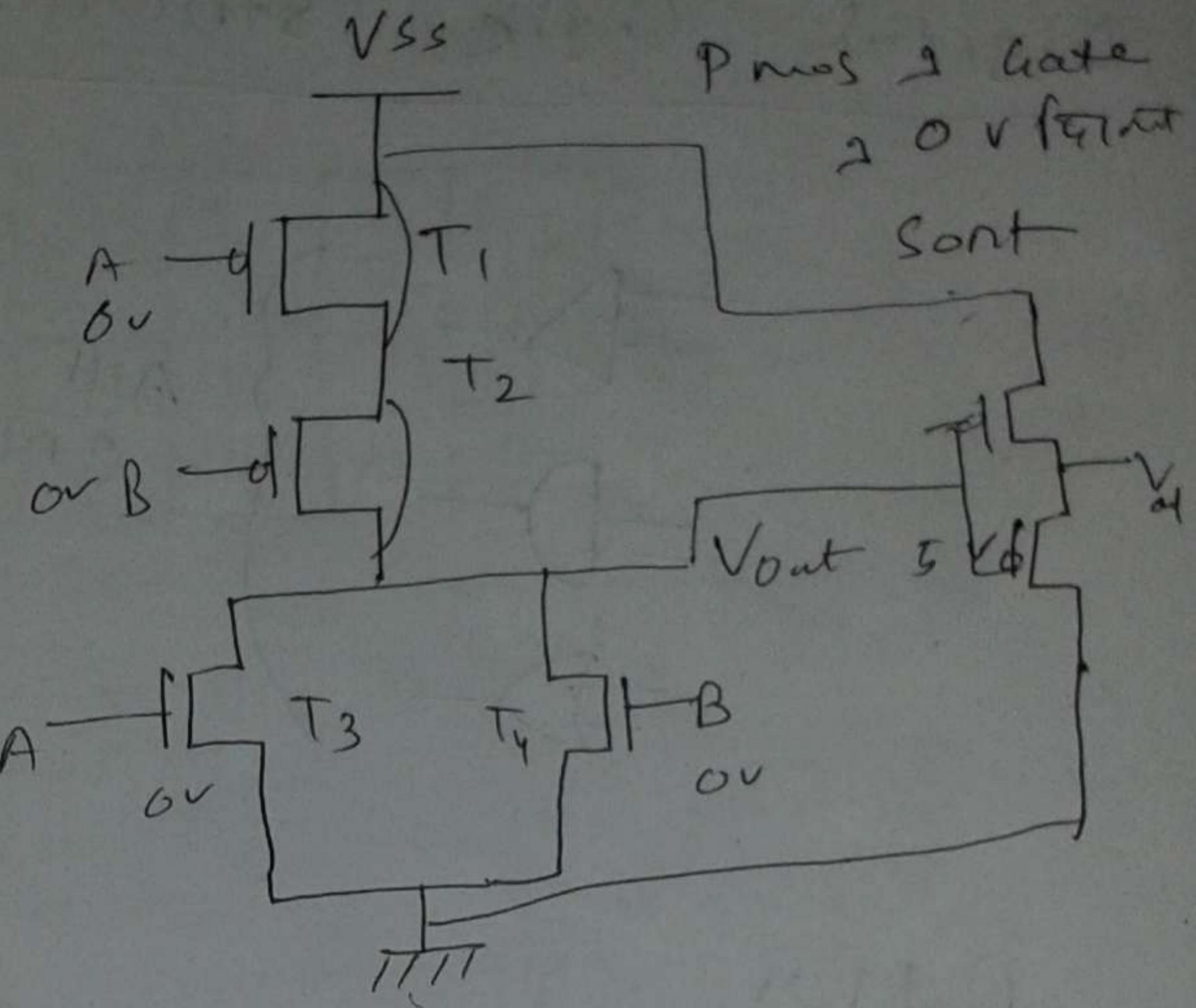


16.11.14

12-C

NOR Gate using CMOS

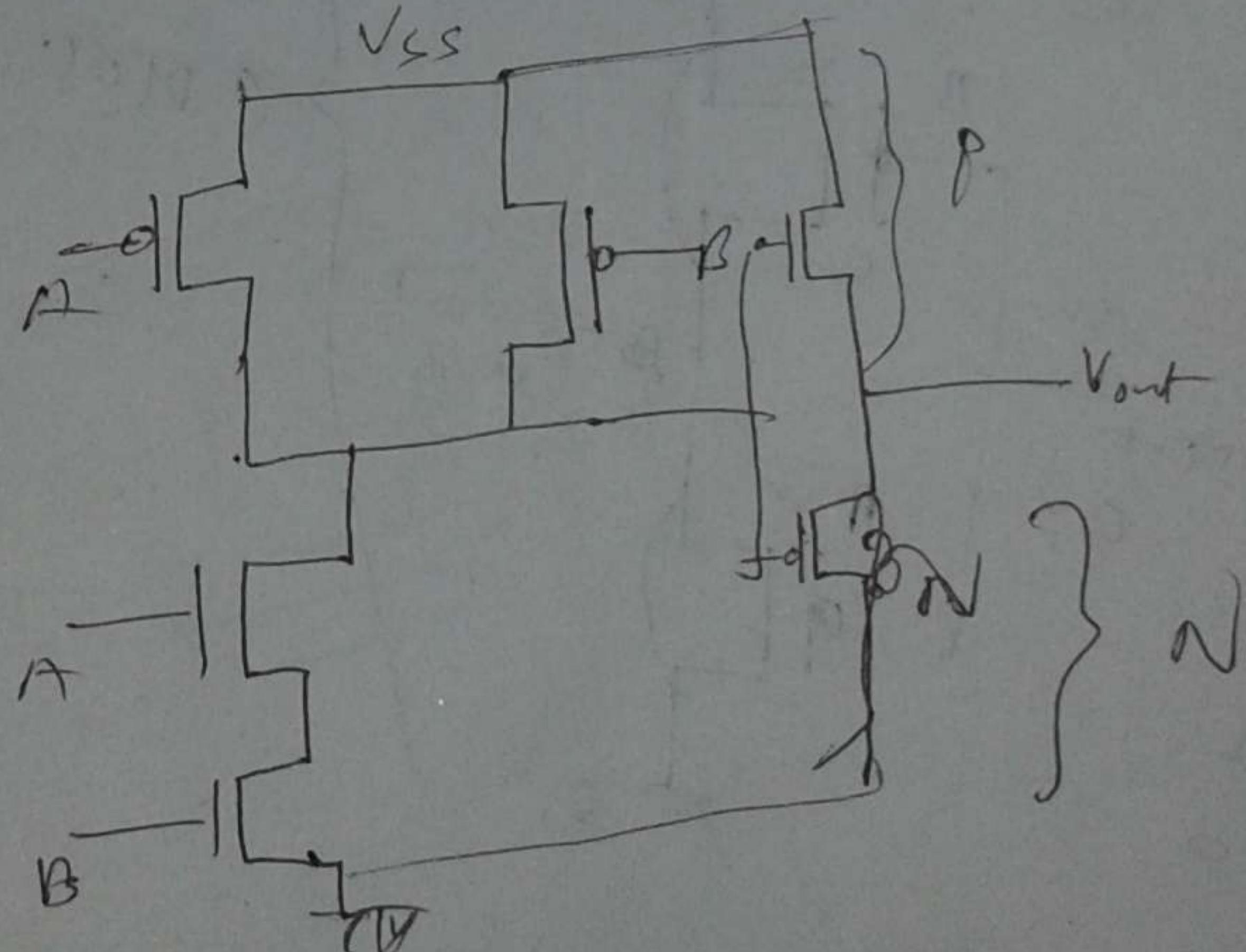
Input		O/P
A	B	
0	0	1
0	1	0
1	0	0
1	1	0



NAND

Input		O/P
A	B	
0	0	1
0	1	0
1	0	0
1	1	0

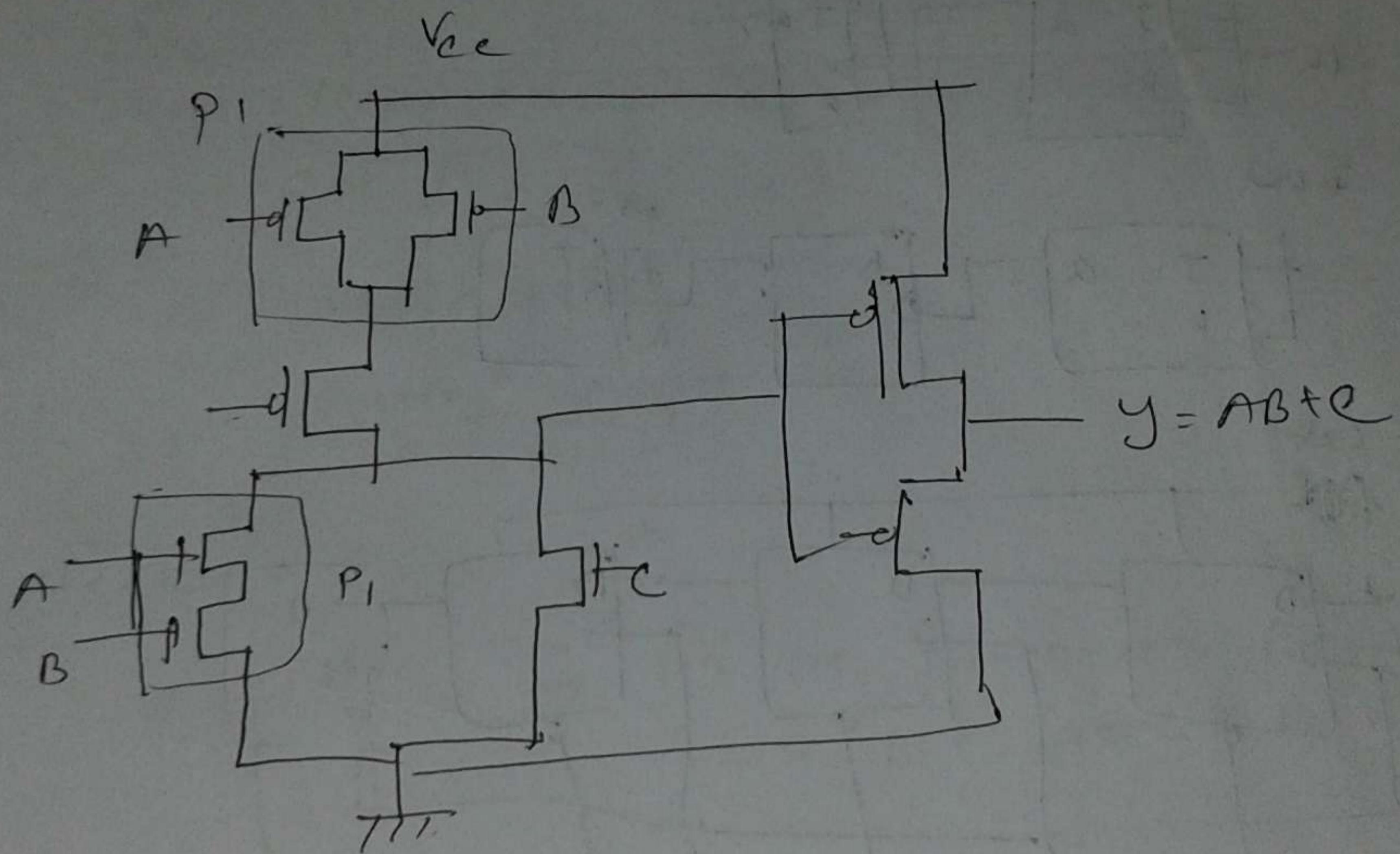
One gate



NAND

$y' = \overline{AB+e}$ implement this boolean func by
C $P_y' = \overline{P_1+e}$
MOS..

$$y = P_1 + e$$



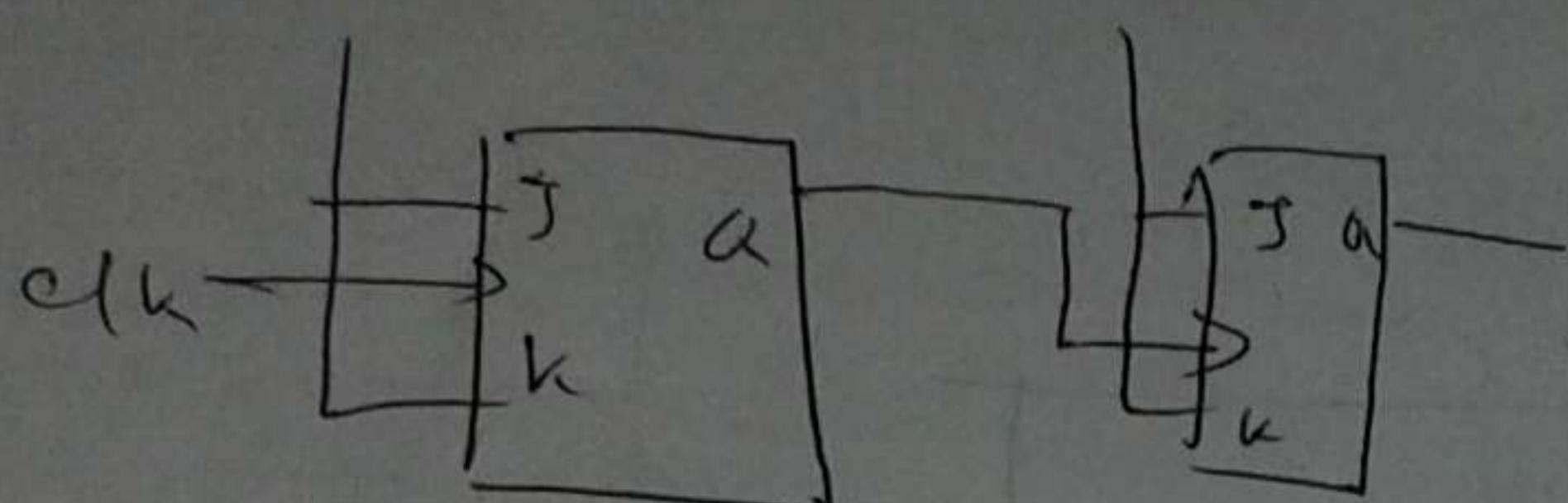
10.11.14

12-E

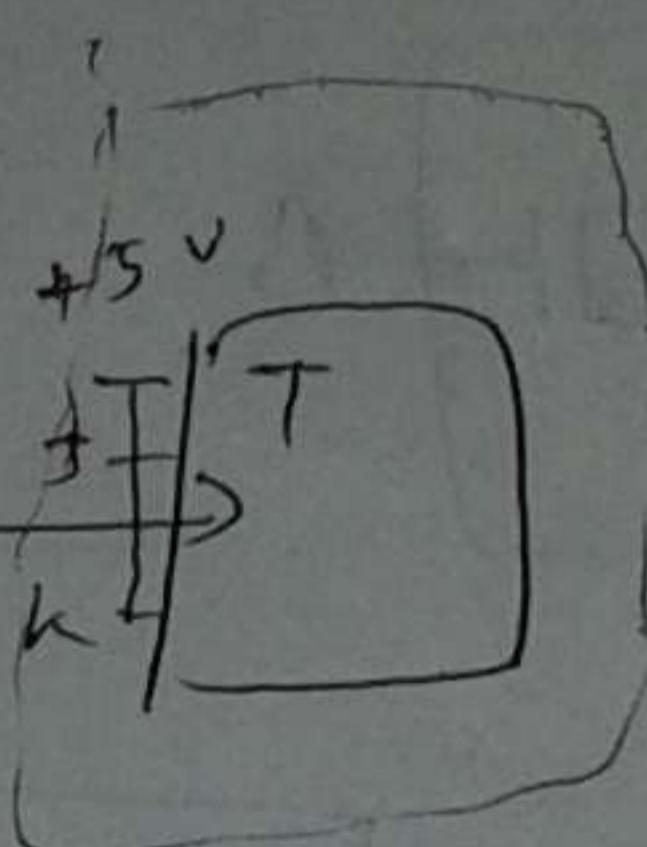
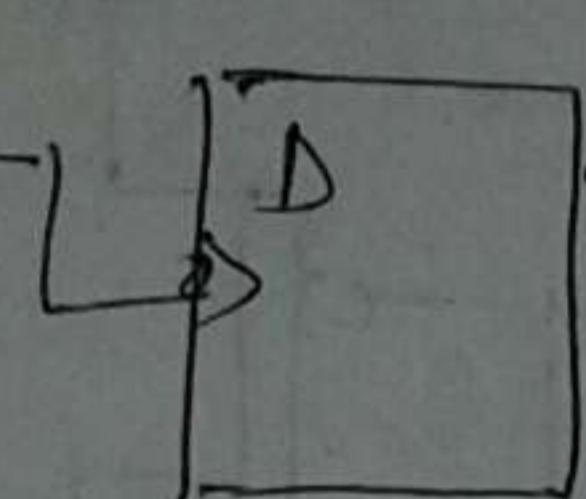
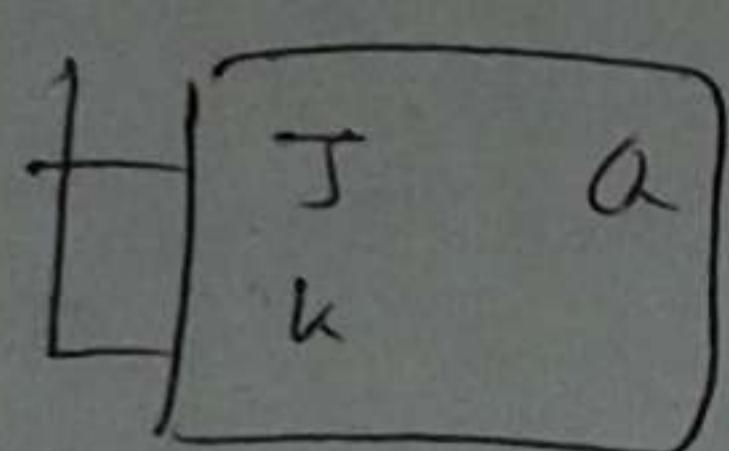
Counting. Asynchronous:

+5v

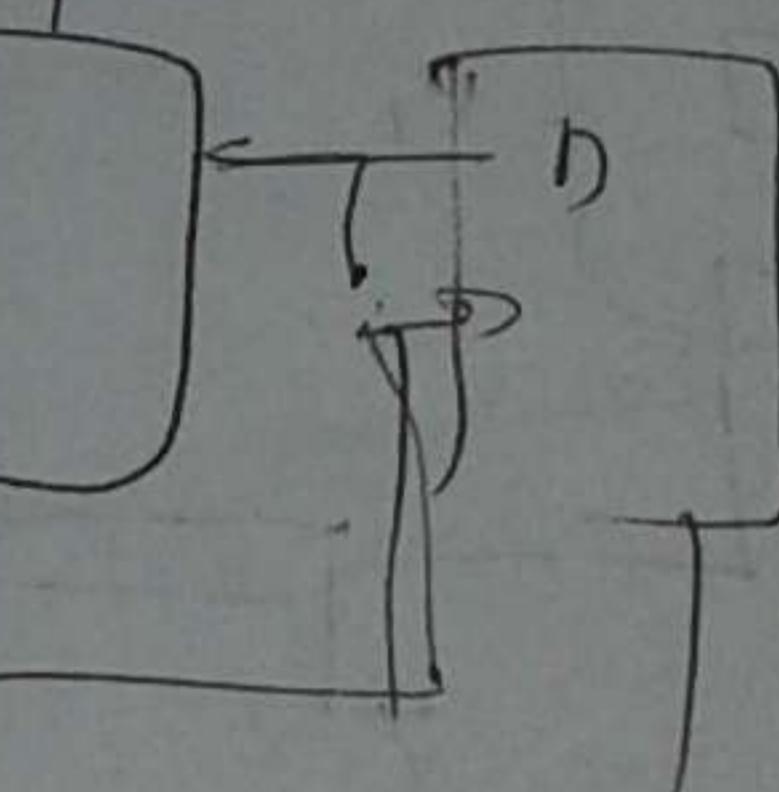
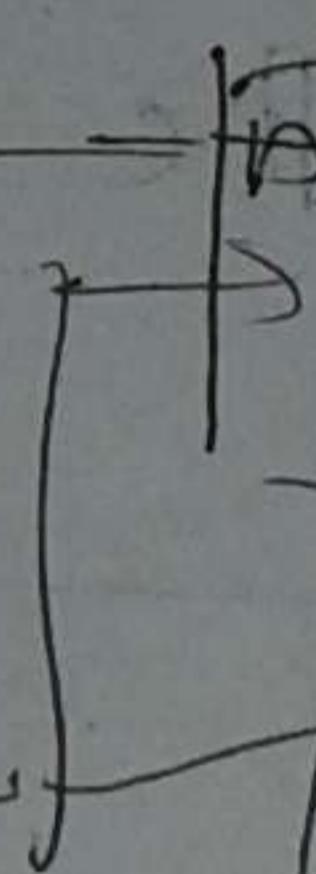
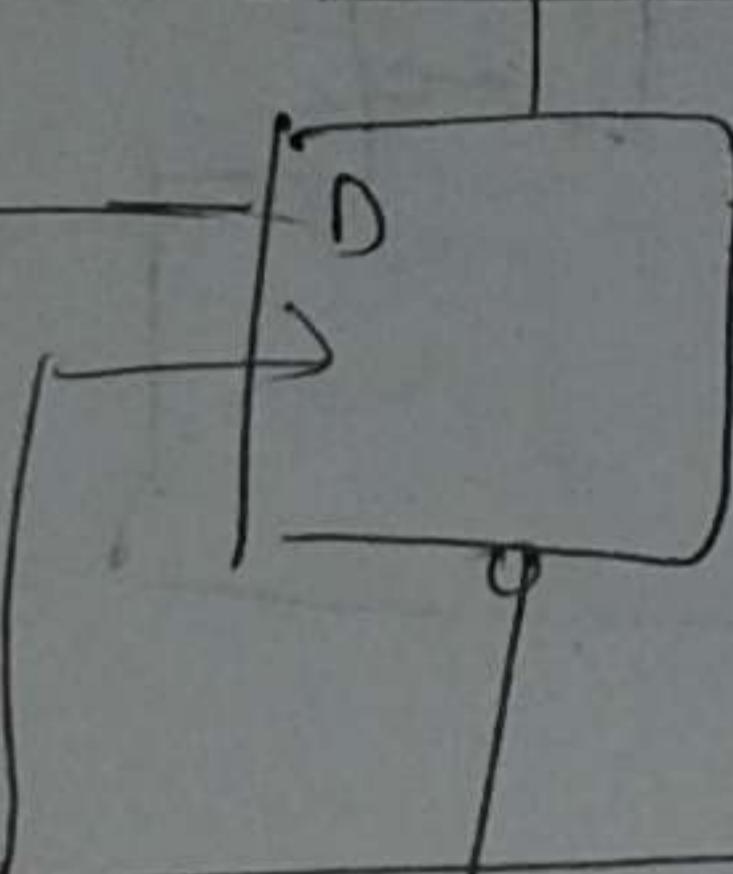
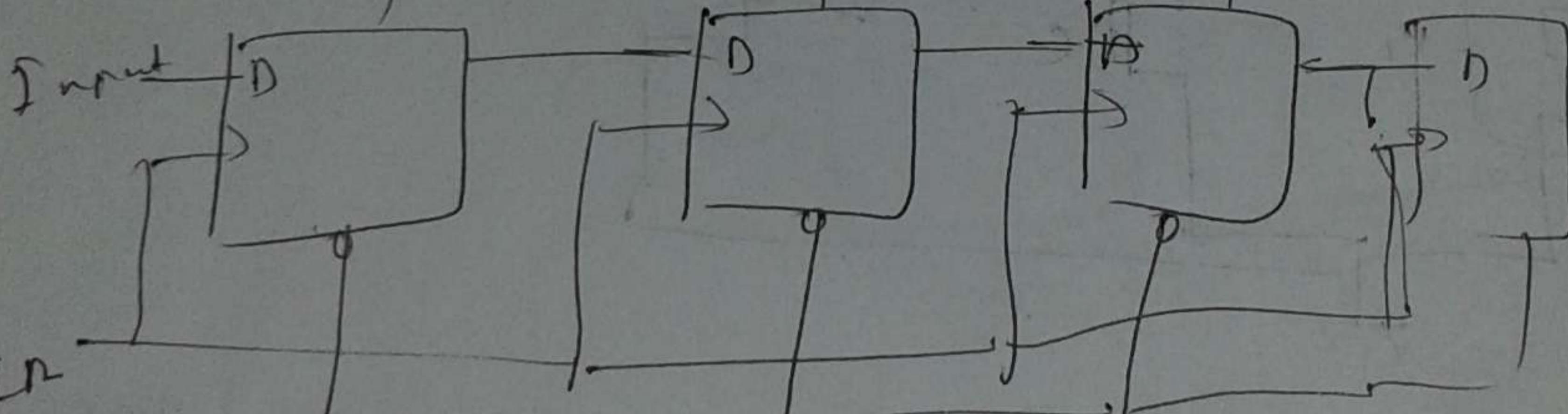
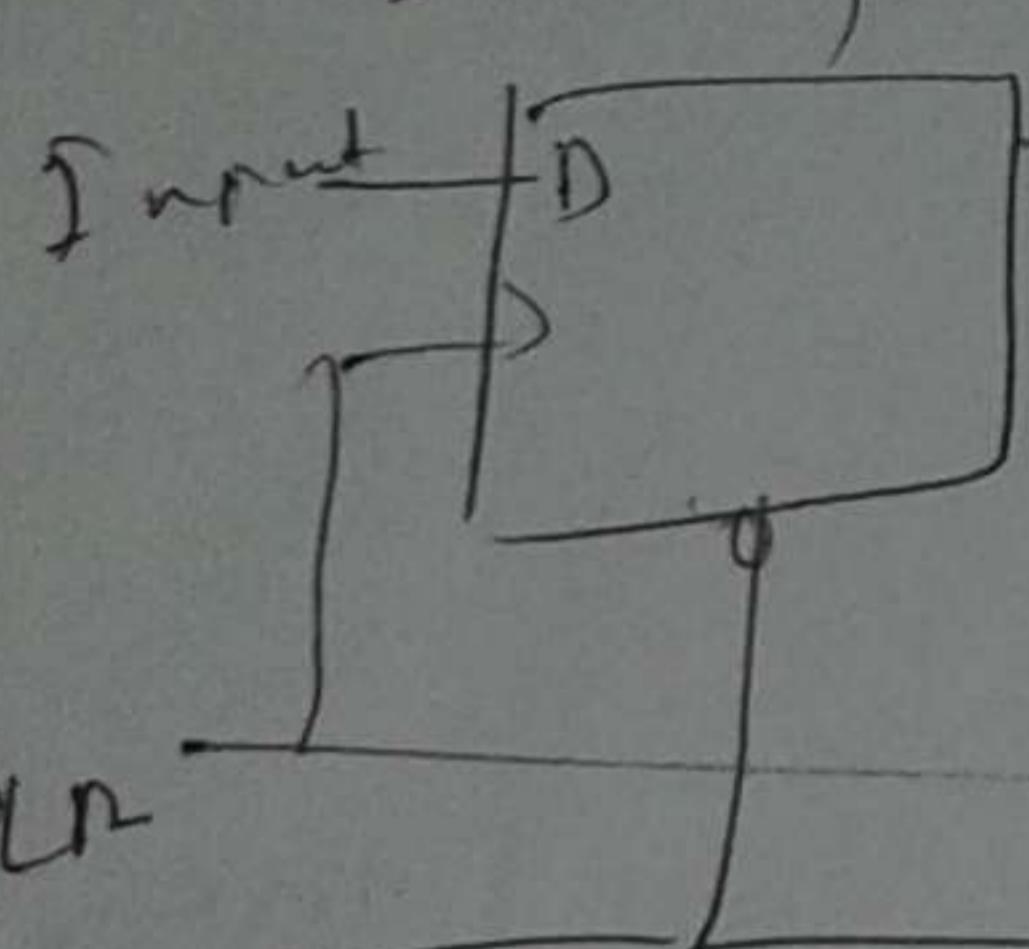
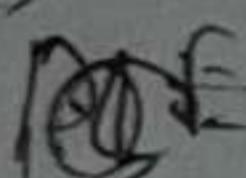
+5v



+5v



PRESET



241194 \Rightarrow Universal shift Register

for operation w.r.t 2M

13-e \Rightarrow quiz.

22.11.14

13-A

{10}

13-E

29.11.14

35_{10}

00000000-0 > 1 byte

00111111-63

$E^f_{16} = 1110\ 1111$

Set resting active
= 0 1

clear = 1 0

$0 - 113_{10} \rightarrow 113$ to Binary \rightarrow Format
2⁷ Bit ~~9⁷~~ FF instead,

$\frac{1024}{2^6} kif_2 = 16$

$MOD \rightarrow 10$

0000
 $\rightarrow 11\ 111$
000

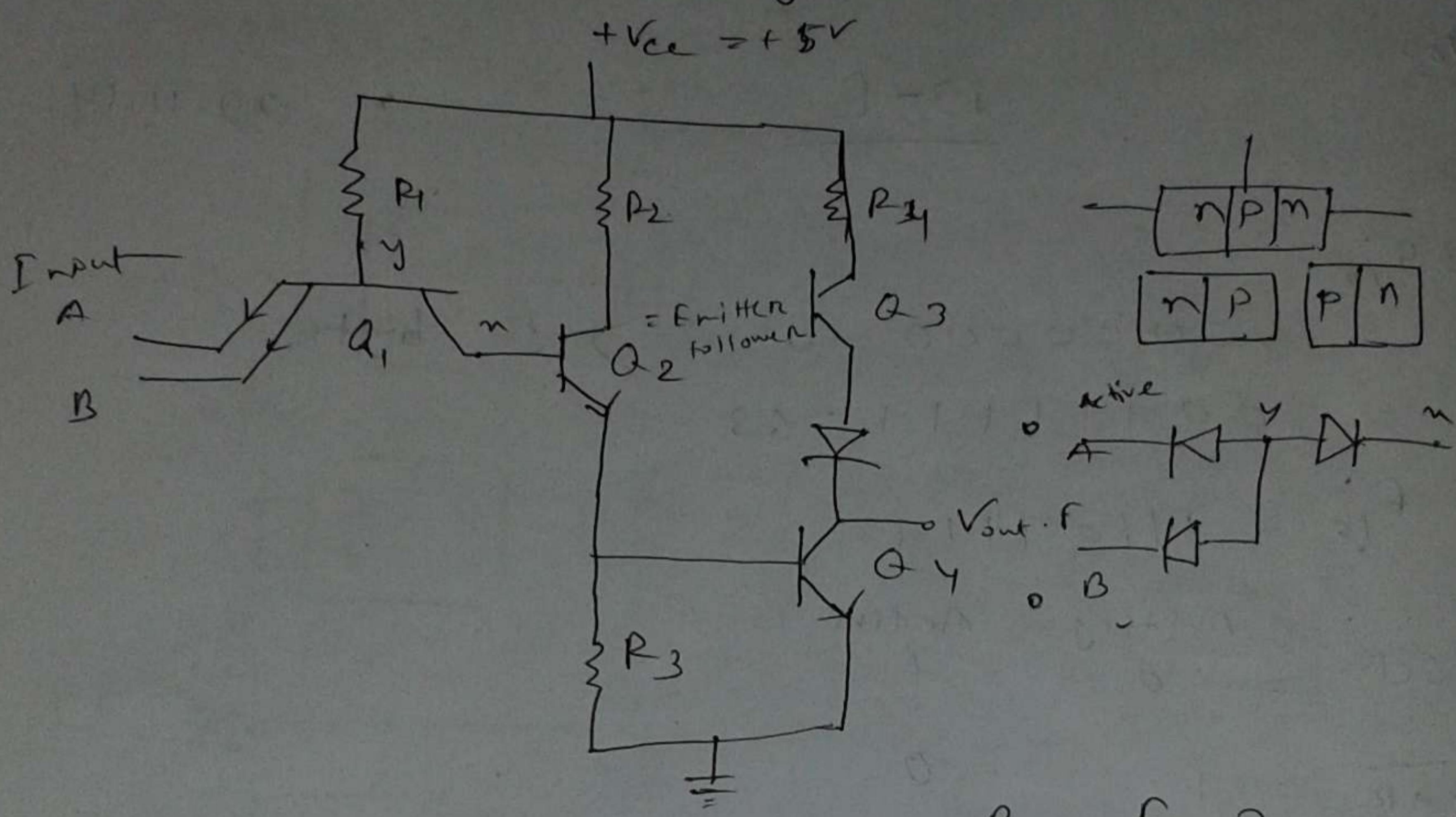
1 0 1 0
↑ ↑
0 0

counter register

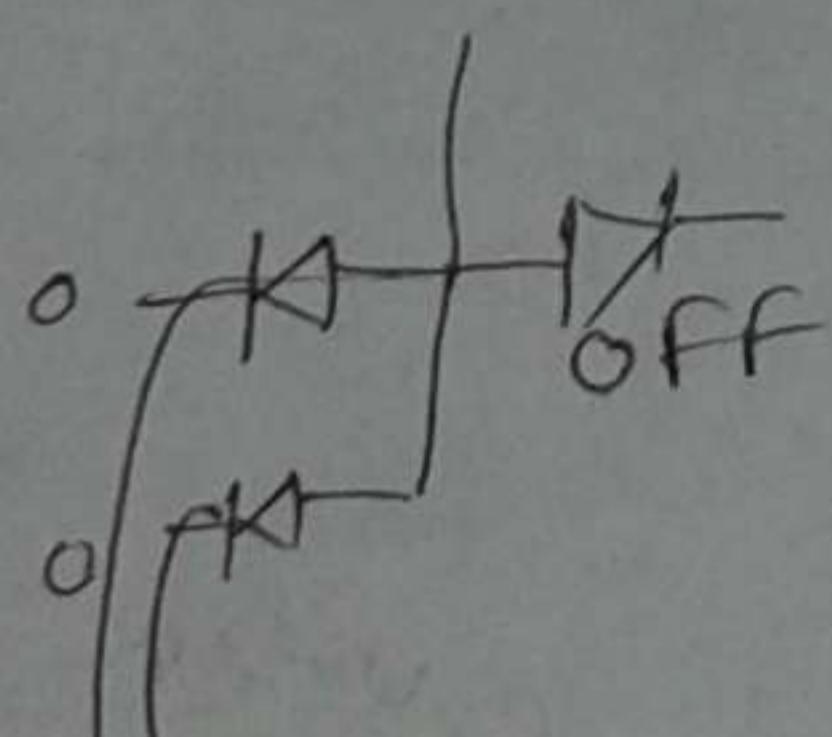
32 - 0000
64 - 0000
70 - 0110

full adder constructed by
2 Half Adder and one
OR

Basic TTL NAND gate :

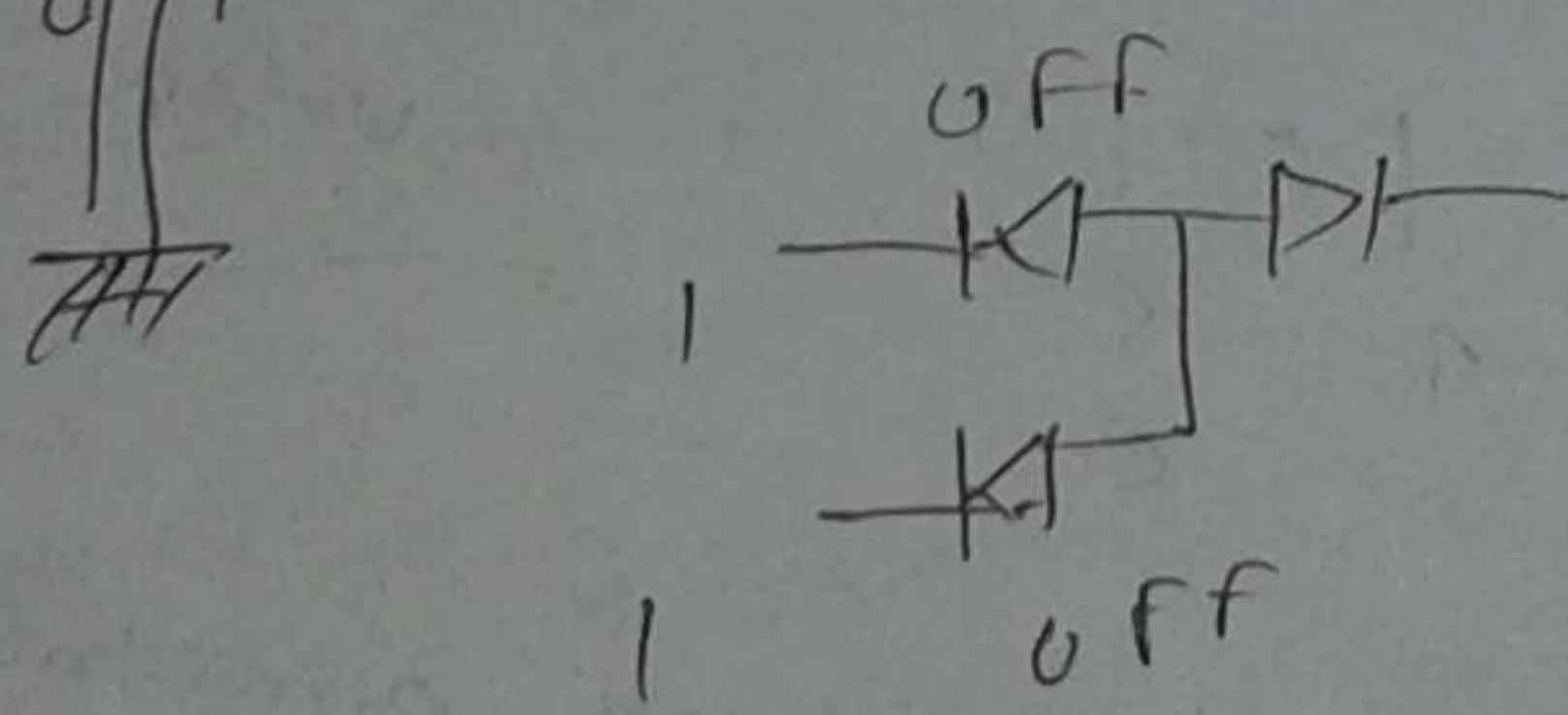


$$\begin{array}{ccc} A & \diagup & B \\ 0 & & 0 \end{array} \quad \begin{array}{c} F \\ 1 \end{array}$$



A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

TTL acts as
NAND
gate



Art 8.2: TTL Logic family

NOR \rightarrow self study

14-A

30.11.14

MOD 55

Shift Register

Synchronous UP/Down counter

2 to 4 decoder / 4-16 decoder

$1 \rightarrow 5 \rightarrow 2 \rightarrow 1 \rightarrow$ output frequency

Operating principle of Binary counter

Johnson counter wave & shape

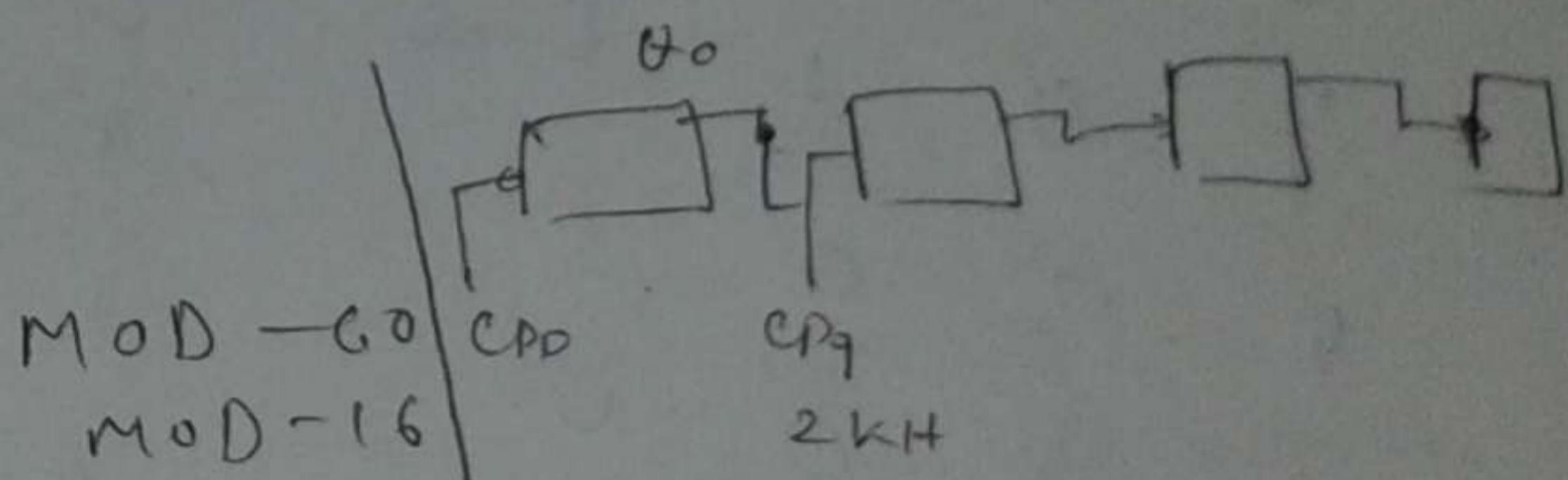
74LS293 (input at CP_i with 2 kHz)

$$\text{output freq.} \Rightarrow \frac{2 \text{ kHz}}{8} = \frac{2 \text{ kHz}}{2^3}$$

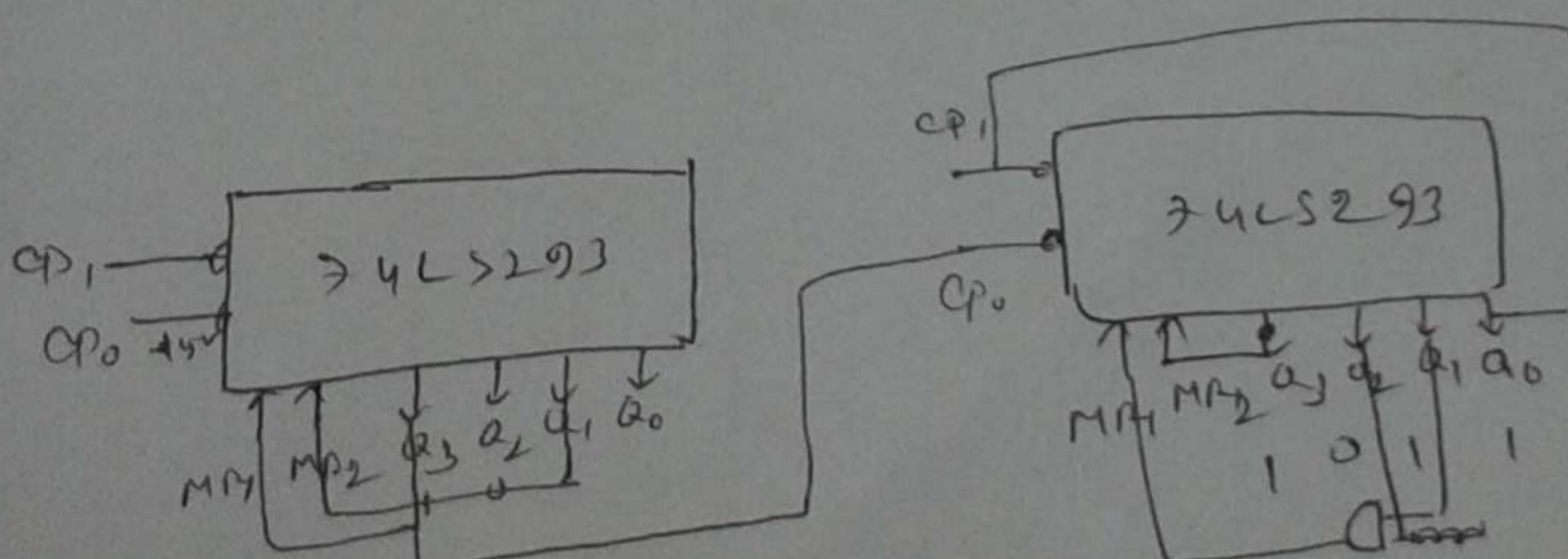
74LS293 (Advantage)

why we use Active low.

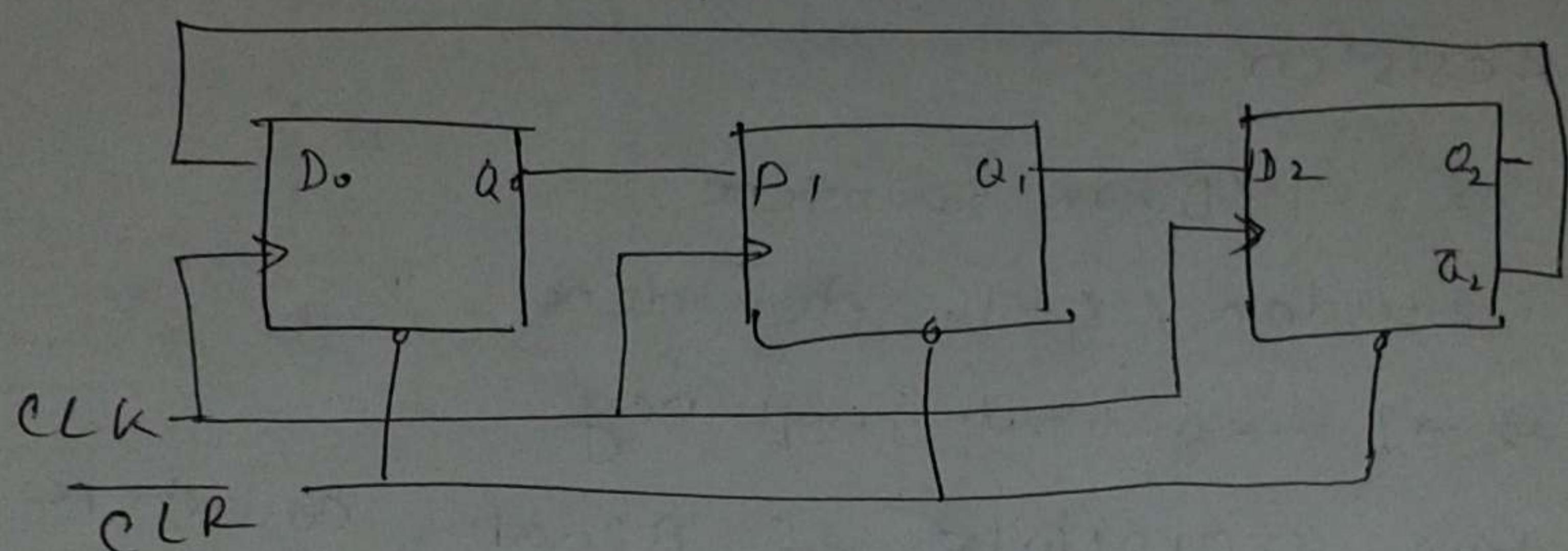
SR FF



MOD - 55 \rightarrow [Mod 11] [Mod 5]



Shift Register:



Johnson Ring counter

	Q ₀	Q ₁	Q ₂	
0	0	0	0	
1	1	0	0	
2	1	1	0	bit 0
3	1	1	1	
4	0	1	1	
5	0	0	1	
6	0	0	0	

Preset

CLR

↓

	Q ₀	Q ₁	Q ₂
0	0	0	0
1	1	0	0
2	0	1	0
3	1	0	0

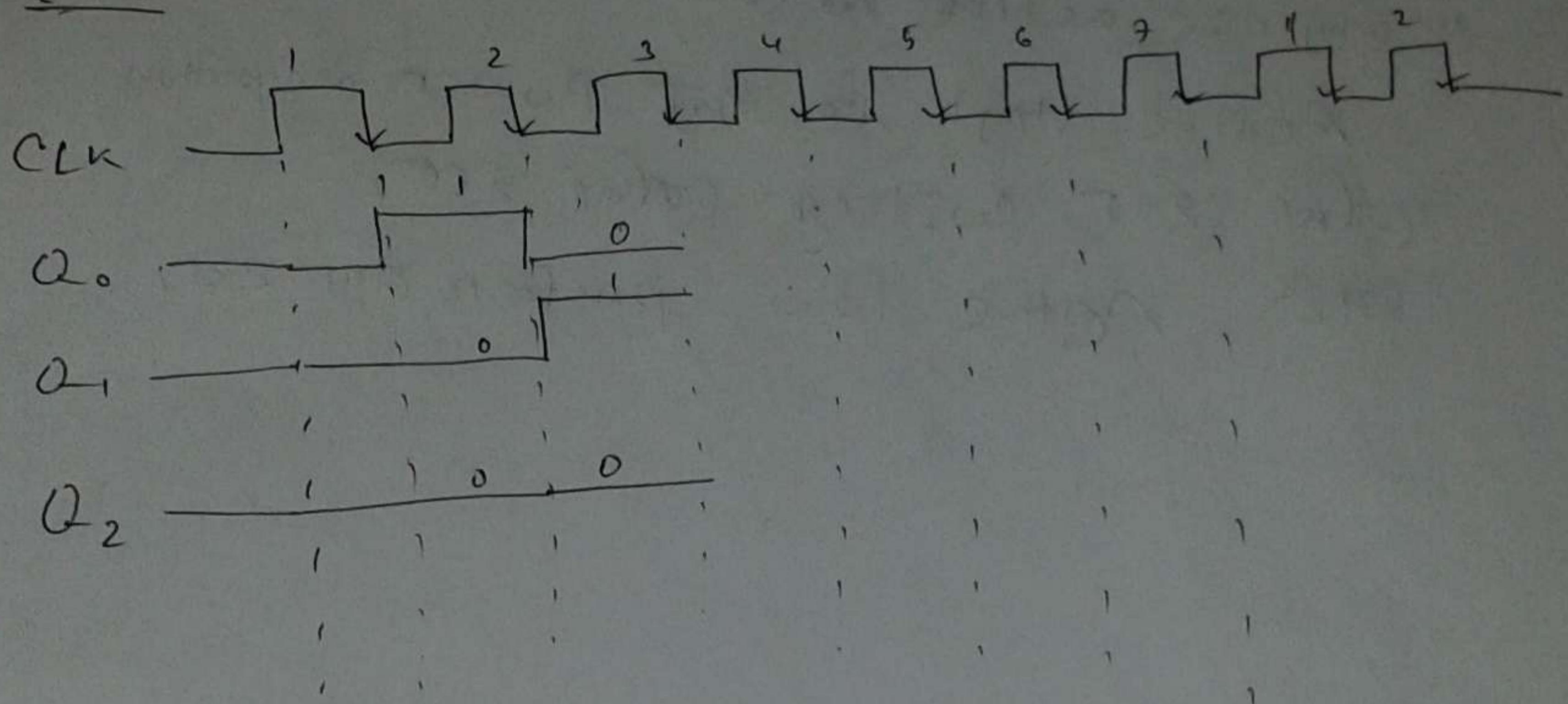
3

Synchronous up/down counter:

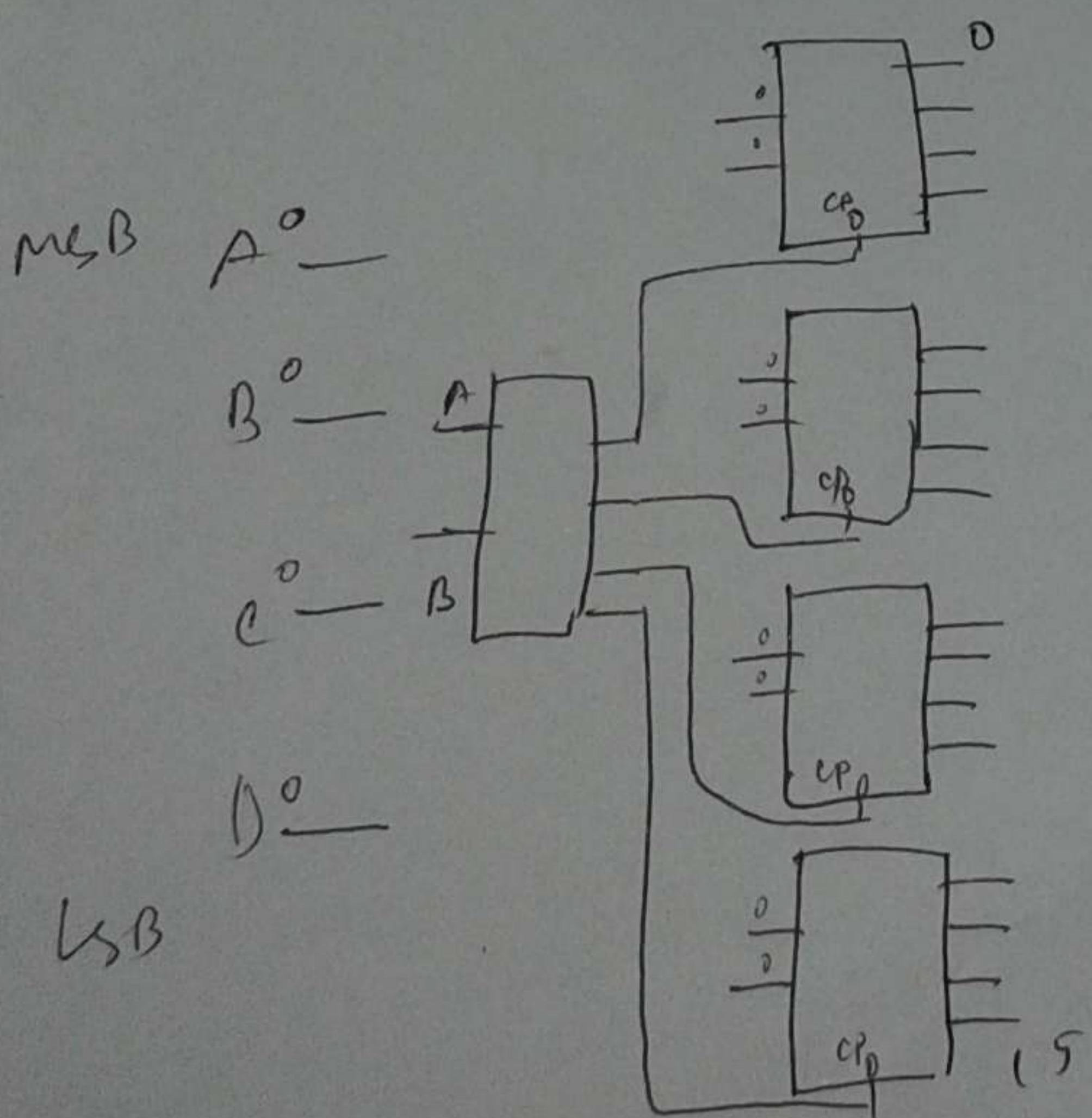
Up counter 0-1-2-3-4-5-6-7-0

Down - 7-6-5-4-3-2-1-0-7

UPC



2:4 Decade:



1-5-2-1 State
25 acre count acre

3rd state

3 kHz Δν

$$\frac{3}{3} = 1$$

Binary counter: T-R flip flop

Active input AND gate
output.

why use active low:

Active high \rightarrow high Power dissipation
~~for 2¹⁵, wasting for 2¹⁵,~~

GT² Active low prefer 2¹⁵,