NMOS Fabrication

Mahit Kumar Paul
Assistant Professor, Dept. of CSE
RUET, Rajshahi-6204

mahit.cse@gmail.com
mahit@cse.ruet.ac.bd

Fabrication

Semiconductor device **fabrication** is the **process** used to manufacture **semiconductor** devices, typically the metal-oxide **semiconductor** (MOS) devices used in the **integrated circuit** (**IC**) chips that are present in everyday electrical and electronic devices.

NMOS Fabrication

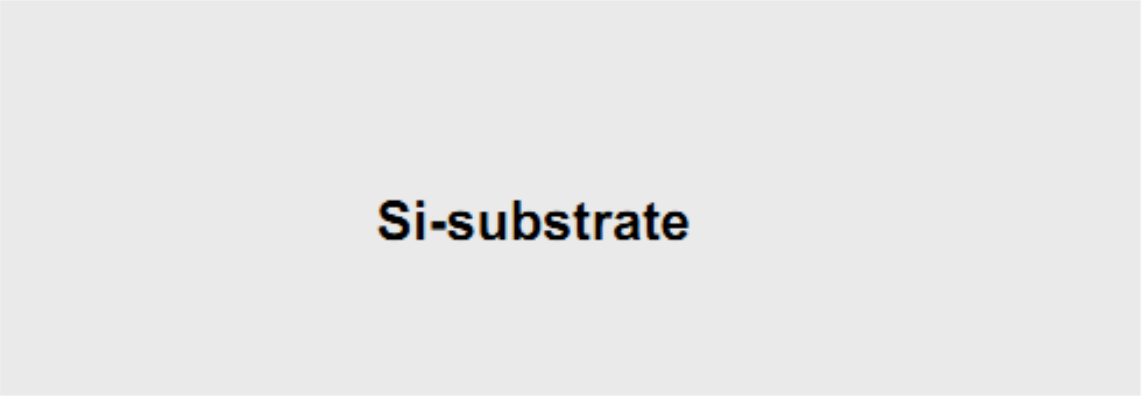

Fig. (1) Pure Si single crystal

Wafer Diameter Trends

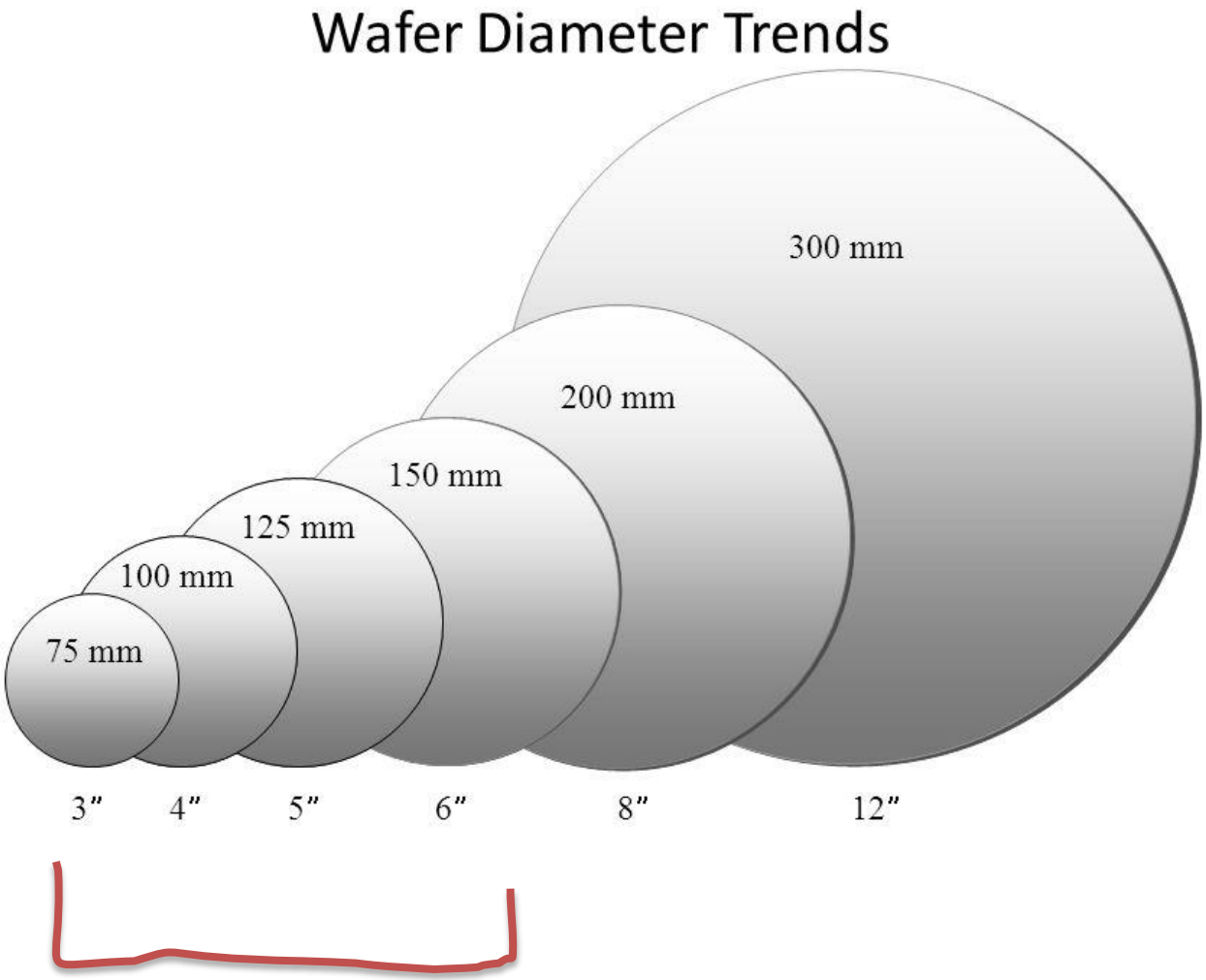

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Fig. (2) P-type impurity is lightly doped

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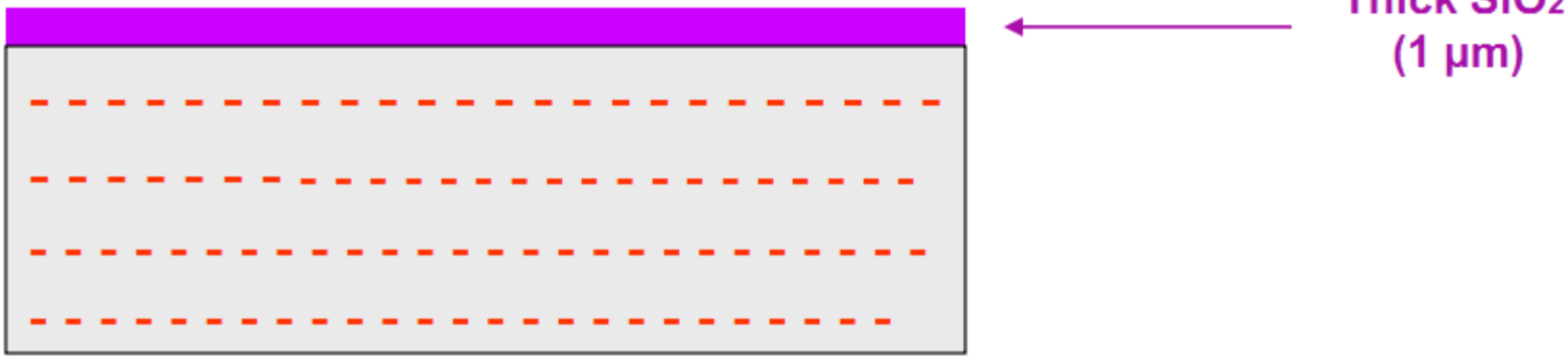

Fig. (3) SiO_2 Deposited over si surface

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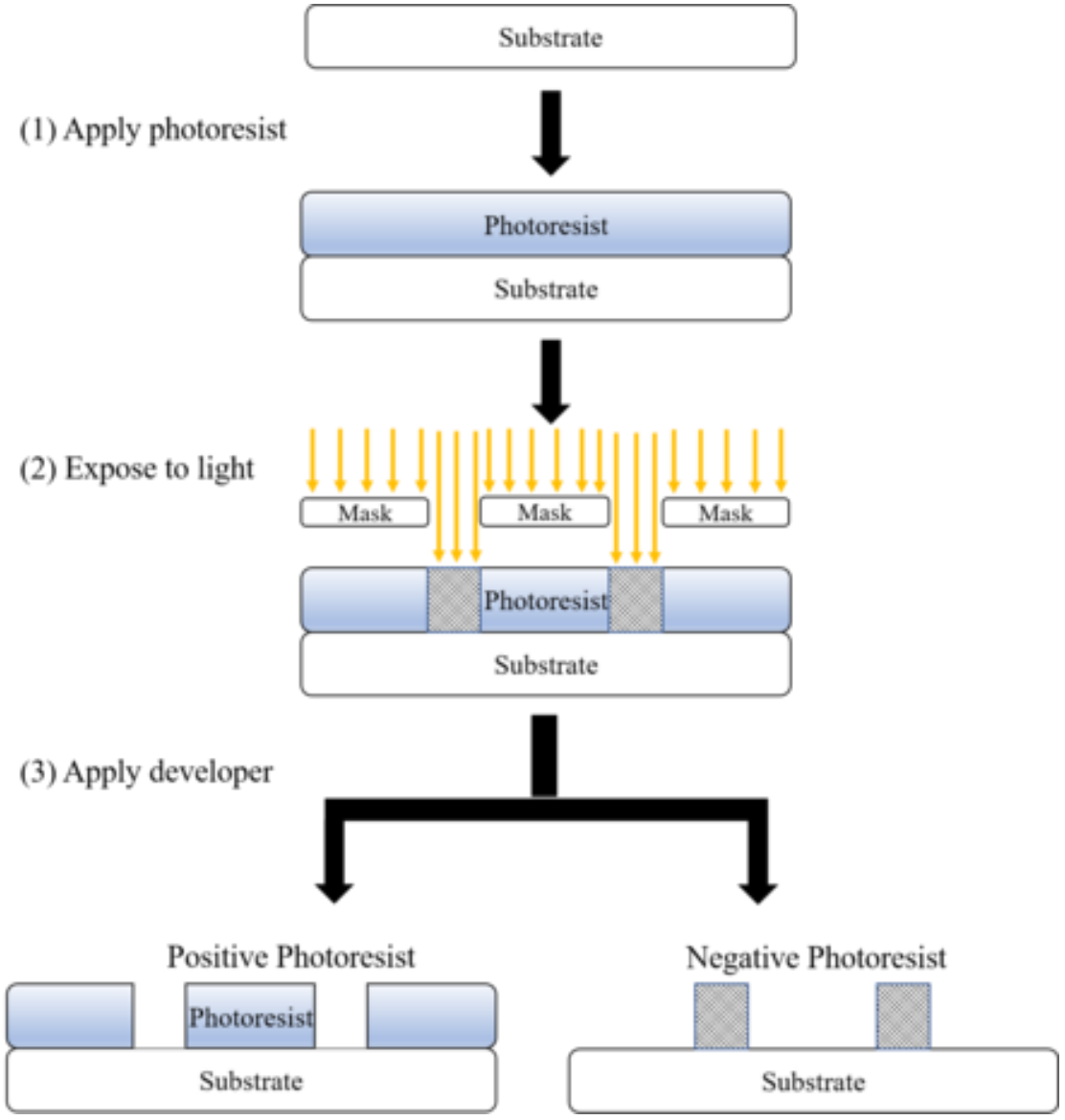
Fig. (4) Photoresist is deposited over SiO_2 layer

Photoresist

- A photoresist is a light-sensitive material used in several processes to form a patterned coating on a surface.

- The process begins by coating a substrate with a light-sensitive organic material. A patterned mask is then applied to the surface to block light, so that only unmasked regions of the material will be exposed to light. A solvent, called a developer, is then applied to the surface. In the case of a positive photoresist, the photo-sensitive material is degraded by light and the developer will dissolve away the regions that were exposed to light, leaving behind a coating where the mask was placed. In the case of a negative photoresist, the photosensitive material is strengthened (either polymerized or hardened) by light, and the developer will dissolve away only the regions that were not exposed to light.

Photoresist…



Photoresist…

Positive Photoresist: A positive photoresist is a type of photoresist in which the portion of the photoresist that is exposed to light becomes soluble to the photoresist developer. The unexposed portion of the photoresist remains insoluble to the photoresist developer.

Negative Photoresist: A negative photoresist is a type of photoresist in which the portion of the photoresist that is exposed to light becomes insoluble to the photoresist developer. The unexposed portion of the photoresist is dissolved by the photoresist developer.

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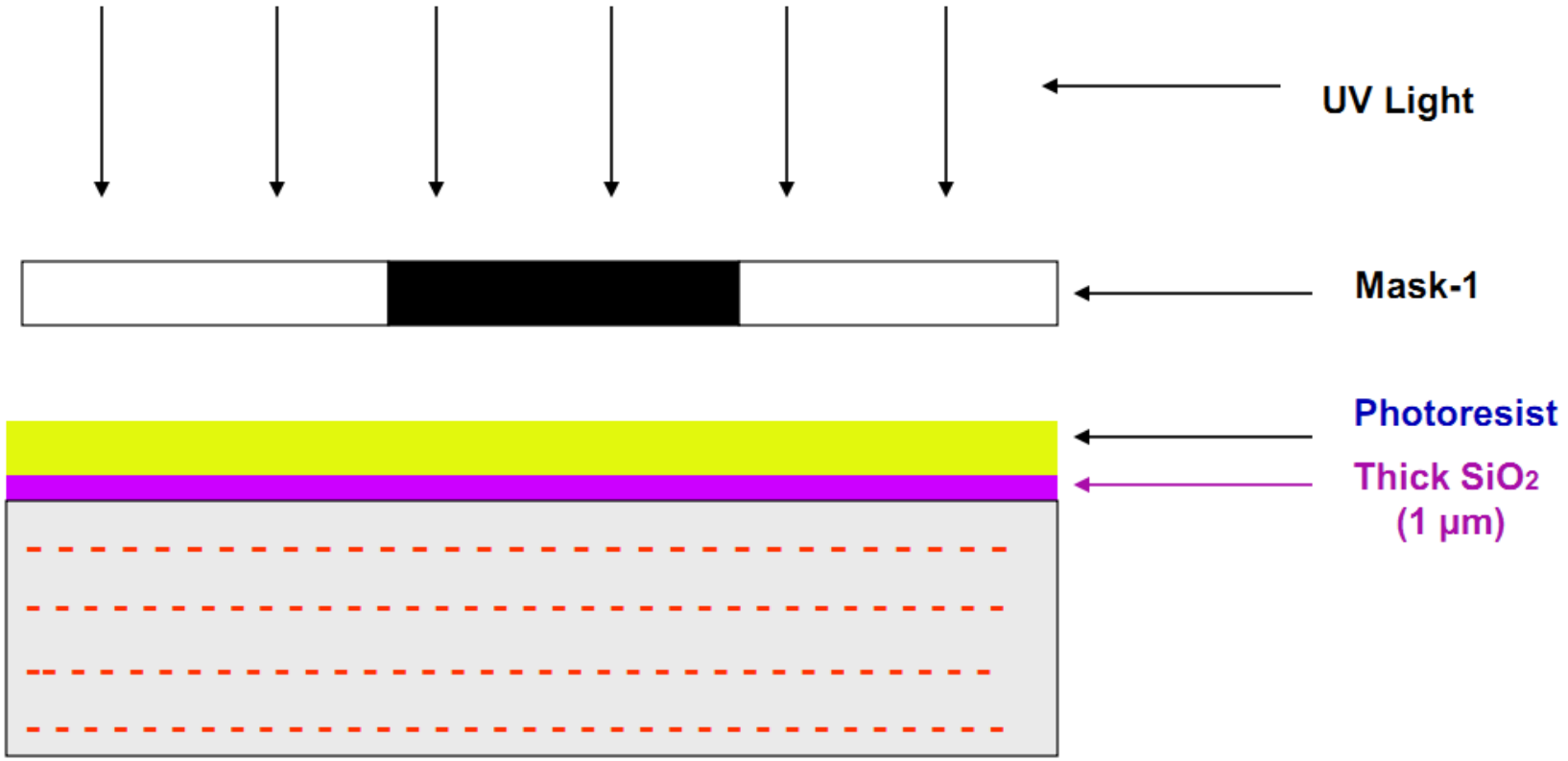

Mask-1 is used to expose the SiO_2 where S, D and G is to be formed.

Fig. (5) Photoresist layer is exposed to UV Light through a mask

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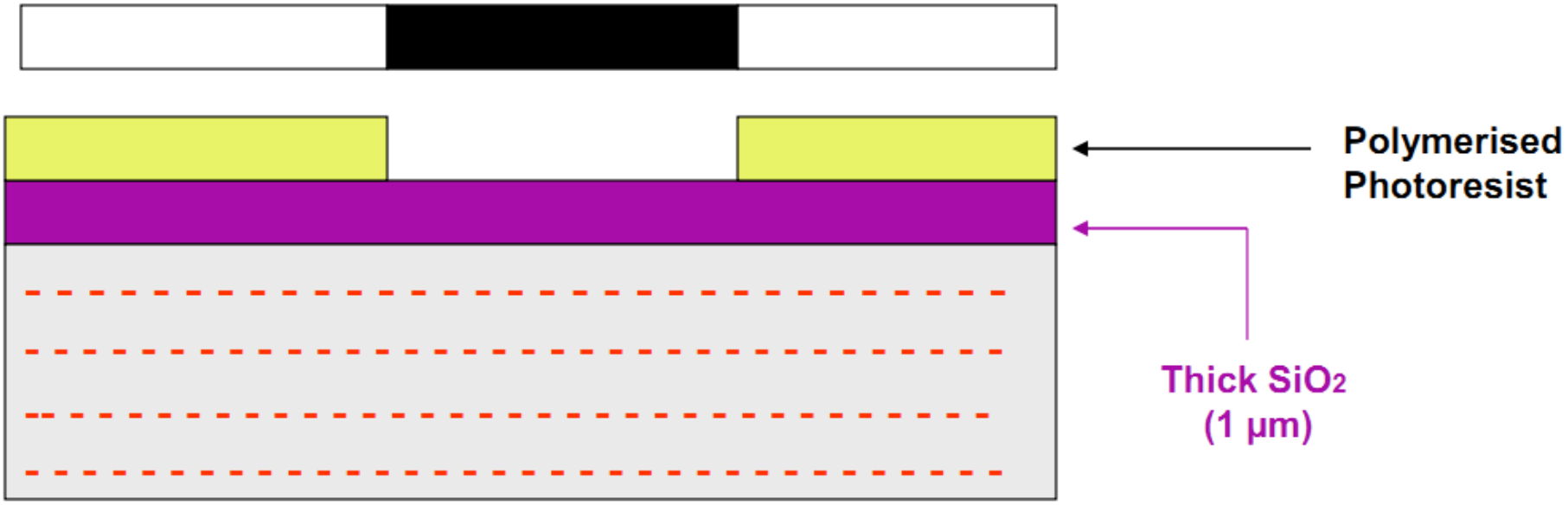

Fig. (6) Developer removes unpolymerised photoresist. It will cause no effect on Si surface

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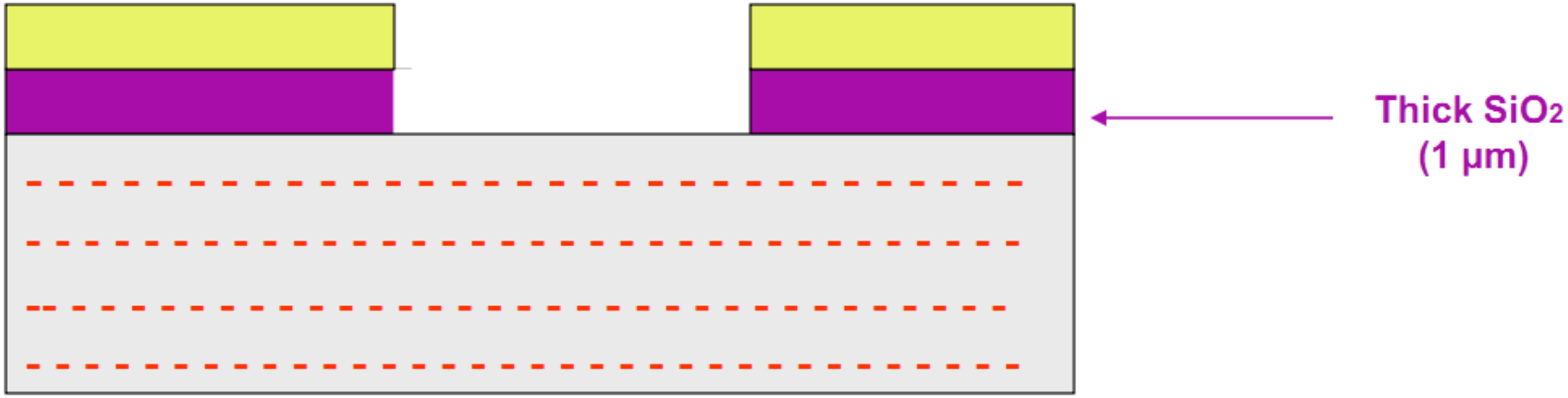

Fig. (7) Etching [HF acid is used] will remove SiO2 layer which is in direct contact with etching solution

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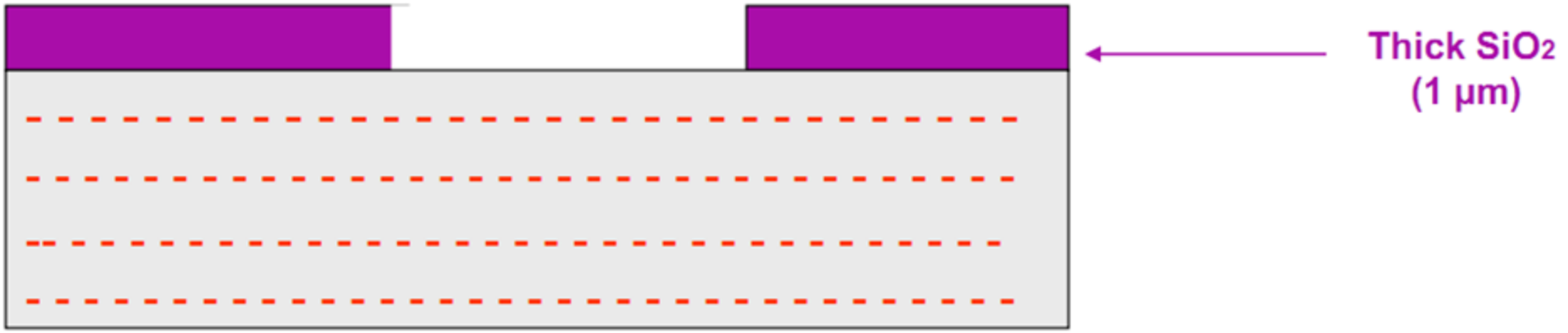

Fig. (7) polymerised photoresist is also etched away [using H2SO4]

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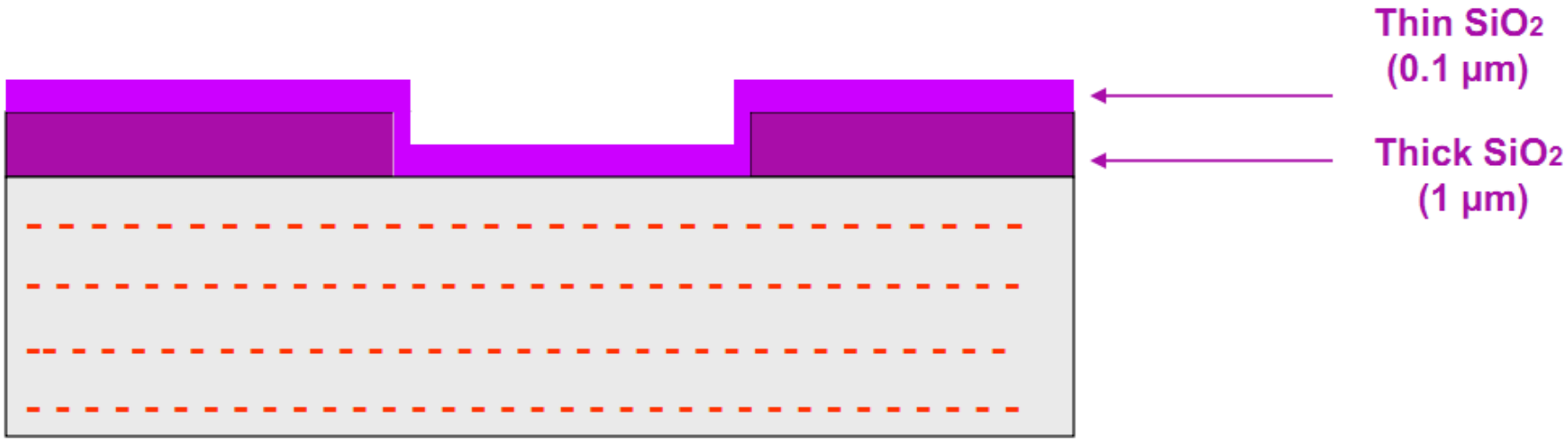

Fig. (8) A thin layer of SiO_2 grown over the entire chip surface

NMOS Fabrication…

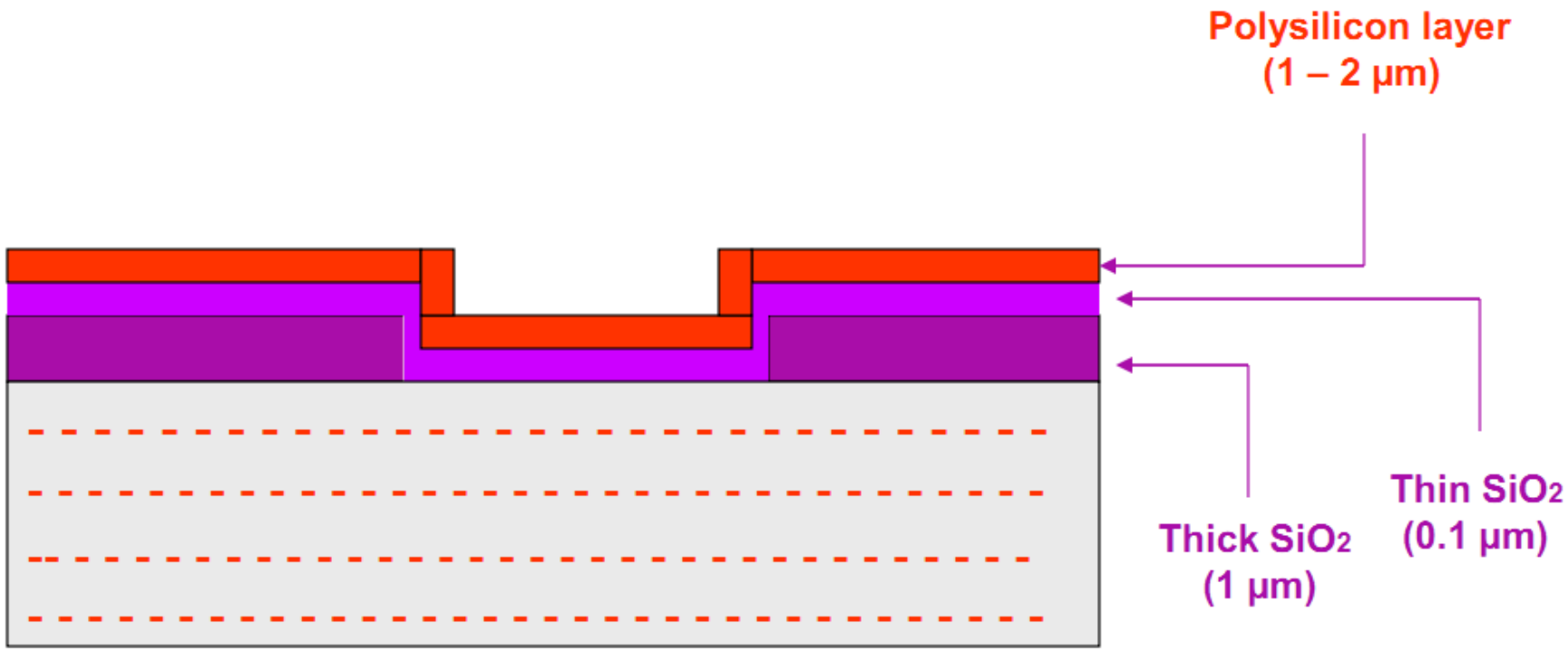

Fig. (9) A thin layer of polysilicon is grown over the entire chip surface to form GATE

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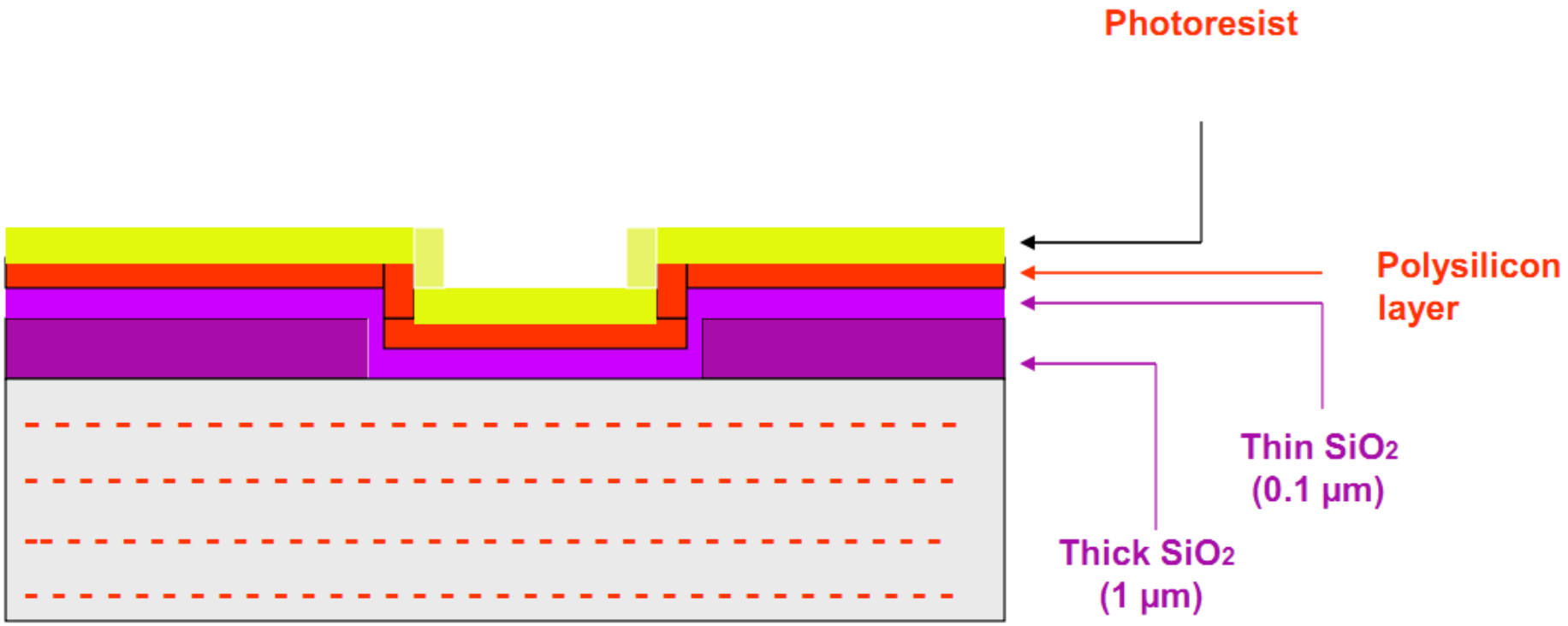

Fig. (10) A layer of photoresist is grown over polysilicon layer

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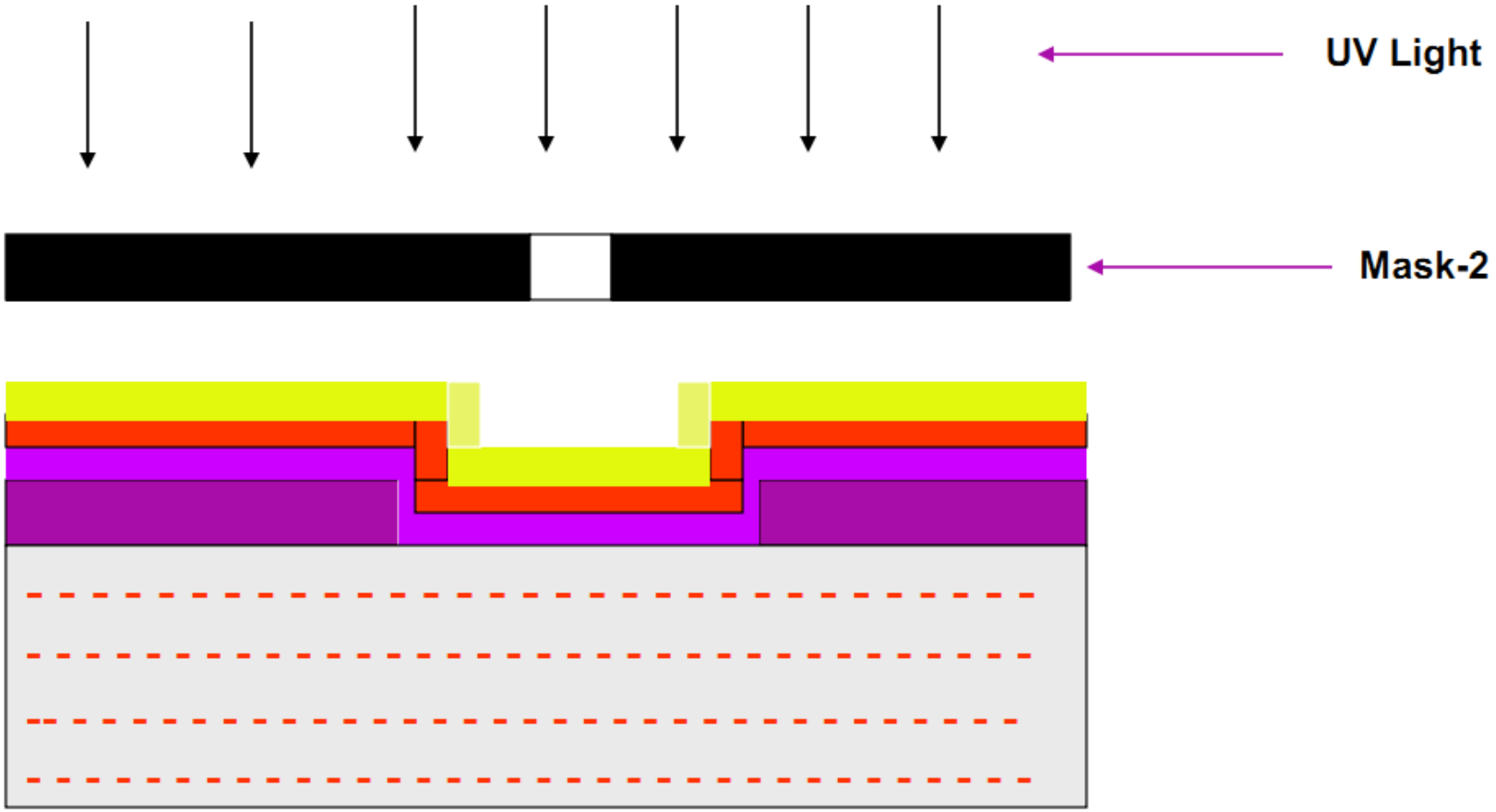

Mask-2 is used to deposit Polysilicon to form gate.

Fig. (11) Photoresist is exposed to UV Light

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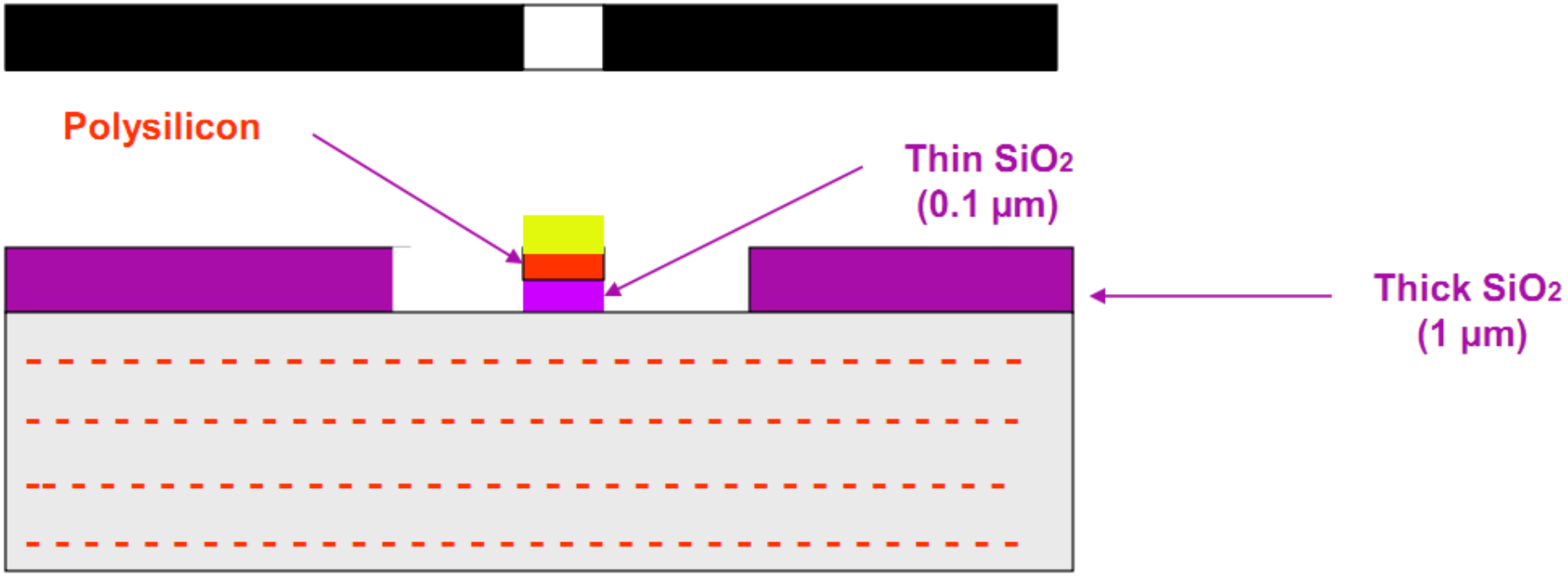

Fig. (12) Etching will remove that portion of Thin SiO2 which is not exposed to UV light

NMOS Fabrication…

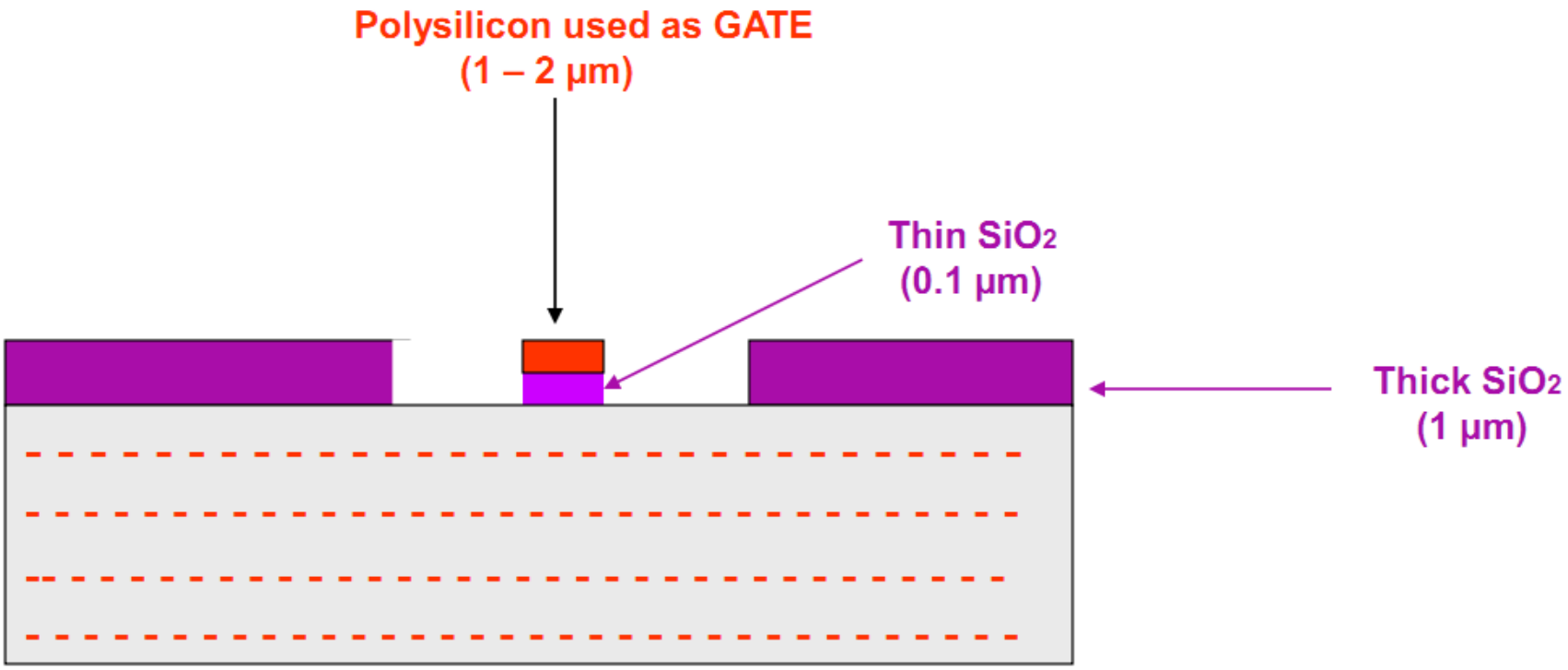

Fig. (13) Polymerised photoresist is also stripped away

NMOS Fabrication…

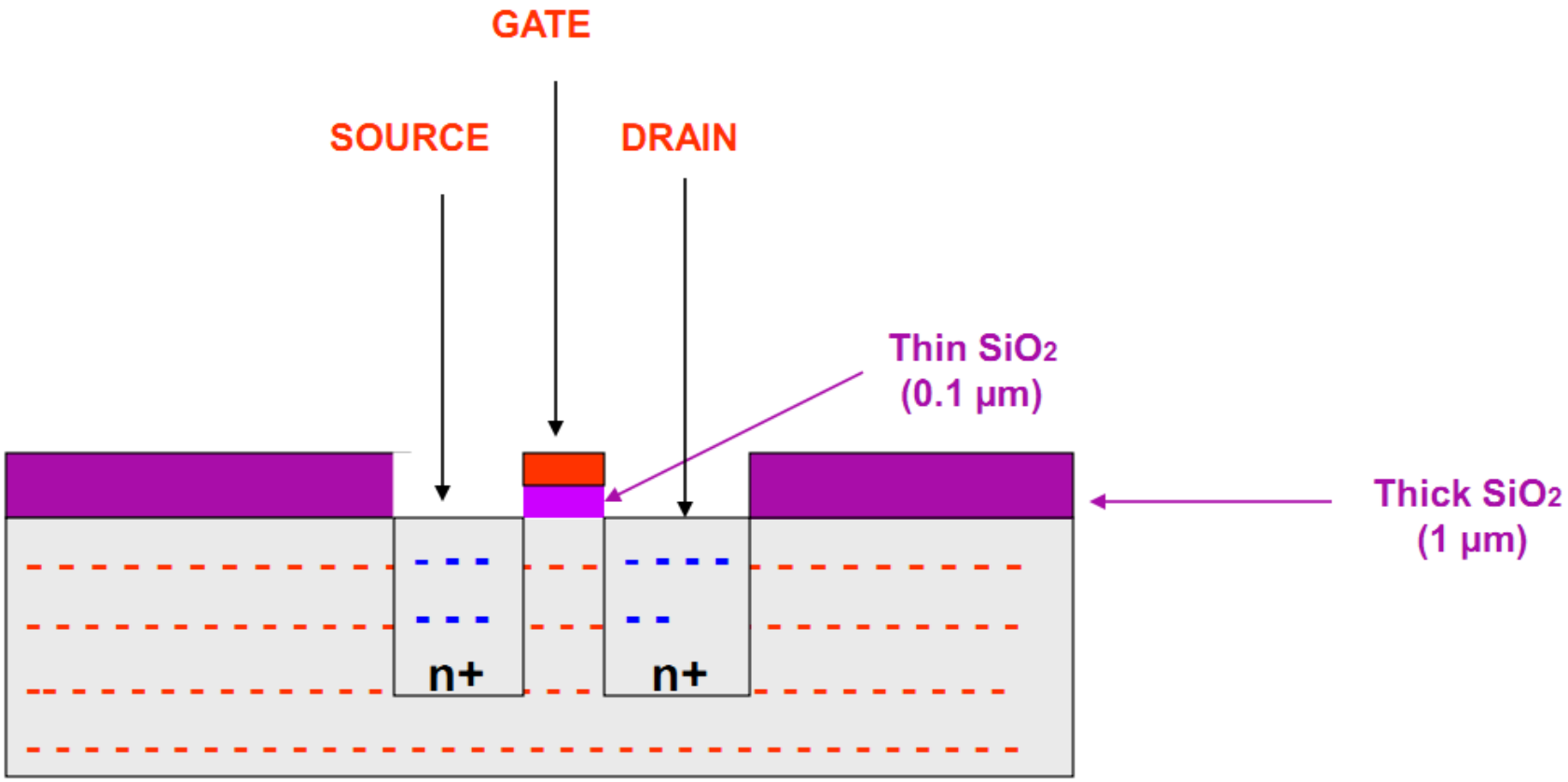

Fig. (14) n⁺ Doping to form SOURCE and DRAIN

NMOS Fabrication…

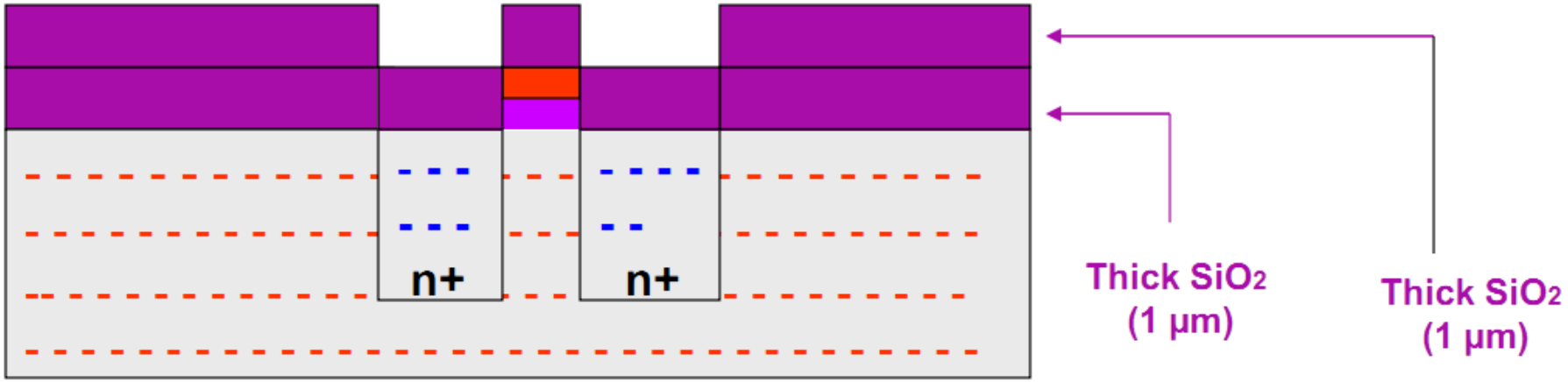

Fig. (15) A thick layer of SiO2 (1 μm) is again grown.

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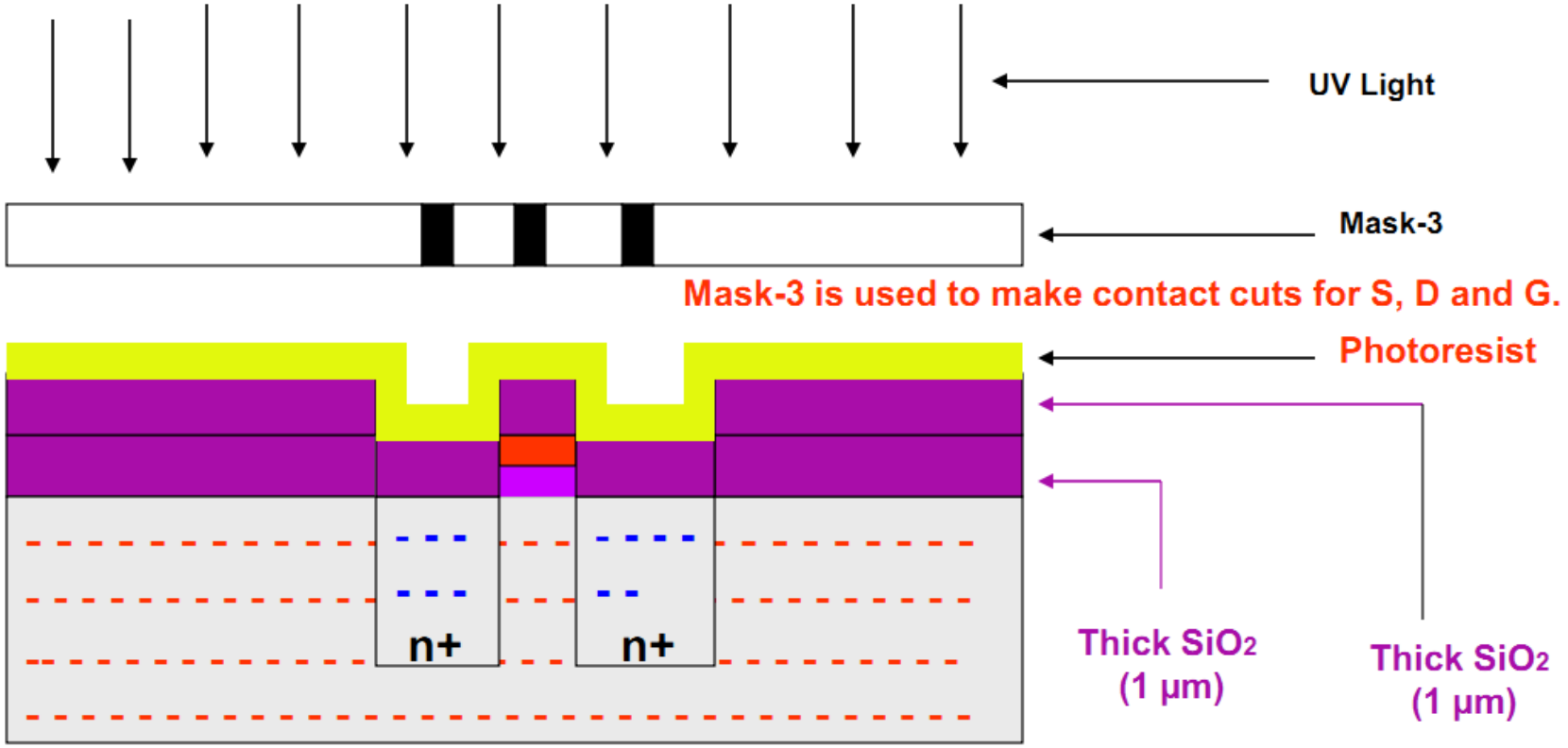

Fig. (16) Photoresist is grown over thick SiO_2. Selected areas of the poly GATE and SOURCE and DRAIN are exposed where contact cuts are to be made

NMOS Fabrication…

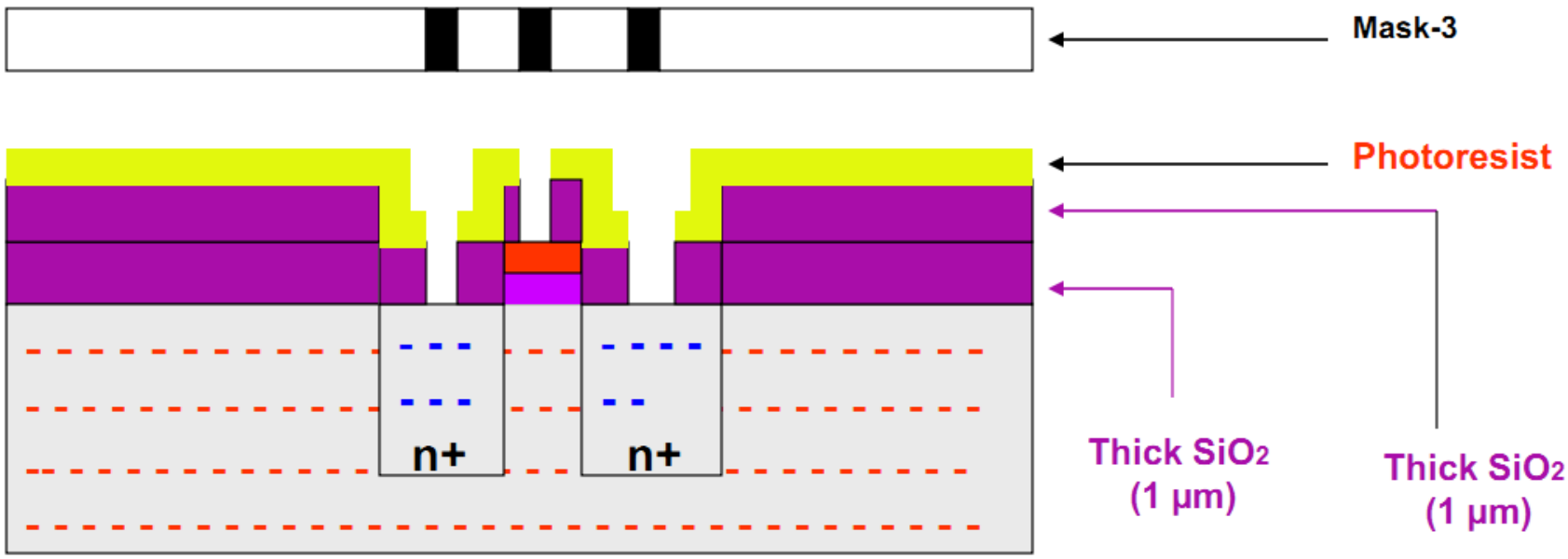

Fig. (17) The region of photoresist which is not exposed by UV light will become soft. This unpolymerised photoresist and SiO_2 below it are etched away.

NMOS Fabrication…

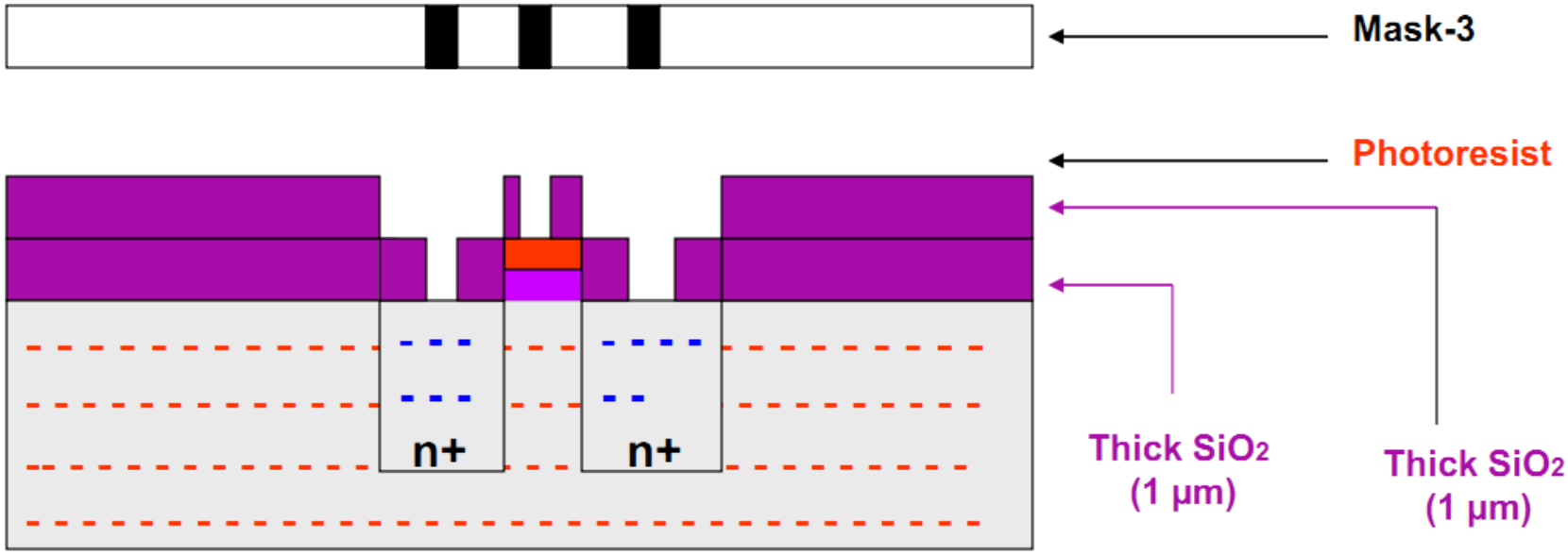

Fig. (18) The contact cuts are formed for S, D and G (hardened photoresist is stripped away).

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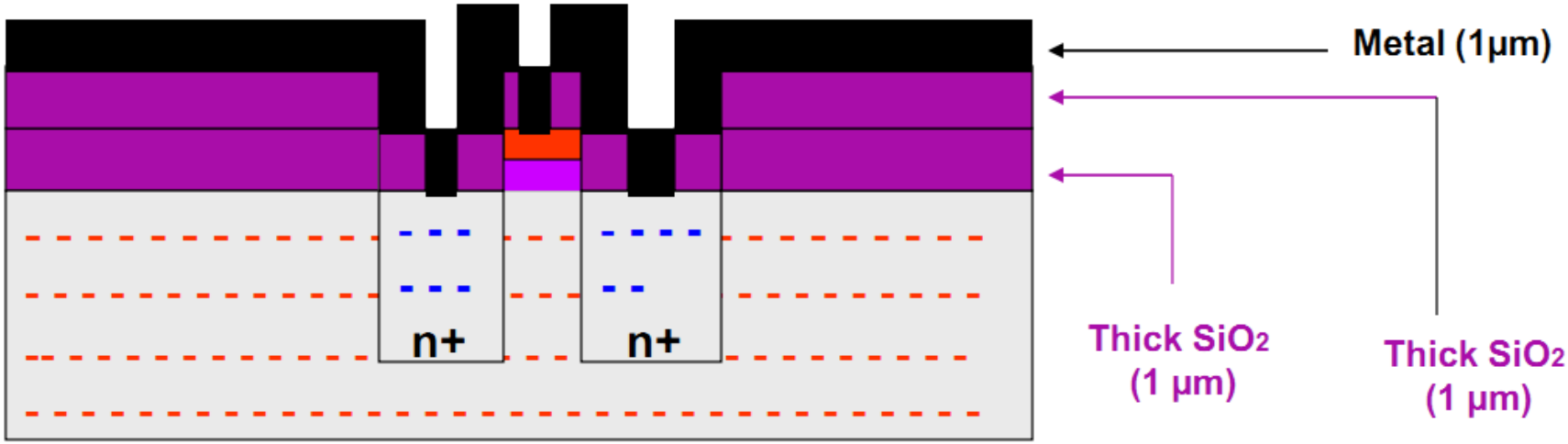

Fig. (19) Metal (aluminium) is deposited over the surface of whole chip (1 μm thickness).

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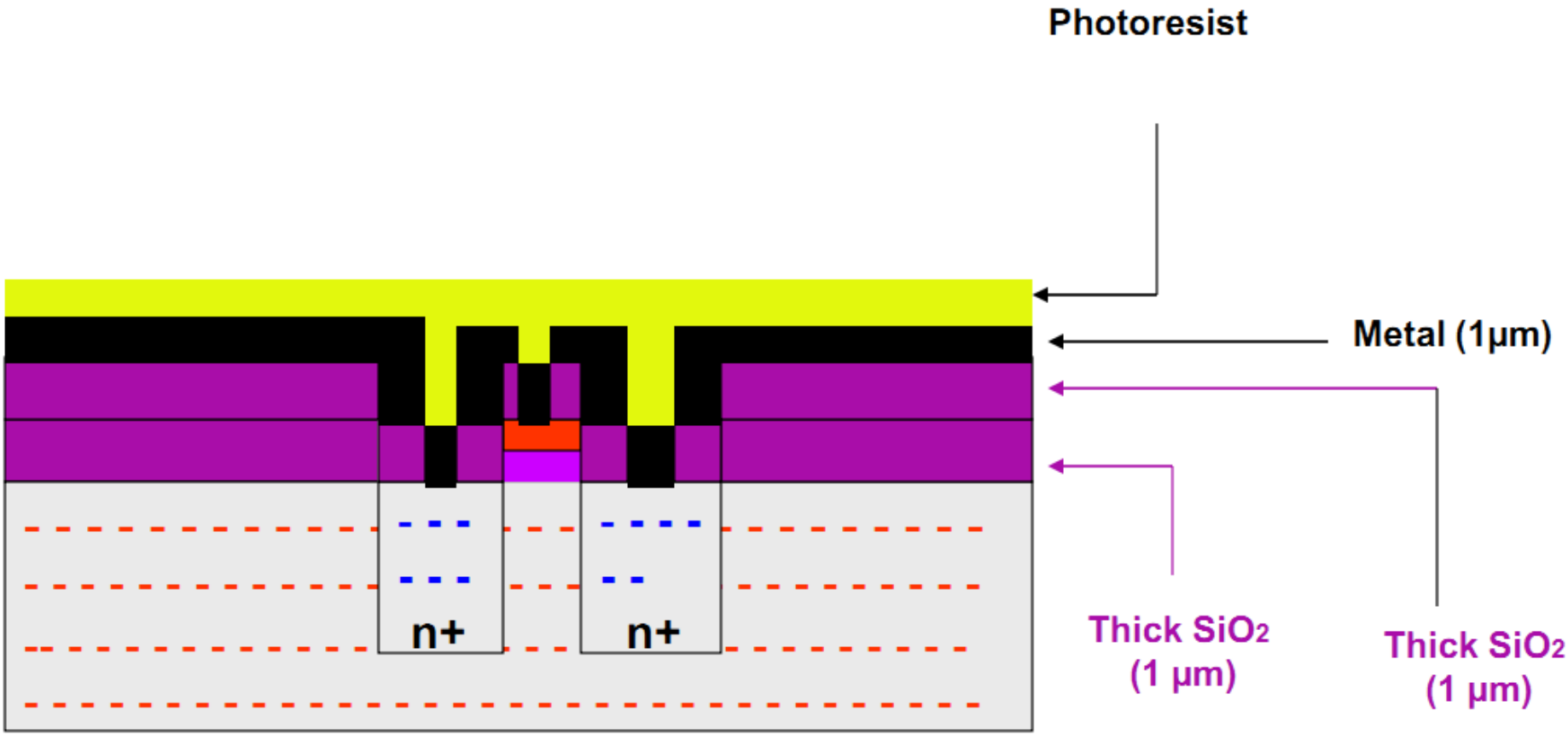

Fig. (20) Photoresist is deposited over the metal.

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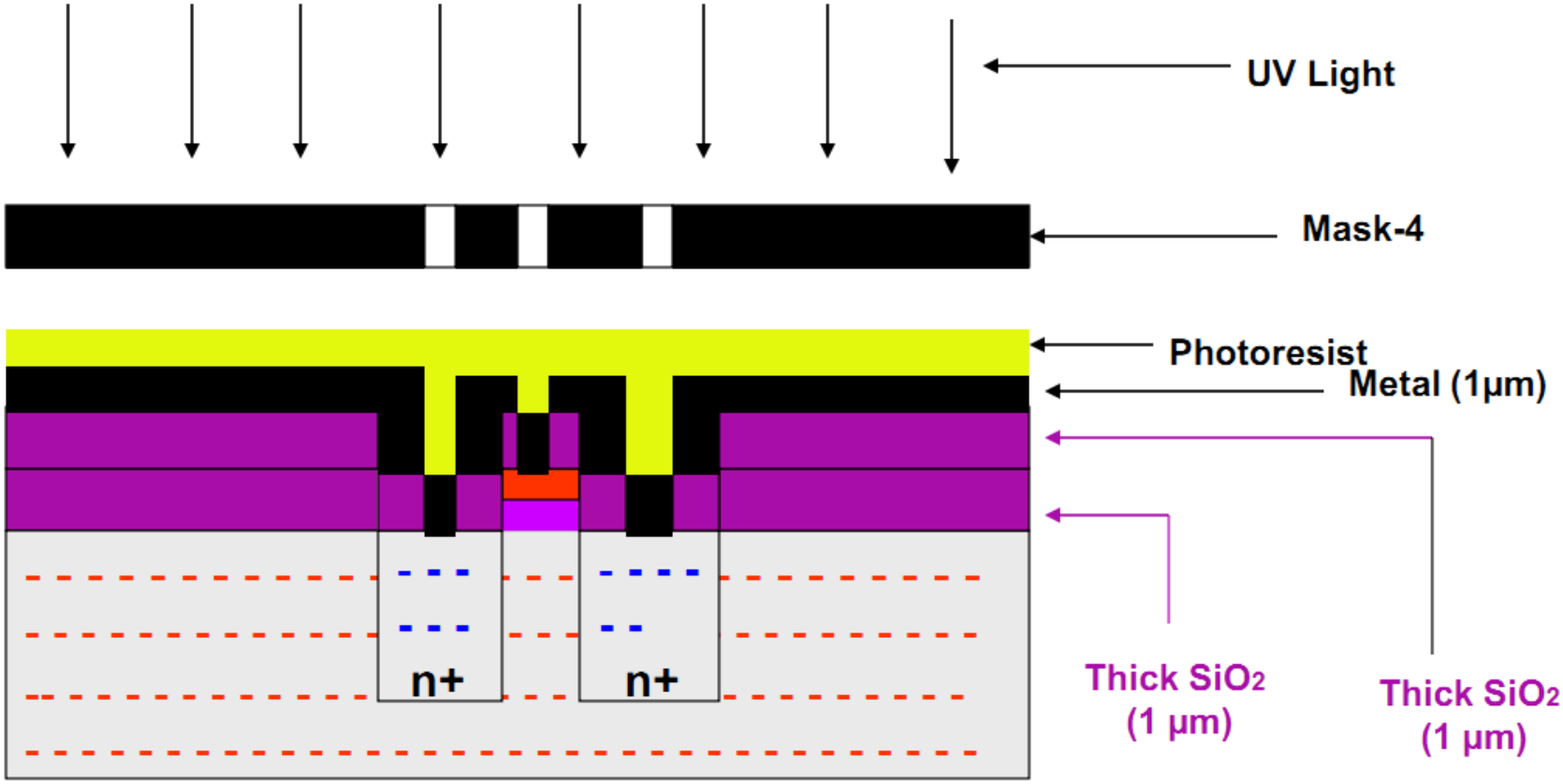

Mask-4 is used to deposit metal in contact cuts of S, D and G.

Fig. (21) UV Light is passed through Mask-4 (with a aim of removing all metal other than metal in contact-cuts).

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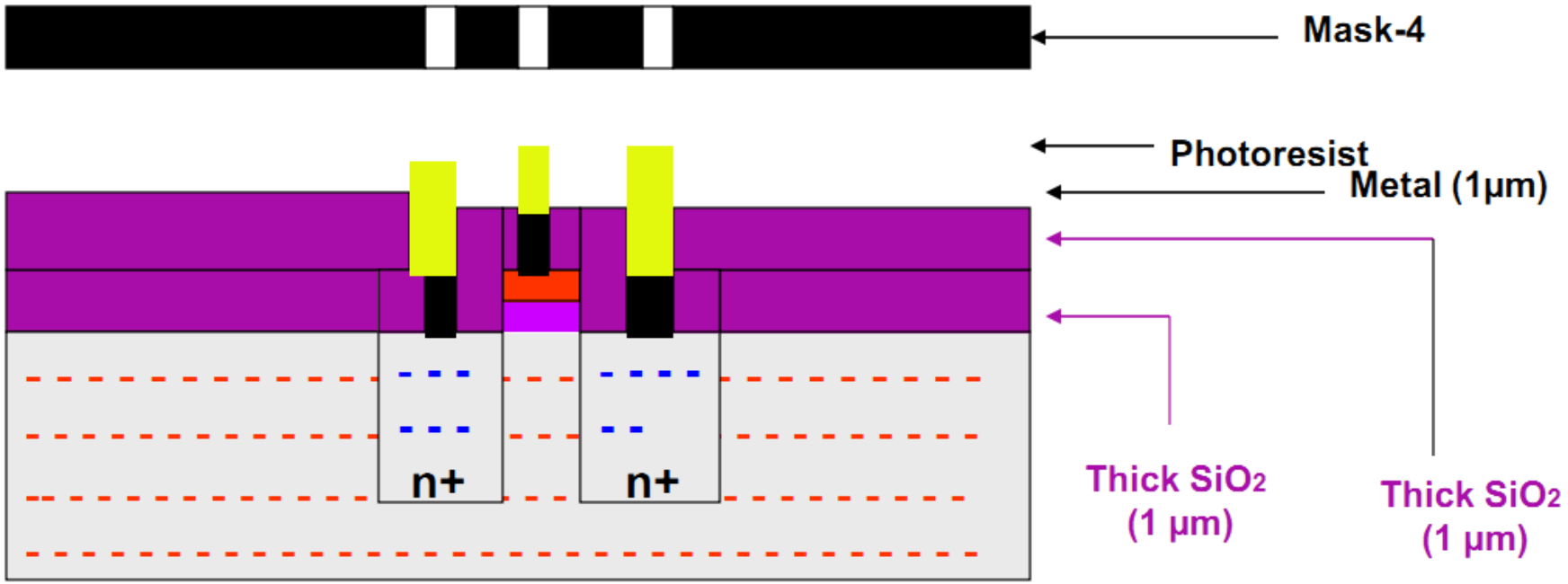

Fig. (22) Photoresist and metal which is not exposed to UV light are etched away.

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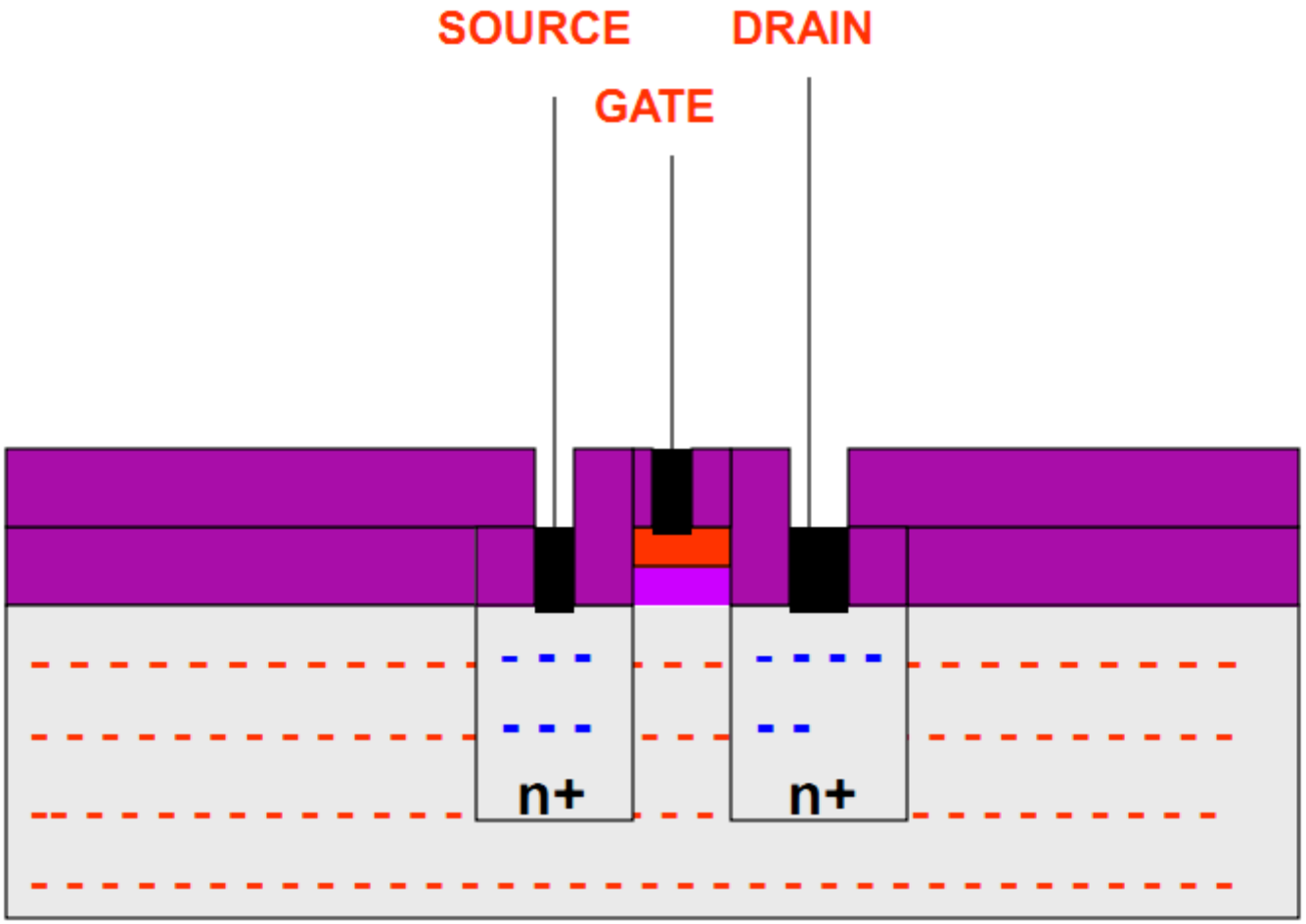

Fig. (23) Final n-MOS Transistor

Acknowledgement

[1] https://www.slideshare.net/SemiDesignSystem/nmos-fabrication-process-55111294

Thanks