Final Main Memory (RAM) Design

Nahin Ul Sadad Lecturer CSE, RUET

Main Memory (SRAM)

RAM chip is shown below:

RA1 [6:0]							RI	21	[1	2:	0]
RA2 [6:0]							RI)2	[1	2:	0]
WA [6:0]			1	28	v 1						
WD [12:0]				zo SR		_					
WE											
		•					•				

Here,

RA1 = Read Address 1

RA1 = Read Address 2

RD1 = Read Data 1

RD2 = Read Data 2

WA = Write Address

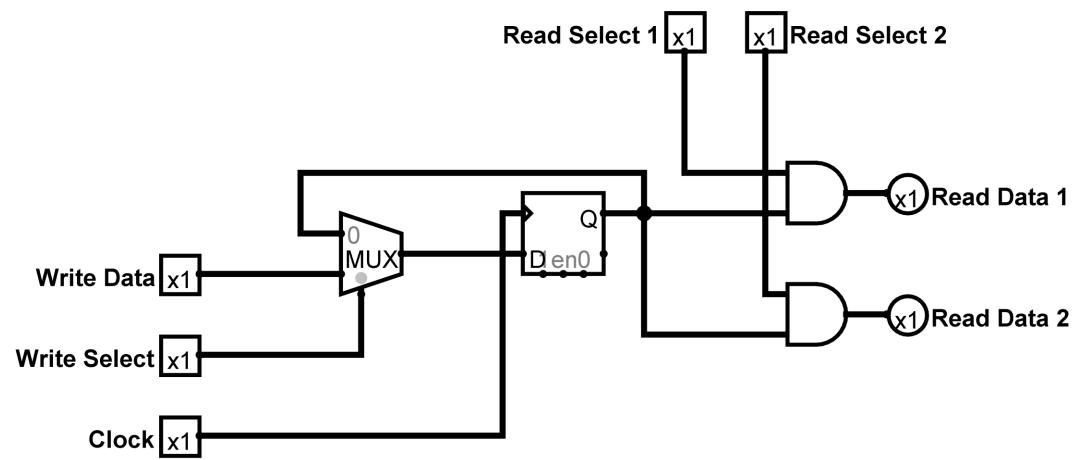
WD = Write Data

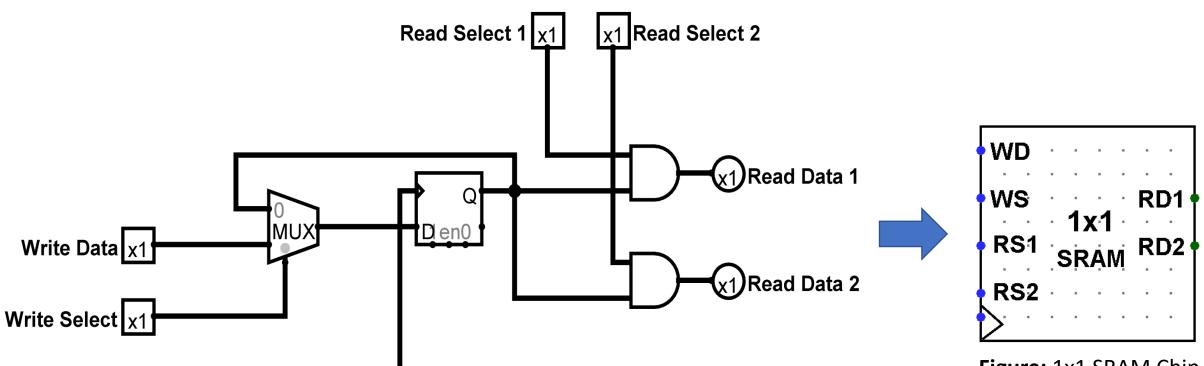
WE = Write Enable

Figure: RAM chip (128x13)

Size of RAM = 128. It can store 128 instructions/data.

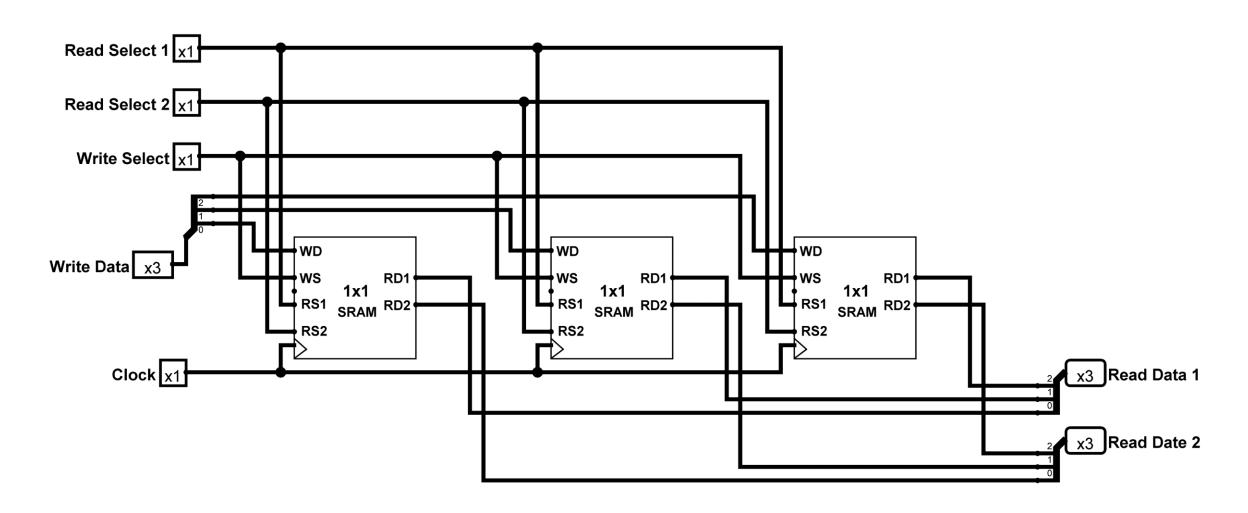
Word Size of RAM = 13. It can store 13bit instruction/data in every address.

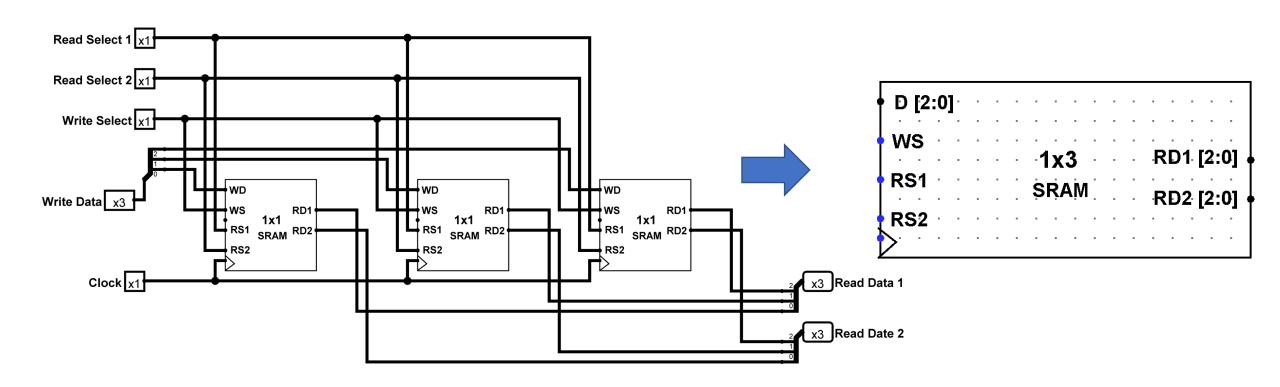


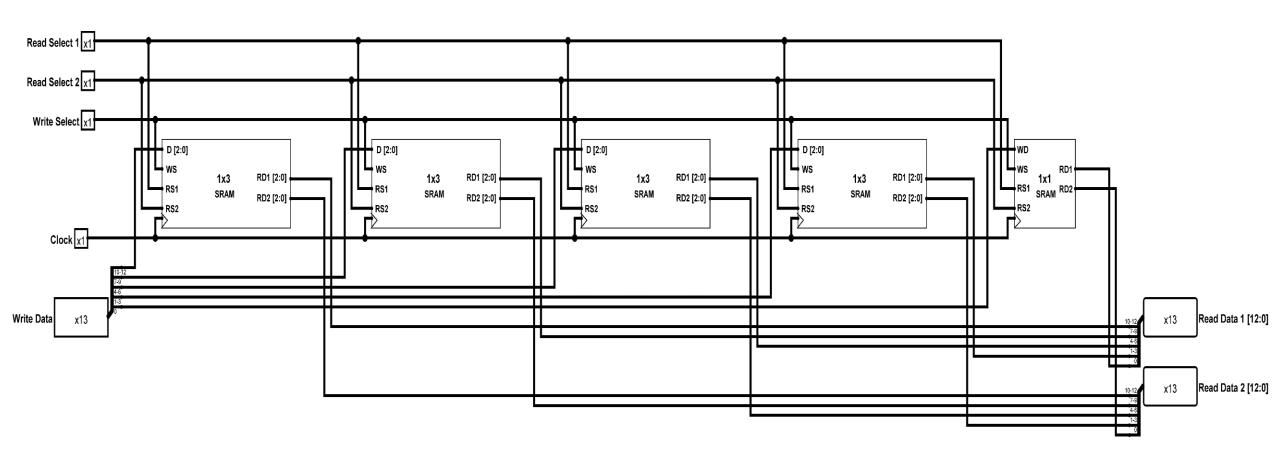


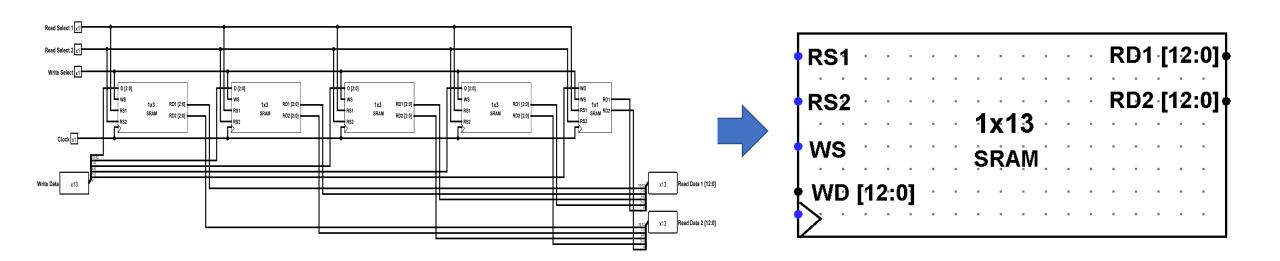
Clock x1

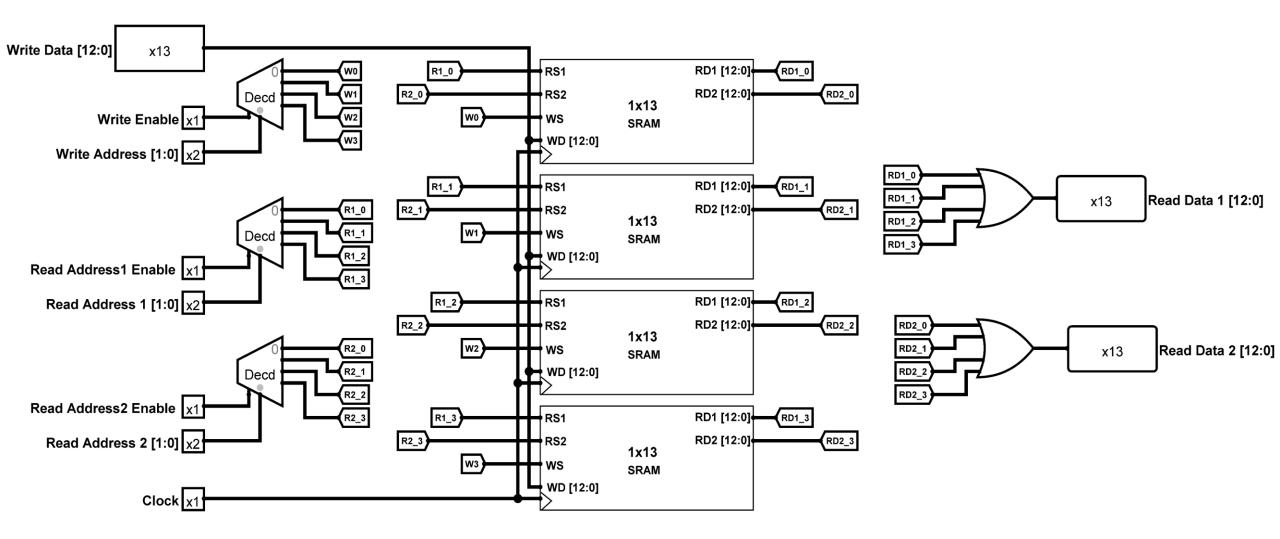
Figure: 1x1 SRAM Chip

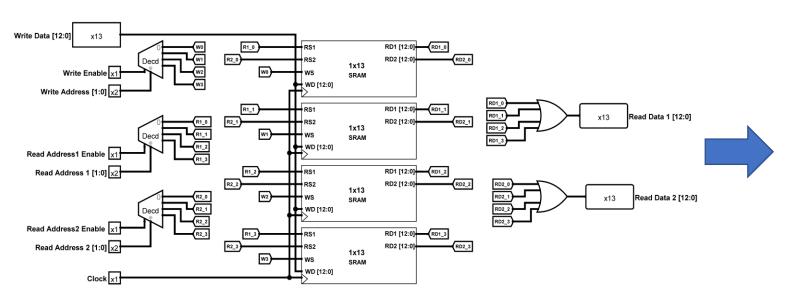




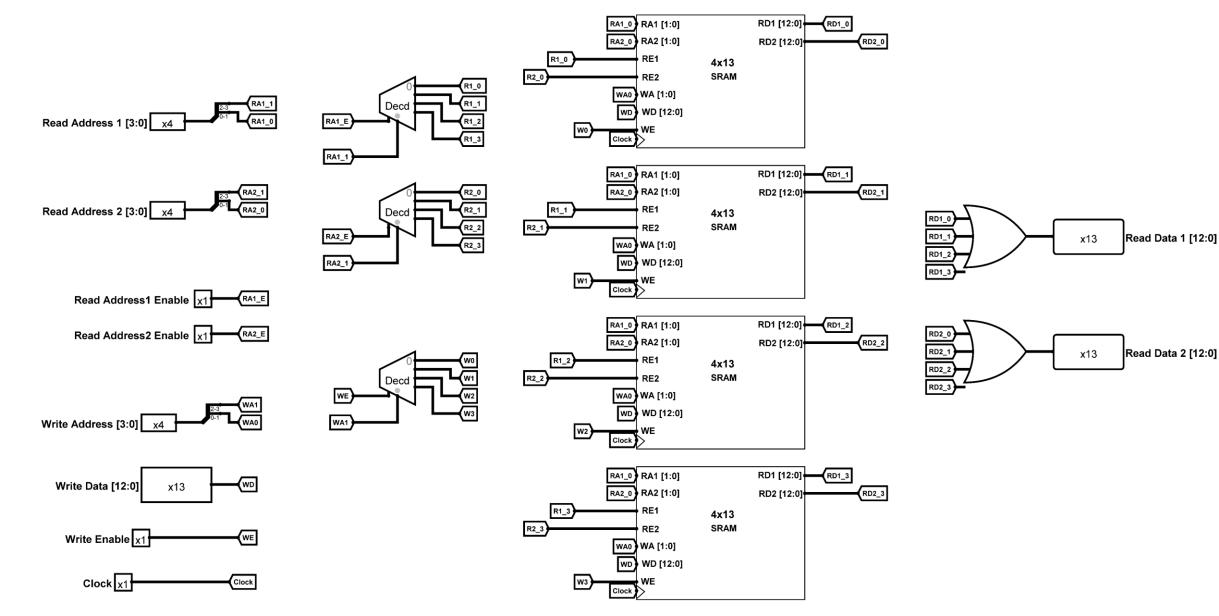


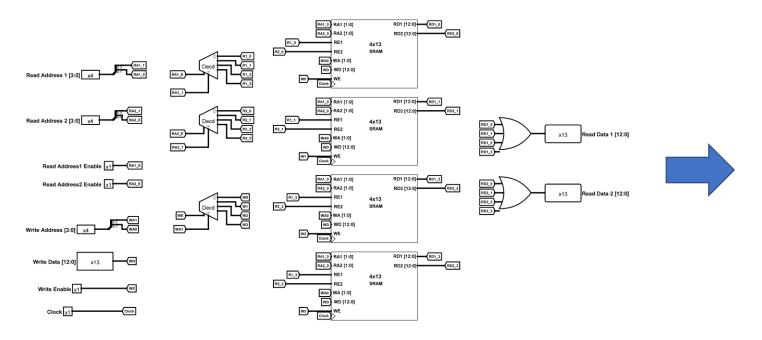




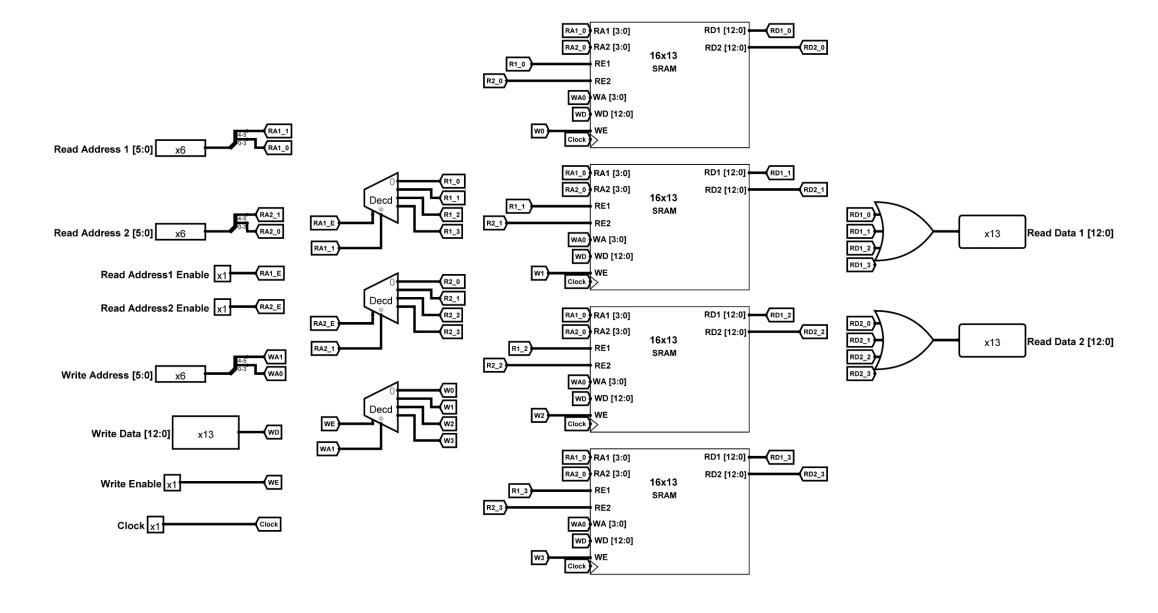


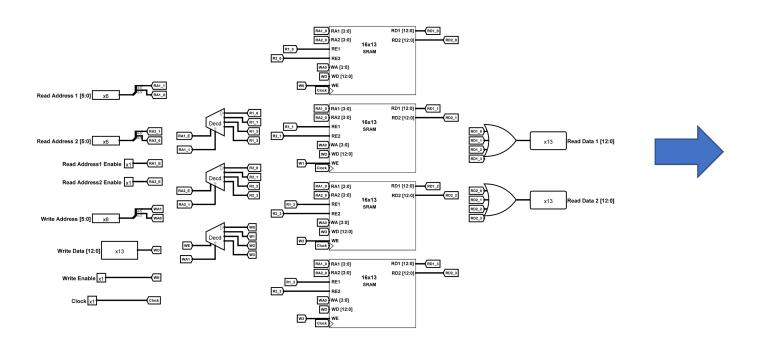
RA1 [1:0]								R	D1	{1	2:	0]
RA2 [1:0]								R	D2	· [1	12	:0]
RE1 · · ·			4)	· (1	3							
RE2			SF	· RA	M							
WA [1:0]												
WD [12:0]												
WE · · ·												
· · · · ·	٠	•	•	•	•	•	•	•	•	•	•	•



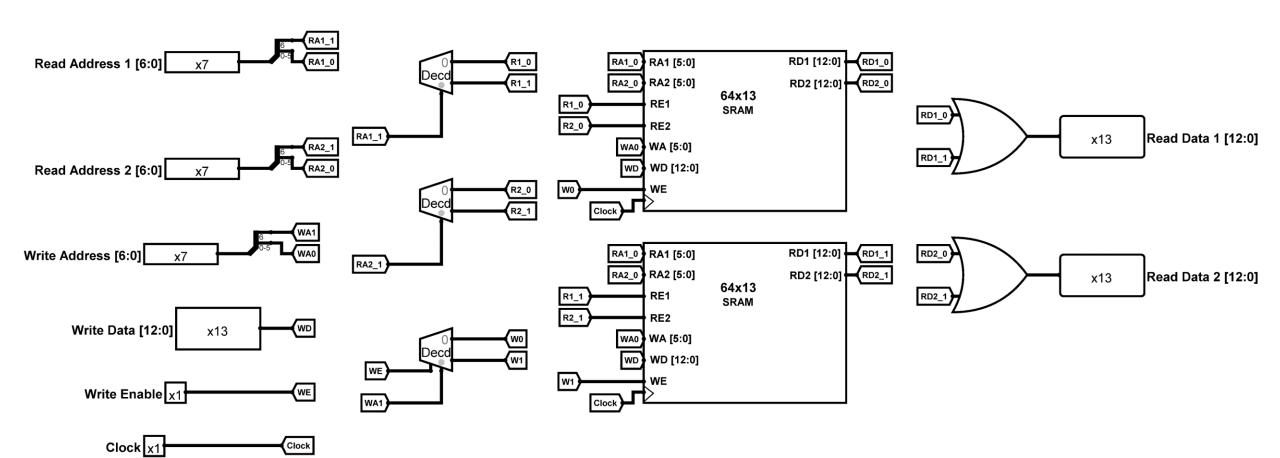


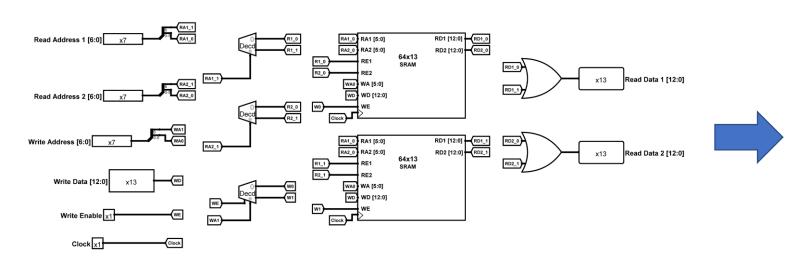
RA1 [3:0]							R	D1	[1	2:	0]
	·1	6:	x 1	3			R	D2	[1	12:	0]
RE1 · · ·	S	R	ķΑ	Ņ					:		
RE2		-									
WA [3:0]											
WD [12:0]							ì				
WE											:
>	•			٠	٠		-				





RA1 [5:0]					· RD1 [12:0]							
RA2 [5:0]		•						R	D2	[1	12:	0]
RE1		64 SF										
RE2								i				
WA [5:0]												
WD [12:0]								ì				
WE		:		:					:			:
>	•	٠	•	•	•	•	•	•	•	•	•	•





RA1 [6:0]								RI	D1	[1	2:	0]
RA2 [6:0]								RI	D2	[1	2:	0]
WA [6:0]			12	ንጸ•	v 1	3						
WD [12:0]				SR		_						
WE												
		•					•					

Thank You ©