

Heaven's Light is Our Guide  
 Rajshahi University of Engineering & Technology  
 B.Sc. Engineering 3<sup>rd</sup> Year 6<sup>th</sup> Semester Examination, 2015  
**Department of Computer Science & Engineering**  
 Course No. CSE 607 Course Title: Peripherals & Interfacing  
 Full Marks: 70 Time: THREE (03) hours

**N.B:**

Answer SIX questions taking THREE from each section.

The questions are of equal value.

Use separate answer script for each section.

PT  
 Pursuit Interrupt control

### SECTION A

- |  | Marks           |
|--|-----------------|
| Q.1(a) Describe the operation performed by the instruction <u>OUT 47h AL</u> .   | 02              |
| (b) How is 8255A PPI configured if its control register contains 9Bl?  | 03 <sup>2</sup> |
| Q.1(c) For higher speed data transfer, why is simple strobe I/O data transfer not used?  | 02              |
| (d) What is the purpose of TEST pin on 8086 microprocessor? Write the differences between 8086 and 8088 microprocessor.  | 04              |
| Q.2(a) Why does 8086 need two memory banks? Explain with example.  | 03              |
| ' (b) Draw a circuit that uses 2732 EPROMs for a 16K x 8 section of memory in an 8086 microprocessor based system using 74LS138 decoder.   | 04 <sup>2</sup> |
| (c) Write down the bit format for sending asynchronous serial data.  | 02              |
| (d) What is the meaning of the statement "The 8251A USART is double-buffered"?   | 02              |
| Q.3(a) A <u>74LS138</u> decoder has its three SELECT inputs, connected to <u>A<sub>11</sub>, A<sub>12</sub>, A<sub>13</sub></u> of the system address bus. It has <u>G<sub>2B</sub></u> connected to <u>A<sub>14</sub></u> , <u>G<sub>2A</sub></u> connected to ground and <u>G<sub>1</sub></u> connected to <u>A<sub>15</sub></u> . Use an address decoder worksheet to determine, what eight 1KB RAMs address blocks the decoder output will select? Also determine, what address ranges will the block-2/RAM1 select? | 06              |
| (b) Describe the purposes of address decoding in micro-computer system.  | 02 <sup>2</sup> |
| (c) Describe the response that an <u>8259A</u> will make if it receives an interrupt signal on its IR1 and IR2 inputs at the same time.  | 03              |
| Q.4(a) Is it possible to select PORT C as an input port and output port at the same time using the command byte of the command register in the 82C55 PPI? Briefly explain.   | 04              |
| ' (b) How many 8259A are required to have 25 interrupt inputs? Why?  | 02              |
| (c) Find out the bit sequence of command byte A for the following arrangement: <u>port A input</u> , <u>port B output</u> and <u>port C input</u> .  | 03              |
| (d) Distinguish between transducer and actuator.   | 02 <sup>2</sup> |

### SECTION B

- |   |                 |
|---|-----------------|
| Q.5(a) What is the advantage of a smaller resolution?   | 02              |
| ' (b) Draw the basic R/2R ladder DAC and prove that $V_{OUT} = (-V_{REF}/16) \times B$ , where B is the value of binary input.  | 04              |
| (c) Why does conversion time increase with the value of analog input voltage?   | 02              |
| (d) Write down the working principle of counter type ADC.   | 03 <sup>2</sup> |
| Q.6(a) A certain memory has a capacity of 32K x 16. Calculate (i) How many bits are in each word? (ii) How many words are being stored? and (iii) How many memory cells does this memory contain? | 03              |
| (b) Design Mask-Programmed ROM to store the function $y = x^3 + 5$ , where input address supplies the value for x and the value of the output data is y.  | 04 <sup>2</sup> |
| (c) Draw the timing diagram of write cycle for static RAM.  | 02              |
| (d) What do you mean by quantization error?   | 02              |
| Q.7(a) Why does DRAM need refresh operation?  | 05              |
| (b) A static RAM IC has a capacity of 16 x 4, one active low chip select input and common data input and output line. Now show how to combine several RAM ICs to form a 16 x 16 module.           | 04              |
| (c) Write down the differences between PROM, PAL and PLA. What is programming or burning in a ROM?  | 07              |
| Q.8(a) Draw the simplified architecture of a 32 x 4 RAM. Also draw a structure of a MROM which can be used to store the function, $y = 2x^2$ .  | 04 <sup>2</sup> |
| (b) Explain and draw the block diagram of 8251A USART.  | 02              |

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### SECTION-A

**Q1** (a) Why is handshaking necessary for interfacing? Write an example with necessary assembly code.  $\frac{2}{3}$

**(b)** Write the differences between fixed and variable port addressing.  $\rightarrow 726 \rightarrow$  Topic

**(c)** How can you interface microprocessor with real world variable? Briefly explain.  $\frac{3}{3}$

**(d)** Using 74LS138, 3 to 8 line decoder, combine eight 2764 EPROM chip for a 64Kx8 section of memory in an 8088 microprocessor system.  $\frac{3}{3}$

**Q2** (a) Draw the interface diagram and necessary assembly code of a 8-digit LED display interfaced to the 8086 microprocessor through an 82C55 PPI.  $\frac{5}{5}$

(b) Draw a PLA architecture for four inputs i.e., A, B, C and D. Now draw a PLA programmed function for the following functions:  $\frac{4}{4}$

$$O_3 = AB + \bar{C} \bar{D} + A\bar{C}$$

$$O_2 = \bar{A}\bar{B}\bar{C} + ABC + \bar{A}\bar{B}C$$

$$O_1 = \bar{A}BCD + A\bar{B}CD + ABC\bar{D}$$

$$O_0 = A + B\bar{D} + C\bar{D}$$

Where  $O_0, O_1, O_2$  and  $O_3$  indicates four outputs.  $\frac{2}{2}$

**(c)** Distinguish between CRT and LCD display system.  $\frac{2}{2}$

**Q3** (a) Describe the response that an 8259A will make if it receives an interrupt signal on its IR<sub>4</sub> and IR<sub>5</sub> inputs at the same time.  $\frac{2}{2}$

(b) What will happen when you want to get cascaded connection of 8259A? Explain with necessary figure.  $\frac{4}{4}$

(c) Draw the internal block diagram of 8237A DMA controller.  $\rightarrow$   $\frac{4}{4}$

**Q4** (a) Why the 8086 INTR input is automatically disabled when the 8086 is RESET?  $\rightarrow$   $\frac{2}{2}$

(b) Write the working principle of interrupt vector table.  $\rightarrow$   $\frac{4}{4}$

(c) What are the purposes of the following signal in strobed input operation of the 82C55  $\frac{5}{5}$

- (i) STB
- (ii) IBF
- (iii) INTR
- (iv) INTE
- (v) PC<sub>6</sub>

### SECTION-B

**Q5** (a) Explain which way the data flow for an IN and OUT instruction.  $\rightarrow$   $\frac{2}{2}$

(b) Describe the working principle of mode 1 strobed input and output operations with appropriate timing diagram.  $\rightarrow$   $\frac{5}{5}$

(c) Describe bit format used for sending asynchronous serial data.  $\rightarrow$   $\frac{4}{4}$

**Q6** (a) Draw the block diagram of a programmable interval timer 8254. Write down a brief note about control word of 8254.  $\rightarrow$   $\frac{5}{5}$

(b) Describe the mode 0 operation of 8254 with a proper timing diagram.  $\rightarrow$   $\frac{4}{4}$

(c) What are the differences between synchronous and asynchronous data transfer operation?  $\rightarrow$   $\frac{2}{2}$

**Q7** (a) What are the purposes of using 8255 PPI?  $\rightarrow$   $\frac{2}{2}$

(b) What will be the conditions of command byte A and command byte B if we want to select the following in 8255A?  $\rightarrow$   $\frac{4}{4}$

Port A: Input, Port B: Output, Port C: Output, Mode: 0.  $\rightarrow$

(c) Draw the transition diagram of 8255A for mode 2 bidirectional operation.  $\rightarrow$   $\frac{4}{4}$

(d) What are the differences between buffer and latch?  $\rightarrow$   $\frac{2}{2}$

**Q8** (a) Explain how parity error can be detected using parity generator.  $\rightarrow$   $\frac{2}{2}$

(b) Explain why we use co-processor. What are the purposes of NEU of 80X87.  $\rightarrow$   $\frac{3}{3}$

(c) Draw the internal structure of the 80X87 arithmetic co-processor and explain the co-processor status register.  $\rightarrow$   $\frac{4}{4}$

(d) Write a program to calculate the area of a circle using 80X87 co-processor.  $\rightarrow$   $\frac{2}{2}$

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## SECTION A

Q1(a)

In strobed output operation of the 82C55, what is the purpose of  $\overline{STB}$  signal? B-916

(b) What are the purposes of using command byte of 82C55? Give with an example.

(c) Which group of pins is used during bi-directional operation of 82C55?

(d) How can you interface a 4x4 keyboard matrix connected to an 8031 microprocessor through the 82C55 PIA? Explain with diagram using necessary assembly code.

Marks  
01%

03

02

05

Q2(a)

Explain which way the data flow for an IN and OUT instruction.

02%

(b) Contrast a memory-mapped I/O with isolated-mapped I/O system.

03

(c) Explain the term hand shaking as it applies to computer I/O system with necessary assembly code.

04

(d) Why is the 8086 memory set up as 2-byte wide banks?

02

*Machine level  
bit by bit read/write even though*

Q3(a)

Describe the working principle of interrupt vector table of 8086 microprocessor.

02%

(b) Draw the internal block diagram of 8259A PIC.

04

(c) Describe the response that an 8259A will make if it receives an interrupt signal on its IR3 and IR5 inputs at the same time. Assume fixed priority for the IR inputs. What response will the 8259A make if it is servicing an IR5 interrupt and an IR3 interrupt signal occurs?

04

Q4(a)

Why the INTR input is automatically disabled as part of the response to an INTR interrupt?

02

(b) Describe the use of the CAS0, CAS1 and CAS2 lines in a system with a cascaded 8259A.

03

(c) Write the working principle of raster scan display controller.

02

(d) Draw the block diagram and explain the operation of 8251A USART.

04

## SECTION B

Q5(a) *Slide 2, Topic 7.50*

What is meant by resolution of a DAC? An 8-bits DAC has an output of 3.92 mA for an input of 01100010. What are the DAC's resolution and full scale output?

03

Design a 4-bit Flash ADC and show the analog input, comparator outputs and digital output using a truth table. Describe the conversion time of Flash ADC briefly.

06

Let a computer is controlling the speed of a motor. The 0 to 2 mA analog current from the DAC is amplified to produce motor speed from 0 to 2000 rpm. Let the step size of DAC is not greater than 2 rpm. Now determine how many bits should be used.

02

Q6(a)

Draw a block diagram of a  $64 \times 8$  RAM. Describe the conditions at each input and output pins when the contents of the address location 11011 are to be read, let 11110000 data are stored on that location. What is its capacity in bytes?

03

(b) Describe the signal activity for a read operation on a dynamic RAM. What is the benefit of address multiplexing?

05

(c) Consider a RAM IC with capacity of  $1K \times 2$  fine active low chip, select input and separate data input and output. Now design a  $1K \times 8$  module by using several  $1K \times 2$  RAM ICs.

03

$$1K \times 1 \times 8 = 1K \times 8$$

$$1K \times 8 = 1K \times 8$$

Q7(a)

Design a  $16K \times 8$  section of memory in an 8088 microprocessor based system by using 74LS138 decoder and 2716 EPROMs. Why it is needed to decode memory?

06

(b) What are the purposes of the following signals in strobed input operation of the 82C55: (i)  $\overline{STB}$  (ii)  $\overline{IEF}$  (iii)  $\overline{INTR}$  (iv)  $\overline{INTE}$  (v)  $\overline{PC}$  &  $\overline{FC}$ .

05

Q8(a)

Draw a PLD architecture for four input i.e. A, B, C and D. Now draw a PLD programmed for the following functions.  $O_3 = AB + \overline{A}\overline{B} + CD + \overline{C}\overline{D}$ ,  $O_2 = ABC + ABD + A\overline{C}$ ,

07

$$O_1 = ACD + ABC\overline{D}$$

04

Draw a PLA programmed for the following functions,  $O_3 = AB + \overline{A}\overline{B}$ ,  $O_2 = ACD + AB$ ,

04

$$O_1 = \overline{ABCD} + ABC\overline{D}$$

04

$$O_0 = ABCD + AD \text{ where } A, B, C \text{ and } D \text{ are four inputs.}$$

04

G

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### SECTION-A

- Q1.** (a) What is meant by fixed addressing and variable addressing? Distinguish between isolated I/O and memory mapped I/O.  $37 \times 1379 - B$  03
- (b) Write a BSR control word subroutine to set bits PC<sub>7</sub> and PC<sub>3</sub> and reset after 10 ms. 02
- (c) Draw the timing diagram of storbed input operation.  $445 - B$  04
- (d) If the command byte of the command register in the 82C55 PPI is 10110110 then mention the status of the mode of selection of ports as well as port directions.  $328 - B$   $\frac{2}{3}$
- Q2.** (a) What is meant by modular programming? What are the purposes of Linker?  $251 - B$  02
- (b) Draw the internal block diagram of the 8284A clock generator. Describe how clock signal is generated in the 8284A.  $302 - B$  04
- (c) Why is demultiplexing of buses necessary? Draw the timing diagram of simplified 8086/8088 write bus cycle.  $310 \geq 315 - B$  03
- (d) If the F/C pin is placed at logic 1 level, the crystal oscillator is disabled. Where is the timing input signal attached to the 8284A under this condition?  $306 - B$   $\frac{2}{3}$
- Q3.** (a) Describe the command bytes of the command register in the 82C55.  $327 - B$  04
- (b) Draw the interface of a  $4 \times 4$  keyboard matrix connected to an 8088 microprocessor through the 82C55 PIA.  $410 - B$   $\frac{2}{3}$
- (c) Draw the internal structure of the  $80 \times 87$  arithmetic co-processor and describe the co-processor control register.  $538 + 540 - B$  05
- (d) Why we use 8259A with 8086 microprocessor?  $2-30-H$   $\frac{1}{3}$
- (e) Describe the purpose of the In-service Register, Interrupt Request Register, Priority Resolver and Interrupt Mask Register of 8259A.  $8-31 - H$  04
- (f) How many 8259A are required to have 36 interrupt inputs? Why?  $517 - 2-33-H$  02
- (g) Draw the block diagram of 64x8 ROM. Draw a structure of a MROM which can be used to store the function.  $v=5$   $727, 800 - T$  04

### SECTION-B

- Q4.** (a) Why the memory for a 8086 is set up as two banks? Describe with example.  $7-30-H$   $\frac{2}{3}$
- (b) Draw the block diagram of 8086 memory bank. What's happened when we want to read a word data to odd address?  $7-31-H$   $\cancel{v=5} - T$  04
- (c) Describe how a DMA controller operates in a microcomputer system with a block diagram.  $11-5-H + 490 - B$  05
- Q5.** (a) Describe a 5-bits DAC operation using a DAC, step size of 2V and input analog voltage,  $V_A = 42.4V$ .  $750 \leftarrow T$  05
- (b) Draw the symbolic figure of 2864 EEPROM and describe the timing diagram for the write operation.  $B06 - T$  04
- (c) A certain 8-bits DAC has a full scale output of 2mA and a full scale error of  $\pm 0.5\%$  F.S. what is the range of possible output for an input of 10000000?  $734 - T$   $\frac{1}{2}$

- Q6.** (a) What is the interrupt vector and the interrupt vector table? What's happened when type-0 interrupt is occurred in 8086 system?  $8-2, 8-3 - H$  04
- (b) Draw a PAL architecture for four inputs i.e., A, B, C and D. Now draw a PAL programmed for the following functions.  
 $O_1 = AB + \bar{CD} + A\bar{C}$ ,  $O_2 = \bar{ABC} + ABC + \bar{ABC}$   
 $O_3 = AB\bar{CD} + \bar{AB}CD + AB\bar{C}\bar{D}$  and  $O_4 = A + B\bar{D} + C\bar{D}$ , where  $O_1, O_2, O_3$  and  $O_4$  indicate four outputs.  $860 - T$  04
- (c) Explain why we use co-processor. What are purpose of 80x87 co-processor  $\frac{3}{3}$

- Q8.** (a) What are the differences between synchronous and asynchronous data transfer operation?  $\cancel{\text{Data communication}}$   $\frac{2}{3}$
- (b) Explain and draw the block diagram of 8251 USART  $14-9 - H$   $\cancel{W^0}$  04
- (c) Describe the response that an 8259A will make if it receives an interrupt signal on its IR<sub>i</sub> and IR<sub>r</sub> inputs at the same time.  $8-32-H$  02
- (d) Distinguish between random and raster scan display.  $13-5-H$  02

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### SECTION A

- ~~Q1.~~ (a) Write down the difference among PLA, PAL, and PROM. 03  
 (b) Define port. What are the difference between fixed port and variable port addressing? 04  
 (c) What is the interrupt instruction for keyboard interfacing? Describe it for different parameters. 03
- ~~Q2.~~ (a) Show the command byte format of the command register of 82C55. 03  
 (b) What is the purpose of the ACK signal in strobed output operation of the 82C55? 02  
 (c) Develop an I/O port decoder, using the PA1618, that generates the following high-bang I/O strobes: 3001H, 3003H, 1005H and 1007H. 04  
 (d) Why are both BHE and BLE ( $A_0$ ) ignored in a 16-bit port address decoder? 02
- ~~Q3.~~ (a) Define machine cycle and instruction cycle. 03  
 How does the circuit in the 8086 make sure that you can not accidentally write a byte or word to ROM? 02  
 (b) Why is the 8086 memory set up as 2-byte wide bank? What logic levels would you find on  $\overline{RD}$  and  $\overline{WE}$  when an 8086 is writing a word to address 013731H? 03  
 (c) A 74LS138 decoder has its three SELECT inputs connected to  $A_0$ ,  $A_1$  and  $A_2$  of the system address bus. It has  $G_1$ ,  $G_2B$  and  $G_1$  connected to  $A_1$ ,  $\overline{RD}$  and +5V respectively. Use an address decoder worksheet to determine what eight ROM address blocks the decoder output will select. 02
- ~~Q4.~~ (a) What is memory coding? Why is it important? 03  
 (b) Explain how memory error can be detected using parity generator. 03  
 (c) Draw the internal structure of the 80x87 arithmetic coprocessor and explain the coprocessor operation. 06

### SECTION-B

- ~~Q5.~~ (a) Explain and draw the block diagram of 8251A USART. 03  
 (b) Describe the bit format used for sending asynchronous data. 01  
 (c) A certain 12 bit BCD digital-to-analog converter has a full scale output of 9.99V.  
 (i) Determine the percentage resolution.  $\frac{1}{12} \times 100\% = 0.02\%$  03  
 (ii) Determine the converter's step size.  $\frac{9.99}{12} = 2.99 \times 10^{-3} V = 2.99 mV$  04
- ~~Q6.~~ (a) With appropriate timing diagram describe the DMA operation. 04  
 (b) Describe the basic functions of a DMA controller. How does it control the I/O R/W and memory R/W signals? 02  
 (c) Why is NRZ recording used on a disk memory system? Describe the modified frequency modulation(MFM) used in a disk memory system. 03
- ~~Q7.~~ (a) Draw the internal structure and timing diagram of mode 2 operation of 82C55. 05  
 (b) Draw the interface diagram and necessary assembly code of an 8-digit LED display interfaced to the 8086 microprocessor through an 82C55 PPI. 05  
 (c) Distinguish between random and raster scan display. 02
- ~~Q8.~~ (a) Each counter in the 8254 function how many different modes? Draw mode 1,2,3 for count 5. 05  
 (b) How many 8259A are required to have 64 interrupt input? 02  
 (c) Draw the internal block diagram of 8284A clock generator. Describe how the clock signal is generated in the 8284A. 03

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SECTION-A

Q1. (i) Draw the circuit connections of the following:

Suppose you want to add 3K X 8, 2732 EPROM to the system where the address range is 0000H-01FFFH.

(ii) Suppose you want to add 2K X 8 RAM to the system, where the address of the first RAM start at 8000H.

Q2. (i) Write the importance of memory address decoder. 7-26

(ii) Define port. What are the differences between fixed and variable port addressing? 3+8-B

Q3. (i) What is handshaking? Why handshaking is necessary in interfacing? Explain with suitable example. 3 2

(ii) If the  $F/C$  pin is placed at a logic 1 level, the crystal oscillator is disabled. Where is the timing input signal attached to the 8284A under this condition?

(iii) What is meant by modular programming? What are the purposes of linker? 2 51-B

Q4. (i) Compare the operation of the following elements: 1 2 3 4  
1 2 3 4  
(i) PLA (ii) PROM and (iii) PAL 1 2 3 4  
1 2 3 4

(ii) What is the advantage of R/2R ladder DACs? Draw the basic R/2R ladder DAC and prove that 4

$$V_{out} = \frac{-V_{ref}}{8} \times B \text{ Where } B \text{ is the value of binary input. } 32-T$$

(iii) How does the circuitry on the SDK-86 make sure that you can not accidentally write a byte or word to ROM? 7-32-H

(iv) Describe the response that an 8259A will make if it receives an interrupt signal on its IR3 and IRS inputs at the same time. 3-32-H

(v) What are the major disadvantages of digital ramp ADC? 7-44-T

Q5. (i) Write a program to calculate the area of a circle using 48X87 co-processor. 565-B

(ii) Explain how memory error can be detected using parity generator. 11-22-H

(iii) Explain why we use co-processor? What are the purposes of NEU of 80387?

(iv) Distinguish between random and raster scan display. 13-11-H-13-5

SECTION-B

Q6. (i) What is meant by software and hardware interrupt? 5-1-H

(ii) Draw the block diagram of circuitry to produce dot matrix character display of CRT. 13-7-H

(iii) Using 74LS138, 7 to 8 line decoder, combine eight 2764 EPROM chips for a 64K X 8 section of memory in an 8086 microprocessor system. Explain with address table. 2 43-B

Q7. (i) Describe briefly the bit format used for sending asynchronous serial data transfer.

(ii) What is the interrupt instruction for keyboard interfacing? Describe it for different parameters.

(iii) What are the differences between synchronous and asynchronous data transfer operation?

(iv) Compare the maximum conversion times of a 10-bit digital-ramp ADC and a 10-bit successive approximation ADC if both utilize a 500 KHz clock frequency. 3 2

(v) How many 8259As are required to have 64 interrupt inputs? When are the CAS0-CAS2 pins used on the 8259A? 8-33-H

(vi) Describe the response that an 8259A will make if it receives an interrupt signal on its IR3 and IRS inputs at the same time. Assume fixed priority for the IR inputs. What responses will the 8259A make if it servicing IRS interrupt and can IR3 interrupt signal occurs?

Total (8-32)

Q8. (i) Why is the 8086 INTR input automatically disabled when the 8086 is RESET?

(ii) What will be the status of command byte A of 82C55 PPI if we want to select the followings:

(a) Port A as input port

(b) Port B as output port

(c) Port C as input port

(d) Why is the 8086 memory set up as 2-byte wide bus?

(e) Explain the working principle of master-slave connection of 8259A PCI with block diagram.

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8-19 + 5-33-H

**V.2. How do you think the government can help?**  
The government can help by:  
- giving more money to schools  
- giving more money to teachers  
- giving more money to students

## SECTION A

~~Q1~~ What is meant by port? What are the difference between variable port addressing and fixed port addressing? ~~03~~

~~Q2~~ Draw the block diagram of 8255A I/OPI ~~03~~

~~Q3~~ What will be the condition of command register D if we want to select the following things in 8255A? ~~03~~

Port A output	1	0	1	0	1	0	1	1	0
Port B input	1	1	0	0	0	0	0	0	0
Port C output	1	0	1	0	1	0	1	0	0
Mode (0)	1	1	0	0	0	0	0	0	0

~~Q4~~ What is 8086? ~~03~~ ~~Q4~~

~~Q5~~ What are the differences among PIA, ISA and PCMCIA? ~~03~~

~~Q6~~ Describe briefly the bit format used for sending a synchronous serial data transfer. ~~03~~

~~Q7~~ Using 74LS138, 3 to 8 line decoder, combine two 2716 PROM chip for a 4K X 8 section of memory in an 8080 microprocessor system. ~~03~~

~~Q8~~ Draw the internal block diagram of the 8281A clock generator. Describe how "lock signal" is regenerated in the 8281A. ~~03~~

~~Q9~~ If the LC Pin is at logic 1 level, the crystal oscillator is disabled. Why? Is the frame input signal attached to the  $\overline{CS}$  pin? ~~03~~ ~~Q9~~

~~Q10~~ Draw the block diagram of circuitry to produce a single's edge triggered delay of 10ns. ~~03~~

~~Q11~~ What are major disadvantages of Digital Peaking? ~~03~~ ~~Q11-T~~

~~Q12~~ Write the working principle of successive approximation ADC with figure. ~~03~~ ~~Q12-T~~

~~Q13~~ Compare the maximum conversion time of a 10 bit digital ramp ADC and a 10 bit successive approximation ADC to achieve a 500 KHz clock frequency. ~~03~~ ~~Q13-T~~

888-100000

Q1	<u>Why is handshaking necessary for interfacing? Write an example with necessary code for handshaking.</u>	3
Q2	<u>Explain and draw the block diagram of 8259A IC.</u>	01
Q3	<u>What is the interrupt instruction for Keyboard interfacing? Describe it for different parameters.</u>	01
Q4	<u>What will happen when you want to put cascaded connection of 8259A? Explain with necessary figure.</u>	2
Q5	<u>Draw the interface diagram and necessary assembly code of an 8 digit LED display interfaced to the 8086 microprocessor through an 8255 PPI.</u>	05
Q6	<u>Why is the 8080 memory set up as 2-byte wide busses?</u>	2
Q7	<u>How does the circuitry on the 8080 make sure that you can not accidentally write a byte or word to ROM?</u>	02
Q8	<u>Draw the internal structure and timing diagram of mode 2 operation of the 8259A.</u>	05
Q9	<u>Why the 8080 INT# input is automatically disabled when the 8080 is RESET?</u>	02
Q10	<u>How read and write operation take place in memory disk.</u>	03
Q11	<u>Describe the response that an 8259A will make if it receives an interrupt signal on its IR# and INT inputs at the same time.</u>	01
Q12	<u>Explain the Mode 1 strobed input and output operation with a diagram.</u>	1

N.B. (i) Answer SIX questions, taking THREE from each Section.  
 (ii) Figures in the margin indicate full marks.  
 (iii) Use separated answer script for each section.

### SECTION-A

- | Marks | SECTION-A  | SECTION-B |
|-------|--|-----------|
| 1     | Q. 1(a) What are the purposes of the 8086 interrupt vector table?  |           |
| 4     | (b) How many 8259As are required to have 64 interrupt inputs? When are the CAS0-CAS2 pins used on the 8259A?     |           |
| 2     | (c) What are the purpose of the IR0-IR7 pins on the 8259A? B - 9 G 9   |           |
| 4     | (d) What is the interrupt instruction for keyboard interfacing? Describe it for different parameters.            |           |
| 1     | Q. 2(a) What are the differences between buffer and latch? I - I 9   |           |
| 6     | (b) What are the advantages of using DMA controller? Draw the block diagram of 8237A DMA controller. J J - 5 H   |           |
| 4     | (c) Compare the operation of the following elements:<br>(i) PLA (ii) PROM and (iii) PAL.                         |           |
| 3     | Q. 3(a) What are the differences between the synchronous data transfer and asynchronous data transfer?           |           |
| 2     | (b) Write a BSR control word subroutine to set bits PC <sub>7</sub> and PC <sub>1</sub> and reset after 10ms.    |           |
| 2     | (c) Why is the 8086 memory set up as 2-byte wide bank?   |           |
| 5     | (d) Why handshaking is necessary for interfacing? Write an example with assembly code for handshaking operation. |           |
| 1     | Q. 4(a) Why is the 8086 INTR input automatically disabled when the 8086 is RESET?                                |           |
| 4     | (b) Design a six bit D/A converter using binary-weighted resistors. Assume the MSB resistor is 20KΩ. 722 - 4     |           |
| 5     | (c) Describe the working principle of model strobed input and output operations with appropriate timing diagram. |           |

### SECTION-B

- | SECTION-B | SECTION-B  |
|-----------|--|
| 2         | Q. 5(a) Why does conversion time increase with the value of the analog input voltage? 744 - T  |
| 3         | (b) Using 74LS138, 3 to 8 line decoder, combine eight 2761 EPROM chip for a 64K × 8 section of memory in an 8086 microprocessor system.  |
| 5         | (c) Explain and draw the block diagram of 8231A USART.   |
| 1         | Q. 6(a) What is SDK-86?  |
| 3         | (b) How can 8086 response to an interrupt? S - 1   |
| 4         | (c) Distinguish between random and raster scan display.  |
| 3         | (d) Describe bit format used for sending asynchronous serial data.   |
| 5         | Q. 7(a) How does the circuitry on the SDK-86 make sure that you can not accidentally write a byte or word to ROM?  |
| 5         | (b) Draw the flow diagram and circuit connections to write the character "A" on a LED matrix character display using 8088 microprocessor.  |
| 5         | (c) A certain 10-bit ADC has a full scale output of 10.23V. Determine,<br>(i) The digital equivalent obtained for V <sub>a</sub> =1345V. step size = $\frac{10.23}{2^{10}-1} = 0.01$ $d_{10} = \frac{1.345}{0.01} = 134.5 \approx 1$<br>(ii) The conversion time. 135 μs<br>(iii) The resolution of this converter. Assume that clock frequency = 1MHz and V <sub>T</sub> = 0.2mV. |
| 2         | Q. 8(a) Explain how memory error can be detected using parity generator?   |
| 4         | (b) Explain why we use co-processor? What are the purpose of NI-U of 8087?   |
| 4         | (c) Draw the internal structure of the 8087 arithmetic co-processor and explain the co-processor status register.  |
| 2         | (d) Write a program to calculate the area of a circle using 8087 co-processor.   |

"Heaven's Light is Our Guide"

Department of Computer Science & Engineering  
Rajshahi University of Engineering & Technology  
B.Sc. Engineering 3<sup>rd</sup> Year 6<sup>th</sup> Semester Examination, 2006  
Course No: CSE 607C Course Title: Peripherals and Interfacing  
Full Marks: 70. Time: Three (03) Hours

N.B. (i) Answer Six questions, taking Three from each Section.

(ii) Figures in the margin indicate full marks.

(iii) Use separate answer script for each section

Junction point

Marks,  
3 1/2

SECTION-A

Q.1 (a) Define port. What are the differences between fixed port addressing and variable port addressing? B-363 Ch-7/1 Pg-1

4

(b) Draw the interface diagram of an 8-digit LED display interfaced to the 8088 microprocessor through an 82C55 PIA. B-375 Ch-9 Pg-9

4

(c) What is the interrupt instruction for keyboard interfacing? Describe it for different parameters. B-396

4

Q.2 (a) Draw the command bytes of the command register in the 82C55. B-383

5

(b) Describe the Mode1 strobed input operation with appropriate timing diagram. B-400

4

(c) Why handshaking is necessary in interfacing? B-367 Pg-15

2 1/2

Q.3 (a) What are the major disadvantages of Digital-Ramp ADC? T-752 Pg-57

2 1/2

(b) Write the working principle of successive-approximation ADC. T-756 Pg-57

6

(c) Compare the maximum conversion times of a 10 bit digital-ramp ADC and a 10-bit successive-approximation ADC if both utilize a 500KHz clock frequency T-755 Pg-261

3

Q.4 (a) Describe byte and word operation in terms of memory bank concept. B-381 Pg-25

4

(b) Draw the pin-out diagram of the 82C55 PPI. B-291 Pg-11

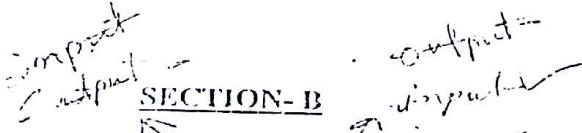
3

(c) Compare the operation of the following elements:

4 1/2

- i) PLA
- ii) PROM
- iii) PAL

SECTION-B



Q.5 (a) What are the differences between buffer and latch? B-365 Pg-23

1 1/2

(b) Draw the block diagram of circuitry to produce dot matrix character display of CRT.

5

(c) What are the advantages of using DMA controller? Draw the block diagram of 8237A DMA controller. B-413 Pg-479

5

Q.6 (a) Why is the 8086 memory set up as 2-byte wide banks?

2 1/2

(b) How does the circuitry on the SID-86 make sure that you cannot accidentally write a byte or word to ROM? || (13)

2

(c) Draw the internal structure and timing diagram of Mode-2 operation of the 82C55. B-401 Pg-15

2

(d) Why is the 8086 INTR input automatically disabled when the 8086 is RESET?

2

Q.7 (a) With appropriate timing diagram describes the DMA operation. B-470 Pg-14 Pg-14

3 1/2

(b) Draw the internal block diagram of 8259A. B-232 Pg-12

3

(c) What are the relative advantages and disadvantages of SRAM and DRAM? Pg-1

5

Q.8 (a) How read and write operation take place in magnetic disk. || (4)

3

(b) Describe bit format used for sending asynchronous serial data. B-481 Pg-1

4

(c) Explain block diagram of 8251A USART. B-470 Pg-1

4 1/2

\*\*\*\*\* The End \*\*\*\*\*

N.B. Answer any Six questions, taking Three from each Section

The questions are of equal value.

Use separate answer script for each section.

SECTION-A

Q.1 (a) What is machine cycle? *A (165)*

(b) Describe the sequence of events on the 8086 data/address bus, the ALE line, the M/IO line, and the RD line as the 8086 fetches an instruction word. *B (125)*

(c) Describe the two purposes of address decoders in microcomputer systems. *A (18)*

(d) Why is the 8086 memory setup as 2-byte wide banks? What logic levels would you find on BHE and AO when an 8086 is writing a word to address 04373H? *A (18)*

BHE	A <sub>0</sub>	1st	D <sub>8-D<sub>15</sub></sub>
0	1		
1	0	2nd	D <sub>7-D<sub>0</sub></sub>

Q.2 (a) How does the 8086 respond to the interrupts? Explain. *A (20)*

(b) Draw the block diagram of 8259A. *A (23)*  
Describe the response that an 8259A will make if it receives an interrupt signal on its IR3 and IRS inputs at the same time. Assume fixed priority for the IR inputs. What response will the 8259A make if it is servicing an IRS interrupt and an IR3 interrupt signal occurs? *A (23)*

Q.3 (a) Why is it necessary to PUSH all registers used in the procedure at the start of an interrupt-service procedure and to POP them at the end of the procedure? *A (21)*

(b) Show the mode set control word needed to initialize an 8255A as follows:

port A-handshake input;

port B-handshake output;

port C- bits PC6 and PC7 as outputs.

(c) How many modes of operation are there to 8255 counter? Draw mode 1, 2, 3 for count = 5. *B (710)*

Q.4 (a) What is 8237 DMA controller? *A (21)*

(b) Describe what happens when any I/O device wants DMA operation to an 8237 DMA controller. *B (27)*

(c) Draw the block diagram of 8254 interval timer and explain the control word of this interval timer. *B (10)*

SECTION-B

Q.5 (a) What is the purpose of STB signal in strobed input operation of the 82055? *B (2, 21)*

(b) Draw the interface of a 4x4 keyboard matrix connected to an 8088 microprocessor through the 82055. *P.A.*

(c) What is handshaking? Why is it important? Explain with an example. *B (1, 17)*

(d) What are the differences between isolated and memory-mapped I/O? *P.A. (3, 9)*

(e) Write down a procedure that transfers the ASCII character from AII to the printer via port B.

(f) How many 8259AS are required to have 64 interrupt inputs?

(g) Why coprocessor is important? *A (762)*

Q.7 (a) Describe the working principle of two-bit flash ADC. *A (762)*

(b) Explain the functions of 3 BIOS interrupt and 3 DOS interrupt.

(c) A certain 12-bit BCD digital-to-analog converter has a full-scale output of 9.99V. *A (781)*

(i) Determine the percentage resolution.

(ii) Determine the converter's step size.

$$\text{Resolution} = \frac{9.99}{2^{12}-1}$$

Q.8 (a) Write the differences between EPROM and Flash memory. *A (716, 1719)*

(b) Why 325 PROM is used as address decoder instead of 74 LS138? *A (185)*

(c) Explain how DMA works for a read operation in case of 8272A floppy-disk controller system. *H (319)*

(d) Compare the maximum conversion times of a 10-bit digital-ramp ADC and a 10-bit successive-approximation ADC if both utilize a 500-KHz clock frequency. *T (758)*

N.B. Answer six questions, taking three from each section.

The questions are of equal value.

Use separate answer script for each section.

### SECTION - A

- Q1. (a) What information processes the COMMAND.COM program?  
 (b) What does the EXTRN directive indicate when placed in program module? B(2<sup>3</sup>)  
 (c) What is TPA? Why it is necessary?  
 (d) Briefly describe the memory mappings of System Area in a microprocessor based system. B(2<sup>3</sup>)
- Q2. (a) What do you mean by modular programming? What are the purposes of Linker? B(2<sup>3</sup>)  
 (b) Draw the internal block diagram of the 8284A clock generator. Describe how clock signal is generated in the 8284A. B(2<sup>3</sup>)  
 (c) Why is demultiplexing of buses necessary? Draw the timing diagram of simplified 8086/8088 write bus cycle. B(1<sup>6</sup>)  
 (d) If the F/C pin is placed at a logic 1 level, the crystal oscillator is disabled. Where is the timing input signal attached to the 8284A under this condition? B(2<sup>3</sup>)
- Q3. (a) Describe with an example why wait state is important? B(3<sup>0</sup>)  
 (b) Interface a wait state generator 74LS164 with the clock generator 8284A and draw the wait state generation timing of the circuit. B(3<sup>0</sup>)  
 (c) What is memory coding? Why it is important? B(3<sup>2</sup>)  
 (d) Using 74LS138 3-to-8 line decoder, combine eight 2764 EPROM chip for a  $64K \times 8$  section of memory in an 8088 microprocessor based system. What will be the address range? B(3<sup>2</sup>)
- Q4. (a) Explain how an parity error can be detected using parity per column? B(3<sup>0</sup>)  
 (b) Explain why we use co-processor? What are the purposes of NI-U of 80X87? B(5<sup>2</sup>)  
 (c) Draw the internal structure of the 80X87 arithmetic coprocessor and explain the coprocessor status register. B(5<sup>2</sup>)  
 (d) Write a program to calculate the area of a circle using 80X87 co-processor. B(5<sup>2</sup>)

### SECTION - B

- Q5. (a) Design a six-bit DAC uses binary-weighted resistors. Assume the MSB resistor is  $20\text{ k}\Omega$ .  
 (b) What is the advantage of R/2R ladder DAC? Draw the basic R/2R ladder DAC and prove that  

$$V_{out} = -\frac{V_{ref}}{8} \times B$$
 Where B is the value of binary input. B(3<sup>3</sup>)
- (c) A certain 10-bit ADC has a full scale output of 10.23V. Determine:  
 i) The digital equivalent obtained for  $V_i = 1.345\text{V}$  B(3<sup>2</sup>)  
 ii) The conversion time B(3<sup>2</sup>)  
 iii) The resolution of this converter. Assume that clock frequency = 1 MHz.  $V_t = 0.2\text{mV}$  B(3<sup>2</sup>)
- (d) Why the conversion time increase with the value of the analog input voltage? B(3<sup>2</sup>)
- Q6. (a) What do you mean by fixed address and variable address? Distinguish between isolated I/O and memory mapped I/O.  
 (b) Write a BSR control word subroutine to set bits PC<sub>7</sub> and PC<sub>6</sub> and reset after 10 ms.  
 (c) Draw the timing diagram of strobed input operation. B(3<sup>2</sup>)  
 (d) If the command byte of the command register in the 82C55 PPI is 10110110 then mention the status of the mode of selection of ports as well as port directions. B(3<sup>2</sup>)
- Q7. (a) Why model 1 of 8254 is called monostable multivibrator? Explain with timing diagram.  
 (b) Write instructions to generate a 1 KHz square wave from counter 1. Assume the gate of counter 1 is tied to 15V through a 10 KΩ resistor. Explain the significance of connecting the gate to +5V. B(3<sup>2</sup>)  
 (c) List the major components of the 8279 keyboard/display interface and explain their functions. B(3<sup>2</sup>)
- Q8. (a) Describe the response that an 8259A will make if it receives an interrupt signal on its IR3 and IR5 inputs at the same time. Assume fixed priority for the IR inputs. What responses will the 8259A make if it is servicing an IR5 interrupt and an IR3 interrupt signal occurs? B(3<sup>2</sup>)  
 (b) Why is NRZ recording used on a disk memory system? Describe the modified frequency modulation (ML-N) used in a disk memory system. B(3<sup>2</sup>)  
 (c) Describe the basic functions of a DMA controller. How does it control the I/O R/W and memory R/W signals? B(3<sup>2</sup>)  
 (d) Why is the DMA controller faster than microprocessor for data transfer? B(3<sup>2</sup>)

**CT#4 CSE-607**

$\sqrt{2}^2 = \frac{1}{2}$

$\sqrt{2}^2$

- Q1. Draw 2-bit flash ADC and write the corresponding truth table. (05)  
Q2. Draw the timing diagram for 5-bit successive approximation ADC when  $V_A=30.5V$  and step size 1.5V. (06)  
Q3. Draw the figure of 4-bit R/2R ladder and also deduce the equation for  $V_{out} = -V_{REF} * B / 16$ . (09)

**CT#3 Course Code: CSE-607**

Time: 30min

Marks: 20

Set: C

$$(24)_{10} = (11000)_2$$

- Q1. Describe the use of the CAS0, CAS1, and CAS2 lines in a system with a cascaded 8259A. (marks 03)  
Q2. Describe the response that an 8259A will make if it receives an interrupt signal on its IR3 and IR5 inputs at the same time. Assume fixed priority for the IR inputs. What response will the 8259A if it is servicing an IR5 interrupt and an IR3 interrupt signal occurs? (marks 04)  
Q3. Suppose you have 256x4 RAM. If you write the RAM, register no 24 and register value 10. What are the pins combination (address pins, input pins (value), Chip Select pin and R/W pin). (marks 05)  
Q4. Draw a MiROM architecture for the following function  $y=x^2+12$ . Where  $x < 4$  (marks 08)

12  
13  
14