

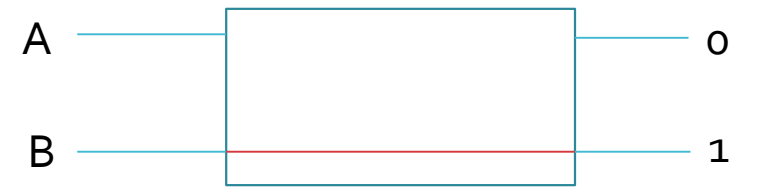
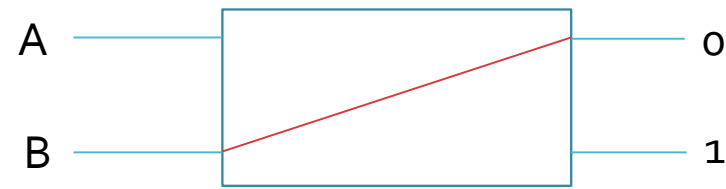
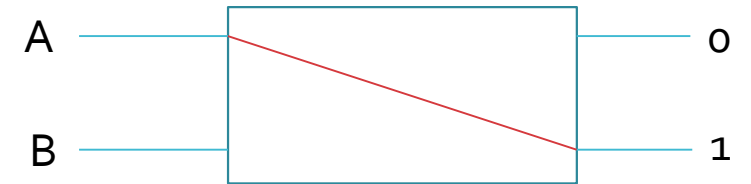
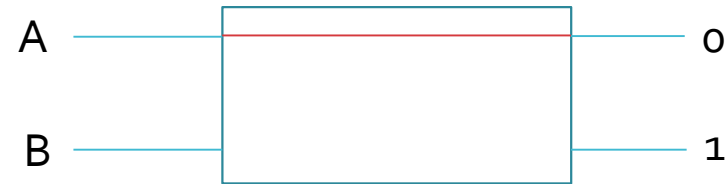
Multistage Switching Networks

Multistage Switching Network

- ❑ **Multistage interconnection networks** (MINs) are a class of high speed computer **networks** usually composed of processing **elements** (PEs) on one end of the **network** and memory **elements** (MEs) on the other end, connected by **switching elements** (SEs).

Crossbar /Interchange Switch

- The basic component of a multistage switching network is a two input, two output interchange/crossbar switch.



- **Main problem** is that if both A and B request the same output terminal, only one of them connected, other will be blocked and resubmitted.

Crossbar /Interchange Switch

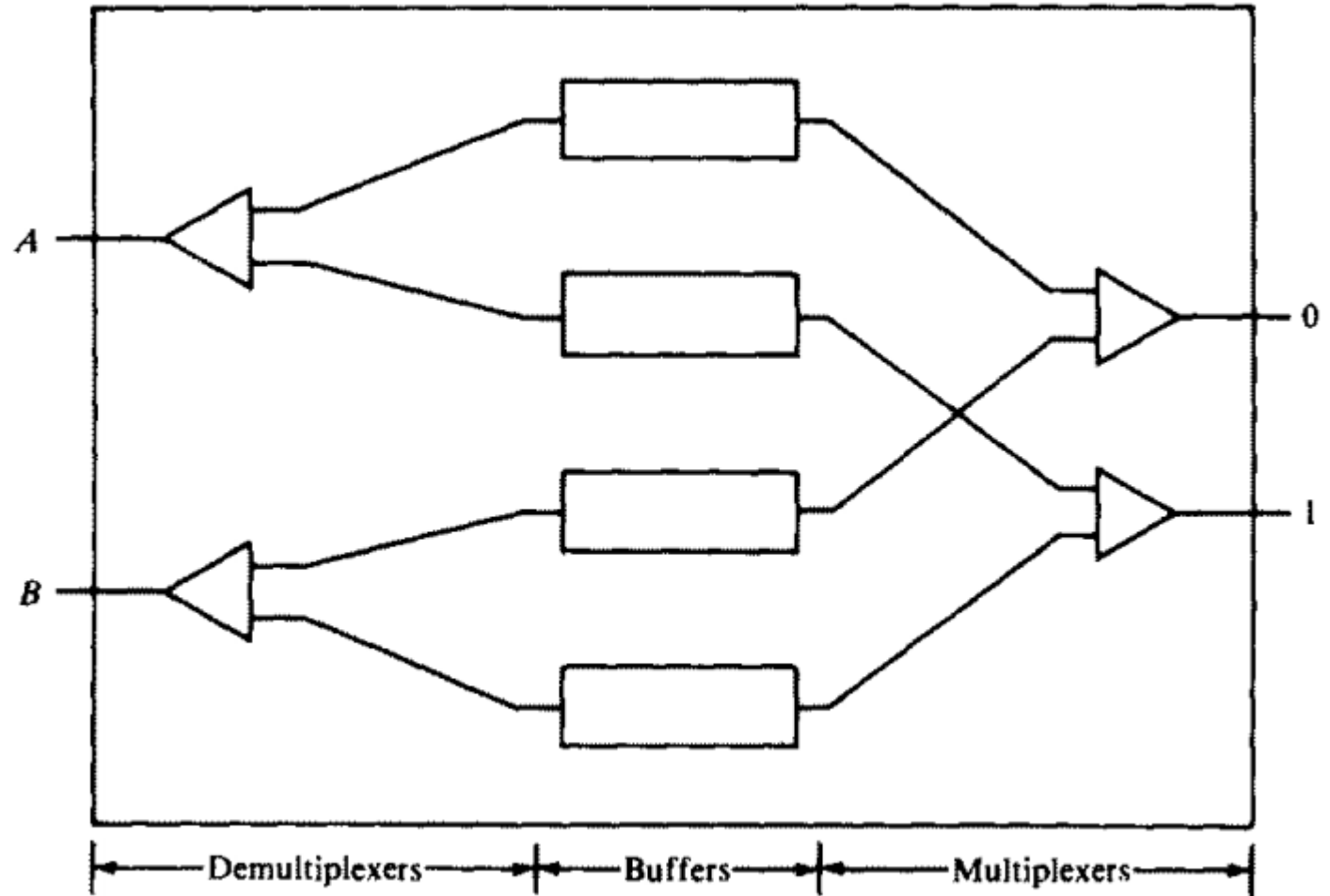


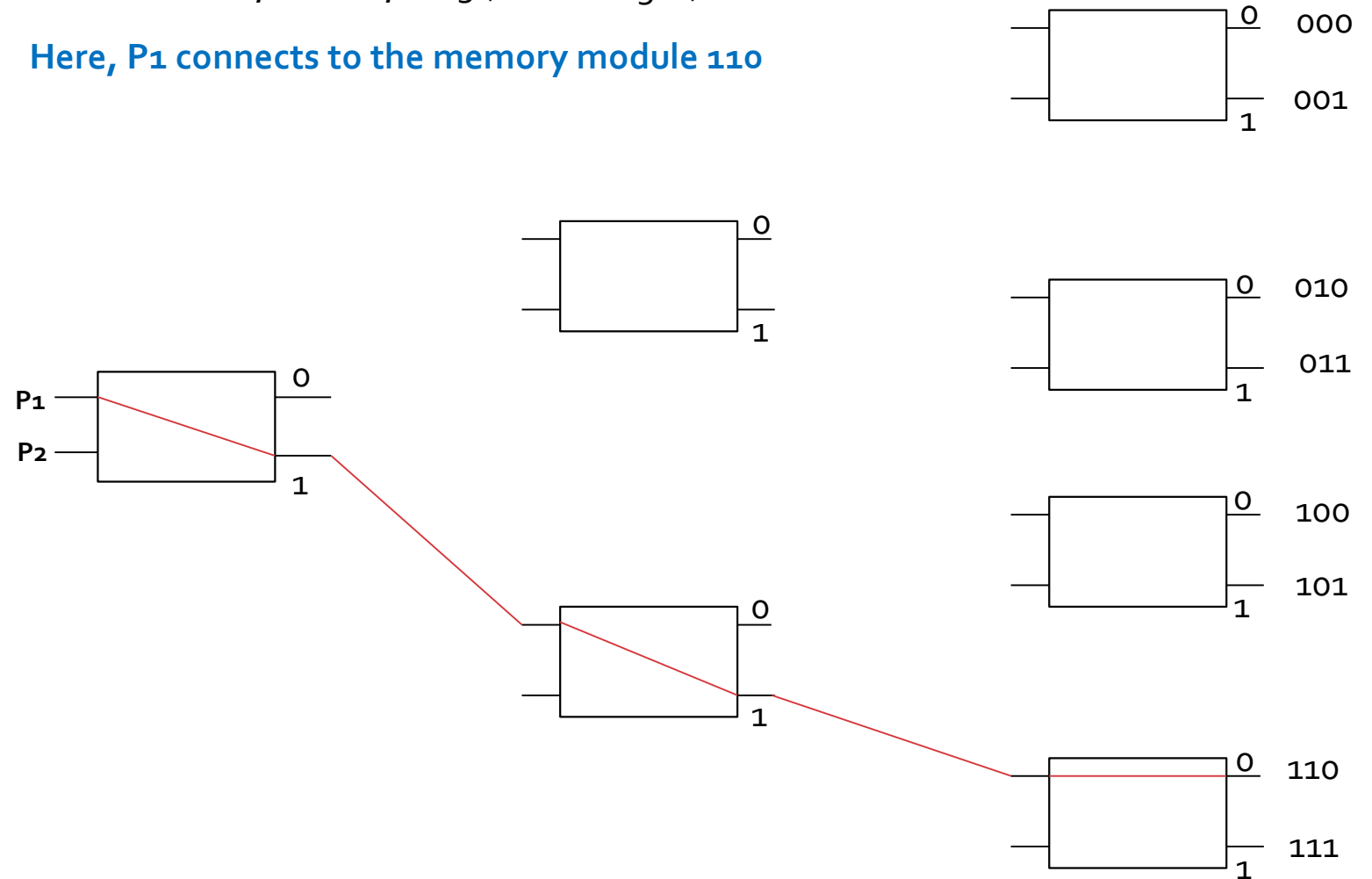
Figure: 2 x 2 Crossbar Switch with buffer

Binary Switch Network

- ❖ Build a binary switch network or 1 x 8 demultiplexer where processor P1 and P2 are connected through switches to the memory modules marked in binary 000 to 111.

➤ **Solution:** Here, $8 = 2^n$, $n = 3$ (no. of stages)

Here, P1 connects to the memory module 110



Delta Network

□ A **delta network** is defined as an $a^n \times b^n$ switching network with n stages consisting of $a \times b$ crossbar modules. The interconnection or link patterns between stages is such that there exists a unique path of constant length from any source to any destination.

Where, $a \rightarrow$ no. of inputs of each module and shuffle

$b \rightarrow$ no. of outputs of each module and base number of final stage output module

$n \rightarrow$ no. of stages

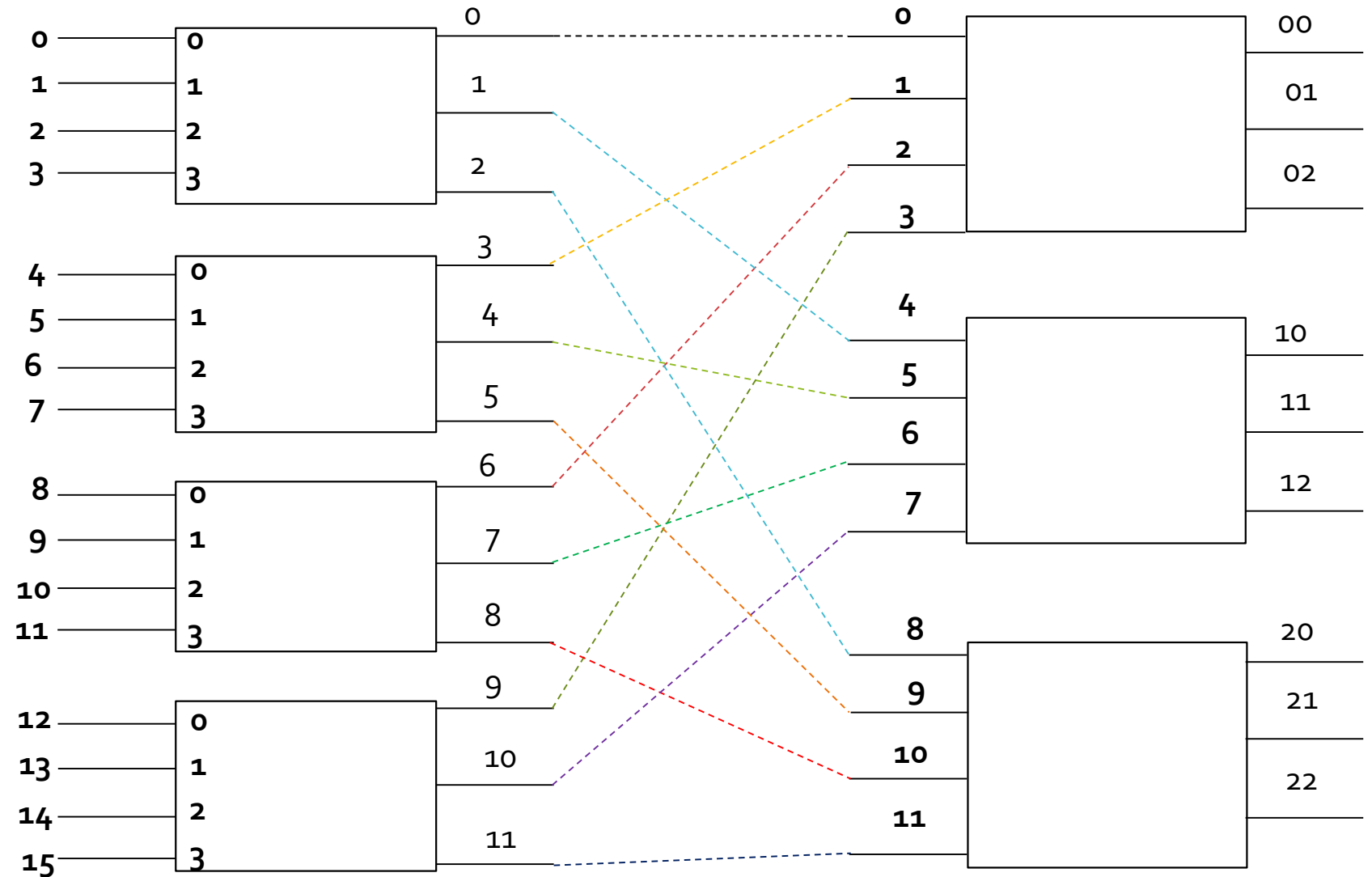
$x \rightarrow$ stage number

$a^{n-x} \times b^{x-1} \rightarrow$ no. of modules in each stage

$$S_{qc}(i) = \begin{cases} q_i \bmod (qc - 1), 0 \leq i < (qc - 1) \\ i, i = (qc - 1) \end{cases}$$

Delta Network

❖ Design a $4^2 \times 3^2$ delta network.



Delta Network

i	q_i	$S_{qc}(i)$
0	0	0
1	4	4
2	8	8
3	12	1
4	16	5
5	20	9
6	24	2
7	28	6
8	32	10
9	36	3
10	40	7
11	44	11

Omega Switching Network

- Omega network has self routing property and used in parallel computing architectures.
- It works for each possible input.
- The interconnection between stages are defined by the logical rotate left of the bits used in the port id's.
- $000 \rightarrow 000 \rightarrow 000 \rightarrow 000$
- $001 \rightarrow 010 \rightarrow 100 \rightarrow 001$
- $011 \rightarrow 110 \rightarrow 101 \rightarrow 011$
- $111 \rightarrow 111 \rightarrow 111 \rightarrow 111$
- If bit '1' then cell out to the lower port
- If bit '0' then cell out to the upper port

8x8 Omega Switching Network

