Color Plate Stick Diagram & Design Rules

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Stick Diagram

- Objectives:
  - To know what is meant by stick diagram.
  - To understand the capabilities and limitations of stick diagram.
  - To learn how to draw stick diagrams for a given MOS circuit.

- Outcome:
  - At the end of this module the students will be able draw the stick diagram for simple MOS circuits.

Stick Diagram…

- VLSI design aims to translate circuit concepts onto silicon.
- Stick diagrams are a means of capturing topography and layer information using simple diagrams.
- Stick diagrams convey layer information through color codes (or monochrome encoding).
- Acts as an interface between symbolic circuit and the actual layout.

Stick Diagram…

- Does show all components/vias.
  - Via is used to connect higher level metals from metal connection
- It shows relative placement of components.
- Goes one step closer to the layout
- Helps plan the layout and routing

A stick diagram is a cartoon of a layout.

Stick Diagram…

- Does ***not*** show
  - Exact placement of components
  - Transistor sizes
  - Wire lengths, wire widths, tub boundaries
  - Any other low level details such as parasitics

Parasitic Extraction is calculation of the parasitic effects in both the designed devices and the required wiring interconnects of an electronic circuit: parasitic capacitances, parasitic resistances and parasitic inductances, commonly called parasitic devices. When two electrical conductors at different voltages are close together, the electric field between them causes electric charge to be stored on them; this effect is parasitic capacitance.

Stick Diagram Color Codes

P diffusion	Yellow/Brown
N diffusion	Green
Polysilicon	Red
Contacts	Black
Metal1	Blue
Metal2	Magenta/Purple
Metal3	Cyan/L.Blue

Stick Diagram Color Codes…

Stick Diagrams – Notations

Contact Cut 

Stick Diagram-Some Rules

Rule 1:

When two or more 'sticks' of the same type cross or touch each other that represents electrical contact.

Stick Diagram-Some Rules…

Rule 2:

When two or more 'sticks' of different type cross or touch each other there is no electrical contact.

(If electrical contact is needed we have to show the connection explicitly)

Stick Diagram-Some Rules…

Rule 3:

When a poly crosses diffusion it represents a transistor.

Note: If a contact is shown then it is ***not*** a transistor.

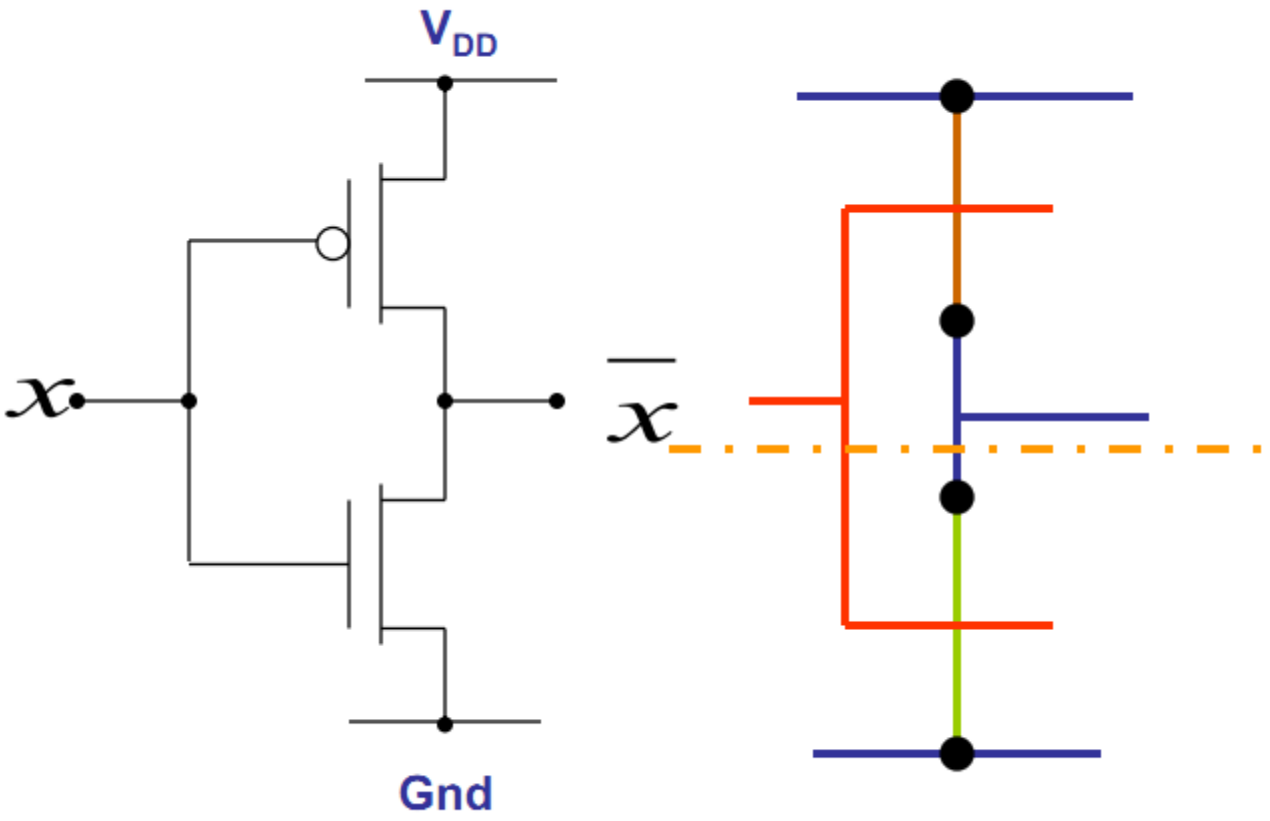
Stick Diagram-Some Rules…

Rule 4:

In CMOS a demarcation line is drawn to avoid touching of p-diff with n-diff. All PMOS must lie on one side of the line and all NMOS will have to be on the other side.

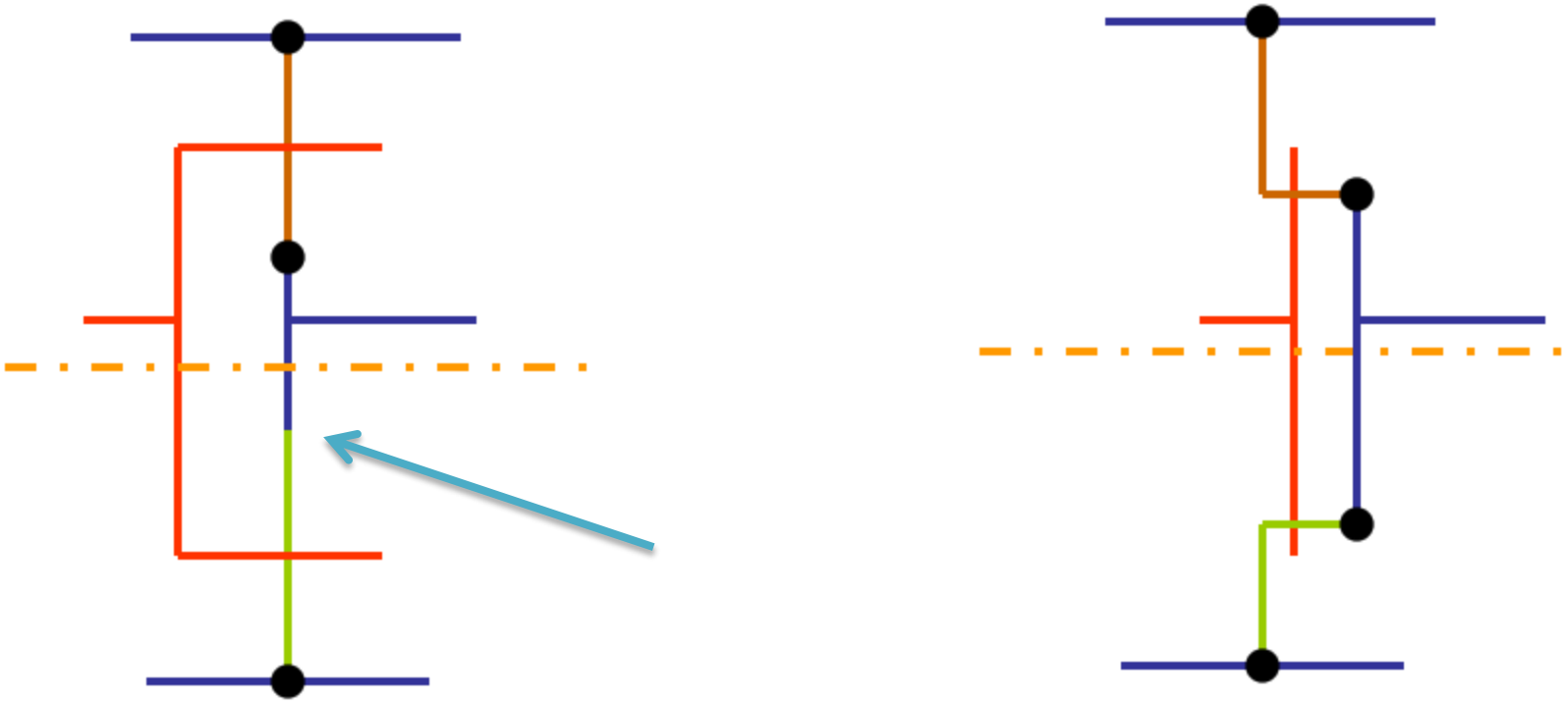
N:B: Only metal and polysilicon can cross the demarcation line

Stick Diagram-Examples



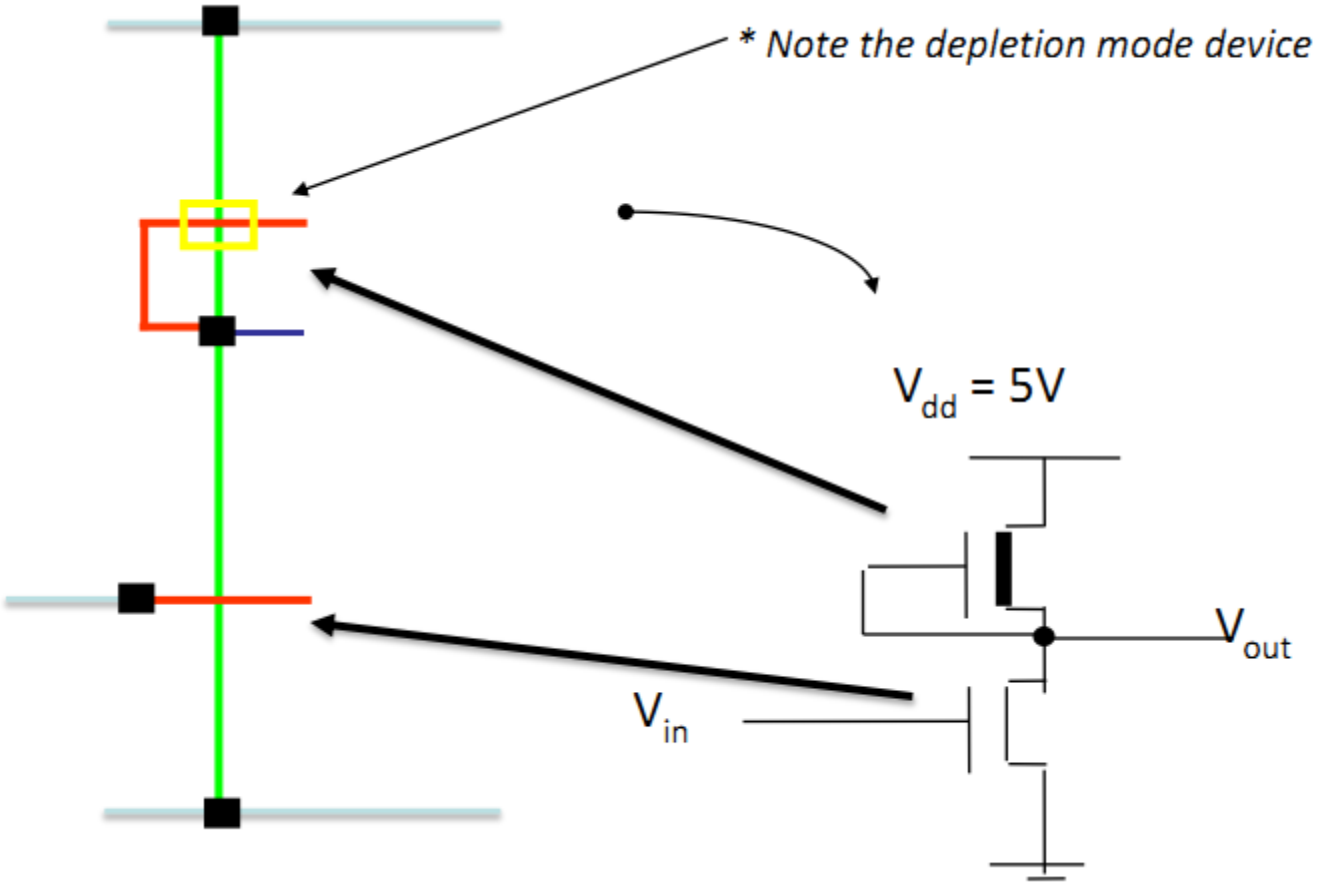
CMOS Inverter (Stick diagram-1)

Stick Diagram-Examples…



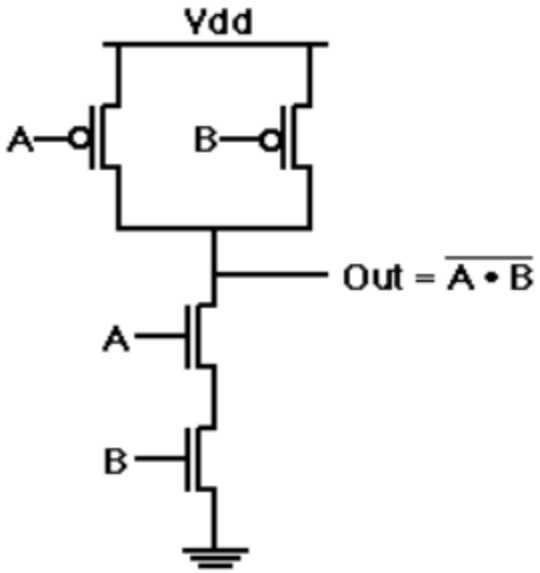
CMOS Inverter (Stick diagram-2)

Stick Diagram-Examples…

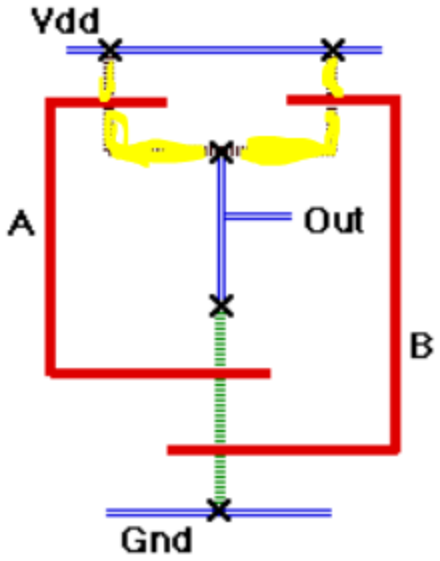


Depletion Load NMOS Inverter

Stick Diagram-Examples…



A	B	$\overline{A \bullet B}$
0	0	1
0	1	1
1	0	1
1	1	0

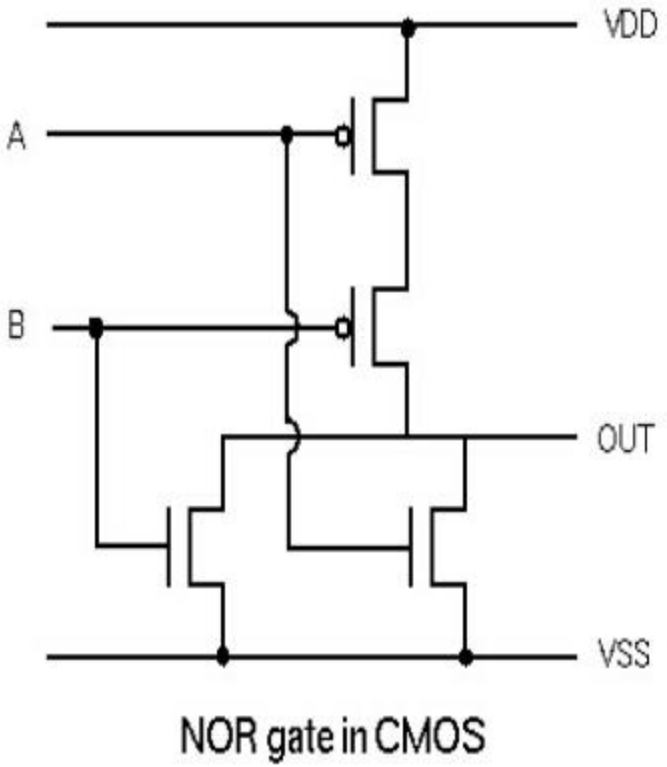


1. Pull-down: Connect to ground If A=1 AND B=1

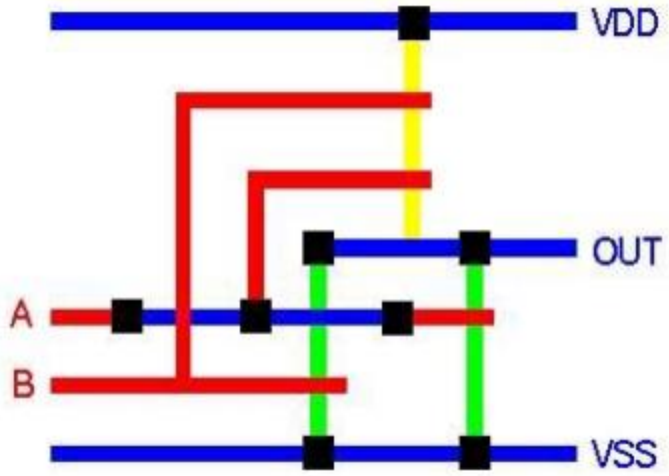
2. Pull-up: Connect to Vdd If A=0 OR B=0

CMOS NAND Gate

Stick Diagram-Examples…



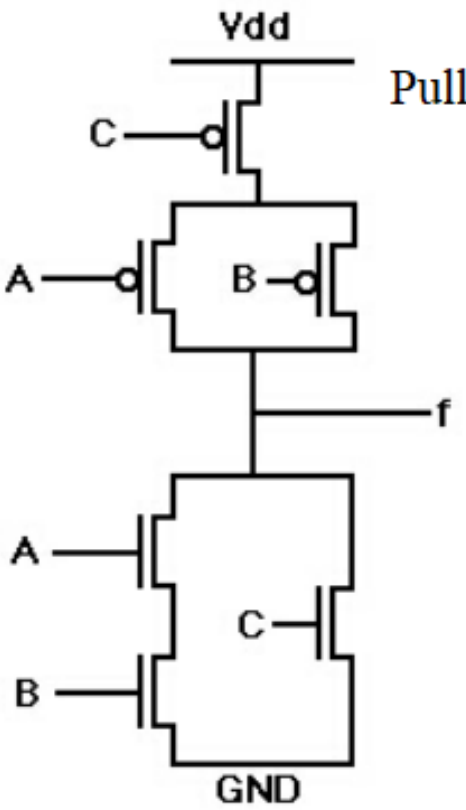
NOR gate in CMOS



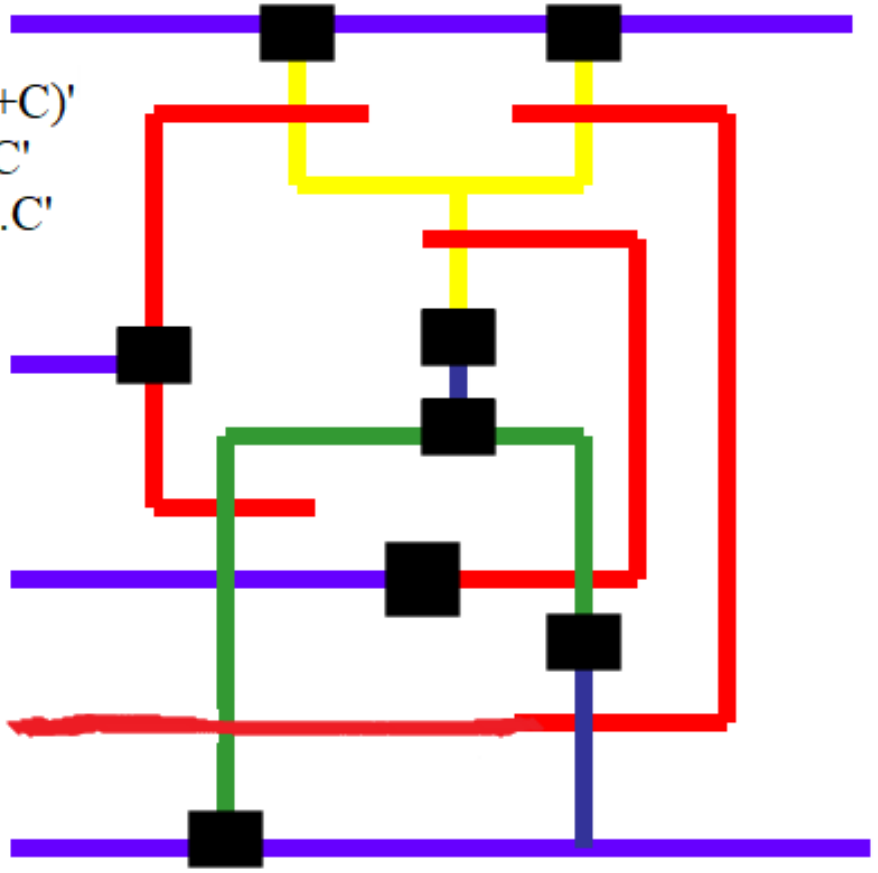
CMOS NOR Gate

Stick Diagram-Examples…

Example: $f = \overline{(A \bullet B) + C}$



Pullup f = ((A.B)+C)'
=(A.B)'.C'
=(A'+B').C'



Pulldown f ' = (A.B)+ C

Design Rules

- Allow translation of circuits, usually in stick diagram or symbolic form, into actual geometry in silicon.
- Interface between circuit designer and fabrication engineer.
- **Design rules** are a series of parameters provided by **semiconductor manufacturers** that enable the designer **to verify the correctness** of a **mask** set.

Design Rules…

Design rules define ranges for features

- Examples:
  - min. wire widths to avoid breaks
  - min. spacing to avoid shorts
  - minimum overlaps to ensure complete overlaps

Design Rules…

- **Design Rule Checking** (DRC) is the area of electronic design automation that determines whether the physical layout of a particular chip layout satisfies **design rules**.
- Three basic DRC check:

  -Width

  -Spacing

  -Enclosure

*https://en.wikipedia.org/wiki/Design_rule_checking

Design Rules…

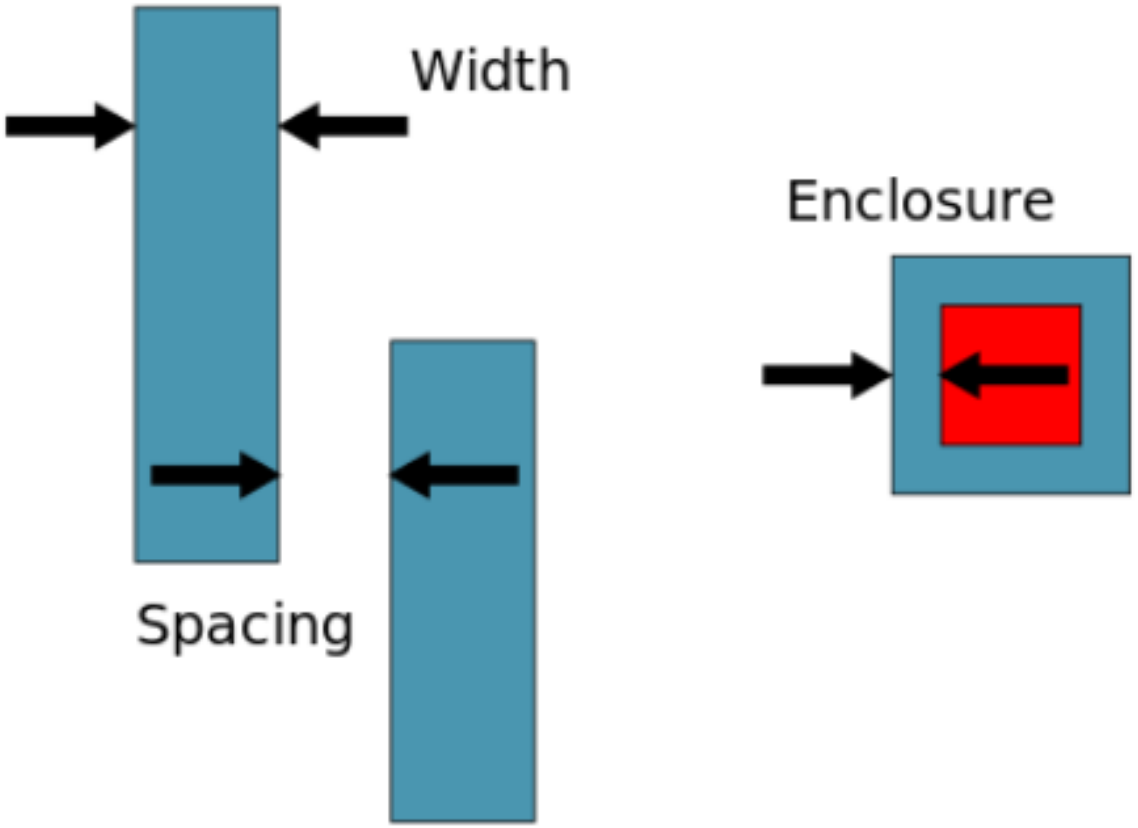


Fig.: Three Basic DRC Check

*https://en.wikipedia.org/wiki/Design_rule_checking

Design Rules…

Objectives

- To obtain a circuit with optimum yield.
- To minimize the area of the circuit.
- To provide long term reliability of the circuit.

*http://ece-research.unm.edu/jimp/vlsiII/labs/layout_lecture.html

Design Rules…

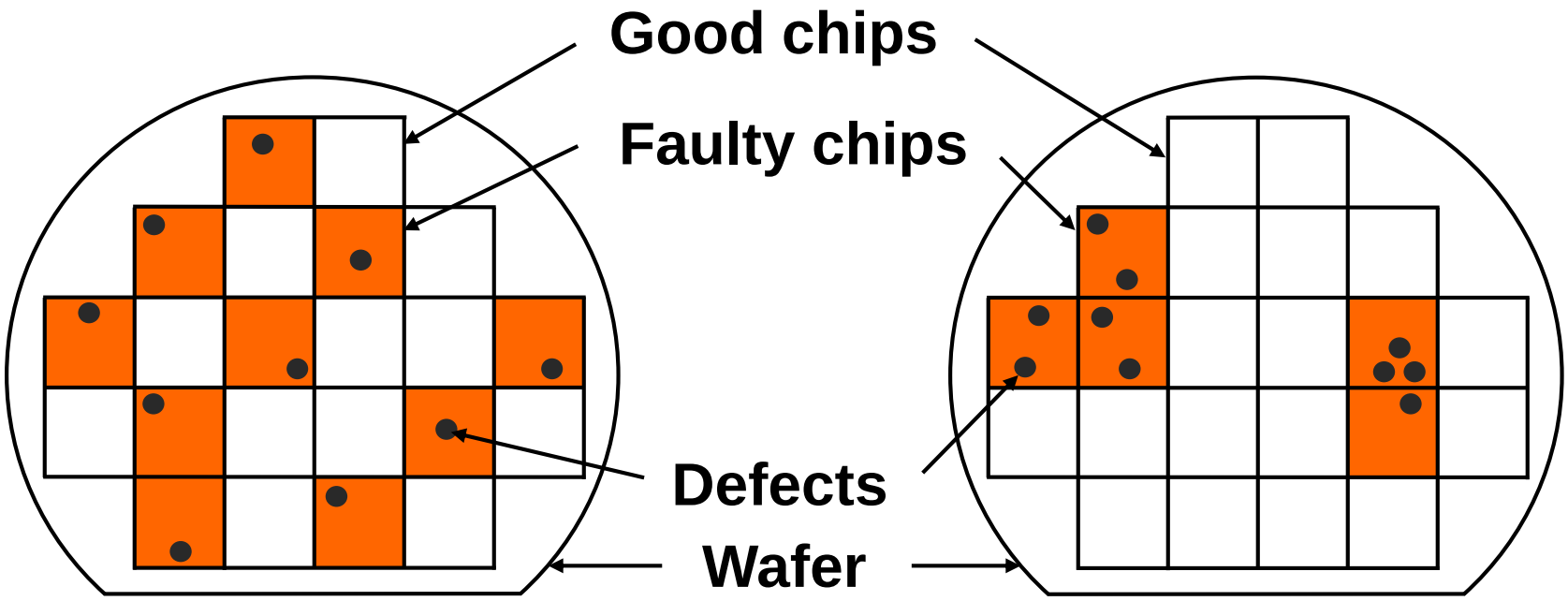
Yield

- A manufacturing defect is a finite chip area with electrically malfunctioning circuitry caused by errors in the fabrication process
- A chip with no manufacturing defect is called a good chip
- Fraction (or percentage) of good chips produced in a manufacturing process is called the yield.
- Yield is denoted by symbol **Y**

https://www.slideshare.net/rohitladdu/reliability-and-yield
https://www.slideshare.net/dilip2993/vlsi-testing

Design Rules…

Yield



Unclustered defects
Wafer yield = 12/22 = 0.55

Clustered defects (VLSI)
Wafer yield = 17/22 = 0.77

Design Rules…

- Two major approaches:
  - Micron rules: stated at absolute dimension (in micron).
  - λ rules: scalable design rules.

λ Based Design Rules

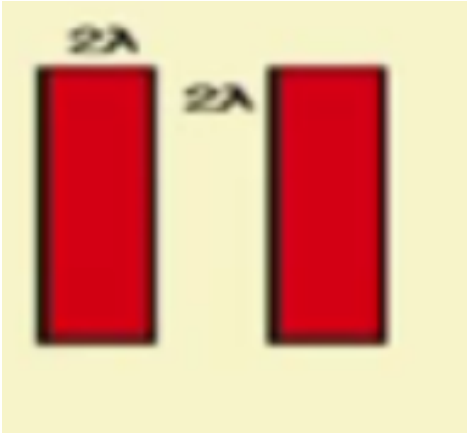
- Design rules based on single parameter, λ
- Provides a process and feature size-independent way of setting out mask dimensions to scale.
- If design rules are obeyed, masks will produce working circuits

*https://www.youtube.com/watch?v=OAxIm8up7QY

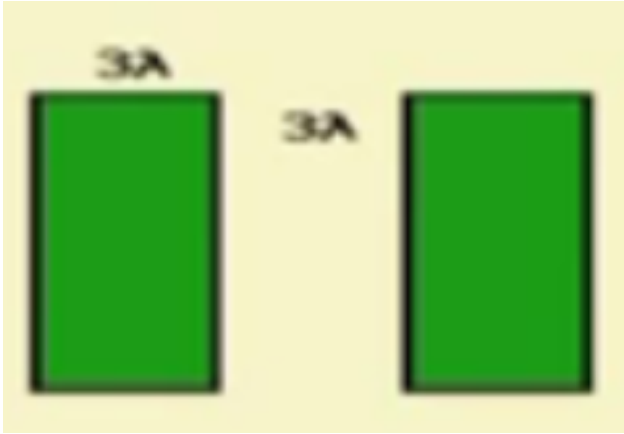
*https://ashwinjs.files.wordpress.com/2017/08/vlsi-unit-3.pdf

λ Based Design Rules…

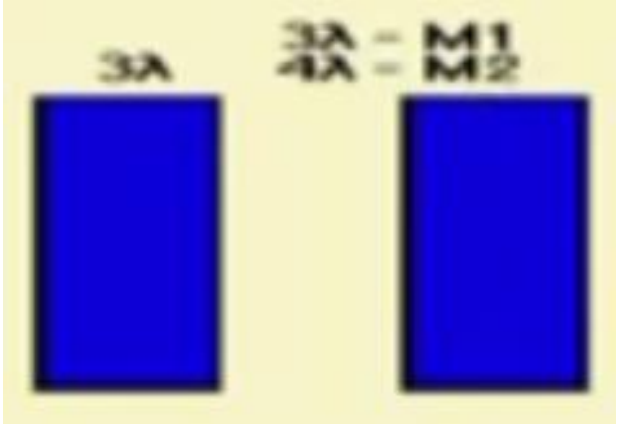
Polysilicon



Diffusion (Active)



Metal

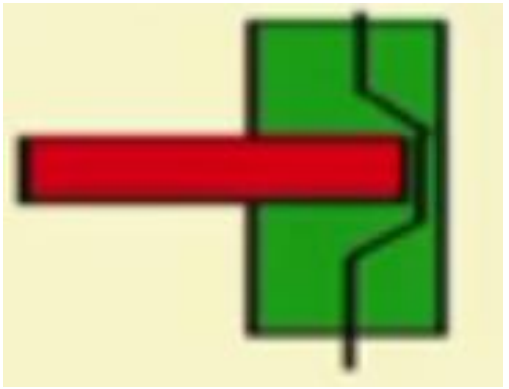


*https://www.youtube.com/watch?v=OAxIm8up7QY

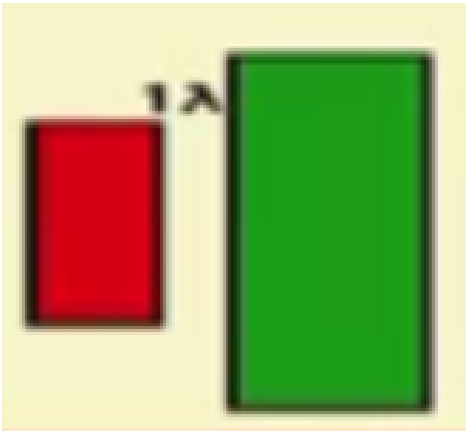
λ Based Design Rules…

Transistor

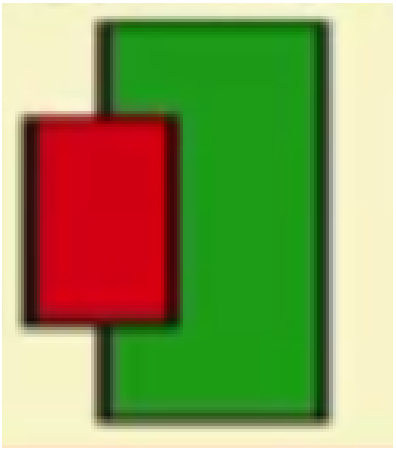
Catastrophic Error



Unrelated poly and diffusion (Poly-Active)



Thinner diffusion but still working



*https://www.youtube.com/watch?v=OAxIm8up7QY

λ Based Design Rules…

$\lambda = 1\mu m$

MINIMUM WIDTH AND SPACING RULES

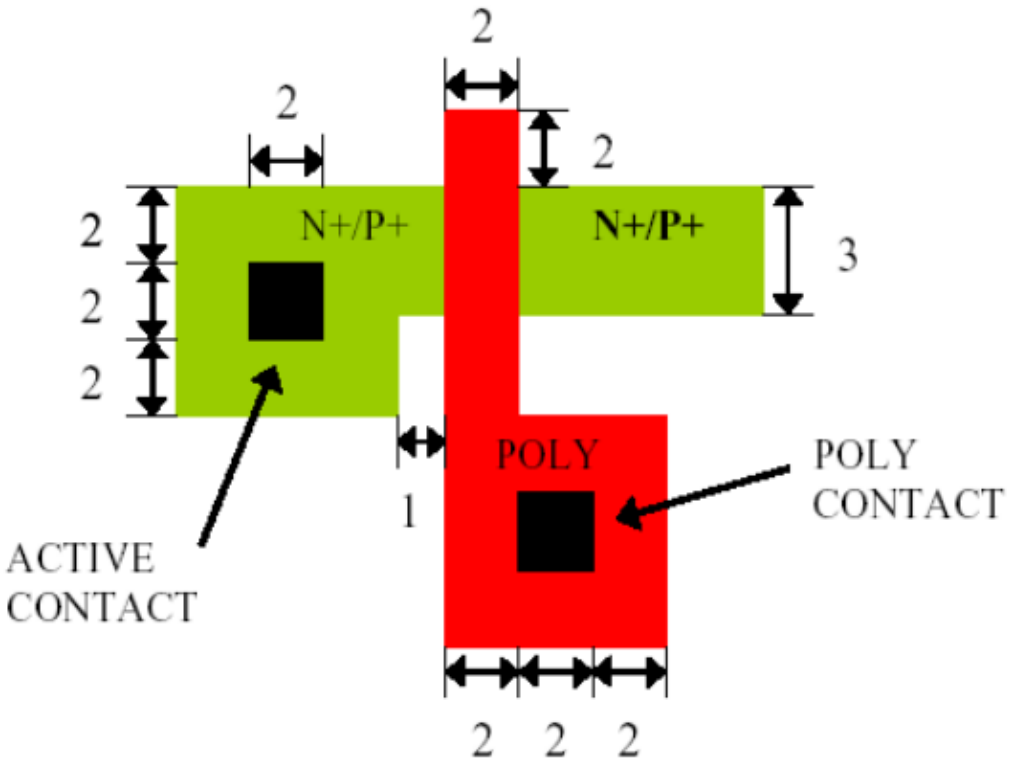
LAYER	TYPE OF RULE	VALUE
POLY	Minimum Width Minimum Spacing	2λ 2λ
ACTIVE	Minimum Width Minimum Spacing	3λ 3λ
~~NSELECT~~	Minimum Width Minimum Spacing	3λ 3λ
~~PSELECT~~	Minimum Width Minimum Spacing	3λ 3λ
METAL1	Minimum Width Minimum Spacing	3λ 3λ

*https://coefs.uncc.edu/amukherj/files/2012/04/design_rules.pdf

λ Based Design Rules…

MOSFET LAYOUT RULES

RULE	MEANING	VALUE
POLY Overlap	Minimum extension over ACTIVE	2λ
POLY-ACTIVE	Minimum Spacing	1λ
MOSFET Width	Minimum N+/P+ MOSFET W	3λ
ACTIVE CONTACT	Exact Size Minimum Space to ACTIVE Edge	2λ x 2λ 2λ
POLY CONTACT	Exact Size Minimum Space to POLY Edge	2λ x 2λ 2λ



*https://coefs.uncc.edu/amukherj/files/2012/04/design_rules.pdf

Micron Rules

- All minimum sizes and spacing specified in microns.
- Rules don't have to be multiples of λ.
- Can result in 50% reduction in area over λ based rules
- Standard in industry.

Read Details here:
https://www.electronics-tutorial.net/Digital-CMOS-Design/CMOS-Layout-Design/Micron-Design-Rules/

Notes

When we talk about lambda based layout design rules, there can in fact be more than one version. The layout rules change with each new technology and the fit between the lambda and micron rules can be better or worse, and this directly affects the scaling factor which is achievable.

Thank You