

82C55

Programmable Peripheral Interface

Interfacing Part III

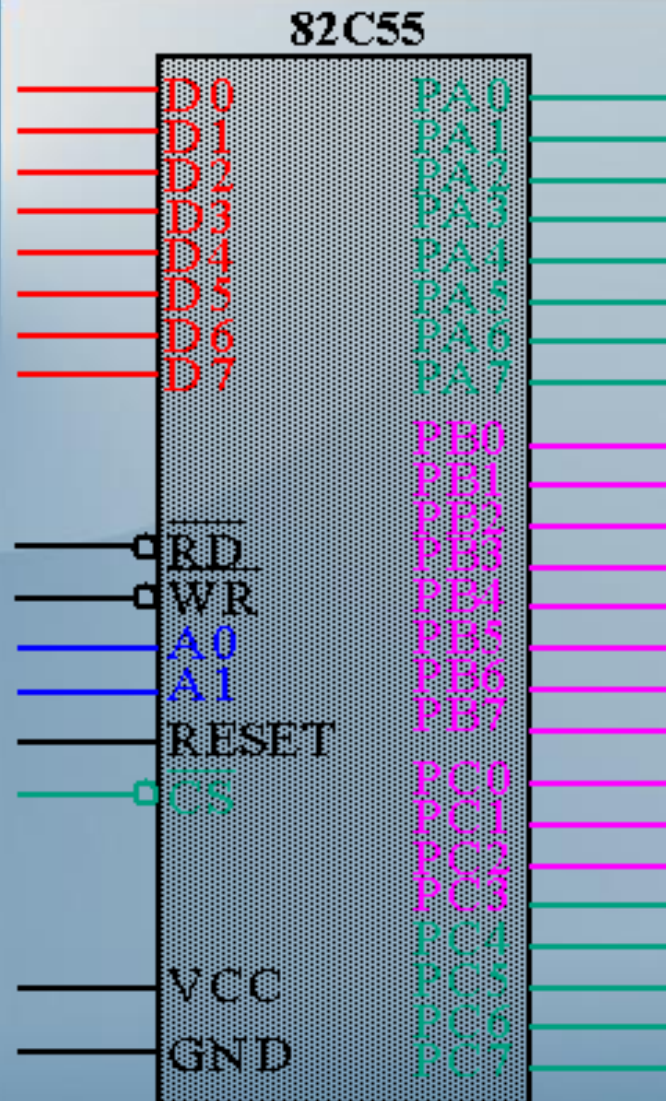
Review

- More on Address decoding
- Interface with memory
- Introduction to Programmable Peripheral Interface 82C55

About 82C55

- The 82C55 is a popular interfacing component, that can interface any TTL-compatible I/O device to a microprocessor.
- It is used to interface to the keyboard and a parallel printer port in PCs (usually as part of an integrated chipset).
- Requires insertion of wait states if used with a microprocessor using higher than an 8 MHz clock.
- PPI has 24 pins for I/O that are programmable in groups of 12 pins and has three distinct modes of operation.

82C55 : Pin Layout



Group A

Port A (PA7-PA0) and upper half of port C (PC7 - PC4)

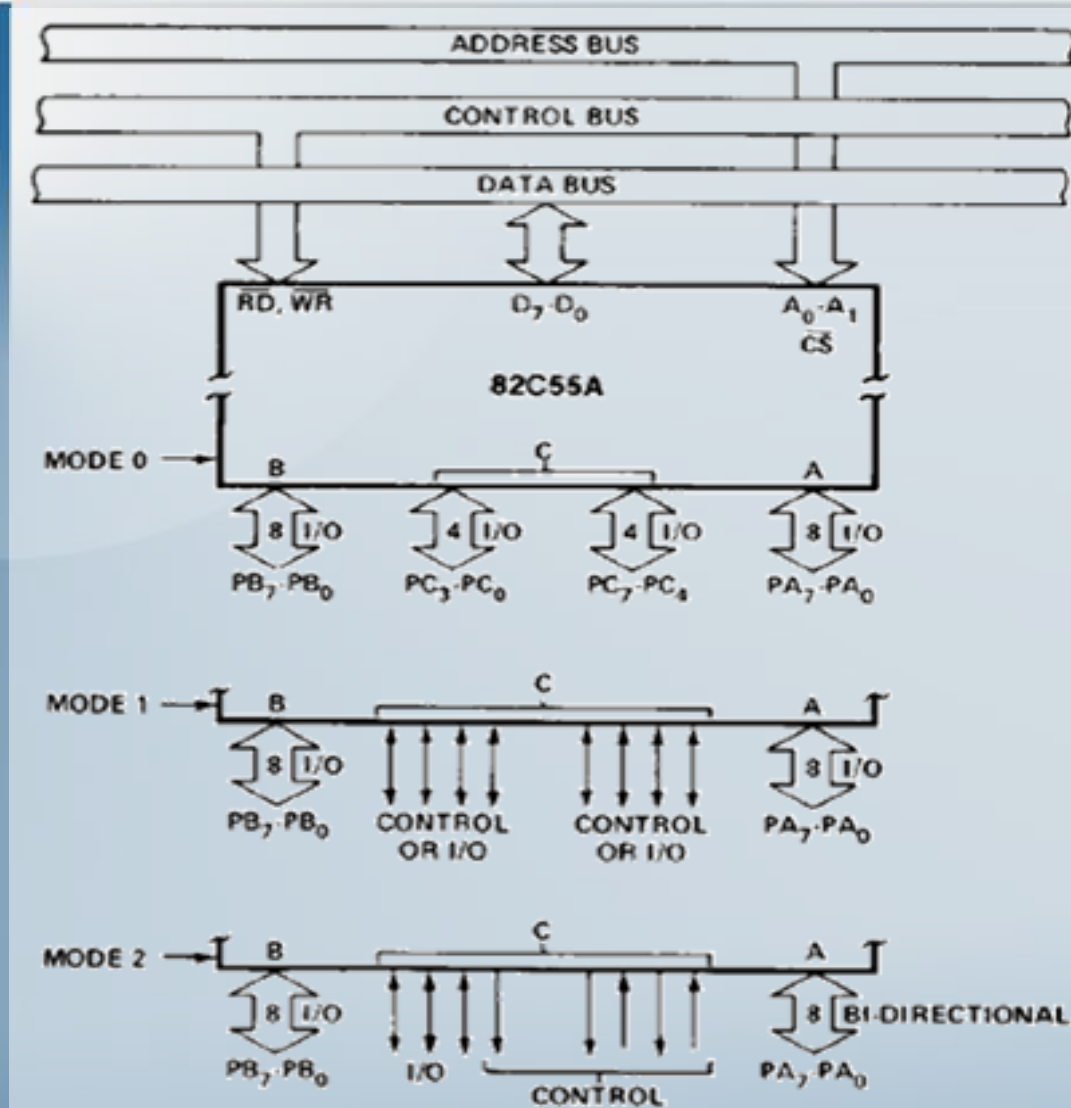
Group B

Port B (PB7-PB0) and lower half of port C (PC3 - PC0)

I/O Port Assignments

A ₁	A ₀	Function
0	0	Port A
0	1	Port B
1	0	Port C
1	1	Command Register

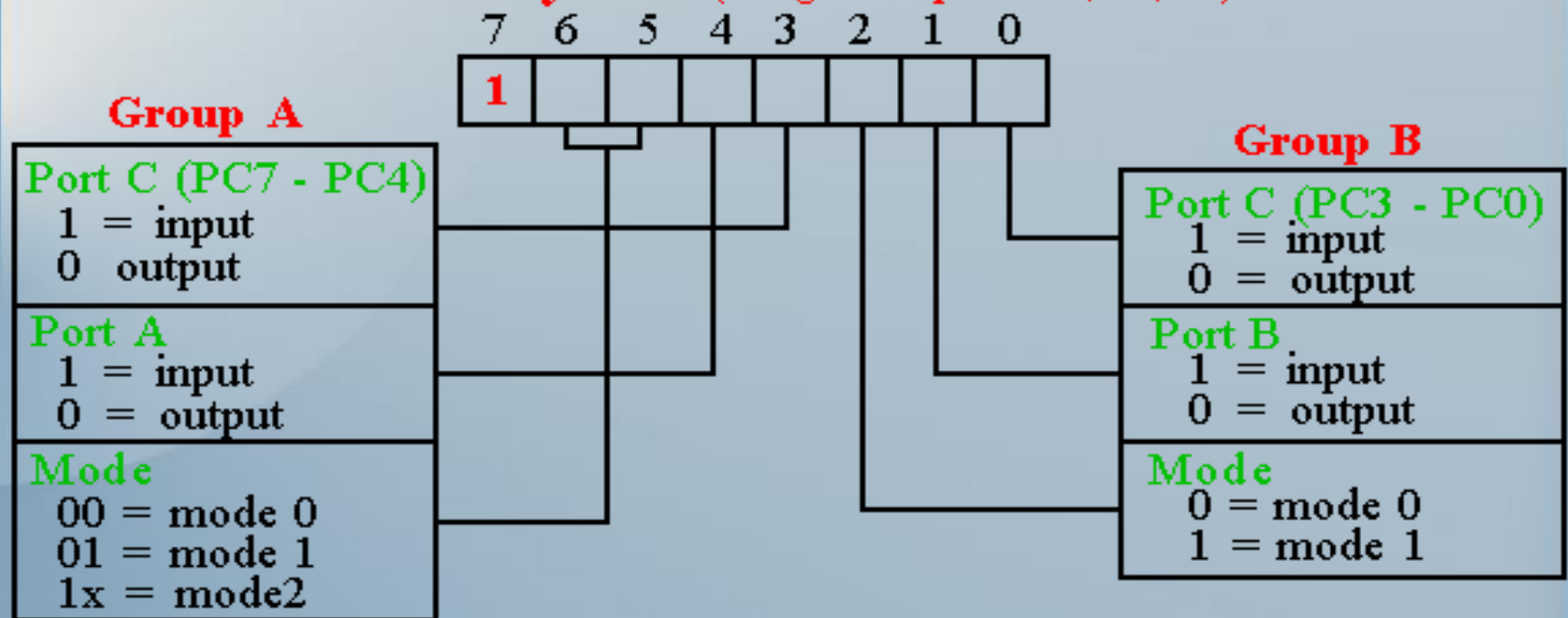
Basic Mode Definitions and Bus Int



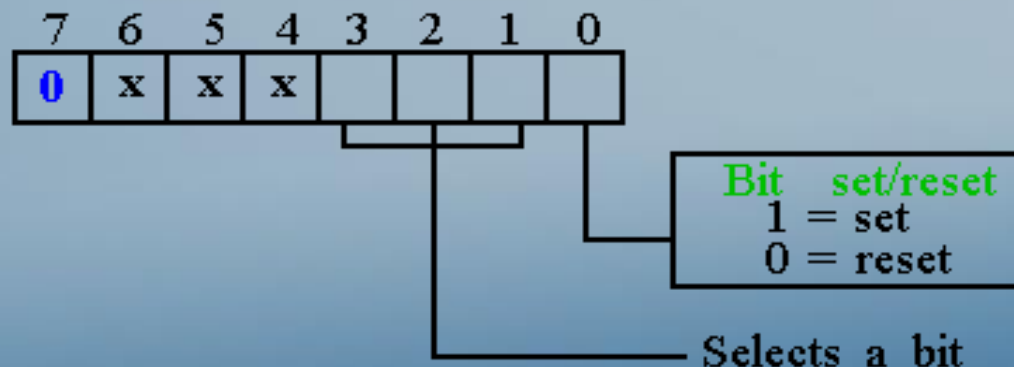
- Mode 0
 - Basic I/O
- Mode 1
 - Strobe I/O
- Mode 2
 - Bi-Dir Bus

Programming 82C55

Command Byte A (Programs ports A, B, C)



Command Byte B (Sets or resets any bits in port C)



Mode 0 (Basic Input/Output).

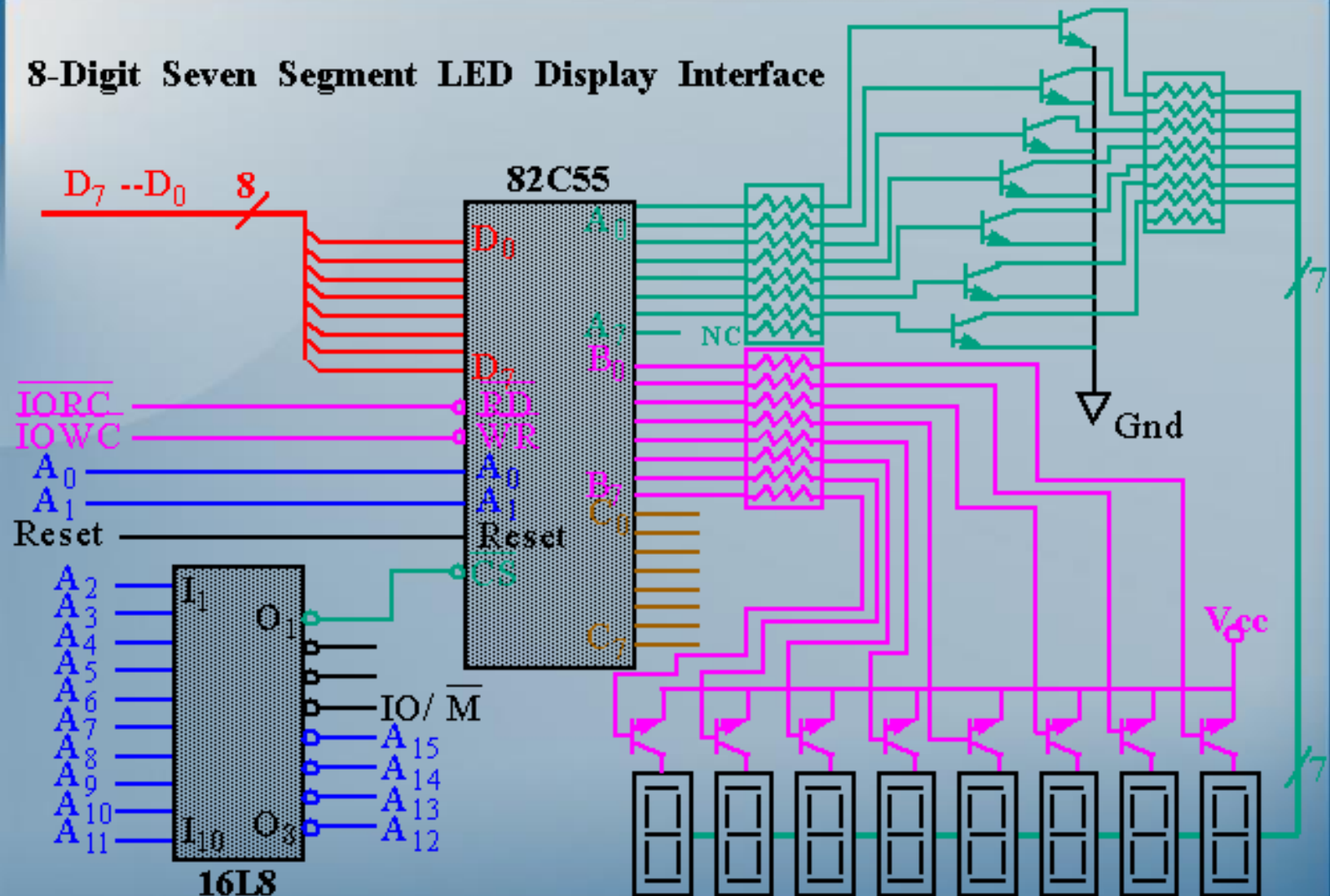
- This functional configuration provides simple input and output operations for each of the three ports.
- No “handshaking” is required, data is simply written to or read from a specified port.

Mode 0 Port definition

A		B		GROUP A			GROUP B	
D ₄	D ₃	D ₁	D ₀	PORT A	PORT C (UPPER)	#	PORT B	PORT C (LOWER)
0	0	0	0	OUTPUT	OUTPUT	0	OUTPUT	OUTPUT
0	0	0	1	OUTPUT	OUTPUT	1	OUTPUT	INPUT
0	0	1	0	OUTPUT	OUTPUT	2	INPUT	OUTPUT
0	0	1	1	OUTPUT	OUTPUT	3	INPUT	INPUT
0	1	0	0	OUTPUT	INPUT	4	OUTPUT	OUTPUT
0	1	0	1	OUTPUT	INPUT	5	OUTPUT	INPUT
0	1	1	0	OUTPUT	INPUT	6	INPUT	OUTPUT
0	1	1	1	OUTPUT	INPUT	7	INPUT	INPUT
1	0	0	0	INPUT	OUTPUT	8	OUTPUT	OUTPUT
1	0	0	1	INPUT	OUTPUT	9	OUTPUT	INPUT
1	0	1	0	INPUT	OUTPUT	10	INPUT	OUTPUT
1	0	1	1	INPUT	OUTPUT	11	INPUT	INPUT
1	1	0	0	INPUT	INPUT	12	OUTPUT	OUTPUT
1	1	0	1	INPUT	INPUT	13	OUTPUT	INPUT
1	1	1	0	INPUT	INPUT	14	INPUT	OUTPUT
1	1	1	1	INPUT	INPUT	15	INPUT	INPUT

82C55: Mode 0, Scan Display

8-Digit Seven Segment LED Display Interface

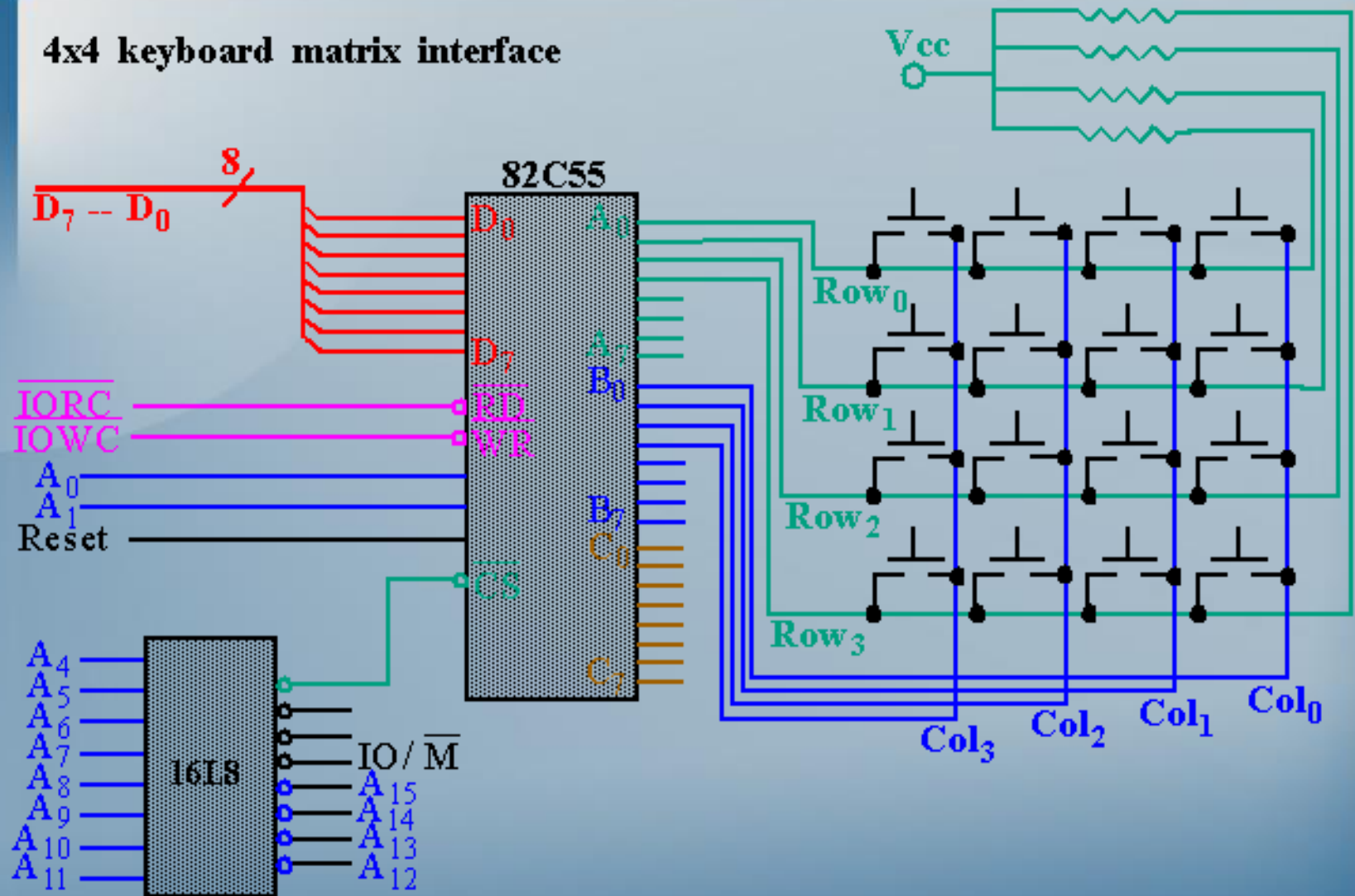


82C55: Mode 0, Scan Display

- Mode 0 operation causes the 82C55 to function as a buffered input device or as a latched output device.
- In previous example, both ports A and B are programmed as (mode 0) simple latched output ports.
- Port A provides the segment data inputs to display and port B provides a means of selecting one display position at a time.
- Different values are displayed in each digit via fast time multiplexing.

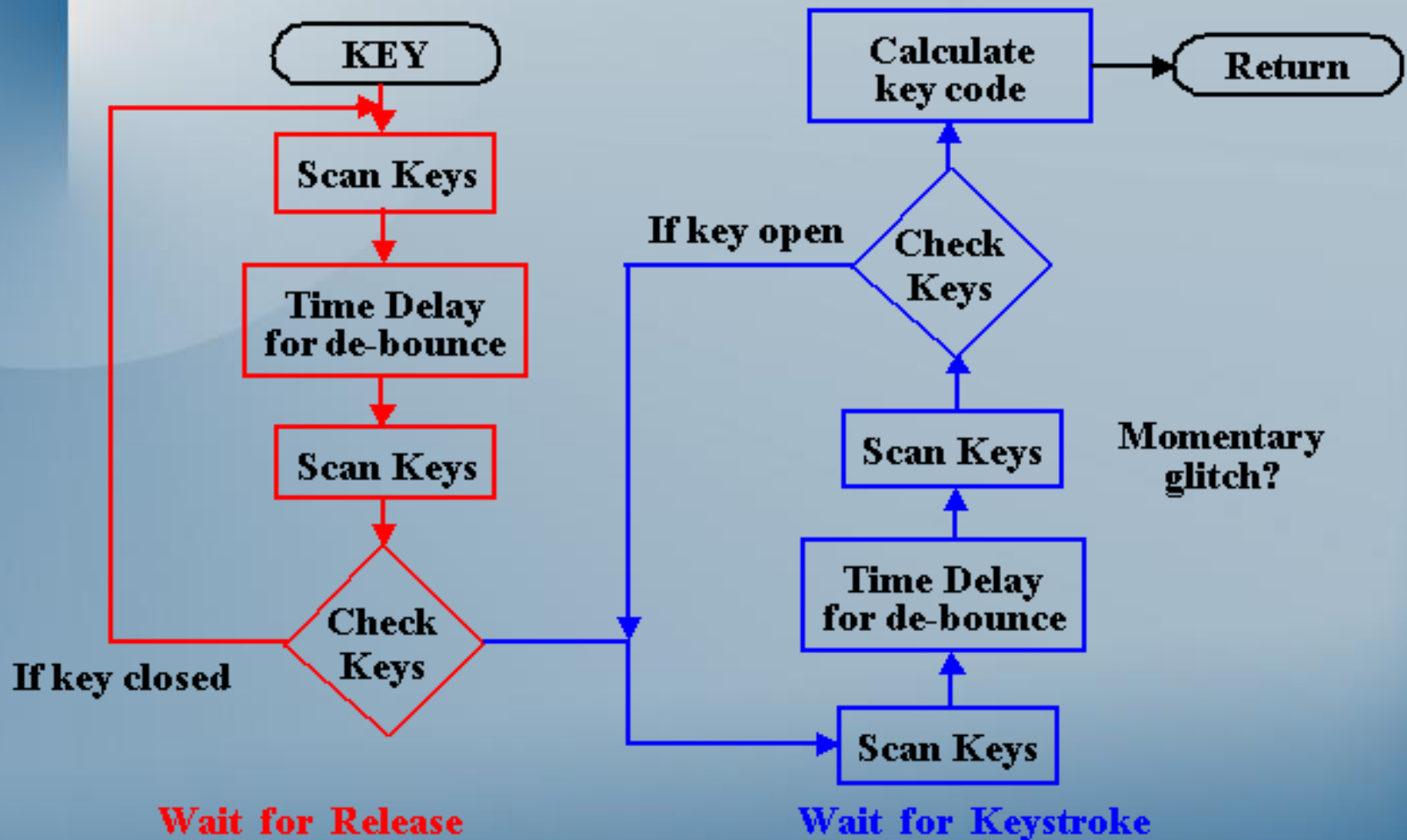
82C55: Mode 0, Scan Key

4x4 keyboard matrix interface



82C55: Mode 0 Operation

Flow chart of a keyboard-scanning procedure



MODE 1 (Strobed Input/Output)

- This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or “handshaking” signals.
- In mode 1, Port A and Port B use the lines on Port C to generate or accept these “handshaking” signals

Mode 1 Basic functional Definitions

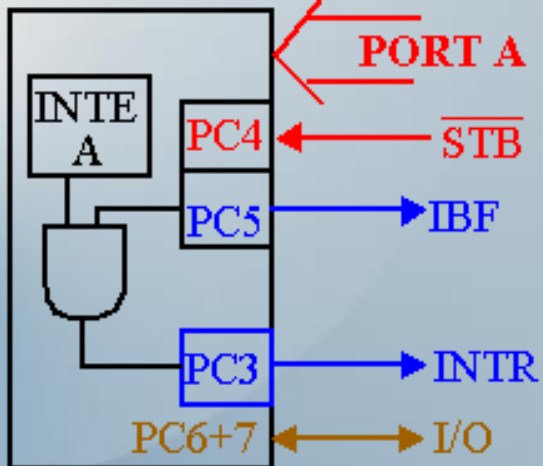
- Two Groups (Group A and Group B).
- Each group contains one 8-bit data port and one 4-bit control/data port.
- The 8-bit data port can be either input or output Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit data port.

82C55: Mode 1 Strobed Input

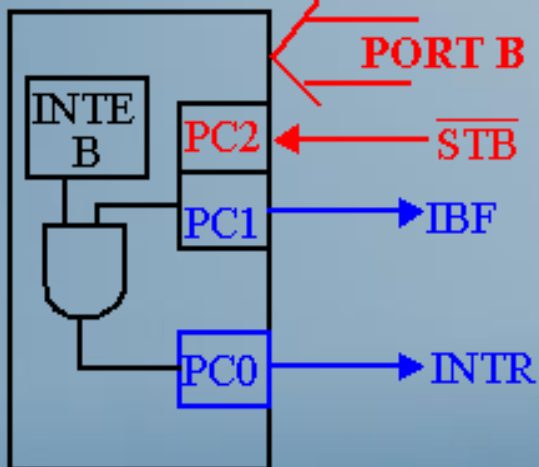
- **~STB** : The strobe input loads data into the port latch on a 0-to-1 transition.
- **IBF** : Input buffer full is an output indicating that the input latch contain information.
- **INTR** : Interrupt request is an output that requests an interrupts.
- **INTE** : The interrupt enable signal is neither an input nor an output; it is an internal bit programmed via the PC4 (port A) or PC2 (port B) bits.
- **PC7,PC6** : The port C pins 7 and 6 are general purpose I/O pins that are available for any purpose.

82C55: Mode 1 Strobed Input

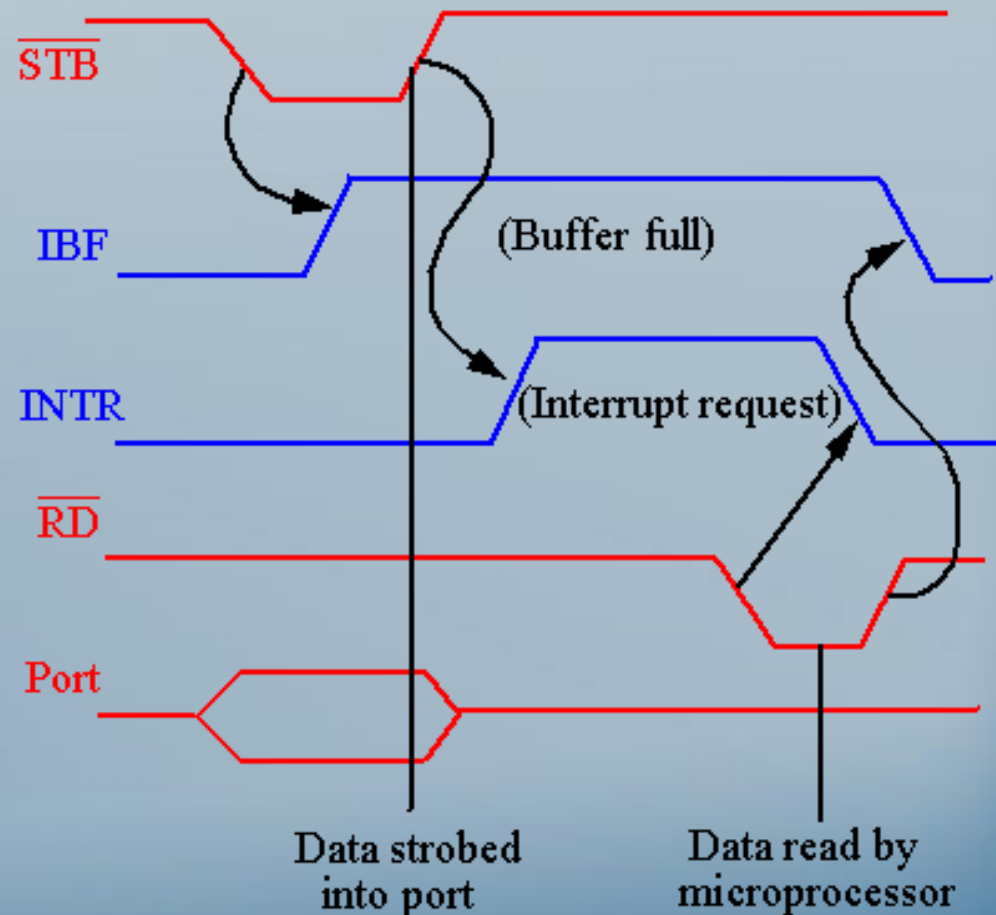
Mode 1 Port A



Mode 1 Port B



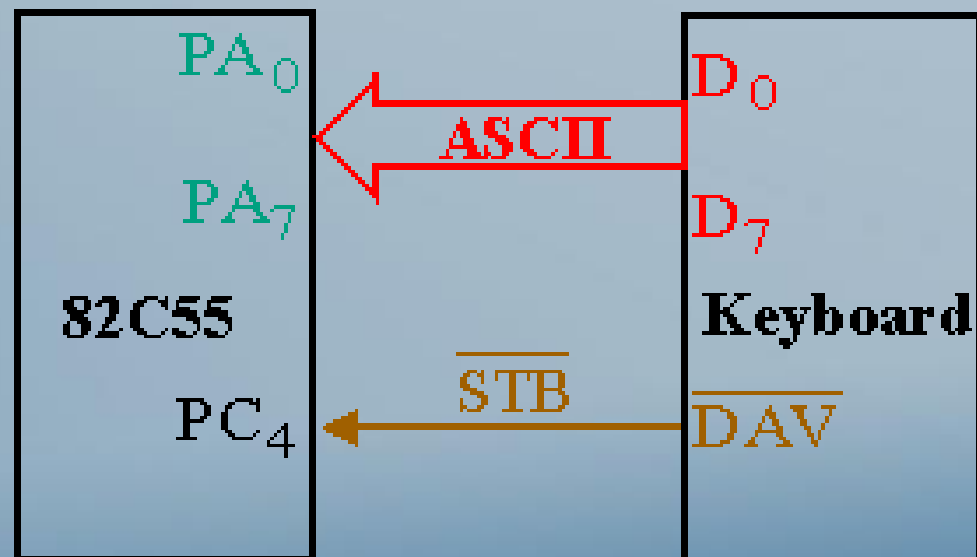
Timing Diagram



Signal definitions for Mode 1 Strobe Input

82C55: Mode 1 Input Exam.

- Keyboard encoder debounces the key-switches, and provides a strobe whenever a key is depressed.
- DAV is activated on a key press strobing the ASCII-coded key code into Port A.

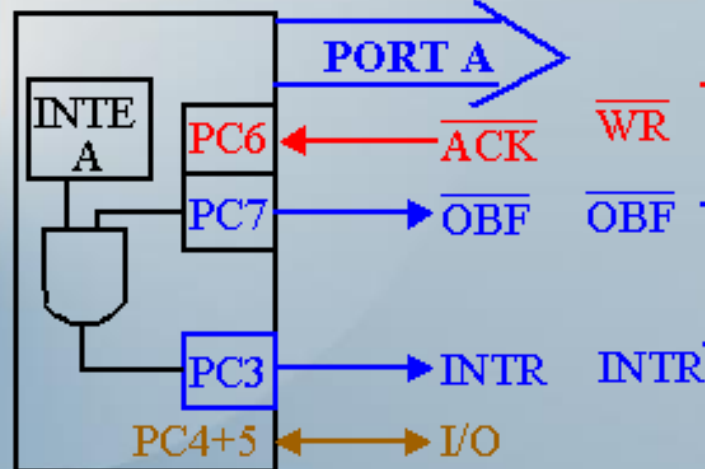


82C55 : Mode 1 Output Exam.

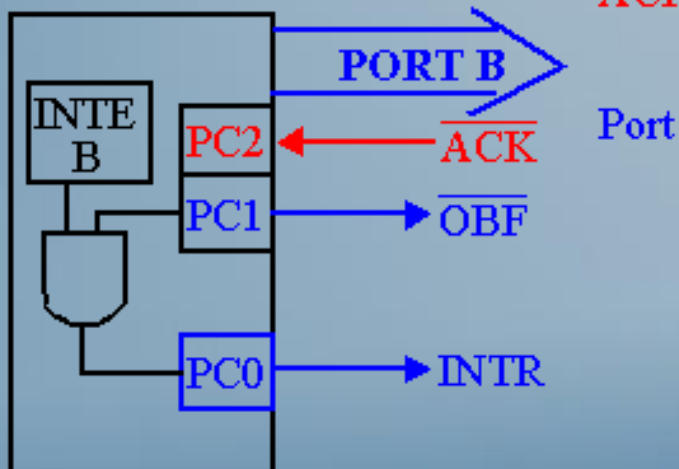
- **~OBF** : Output buffer full is an output that goes low when data is latched in either port A or port B. Goes low on ~ACK.
- **~ACK** : The acknowledge signal causes the ~OBF pin return to 0. This is a response from an external device.
- **INTR** : Interrupt request is an output that requests an interrupt.
- **INTE** : The interrupt enable signal is neither an input nor an output; it is an internal bit programmed via the PC6(Port A) or PC2(port B) bits.
- **PC5,PC4** : The port C pins 5 and 4 are general-purpose I/O pins that are available for any purpose.

82C55 : Mode 1 Output Exam.

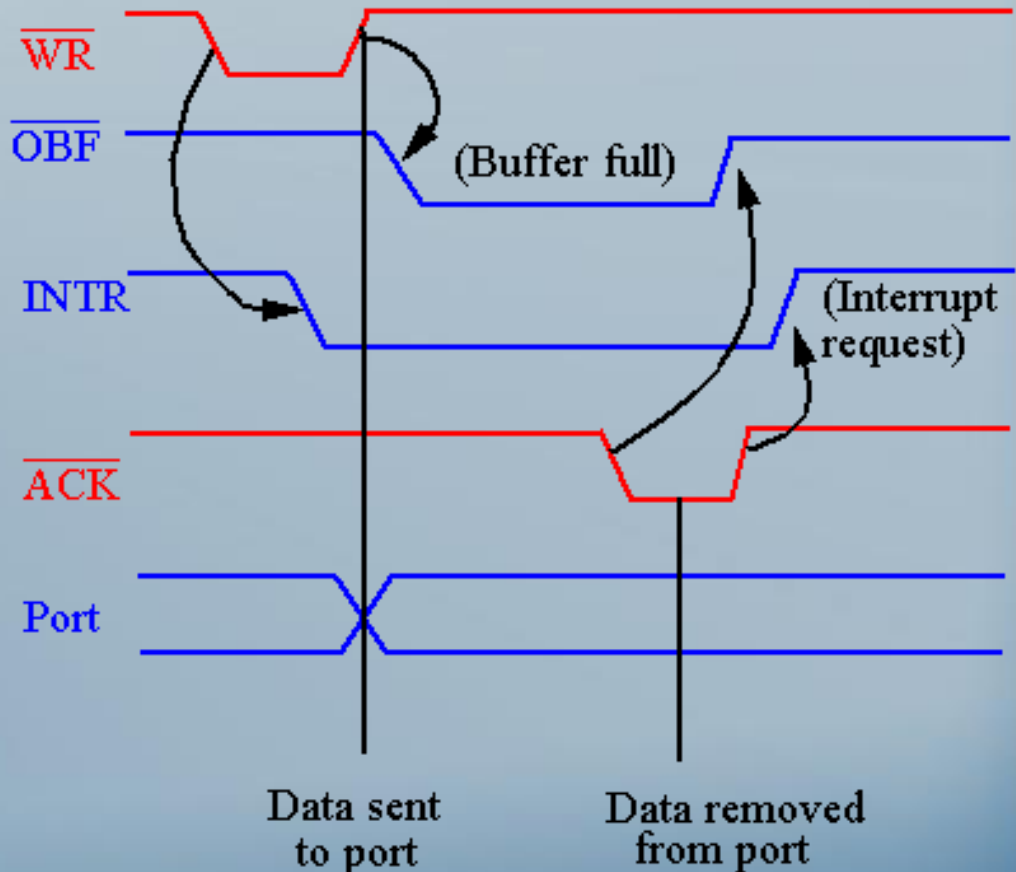
Mode 1 Port A



Mode 1 Port B



Timing Diagram



82C55: Mode 2 Bi-directional Operation

- This functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bidirectional bus I/O).
- “Handshaking” signals are provided to maintain proper bus flow discipline in a similar manner to MODE 1.
- Interrupt generation and enable/disable functions are also available.

MODE 2 Basic Functional Definitions:

- Used in Group A only.
- One 8-bit, bi-directional bus port (Port A) and a 5-bit control port (Port C).
- Both inputs and outputs are latched.
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A).

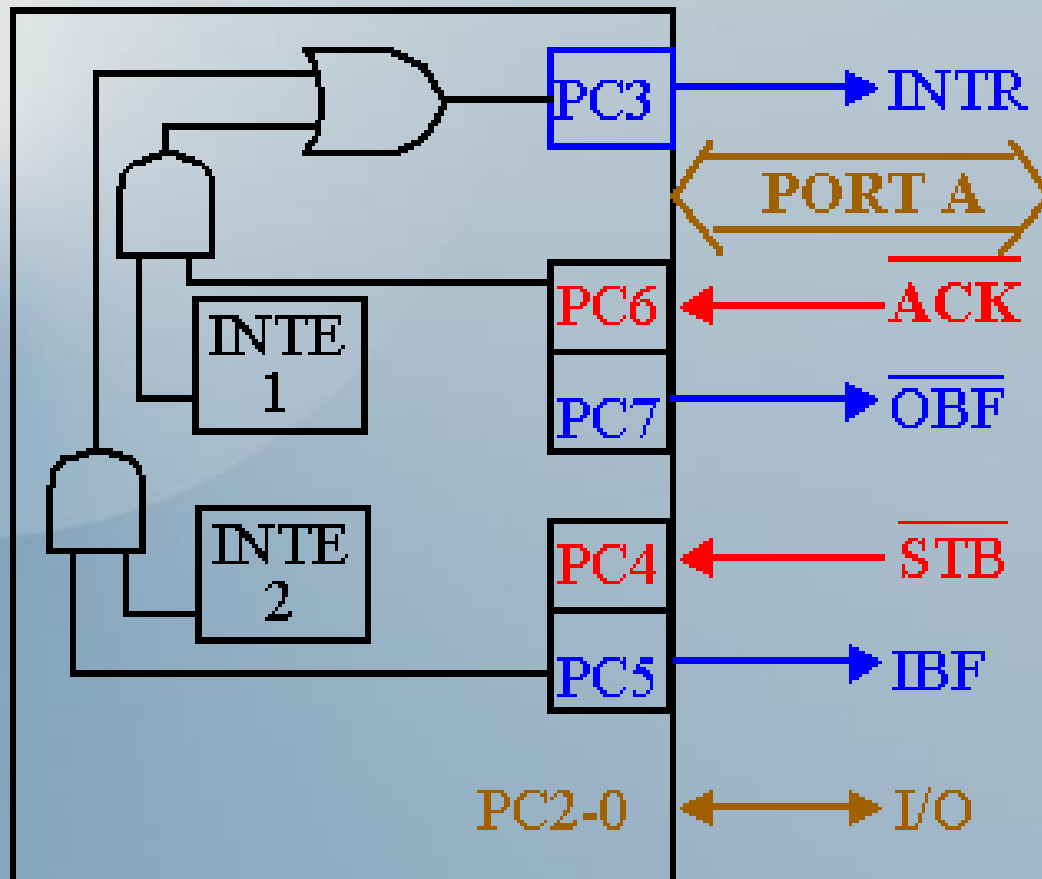
82C55: Mode 2 Bi-directional Operation

- **INTR** : Interrupt request is an output that requests an interrupt.
- **~OBF** : Output Buffer Full is an output indicating that that output buffer contains data for the bi-directional bus.
- **~ACK** : Acknowledge is an input that enables tri-state buffers which are otherwise in their high-impedance state.
- **~STB** : The strobe input loads data into the port A latch.

82C55: Mode 2 Bi-directional Operation

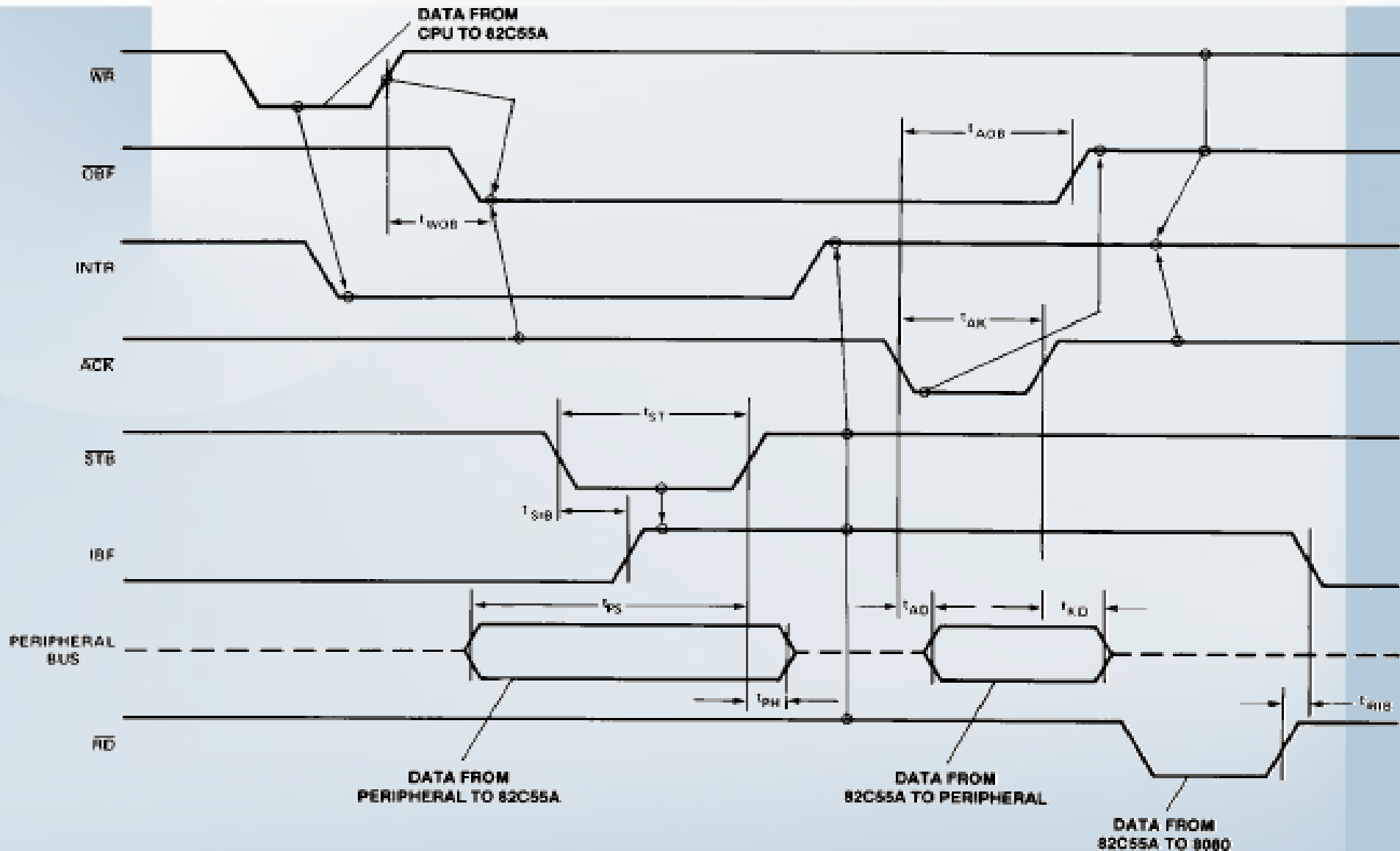
- **IBF** : Input buffer full is an output indicating that the input latch contains information for the external bi-directional bus.
- **INTE** : Interrupt enable are internal bits that enable the INTR pin. BIT PC6(INTE1) and PC4(INTE2).
- **PC2,PC1,PC0** : These port C pins are general-purpose I/O pins that are available for any purpose.

82C55: Mode 2 Bi-directional Operation



- Timing diagram is a combination of the Mode 1 Strobed Input and Mode 1 Strobed Output Timing diagrams.

Mode 2 Timing Diagram



Mode definition summary

	MODE 0			MODE 1			MODE 2		
	IN	OUT		IN	OUT		GROUP A ONLY		
PA ₀	IN	OUT		IN	OUT		↔	MODE 0 OR MODE 1 ONLY	
PA ₁	IN	OUT		IN	OUT		↔		
PA ₂	IN	OUT		IN	OUT		↔		
PA ₃	IN	OUT		IN	OUT		↔		
PA ₄	IN	OUT		IN	OUT		↔		
PA ₅	IN	OUT		IN	OUT		↔		
PA ₆	IN	OUT		IN	OUT		↔		
PA ₇	IN	OUT		IN	OUT		↔		
PB ₀	IN	OUT		IN	OUT		—	MODE 0 OR MODE 1 ONLY	
PB ₁	IN	OUT		IN	OUT		—		
PB ₂	IN	OUT		IN	OUT		—		
PB ₃	IN	OUT		IN	OUT		—		
PB ₄	IN	OUT		IN	OUT		—		
PB ₅	IN	OUT		IN	OUT		—		
PB ₆	IN	OUT		IN	OUT		—		
PB ₇	IN	OUT		IN	OUT		—		
PC ₀	IN	OUT		INTR _B	INTR _B		I/O	MODE 0 OR MODE 1 ONLY	
PC ₁	IN	OUT		IBF _B	$\overline{\text{OBF}}_{\text{B}}$		I/O		
PC ₂	IN	OUT		$\overline{\text{STB}}_{\text{B}}$	$\overline{\text{ACK}}_{\text{B}}$		I/O		
PC ₃	IN	OUT		INTR _A	INTR _A		INTR _A		
PC ₄	IN	OUT		$\overline{\text{STB}}_{\text{A}}$	I/O		$\overline{\text{STB}}_{\text{A}}$		
PC ₅	IN	OUT		IBF _A	I/O		IBF _A		
PC ₆	IN	OUT		I/O	$\overline{\text{ACK}}_{\text{A}}$		$\overline{\text{ACK}}_{\text{A}}$		
PC ₇	IN	OUT		I/O	$\overline{\text{OBF}}_{\text{A}}$		$\overline{\text{OBF}}_{\text{A}}$		

More on interface, next time.