Heaven's Light is our Guide

Rajshahi University of Engineering & Technology
B.Sc. Engineering 3rd Year 6th Semester Examination, 2015
Department of Computer Science & Engineering
Course No. CSE 603 Course Title: Computer Architecture
Full Marks: 70 Time: THREE (03) hours

N.B:

Answer SIX questions taking THREE from each section.
The questions are of equal value.
Use separate answer script for each section

SECTION A

		Marks
Q.1(a)	What do you mean by the followings: (i) Computer Architecture (ii) Computer Organization.	03
(b)	Define (i) Multiprocessor Organization (ii) Cluster Computing (iii) VGA port and (iv) HDMI port.	06
(c)	Explain the importance of a cache memory in Computer Architecture.	02⅔
Q.2(a)	How does an ALU work? Discuss Booth's algorithm with necessary example.	04
(b)	Define (i) 1's compliment and (ii) 2's compliment for data processing.	02
(c)	Discuss the problem of sign magnitude representation of any number.	02
(d)	With necessary diagram, describe hardware implementation of unsigned binary multiplication.	03⅔
Q.3(a)	Draw the CPU structure and hence describe the functions of it in brief.	05⅔
(b)	What do you mean by instruction cycle? With neat sketch, describe the fetch, execute and interrupt cycles.	06
Q.4(a)	What do you mean instruction pipelining? Write the advantages and disadvantages of it.	03⅔
(b)	What are the differences between instruction level parallelism (ILP) and parallel processing?	03
(c)	Write down the necessary examples which show the advantages of ILP execution over sequential execution.	03
(d)	What are the ILP challenges to achieve parallelism?	02

SECTION B

Q.5(a)	Describe the different addressing modes with at least one example for each.	05⅔
(b)	Briefly discuss the followings: (i) Von Neumann Architecture and (ii) Flynn's Classical Taxonomy.	06
Q.6(a)	Describe briefly (i) SISD (ii) SIMD (iii) MISD and (iv) MIMD.	06
(b)	Briefly describe the functions of the main components of a computer system.	05⅔
Q.7(a)	What are the advantages of symmetric multiprocessor architecture over uni-processor architecture?	04
(b)	Write down the characteristics of Reduced Instruction Set Architecture.	04
(c)	How pipelining is used to enhance performance in the context of a RISC architecture?	03⅔
Q.8(a)	What is effective address? Consider the instruction MOV ALPHA [SI][BX], CL. If [BX] = 0200H, ALPHA = 08H, [SI] = 1000H and [DS] = 3000H. Then calculate the effective address where the content of CL will move in based Indexed addressing mode.	03⅔
(b)	Briefly explain (i) Big-Endian and (ii) Little-Endian representation.	04
(c)	Justify your answer for the statement "RISC is better than CISC or vice versa".	04

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Rajshahi University of Engineering & Technology

B.Sc. Engineering 3rd Year 6th Semester Examination, 2011

Department of Computer Science & Engineering

Course no: **CSE 603** Course Title: **Computer Architecture**

Full marks: 70 Time: Three (03) hours

N.B. Answer **six** questions, taking **three** from each section.
The questions are of equal value.
Use separate answer script for each section.

SECTION-A

Q1. (a) Draw the high performance architecture of bus configuration. 04

(b) In the high performance architecture of bus configuration why the main memory is moved off of the local bus & placed onto a system bus? $3\frac{2}{3}$

(c) What technology is used to design power PC processors? List out four features of this technology. $2\frac{2}{3}$

Q2. (a) What is the main problem of Daisy Chaining Approach? Discuss it with proper figure. 05

(b) What are the key tasks for pnp automates? 04

(c) Draw the figure of PCI bus in desktop system. $2\frac{2}{3}$

Q3 (a) Draw a flow chart for cache read operation. 04

(b) Draw the block diagram PCI configuration in a typical multiprocessor system. 04

(c) Since processor's I/O capability is different from the speed of the PCI bus how they can be coupled together? $3\frac{2}{3}$

Q4. (a) What is address number? Represent the following equation by one and two address number $Z=(A/B)/(C*D-E)$ 06

(b) Consider that five instructions to execute I_1, I_2, I_3, I_4 and I_5 and each has 4 steps *(F, D, E, W)*. Each part has *1.5* clock cycles to execute. Compare the performance of *(i)* pipelining (ii) super pipelining (iii) scalar pipelining. $5\frac{2}{3}$

SECTION-B

Q5. (a) Choose which techniques (SISD, SIMD, MISD and MIMD) used for designing the followings and why? (i) uniprocessor (ii) vector processor (iii) Array processor (iv) systolic array. 06

(b) Draw the block diagram of a digital computer. 03

(c) Describe the Von Neuman architecture. $2\frac{2}{3}$

Q6. (a) Draw the memory organization of *512KB×1* dynamic memory chip. 04

(b) In control unit organization, what are the functions of control step counter, status flags & condition code? $3\frac{2}{3}$

(c) What is meant by microprogramming language, microinstruction and microprogram? 04

Q7. (a) Explain microroutine and microinstruction with example. 04

(b) Draw the block diagram of microprogrammed control unit that allows conditional branching. 04

(c) Explain indirect addressing. 02

(d) What is byte addressability? $1\frac{2}{3}$

Q8. (a) What is RAID? Describe its key concepts. $3\frac{2}{3}$

(b) What are the problems of RAID. 02

(c) Describe which RAID level is selected and why for the following conditions. 06

(i) When you want to transfer data parallelly by saving their parity.

(ii) When you want to save the parity of the datas in distributed location.

(iii) When you want to avoid double disk failure.

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"Heaven's light is our guide"

Rajshahi University of Engineering & Technology
B.Sc. Engineering 3rd Year 6th Semester Examination, 2010
Department of Computer Science & Engineering
Course no: CSE 603 Course Title: Computer Architecture
Full marks: 70 Time: Three (03) hours

N.B. Answer **six** questions, taking **three** from each section
The questions are of equal value
Use separate answer script for each section.

SECTION-A

Q1. (a) Draw and explain internal connection between processor and memory. 02

(b) What is address number? Show the execution of the instruction, Y=(A+B-C)/(D+E) by using one address instruction $4\frac{2}{3}$

(c) Explain the Von Neumann Architecture 03

(d) Criticize the following statement "using a faster processor chip results in a corresponding increase in performance of a computer even if the main memory speed remains the same" 02

Q2. (a) Distinguish between RISC and CISC. $2\frac{2}{3}$

(b) Draw the timing diagram of a Read operation. 03

(c) Write the control steps sequence for the single bus structure for the following instruction 04
ADD (R3), R1

(d) Why the MFC signal is needed when reading from or writing to the main memory? 02

Q3. (a) Briefly describe MAR, MDR, PC and IR with figure. 05

(b) A disk unit has 12000 tracks. Tracks are divided into 800 sectors and each sectors contains 512 bytes of data. If the diameter of the inner cylinder is 2 inches and outer cylinder is 5 inches then calculate $4\frac{2}{3}$
I. Total capacity of the disk
II. maximum bit density
III. Format of disk address word

(c) What is meant by instruction level parallelisms? 02

Q4. (a) Write down the pros and cons of micro-programmed control unit over hardware control unit. 03

(b) Given a 32×8 ROM chip with an enable input, show the external connections necessary to construct a 128×8 ROM with four chips and a decoder. $5\frac{2}{3}$

(c) What is the purpose of buffer gate in the clock input of a register? 03

SECTION-B

Q5. (a) What is meant by "data path unit" and "control unit" of a digital system? 04

(b) Draw the model of control unit and states its various inputs. $3\frac{2}{3}$

(c) Discuss the incremental processor organization. 02

Q6. (a) Briefly explain i) Big-endian and ii) Little-endian storage schemes. 02

(b) What are the differences between EPROM and FLASH memory? $4\frac{2}{3}$

(c) Write the characteristics of some common memory technologies such as magnetic disk, compact disk ROM, metal oxide semiconductor with respect to primary storage medium, access mode and performance. 03

(d) In control unit organization, what are the functions of control step counter, status Flag and Condition code? $3\frac{2}{3}$

Q7. (a) Discuss the data flow of different instruction cycles with neat sketch. 03

(b) What are the important advantages of PowerPC processor in comparison to Pentium processor? 03

(c) What are the advantages of cache memory over main memory? 02

(d) Explain the two-channel DMA controller with necessary figure. 03

Q8. (a) What is meant by fetch phase and execution phase? What will be happened inside the CPU after execution of an instruction? 03

(b) Discuss about the different ways of implementing a multiprocessor system. $5\frac{2}{3}$

(c) Consider 4 instructions to execute (I_1, I_2, I_3, I_4) and each instruction has 4 parts (F, D, O, W). Assuming each part takes 2 clock cycle to execute; compare the performance of
I. Pipeling
II. Super-pipeling
III. Super-scaler approach

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Heaven's Light is our Guide

Rajshahi University of Engineering and Technology

B. Sc. Engineering 3rd Year 6th Semester Examination 2012

Department of Computer Science and Engineering

Course No. CSE 603 Course Title: Computer Architecture

Full Marks: 70 Time: THREE (03) hours

Answer **SIX** questions taking **THREE** from each section

The questions are of equal value.

Use separate answer script for each section

SECTION A

		Marks
Q1(a)	Criticize the following statement "Using a faster processor chip results in a corresponding increase in performance of a computer, even if the main memory speed remains the same"	02½
(b)	With figure briefly describe MAR, MDR, PC and IR.	04
(c)	What is meant by fetch phase and execution phase? What happens inside the CPU after execution of an instruction? Explain briefly.	05
Q2	Suppose you are a server administrator you have to implement RAID technology in your server. RAID creates computer data storage schema that divides and/or replicate data among multiple computer hard drives.	
	(a) What is RAID? Describe the problems of RAID.	02½
	(b) Are RAID level 0,4 and 0+1 true? Justify in favour your answer.	05
	(c) Which RAID level should be implemented for the following conditions—	0.5
	i). Required minimum of two disk ii) Mirroring concept and iii) One write or two reads are possible at the same time.	
Q3(a)	From the following pin configuration design a memory chip. Total no. of pins: 14 and Output pins : 03	04
(b)	Design a ROM chip which can be rewritten many times but not more than 9000 times and it can not be changed/erased data from a specific point and need 13V to change it current state.	05
(c)	Draw the block diagram of a digital computer.	02½
Q4(a)	Explain DMA operation during I/O.	02½
(b)	Consider 6 instructions to execute (I_1, I_2, I_3, I_4, I_5, and I_6) and each one has 4 parts (F, D, O, and W) Assuming each part takes 2 clock cycle to execute and there are intermediate storage buffers after each stage and the delay of each buffer is 0 clock cycle; compare the performance of—	06
	i). Non-pipelining architecture	
	ii). Pipelining architecture and	
	iii). Supper-pipelining architecture.	
(c)	Show the execution process of the instruction, $Y = (A - B)/(C + D * E)$ using two address instruction	03

SECTION B

Q5(a) Analyze the data dependencies among the following statements:

$S1: Load \quad R1, 1024$

$S2: Load \quad R2, M(10)$

$S3: Add \quad R1, R2$

$S4: Store \quad M(1024), R1$

$S5: Store \quad M((R2)), 10$ 4

Answer the following questions:

i). Draw a dependency graph to show all the dependencies. 03

ii). Are there any resource dependencies if only one copy of each functional unit is available in the CPU? 04

(b) Sketch a suitable bus architecture for the following arrangements: 04½

Available devices: Processor, Memory, Faster devices, Slower devices

Available buses : local buses, high-speed bus, expansion bus.

Q6(a) A memory location contains the pattern 00101100. What does this pattern represent when interpreted as a binary number? What does it represent as an ASCII code? 03½

(b) Write a program that can evaluate the expression $A * B + C * D$ in a single accumulator processor. Assume that the processor has *Load, Store, Multiply* and *Add* instruction, and that all values fit in the accumulator. 04

(c) Design main memory arrangement for the following program: 04

```
        Move N, R1
        Move # Num, R1
        Clear R0
Loop    Add (R2), R0
        Increment R2
        Decrement R1
        Branch > 0   Loop
```

Q7(a) Draw an input interface circuit connecting a keyboard to an asynchronous bus. 03

(b) Briefly explain with necessary figure the two-channel DMA controller. 03

(c) What is meant by control signals? Draw the model of the control unit and discuss its different inputs and outputs 03

(d) Prove that the multiplication of two n-digit numbers in base B gives a product of no more than $2n$ digits 02½

Q8(a) Describe the optical and magnetic read/write mechanism with necessary diagram 03

(b) Define micro operations. Write down the sequence of events of different instruction cycle 03

(c) Describe the internal processor organization with necessary data paths and control singles. 03

(d) What is meant by I/O interface? Discuss different parts of I/O interface for an input device. 02½

Rajshahi University of Engineering & Technology
B.Sc. Engineering 2nd year 1st Semester Examination 2013
Department of Computer Science & Engineering
Course no: CSE 603 Course Title: Computer Architecture
Full marks: 70 Time: Three (3) hours

N.B. Answer **six** questions, taking three from each section.
The questions are of equal value.
Use separate answer script for each section.

SECTION-A

Q1. (a) Define pipeline processing. 2
(b) Write in detail about various addressing modes. 4
(c) List the steps involved in the instruction execution. 3
(d) What is the need for reduced instruction chip. 2

Q2. (a) What are the difference between the hardwired control organization and micro programmed control organization. 3
(b) What are the differences between main memory and virtual memory? 2
(c) Draw and explain the operation of a 6-transistor SRAM cell. 4
(d) How many bits does cache have, if cache block size is 1 word and it contains 8 blocks. 2 bit tag and 1 bit valid bit.

Q3. (a) Explain the virtual memory basis with page mapping. $3\frac{2}{3}$
(b) Illustrate the characteristics of some common memory technologies. 4
(c) What is DVD? Why DVD stores more data than CD-ROM? Explain. 3

Q4. (a) Explain the concept of pipelining in CPU design. 4
(b) Compare the RISC and CISC architecture. 3
(c) Explain the need for having a hierarchical memory organization and explain the hierarchy in detail with a block diagram. $3\frac{2}{3}$

SECTION-B

Q5. (a) Convert the following high level instruction into corresponding set of reassembly instruction carried out by a machine that uses single address instruction scheme. $3\frac{1}{3}$
Instructions available are: Load, Sub, Add, Mpy, Mov, Store
$A = A + B + D$ 3
(b) Give three examples of zero address instructions with their purposes. 5
(c) Given single bus organization of process complements with only the following control signals. How many bits will be occupied for these control signals in a single micro-instruction in field-encoded organization scheme? $3\frac{2}{3}$

Q6. (a) What are the differences between USB 2.0 and USB 3.0 version of Universal Serial Bus (USB)? Explain briefly. 3
(b) What is "Operand for Warding"? Why is it used in pipeline of instructions? Explain with example. 5
(c) What is branch folding? Can the use of an instruction queue get mid off all problems of "branch penalty" in case of pipelining? Why? $3\frac{2}{3}$

Q7. (a) Explain DMA operation during I/O. 3
(b) Describe a scenario where RAID 1 is ~~buffer~~ to implement instead of RAID 0. 5
(c) Explain 'straight line sequencing' of instruction with example. $3\frac{2}{3}$

Q8. (a) What is Von-Neumann architecture and how is it different from the concept of Harvard Architecture. 3
(b) Why priority assignment is required for interrupting devices in a computer? Draw a block diagram of implementation of interrupt priority scheme using individual interrupt-request and acknowledgement. 5
(c) Briefly explain the followings:
(i) capacitive and resistive touch screen (ii) HDMI port.

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...omputing (iii) VGA 06

Dept. of CSE, RUET (4 cycle C day- 7th April, 2016)

Class Test: 1 CSE 603 Time: 20 Min Marks: 20

Q.1 What is the basic difference between Computer Architecture and Organization? (06)

Q.2 Write in brief about the main components including functions of Computer Architecture. (14)

Dept. of CSE, RUET// 26th April 2016

Class Test: 2 CSE 603 Time: 20 Min Marks: 20

Q.1 How does an ALU work? Discuss Booth's Algorithm with necessary example. (04+08)

Q.2 Discuss the problem of sign magnitude representation. Define (i) 1's compliment and (ii) 2's compliment with necessary example. (04+04)

Dept. of CSE, RUET

Class Test: 3 CSE 603 Time: 20 Min Marks: 20

Q.1 What do you mean by the Instruction pipelining? Write the advantages and disadvantages of it. (06+04)

Q.2 Explain (i) RISC and (ii) CISC. Which one (RISC or CISC) is better and why? (05+05)

CT-04

1. Explain parallel computing. Write basic comparison with serial computing. (3+5)

2. Briefly describe (i) SISD (ii) SIMD (iii) MISD (iv) MIMD (4*3 = 12)

...ion show the advantages ...