Final Register Set Design

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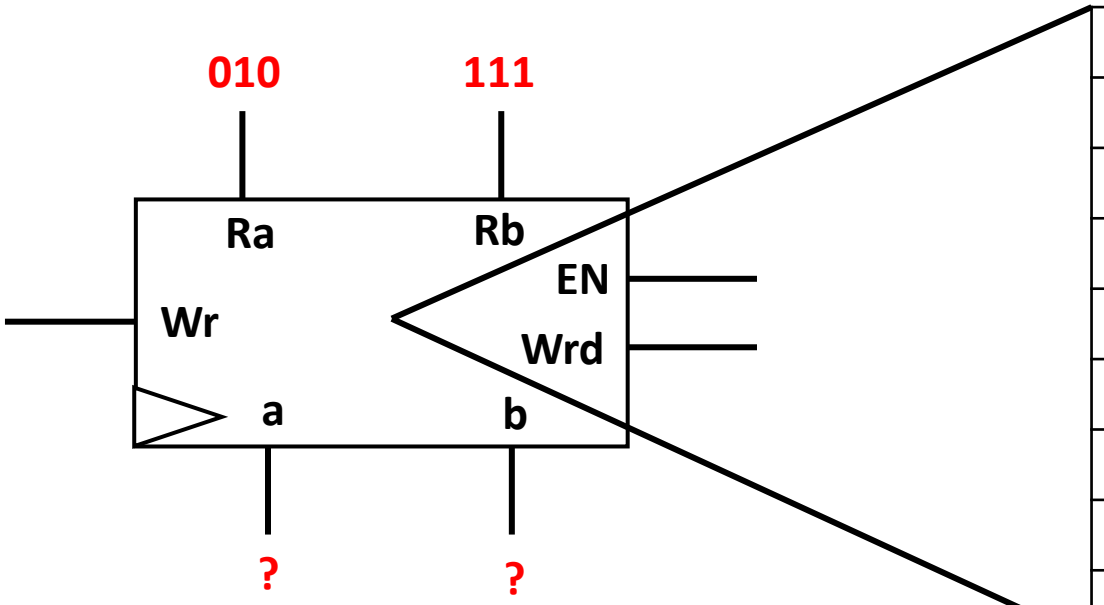
Register Set Review

4-bit Register Set (Reading)



Address	Register	Value stored
000	R0	0111 (7)
001	R1	0100 (4)
010	R2	0011 (3)
011	R3	0111 (7)
100	R4	1000 (8)
101	R5	0001 (1)
110	R6	1000 (8)
111	R7	0010 (2)

Suppose, Register set has eight 4-bit registers.

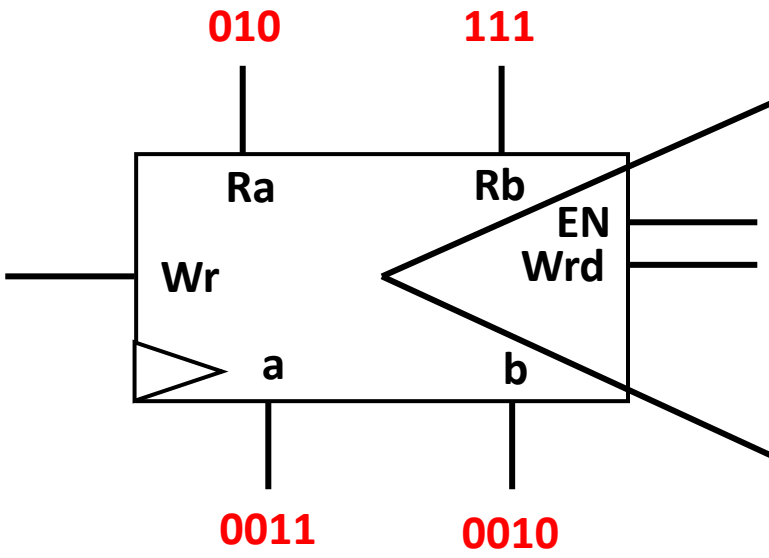
Since Register Set has 8 registers, it will need $log_2 8 = 3$ address lines.

Since registers are 4-bit registers, so it will store 4-bit value.

Reading in Register Set

Ra will take address of register and show value stored in that register in a (4-bit value).
and
Rb will take address of register and show value stored in that register in b (4-bit value).

4-bit Register Set (Reading)



Address	Register	Value stored
000	R0	0111 (7)
001	R1	0100 (4)
010	R2	0011 (3)
011	R3	0111 (7)
100	R4	1000 (8)
101	R5	0001 (1)
110	R6	1000 (8)
111	R7	0010 (2)

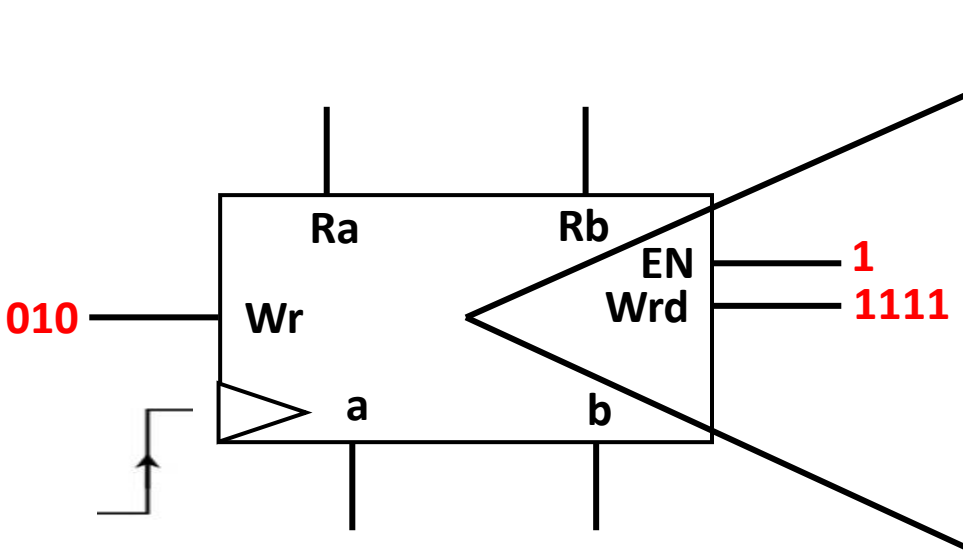
R2 register has 0011 (3) value stored.

R7 register has 0010 (2) value stored.

Reading in Register Set

Ra will take address of register and show value stored in that register in a (4-bit value).
and
Rb will take address of register and show value stored in that register in b (4-bit value).

4-bit Register Set (Writing)



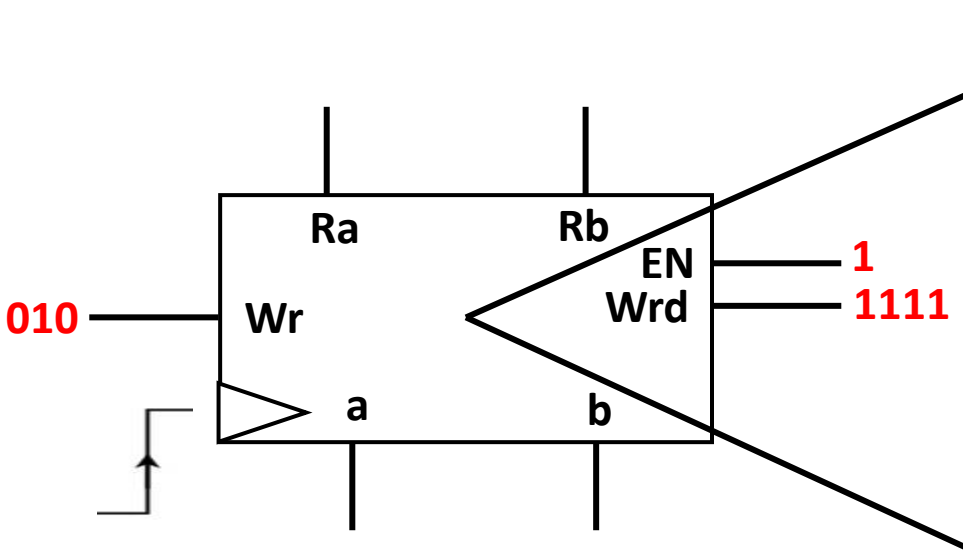
Address	Register	Value stored
000	R0	0111 (7)
001	R1	0100 (4)
010	R2	0011 (3)
011	R3	0111 (7)
100	R4	1000 (8)
101	R5	0001 (1)
110	R6	1000 (8)
111	R7	0010 (2)

What will happen?

Writing in Register Set

EN will enable/disable writing operation in register set. (1-Enable/0-Disable)
and
Wr will take address of register to be written.
and
Wrd will take (4-bit value) value to be written in Wr register.

4-bit Register Set (Writing)



Address	Register	Value stored
000	R0	0111 (7)
001	R1	0100 (4)
010	R2	1111 (15)
011	R3	0111 (7)
100	R4	1000 (8)
101	R5	0001 (1)
110	R6	1000 (8)
111	R7	0010 (2)

What will happen?

Writing in Register Set

EN will enable/disable writing operation in register set. (1-Enable/0-Disable)
and
Wr will take address of register to be written.
and
Wrd will take (4-bit value) value to be written in Wr register.

Final Register Set Design

Register Set

Register Set chip is shown below:

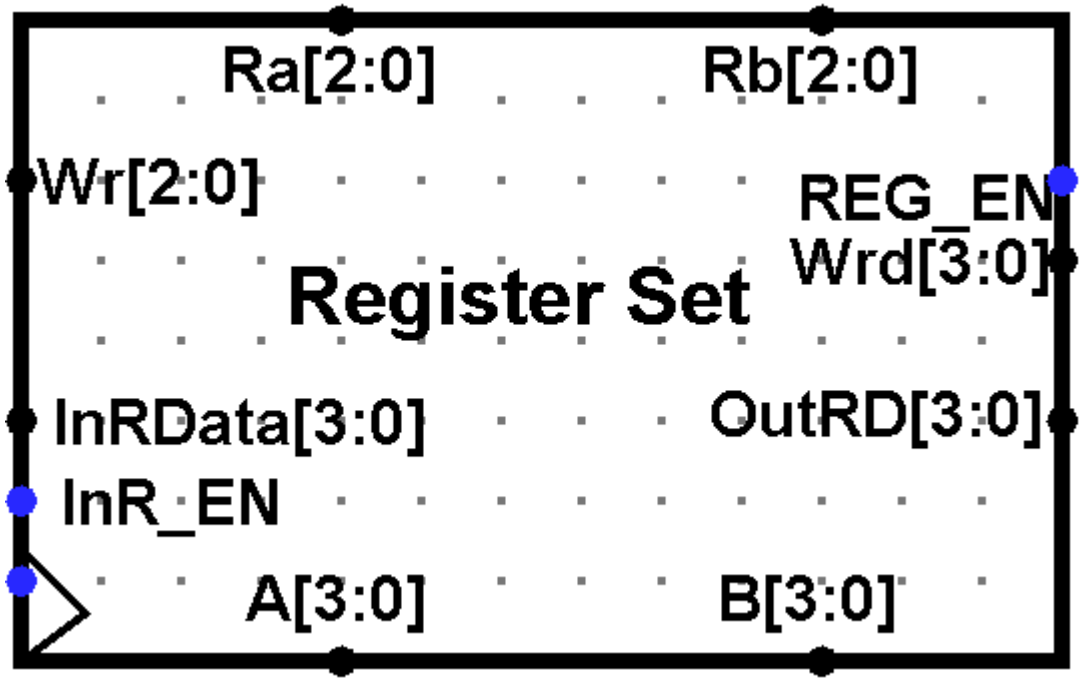


Figure: 4-bit Register Set with 8 Registers Chip

Here,
Ra = Register A
Rb = Register B
A = Data of Register A
B = Data of Register B

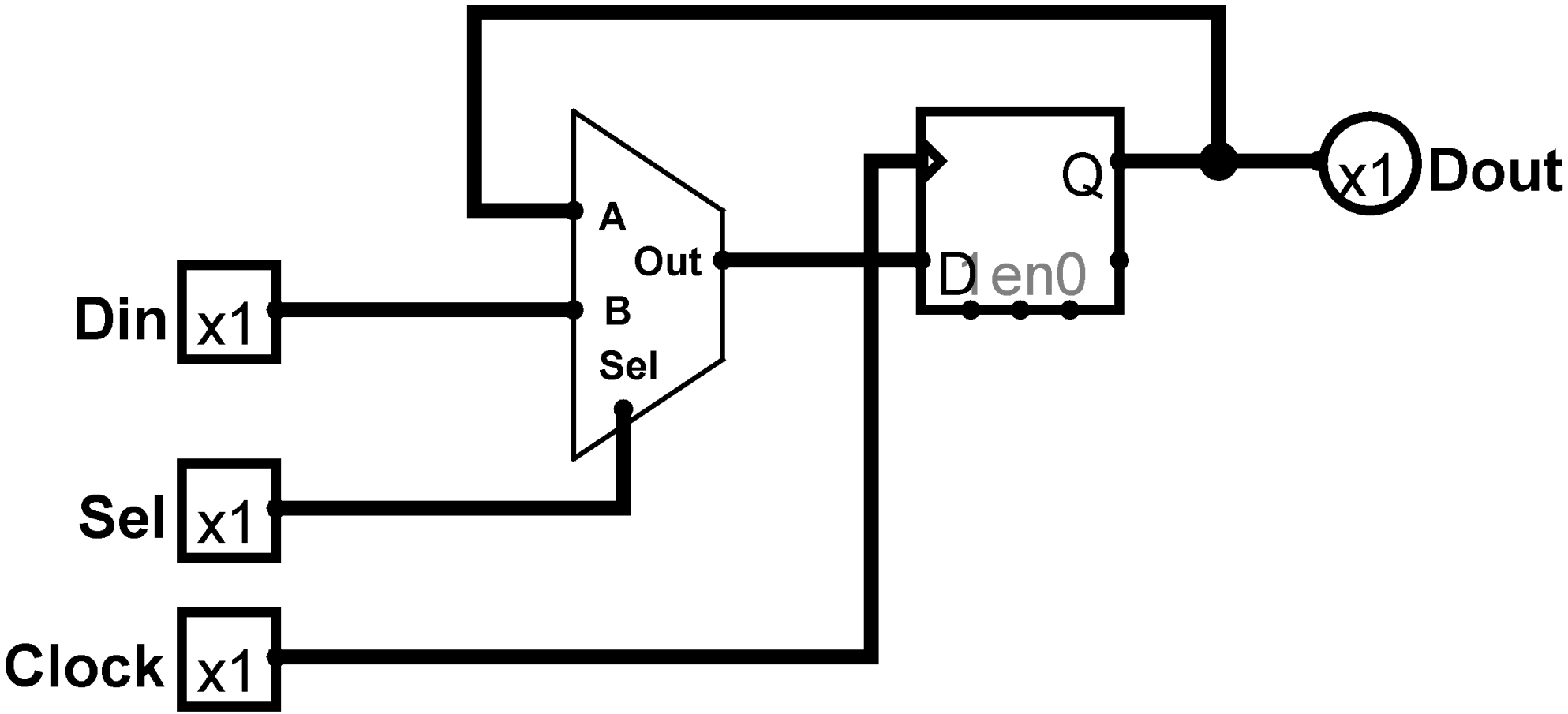
Wr = Register to be written
Wrd = Data to be written in Wr
REG_EN = Write in Register Enable

InRData = Data to be written in Input Register
InR_EN = Write Enable in Input Register

OutRD = Data in Output Register

1-bit Register Cell

1-bit Register



1-bit Register

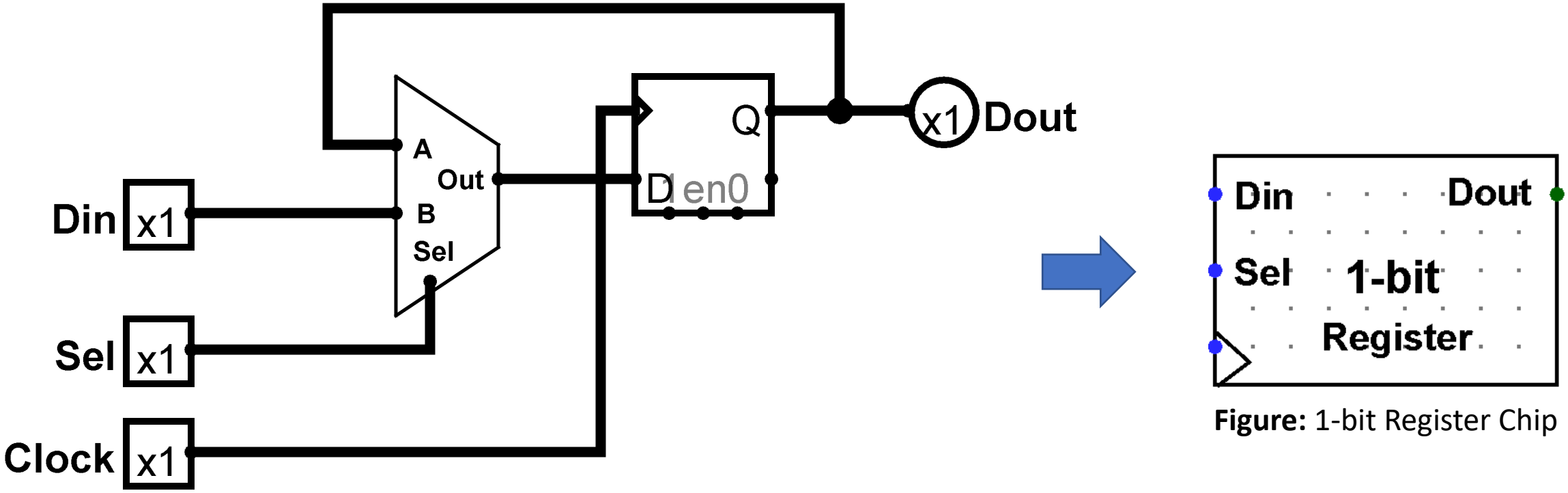
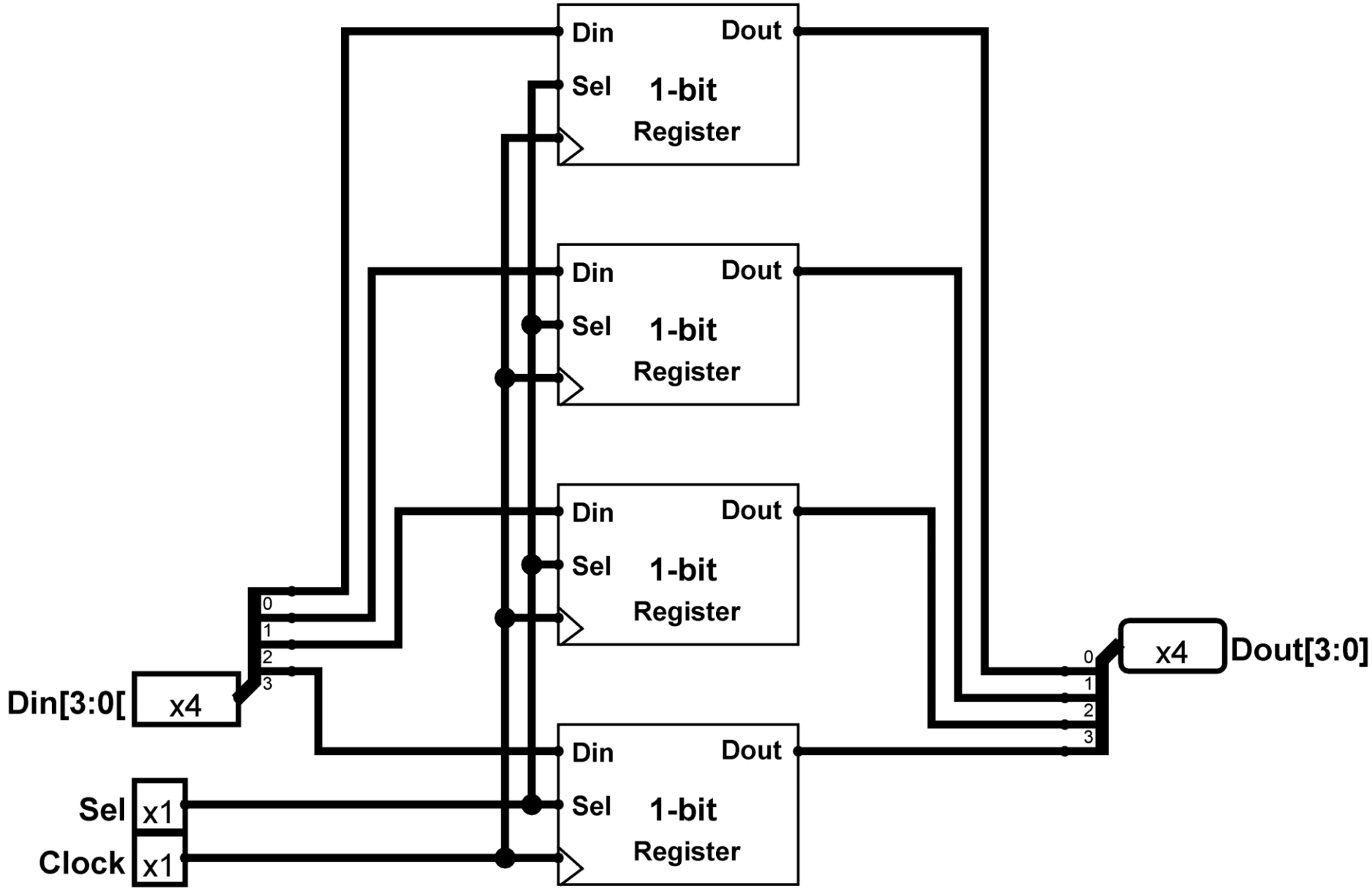


Figure: 1-bit Register Chip

4-bit Register Cell

4-bit Register



4-bit Register

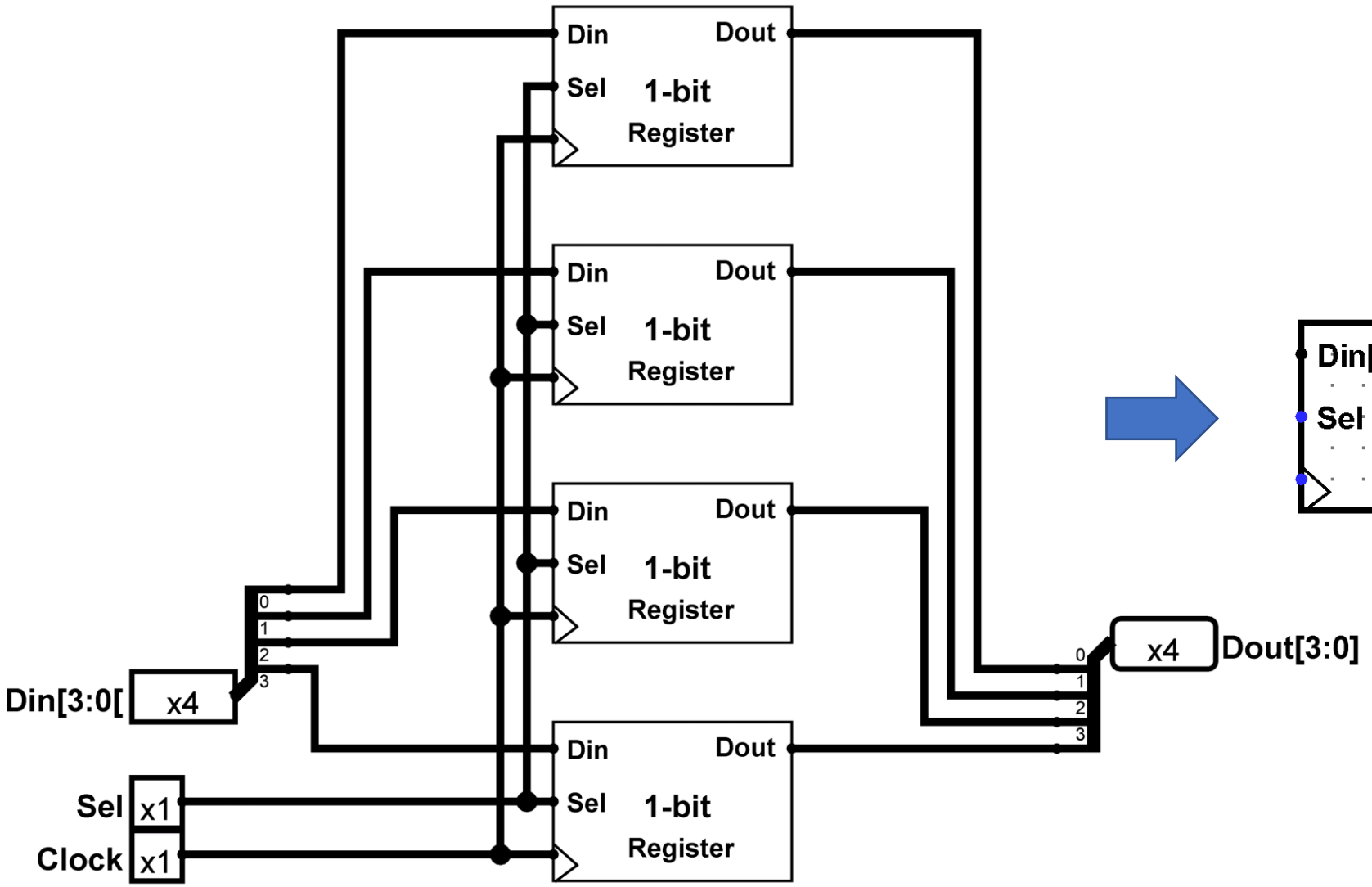
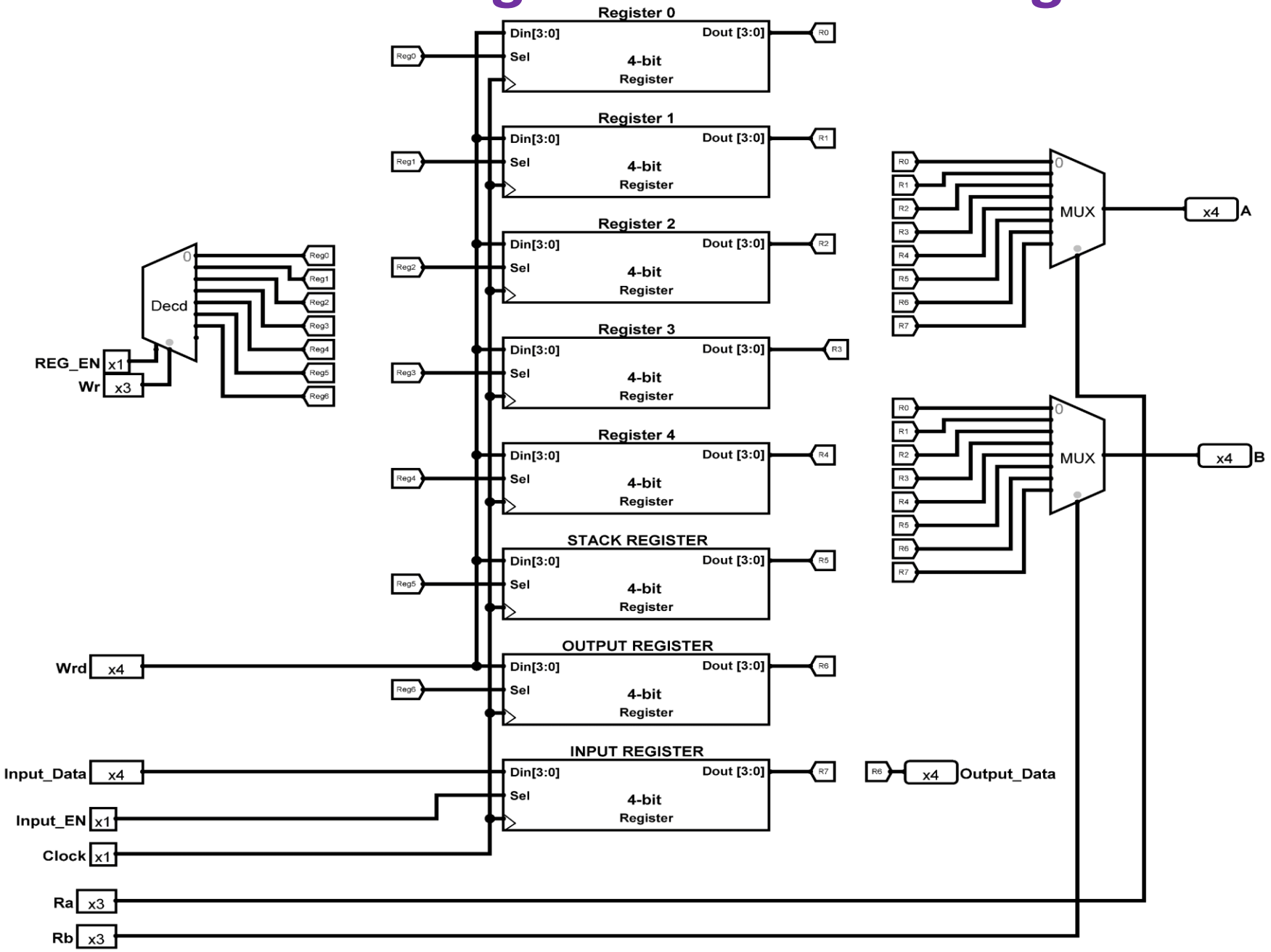


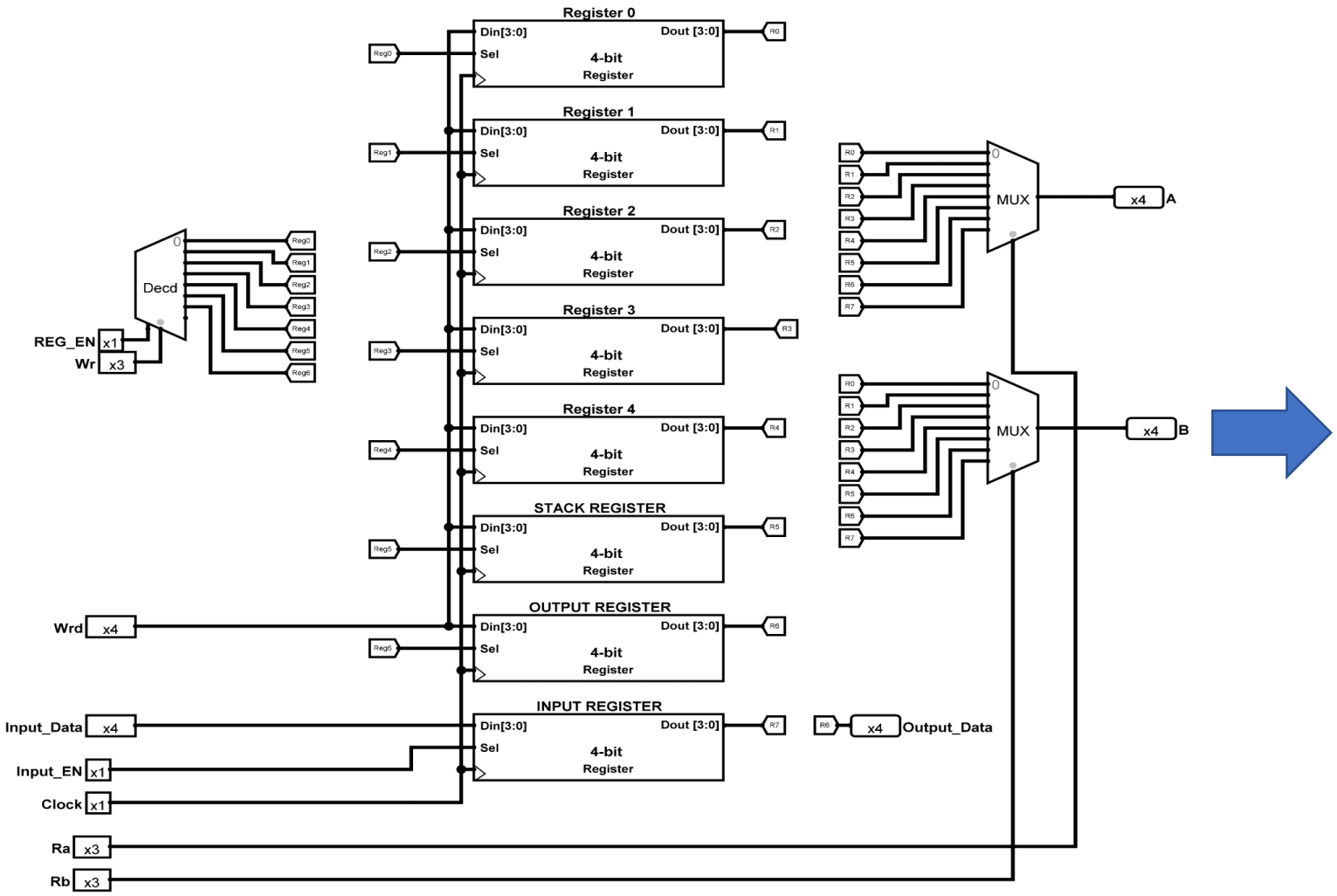
Figure: 4-bit Register Chip

4-bit Register Set with 8 Registers

4-bit Register Set with 8 Registers



4-bit Register Set with 8 Registers



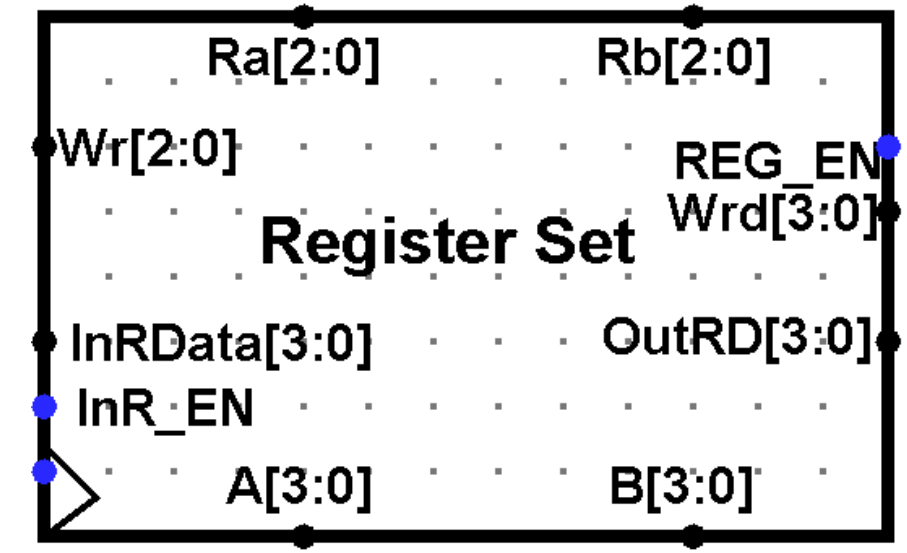
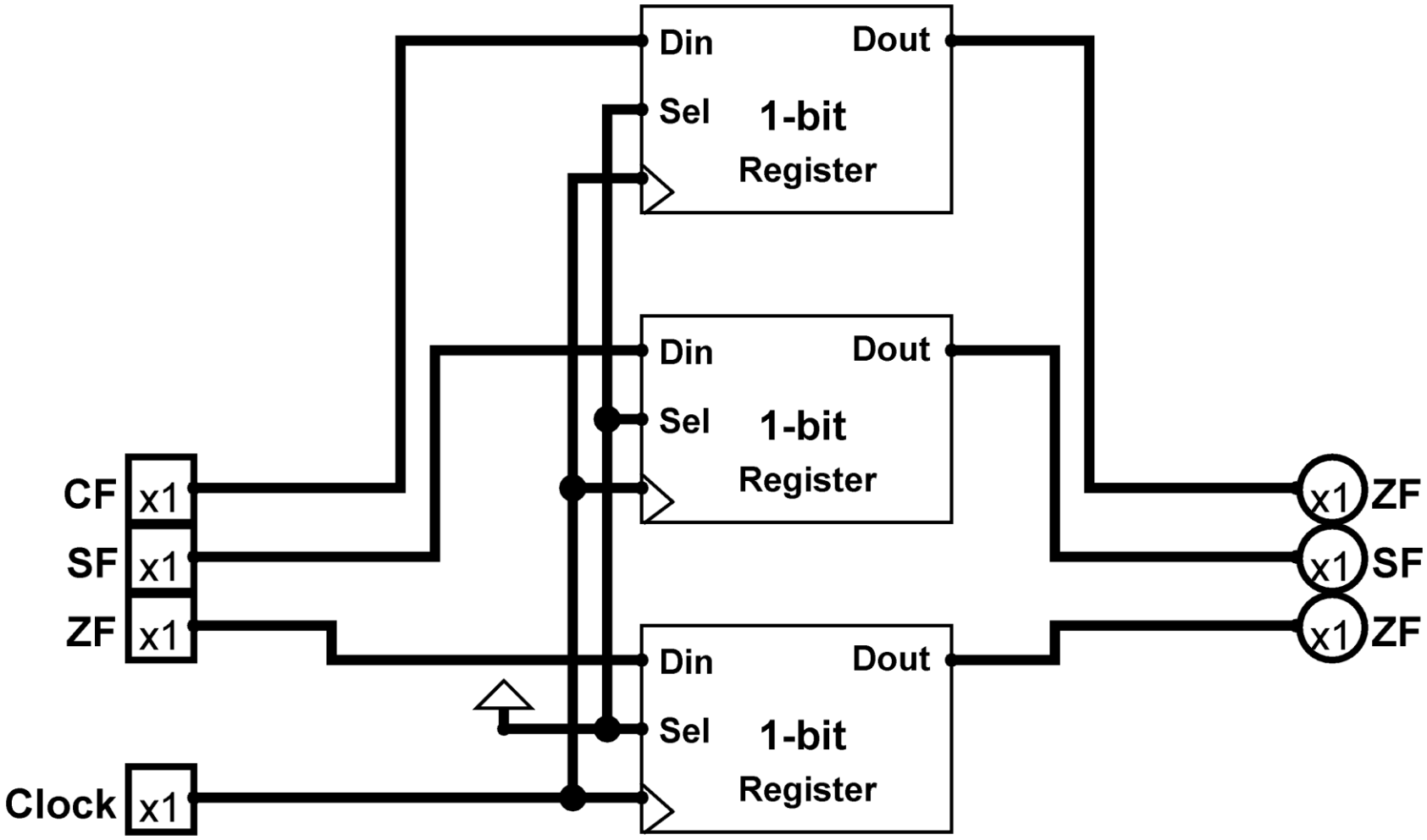


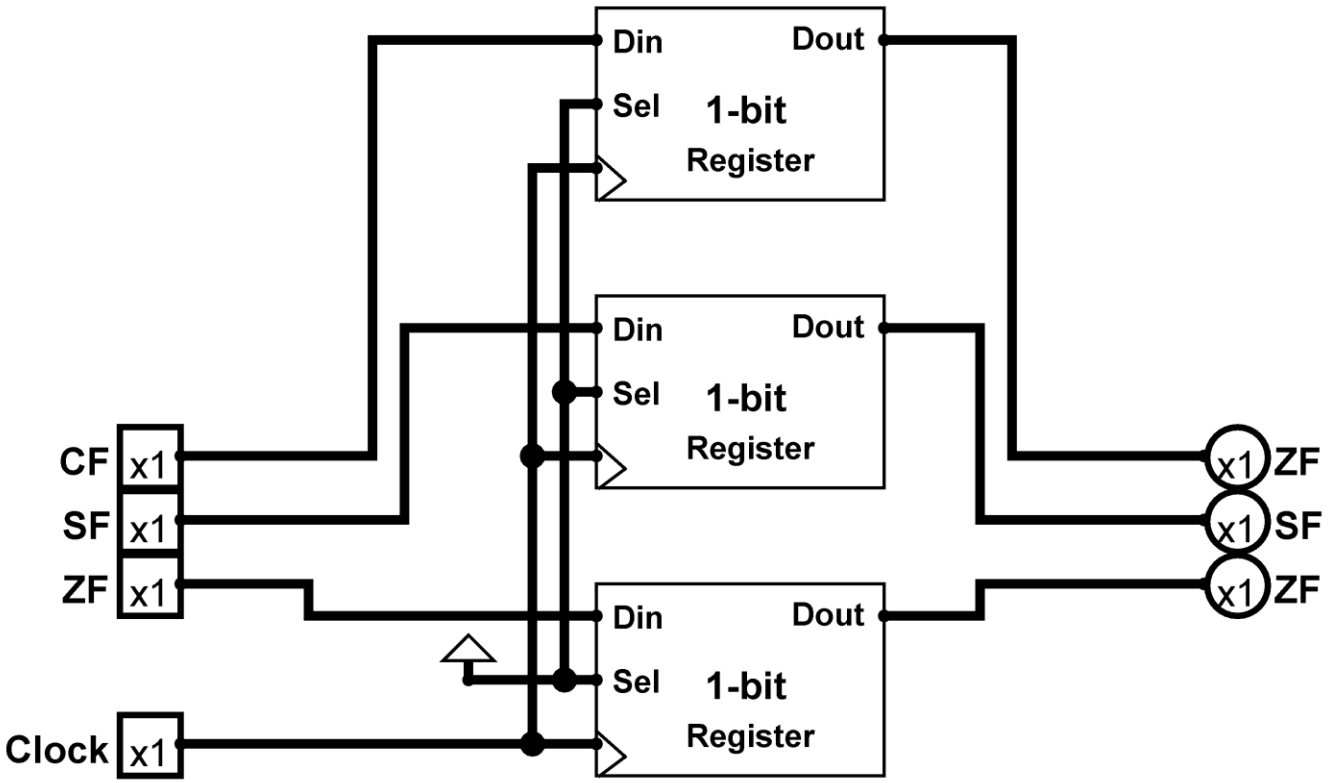
Figure: 4-bit Register Set with 8 Registers Chip

4-bit FLAG Register

4-bit FLAG Register



4-bit Register Set with 8 Registers



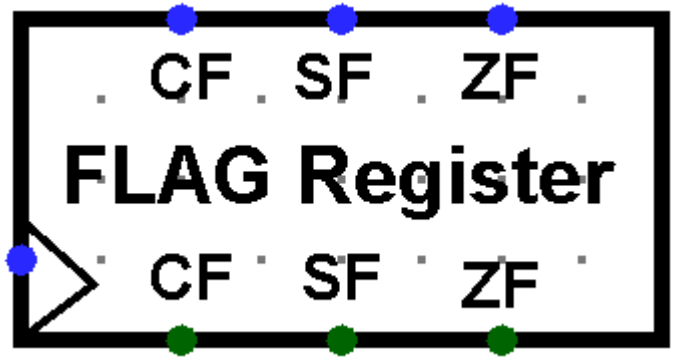


Figure: FLAG Register

Thank You ☺