Transistors are normally employed as amplifiers. In order to operate the transistors properly, firstly they must be dc-biased. A dc operating point must be set so that signal variations at the input terminal are amplified and accurately reproduced at the output terminal with minimum distortion.

Through proper design, transistor can be used as an electronic switch for computer and control applications. Applying transistor as a switch will also be discussed in this chapter.

4.1 Operating Point

As discussed in the previous chapter, when you bias a transistor, you establish a certain current and voltage condition. This means that at the dc operating point, I_C and V_{CE} have specified values. The dc operating point is often referred to as the Q-point (quiescent point). As in Fig 4. 1, the specific collector current and collector-emitter voltage at the Q-point is denote as I_{CQ} & V_{CEQ} respectively.

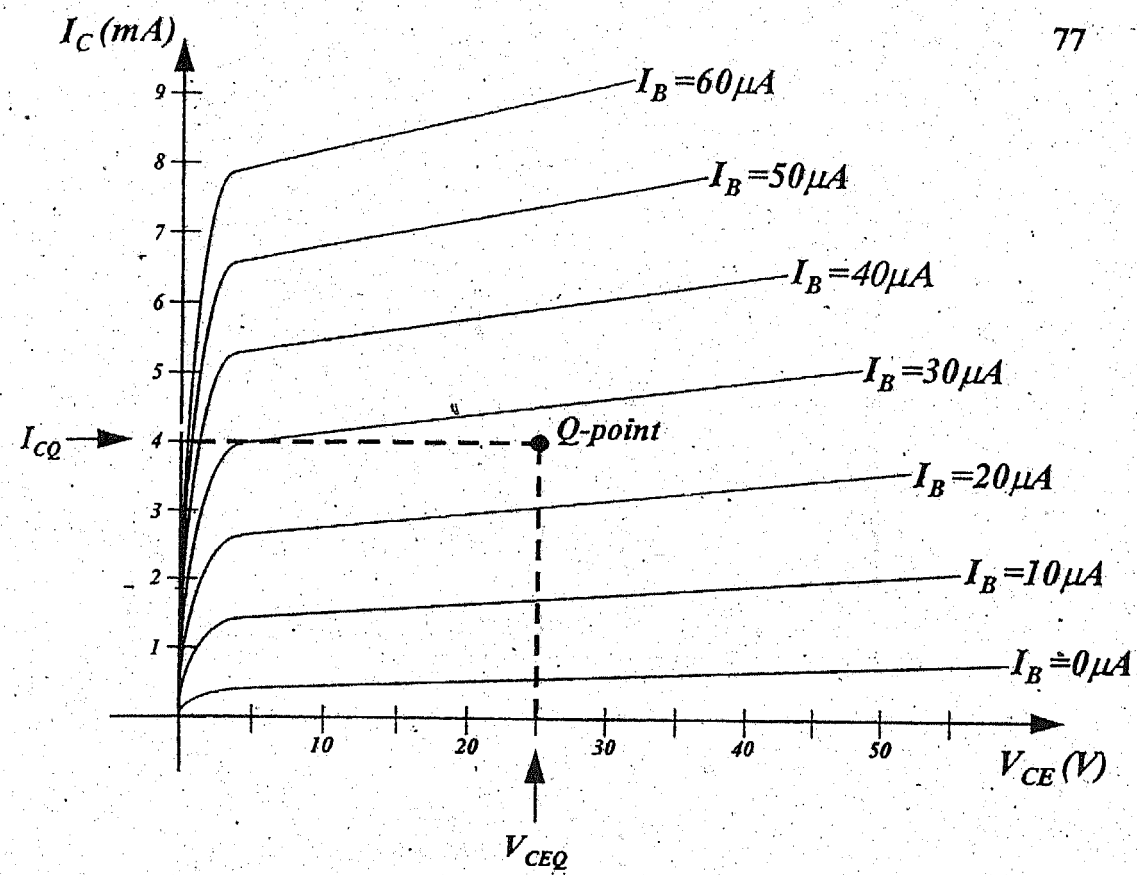


Fig 4. 1

For small signal amplifier design, the Q-point of the transistor is always designated in the Active Region. It is always preferred to have the Q-point to be in the middle of the active region, so that allowing full signal swing in the region and able it to produce un-distorted output.

Waveform distortion occurs under certain input signal conditions, or the Q-point is not appropriately located in the output characteristic curves.

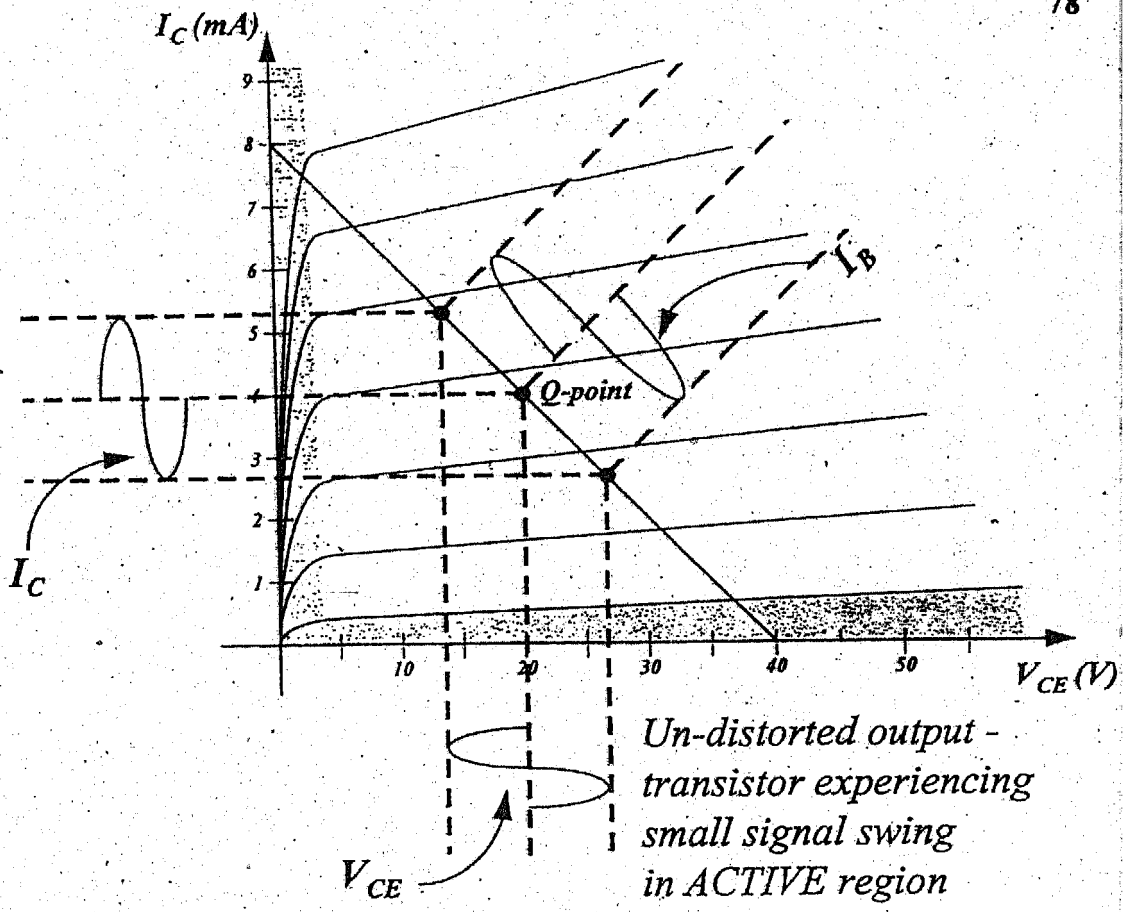


Fig 4..2

The biasing point (Q-point) in Fig 4. 2 is chosen to be at the middle o active region, a small signal current swing at the input (*base a current*) will produce a undistorted amplified signal swing at th output (V_{CE}). In this case, there is still lots of room to operate in th active region.

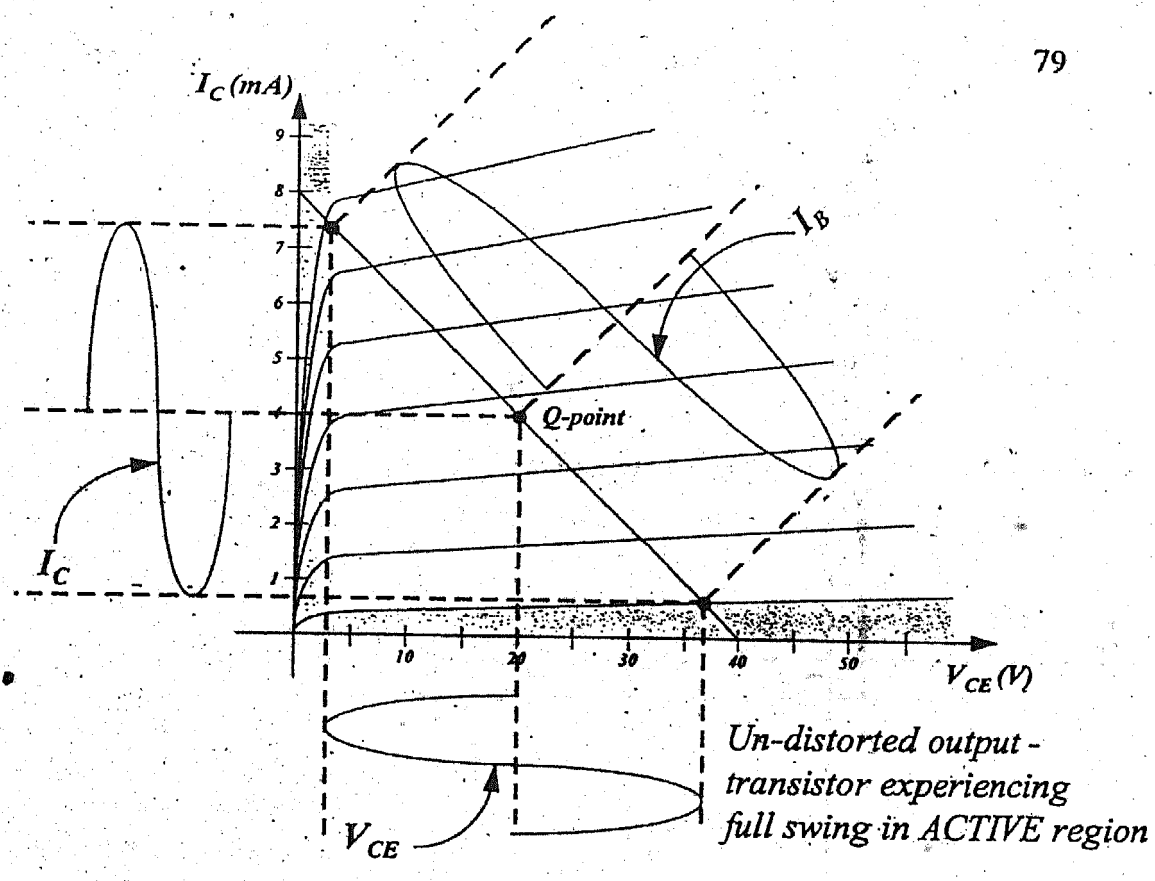


Fig 4. 3

In Fig 4. 3 , the Q-point is also designed in the middle of active region and input signal has reached full swing of the active region without causing distortion at the output.

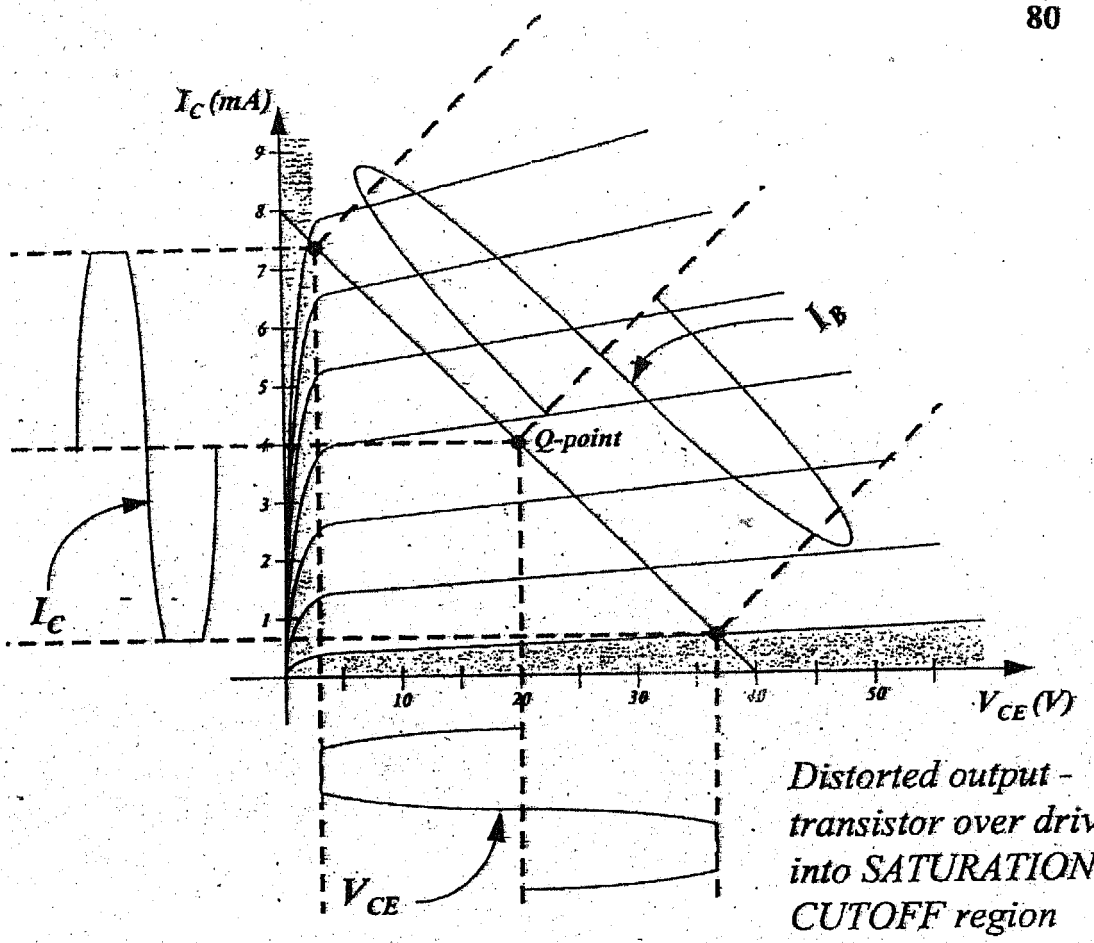


Fig 4. 4

If the transistor is over driven out of the active region limit, it wil cause distorted output as shown in Fig 4. 4.

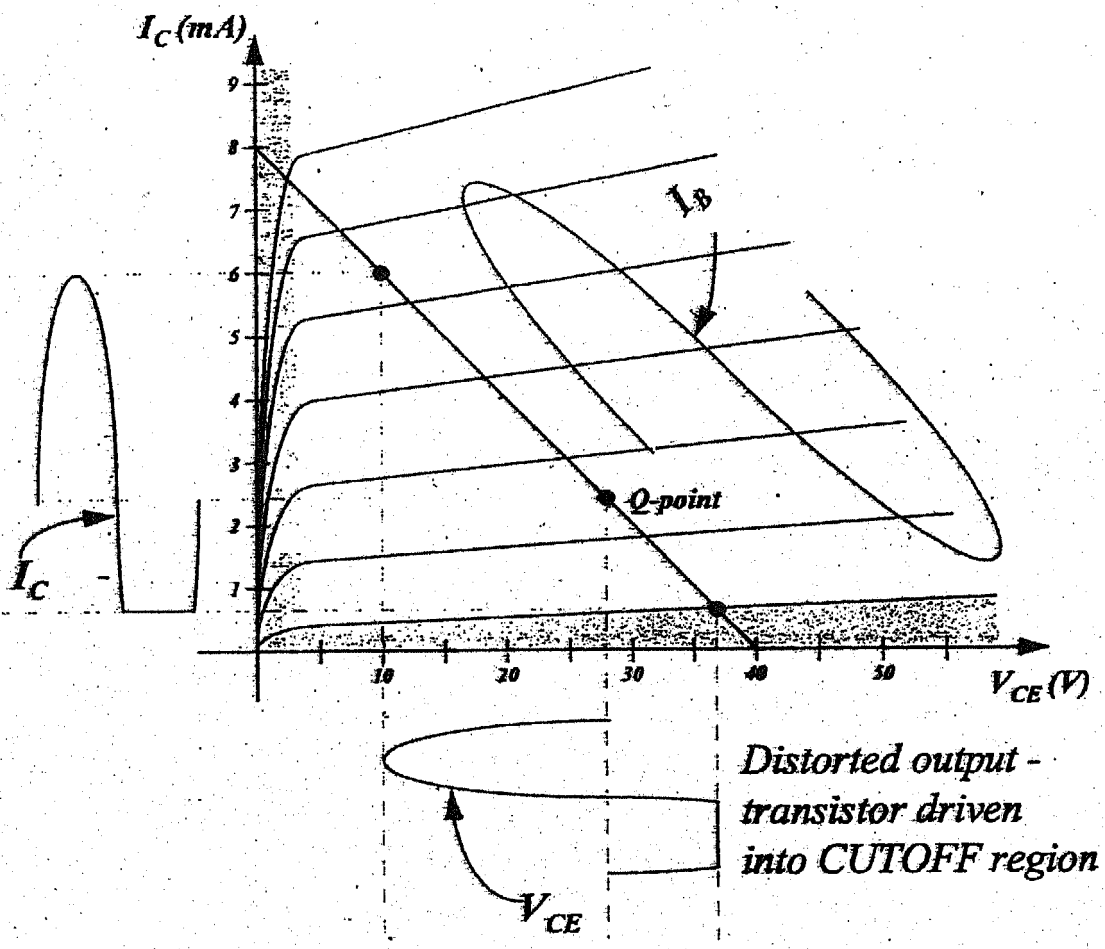


Fig 4. 5

Fig 4. 5 shows the biasing point located not in the middle of active region but towards the cutoff region. The output waveform is distorted due to clip off at the cutoff region compared to the same input signal magnitude as in Fig 4. 3.

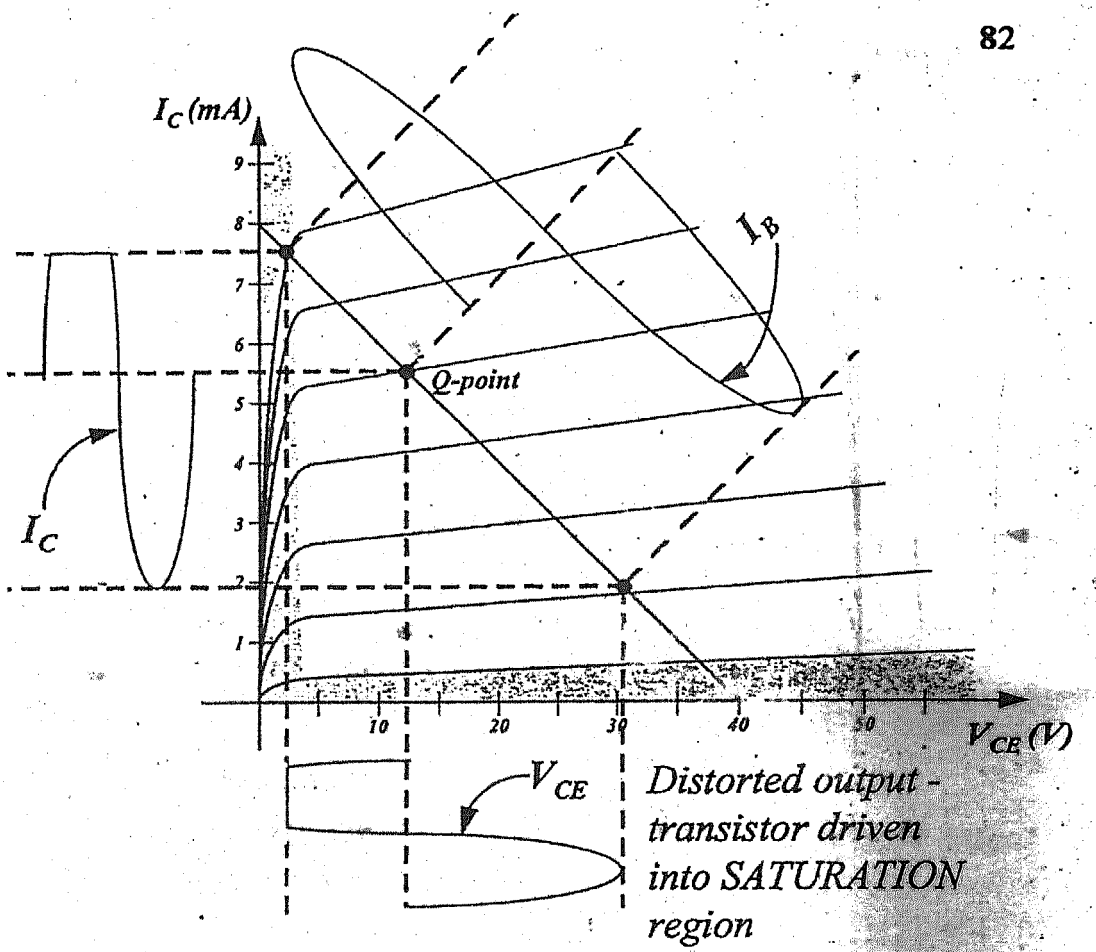


Fig 4. 6

Fig 4. 6 shows the biasing point located not in the middle of active region but towards the saturation region. The output waveform is distorted due to clip off at the saturation region compared to the same input signal magnitude as in Fig 4. 3.

It is by means of biasing networks. Which means inter-connection of resistors and the transistor to form the operating current (I_{CQ}) and voltage (V_{CEQ}) conditions.

In this chapter, four of such dc biasing networks will be discussed. They are *fixed bias circuit, emitter-stabilized circuit, voltage divider circuit & dc bias with voltage feedback circuit.*

All these four biasing circuits have the same function as to bias the transistor to operate as an amplifier. However they defer from one another in terms of Q-point stability due to the change of surrounding or junction temperature.

4.2 Fixed-bias circuit

A complete single stage amplifier is shown in Fig 4. 7 which include the input & output ac coupling capacitors C_1 & C_2. Fixed bias circuit is the simplest of all other three biasing circuit which requires only two biasing resistor R_B and R_C.

Once the dc biasing condition (Q-point) has been establihsed. A small ac signal can be applied at the input, and the transistor amplifier will produce an amplified inverted replica of the input signal.

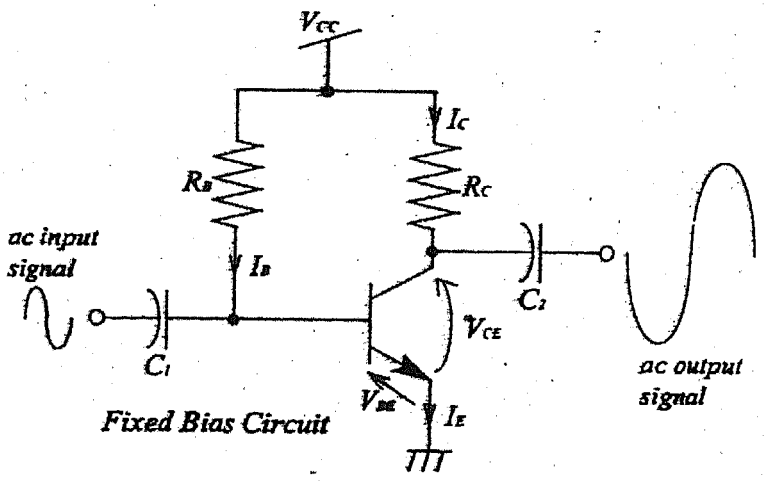


Fig 4. 7

The ac analysis of the amplifier will be cover in second year of your study under module EG2002. As we are more concerned about dc analysis in this module (EG1004) , we could reduce the circuit in Fig 4. 7 to Fig 4. 8 by removing the ac coupling capacitors C_1 & C_2.

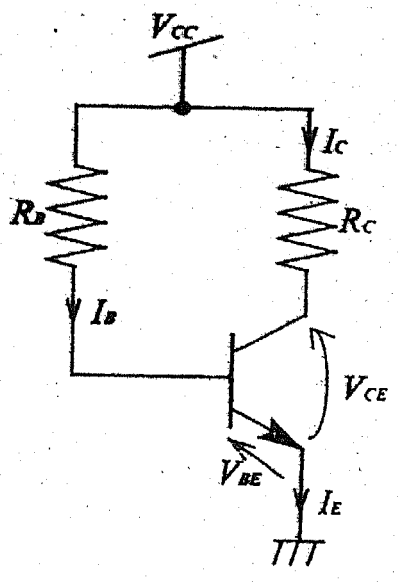


Fig 4. 8

In Fig 4. 8, R_B is used to control the amount of I_B flowing into the base terminal hence controlling I_C flowing in the output loop (recall that $I_C = \beta I_B$). Resistor R_C is used to control the voltage (V_{CE}) drop across collector-emitter terminals.

How do we determine the values of R_B & R_C so that the transistor Q-point is operating at the desired location in active region ?

For this analysis, we could further modify (or re-draw) the circuit in Fig 4. 8 into input and output loop as shown in Fig 4. 9. For this circuit, we could easy form an input loop equation and output loop equation by using the basic equations discussed in previous chapter, KVL, KCL & Ohm's law to solve for R_B & R_C.

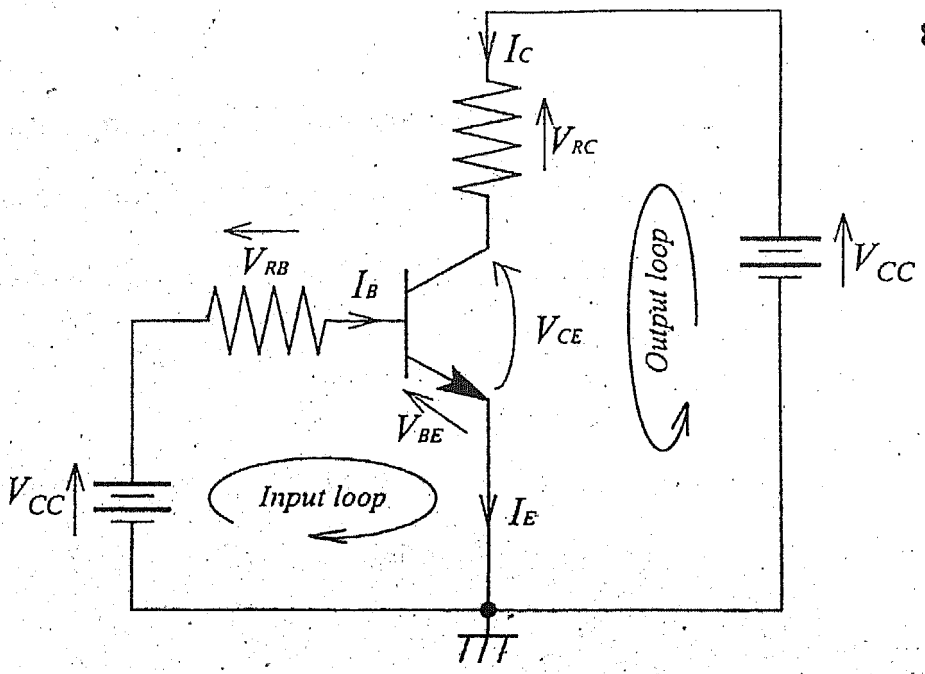


Fig 4. 9

Input Loop Equation :

$$\overrightarrow{V_{CC}} = \overleftarrow{V_{RB}} + \overleftarrow{V_{BE}}$$

or

$$V_{CC} = I_B R_B + V_{BE}$$

Output Loop Equation :

$$\overrightarrow{V_{CC}} = \overleftarrow{V_{RC}} + \overleftarrow{V_{CE}}$$

or

$$V_{CC} = I_C R_C + V_{CE}$$

In most design cases, the supply voltage V_{CC} are specified. We also would know what operating conditions is required for I_{CQ} & V_{CEQ}. The dc current gain β_{dc} of the transistor can be found from the data sheet which can be retrieve from the **Internet** nowadays.

EXAMPLE

Take Fig 4. 1 for example, the required operating conditions $I_{CQ} = 4$ *mA* & $V_{CEQ} = 25V$. Assuming $V_{CC} = 50V$, and $\beta_{dc} = 150$ from the data sheet.

We will solve the output loop equation to determine the value of R_C.

$$V_{CC} = V_{RC} + V_{CE}$$
$$V_{CC} = I_C R_C + V_{CE}$$
$$50V = (4mA)(R_C) + 25V$$
$$R_C = \frac{50V - 25V}{4mA}$$
$$= \frac{25V}{4mA}$$
$$= 6.25k\Omega$$

We could calculate I_B from I_C & β_{dc},

$$I_C = \beta I_B$$

$$I_B = \frac{I_C}{\beta}$$

$$= \frac{4\ mA}{150}$$

$$= 26.7\,\mu A$$

With I_B known, R_B can be calculated from the input loop equation.

$$V_{CC} = V_{RB} + V_{BE}$$

$$V_{CC} = I_B R_B + V_{BE}$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_B}$$

$$= \frac{50V - 0.7V}{26.7\,\mu A} \qquad V_{BE} \text{ is known to be } 0.7V$$

$$= 1.85\,M\Omega$$

We have now completed the dc biasing design for a transistor operating as an amplifier using fixed biasing configuaration. As shown in Fig.4. 10, the operating point is designated at conditions $I_{CQ} = 4\ mA$ & $V_{CEQ} = 25V$ with the appropriate resistors values employed.

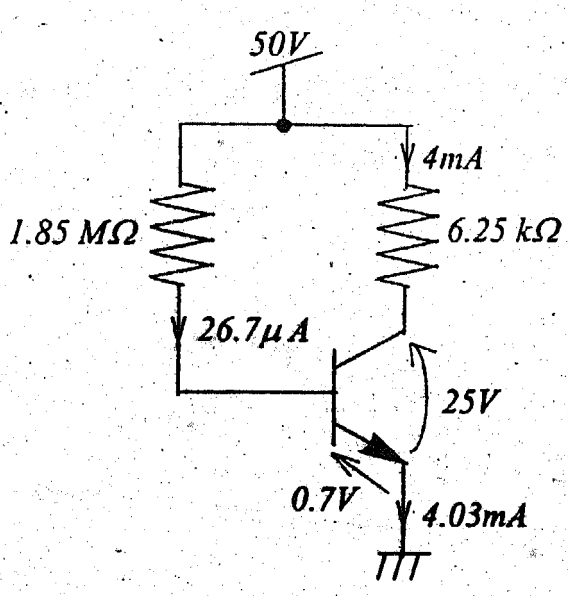


Fig 4. 10

The circuit discussed above can also be analyze graphically. We will now investigate how the network parameters define the possible range of Q-points and how the actual Q-point is determined. This method is know as **Load Line Analysis.**

Before the transistor is biased to any resistor network, there is a possibility that the Q-point can be just about any where in the output characteristic curves shown in Fig 4. 11.

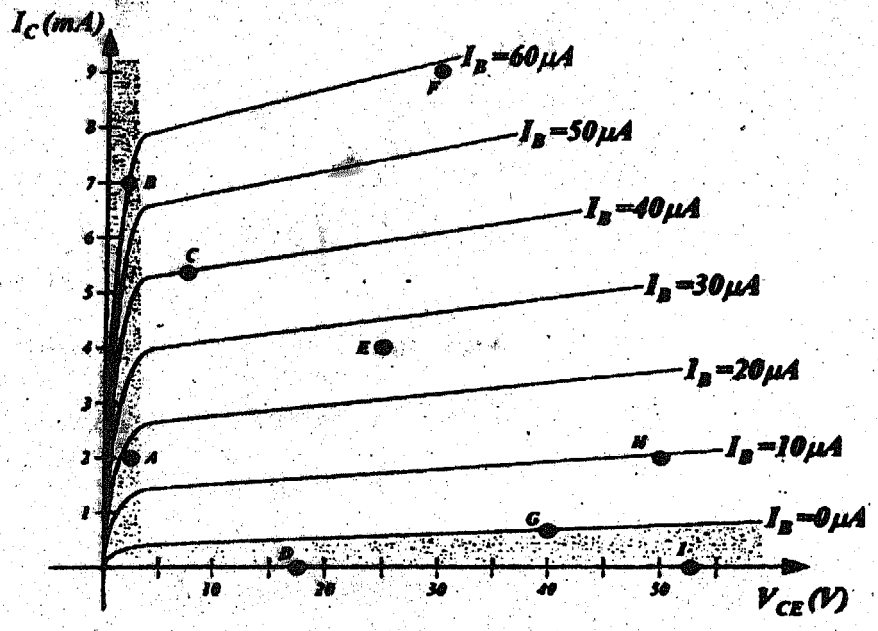


Fig 4. 11

However, once the transistor is biased with a certain resister network configuration as in Fig 4. 7, the operating point in the entire characteristic curves is now restricted to only along the load line shown in Fig 4. 12.

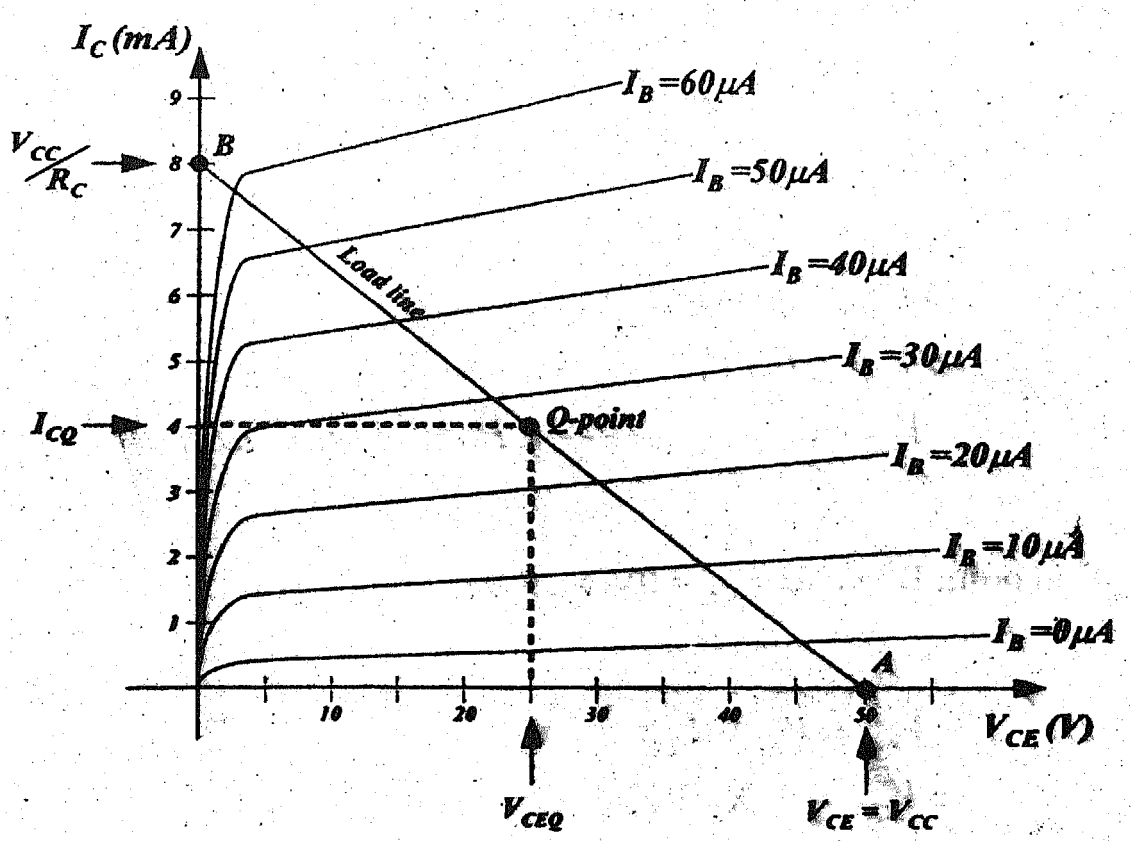


Fig 4. 12

The load line can be obtain form the output loop equation of the circuit.

$$V_{CC} = V_{RC} + V_{CE}$$

Since the load line is a straight line, you require only two points to draw the line and super-impose onto the output characteristic curves. The easy points to determine the load line are on the axes where either I_C is equal to zero or V_{CE} is equal to zero.

Therefore point A is found when we let $I_C = 0\text{A}$,

$$\begin{aligned}
&\because V_{CC} = V_{RC} + V_{CE} \\
&\Rightarrow V_{CC} = I_C R_C + V_{CE} \\
&\Rightarrow V_{CC} = (0\,A)(R_C) + V_{CE} \\
&\Rightarrow V_{CC} = 0 + V_{CE} \\
&\therefore V_{CE} = V_{CC} \qquad \text{------ } \textit{Point A on x-axis}
\end{aligned}$$

To find point B, we let $V_{CE} = 0\text{V}$ we have

$$\begin{aligned}
&\because V_{CC} = V_{RC} + V_{CE} \\
&\Rightarrow V_{CC} = I_C R_C + V_{CE} \\
&\Rightarrow V_{CC} = I_C R_C + 0 \\
&\therefore I_C = \frac{V_{CC}}{R_C} \qquad \text{------ } \textit{Point B on y-axis}
\end{aligned}$$

After the load line has been found, where exactly should the Q-point be located along the load line ? This will depend on what is the I_B apply at the base terminal.

The shift of Q-point along the load line from Q1 to Q2 or to Q3 depends on what is the I_B injected to the transistor, I_{B1} , I_{B2} or I_{B3} respectively. Hence, yield I_{C1}, I_{C2}, I_{C3} & V_{CE1}, V_{CE2}, V_{CE3} accordingly. Refers to Fig 4. 13.

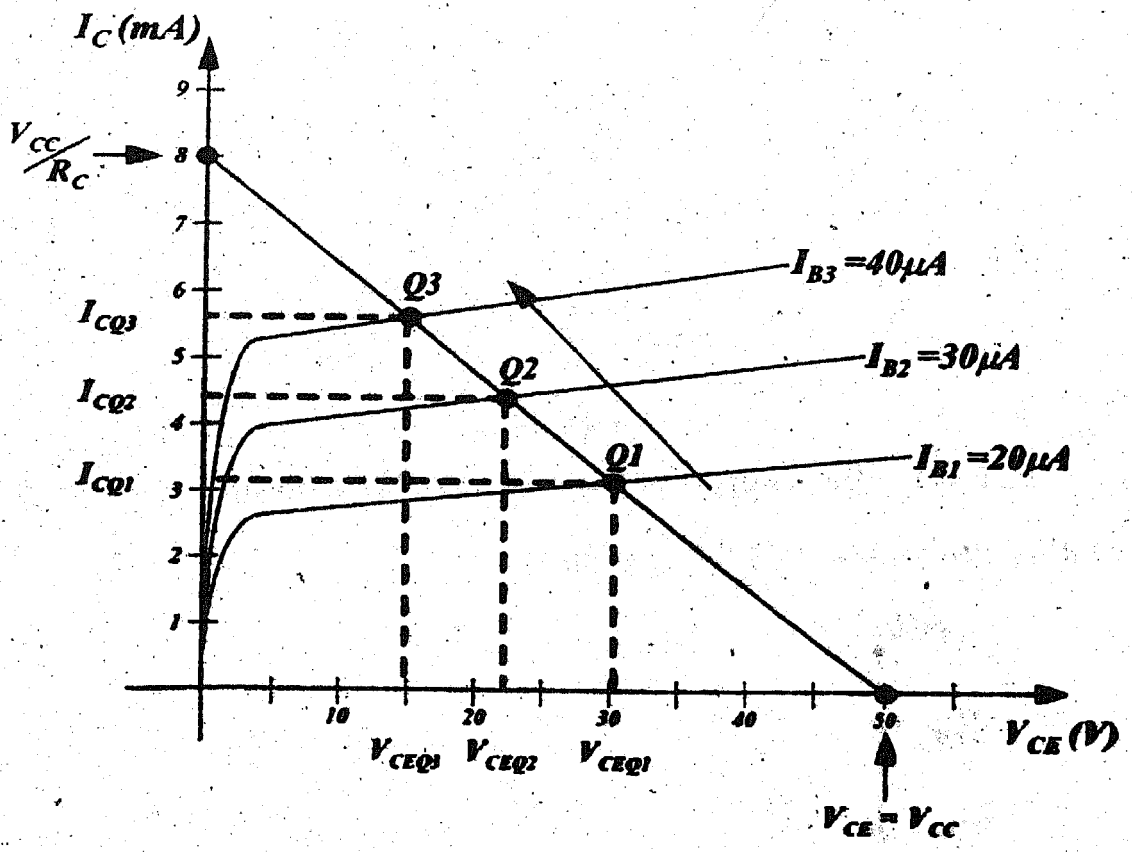


Fig 4. 13

Likewise, the Q-point can also be shifted from Q1 to Q3 with I_B is kept constant as in Fig 4. 14.

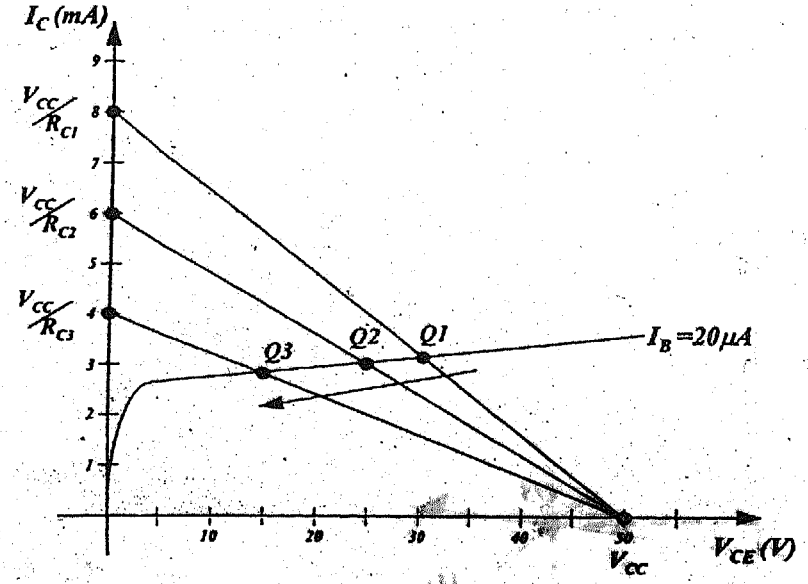


Fig 4. 14

Or by changing the supply voltage of the fixed biasing circuit, will also alter the location of the Q-point.

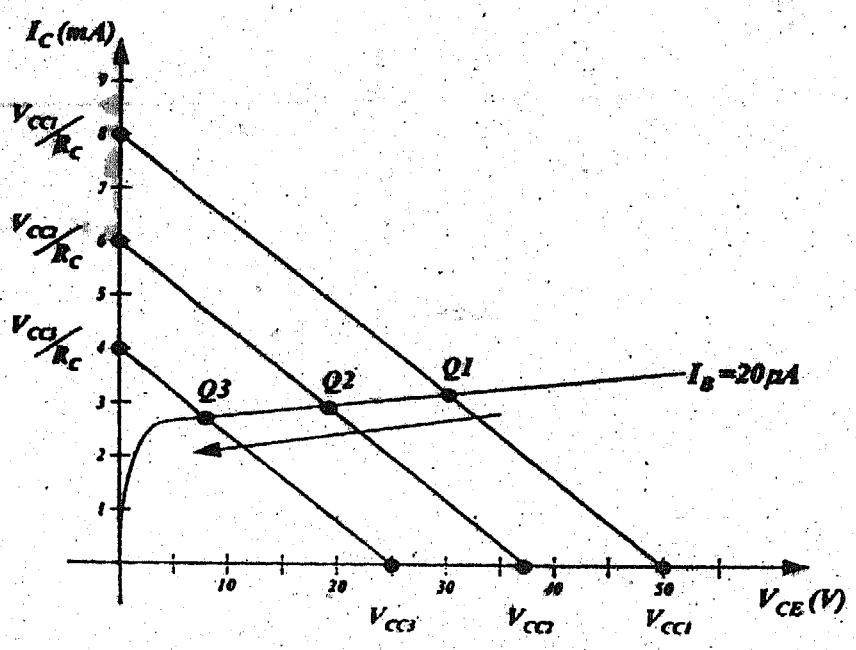


Fig 4. 15

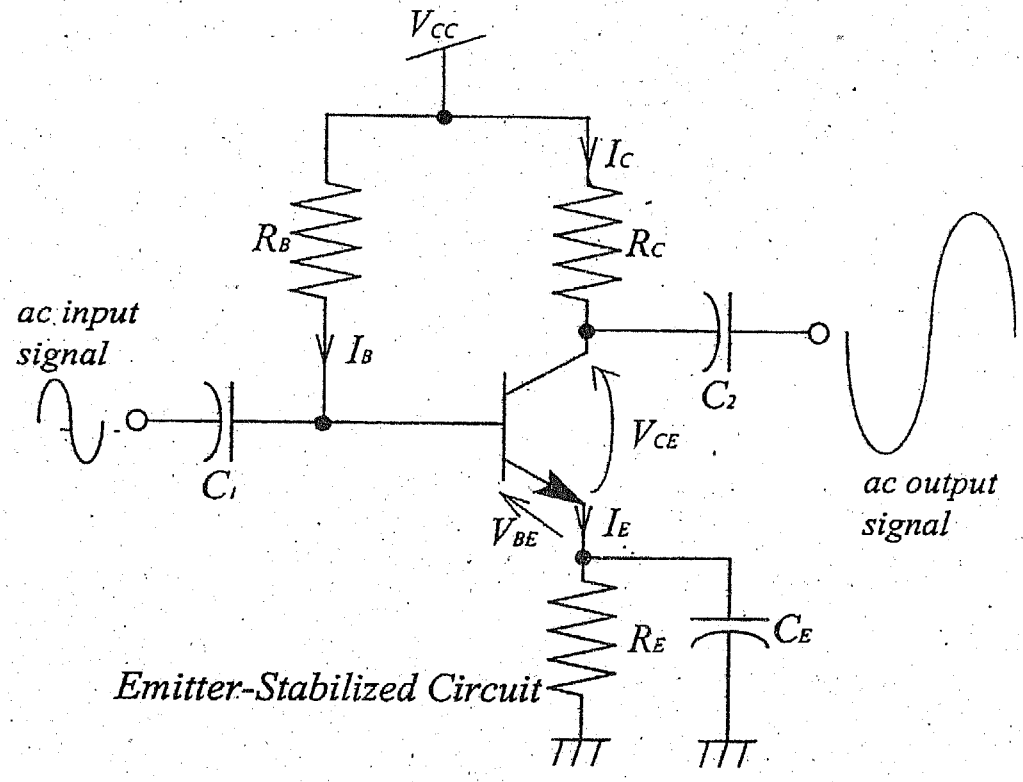


Fig 4. 16

This biasing circuit depicted in Fig 4. 16 contains an emitter-resistor to improve the stability level over that of the fixed bias configuration. Again, for dc analysis, the circuit can be reduce to Fig 4. 17 by removing the coupling and decoupling capacitors.

Put Fig 4. 17 into its input loop and output loop format as in Fig 4. 18. You could now form the input and output loop equations to solve for the circuit.

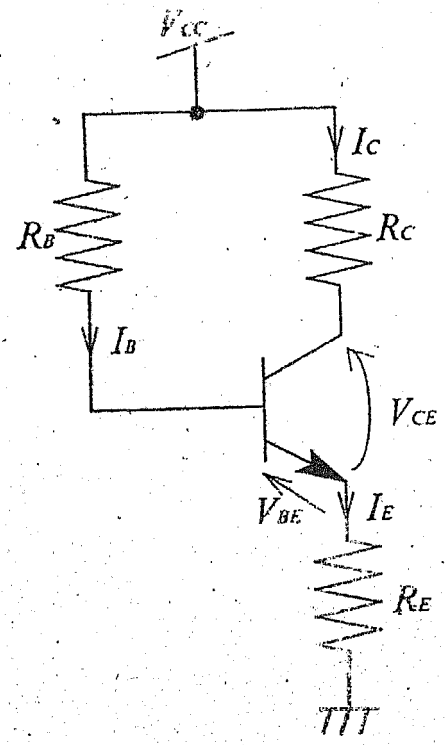


Fig 4. 17

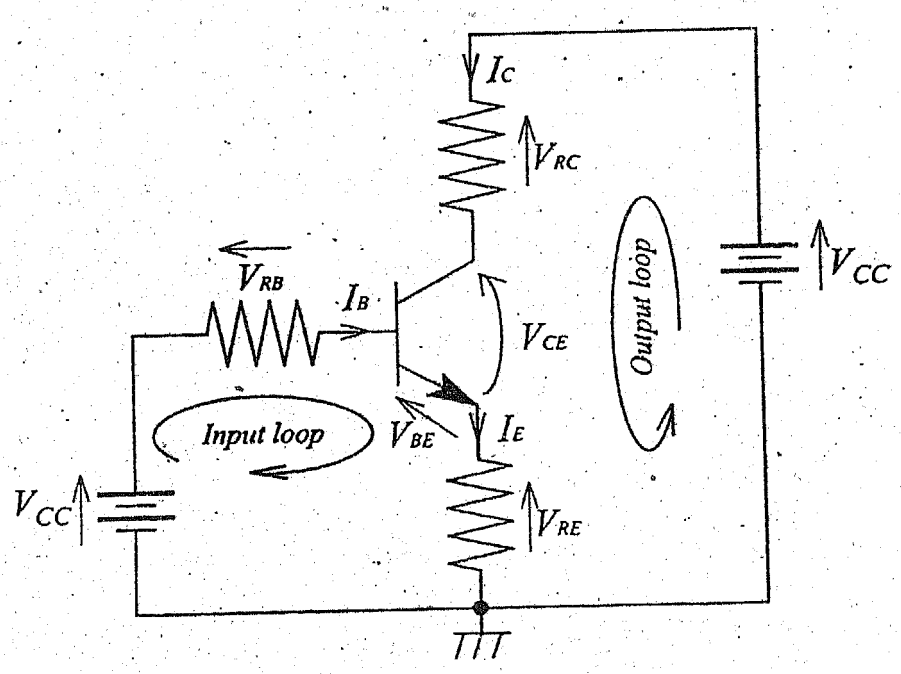


Fig 4. 18

Input Loop Equation :

$$\overrightarrow{V_{CC}} = \overleftarrow{V_{RB}} + \overleftarrow{V_{BE}} + \left[\overleftarrow{V_{RE}}\right]$$

or

$$V_{CC} = I_B R_B + V_{BE} + \left[I_E R_E\right]$$

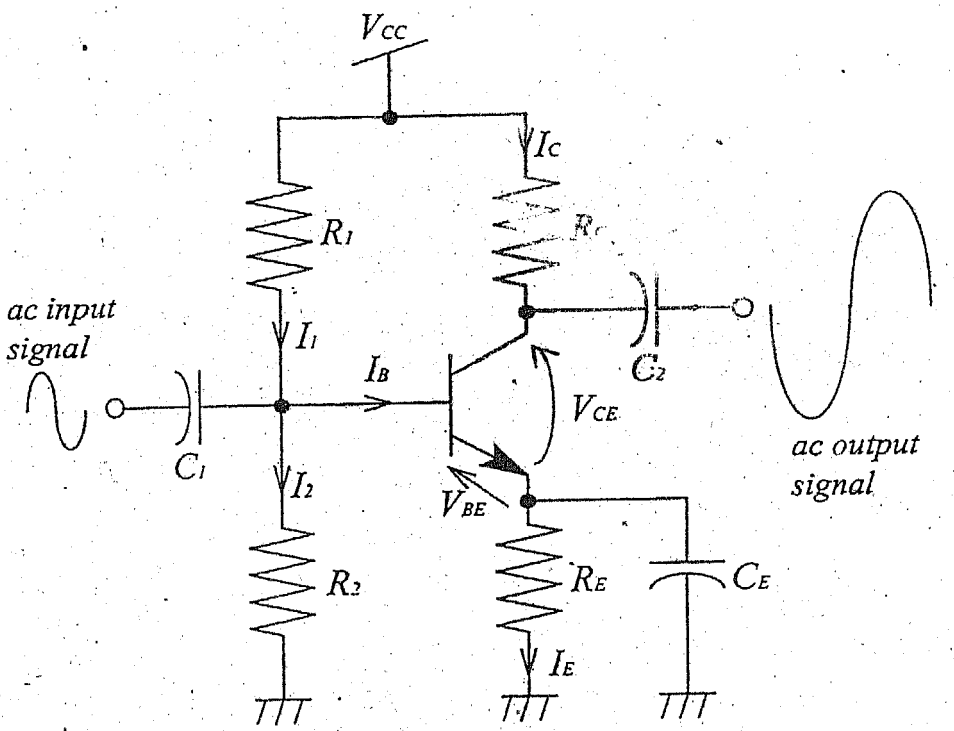
Output Loop Equation :

$$\overrightarrow{V_{CC}} = \overleftarrow{V_{RC}} + \overleftarrow{V_{CE}} + \left[\overleftarrow{V_{RE}}\right]$$

or

$$V_{CC} = I_C R_C + V_{CE} + \left[I_E R_E\right]$$

This biasing circuit is most widely used. A dc bias voltage at the base of the transistor is developed by a resistive voltage-divider consisting of R_1 and R_2 as shown in Fig 4. 19.



Voltage Divider Bias Circuit

Fig 4. 19

Reduce the circuit in Fig 4. 19 to Fig 4. 20,

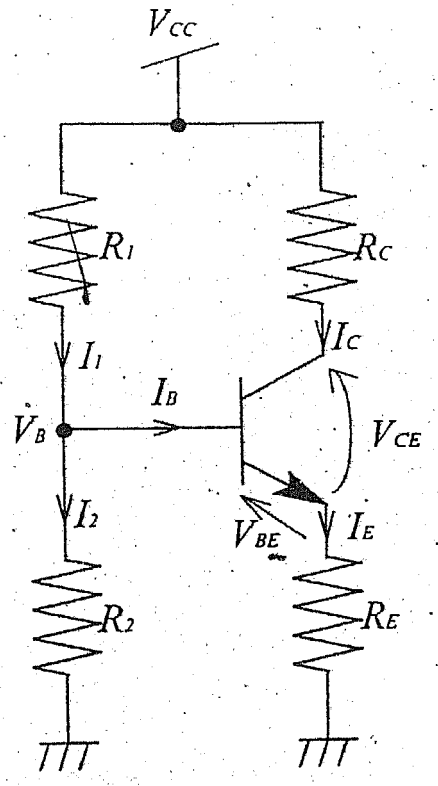


Fig 4. 20

Redraw the circuit in Fig 4. 20 to appear like in Fig 4. 21.

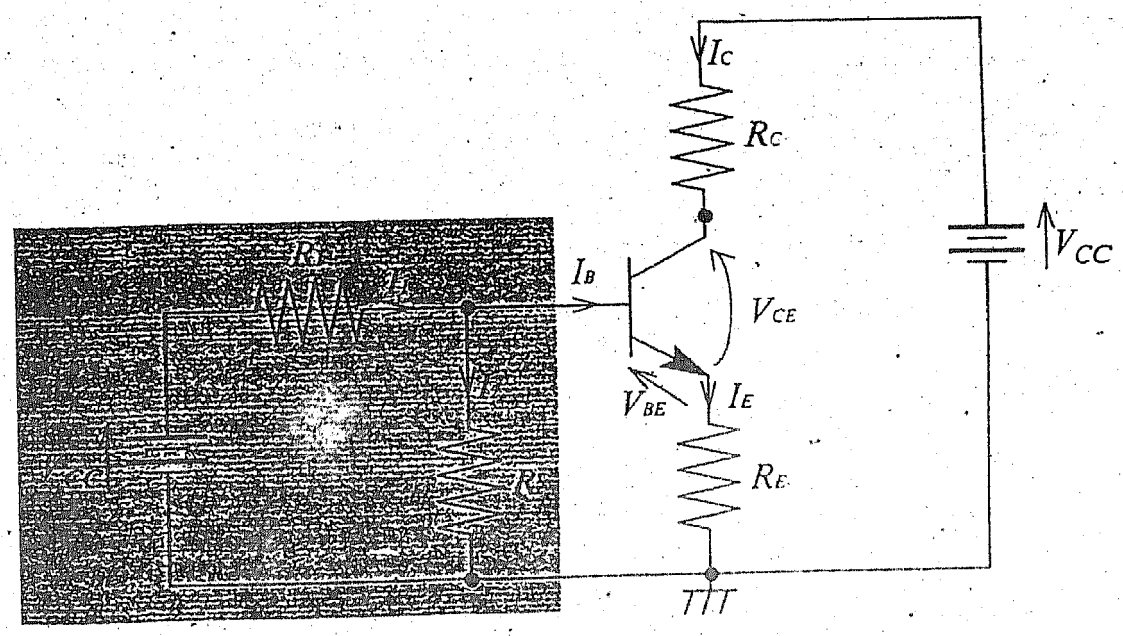


Fig 4. 21

Notice that the input of Fig 4. 21 does not form a simply loop as in fixed bias and emitter-stabilized circuits. We will have to further transform the circuit by applying Thevenin's theorem.

By apply Thevenin's equivalent, we can transform the input circuit of Fig 4. 21 to Thevenin's equivalent circuit which is a simple loop as shown in Fig 4. 23.

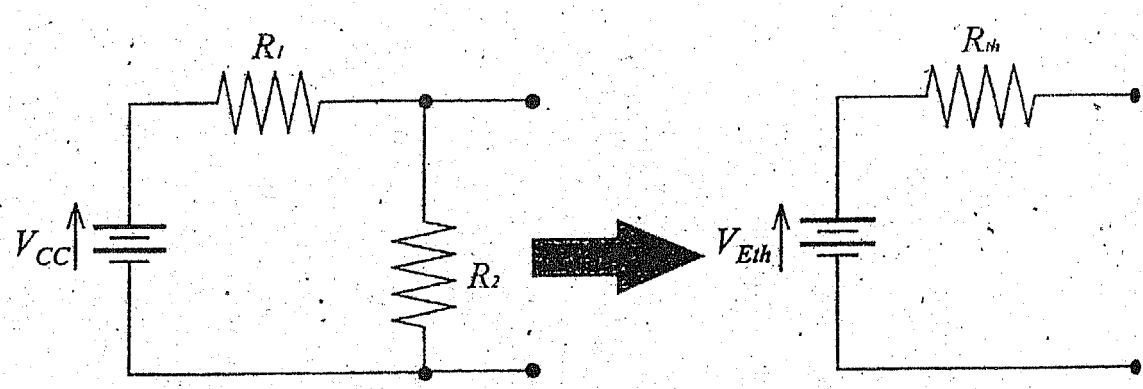


Fig 4. 22

To determine E_{th} , it is given by the open circuit voltage looking into the terminals as shown in Fig 4. 23, which is also equal to V_{R2} .

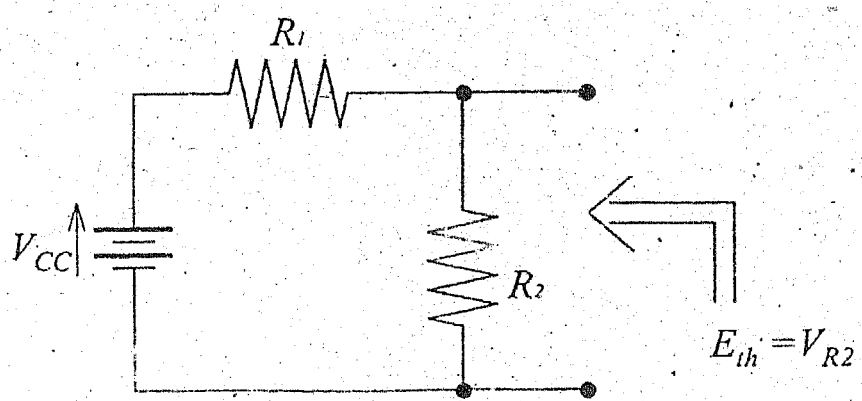


Fig 4. 23

$$E_{th} = V_{R2} = \frac{R_2}{R_1 + R_2} V_{CC}$$

For determining R_{th} , all voltages have to be short circuited as in Fig 4. 24. Then the Thevenin resistance is the equivalent resistance looking into the open circuit terminal which is the parallel resistance of R_1 & R_2 .

$$R_{th} = \frac{1}{R_1} + \frac{1}{R_2} = \frac{R_1 \times R_2}{R_1 + R_2}$$

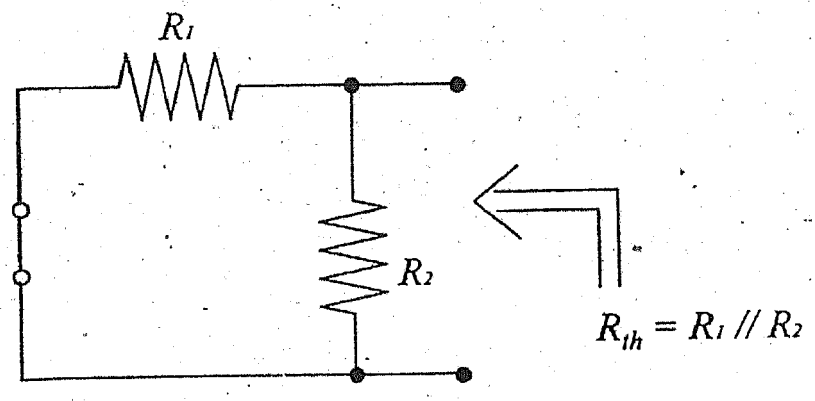


Fig 4. 24

Replace the input circuit by the Thevenin's equivalent circuit we have a simply input loop shown in Fig 4. 25.

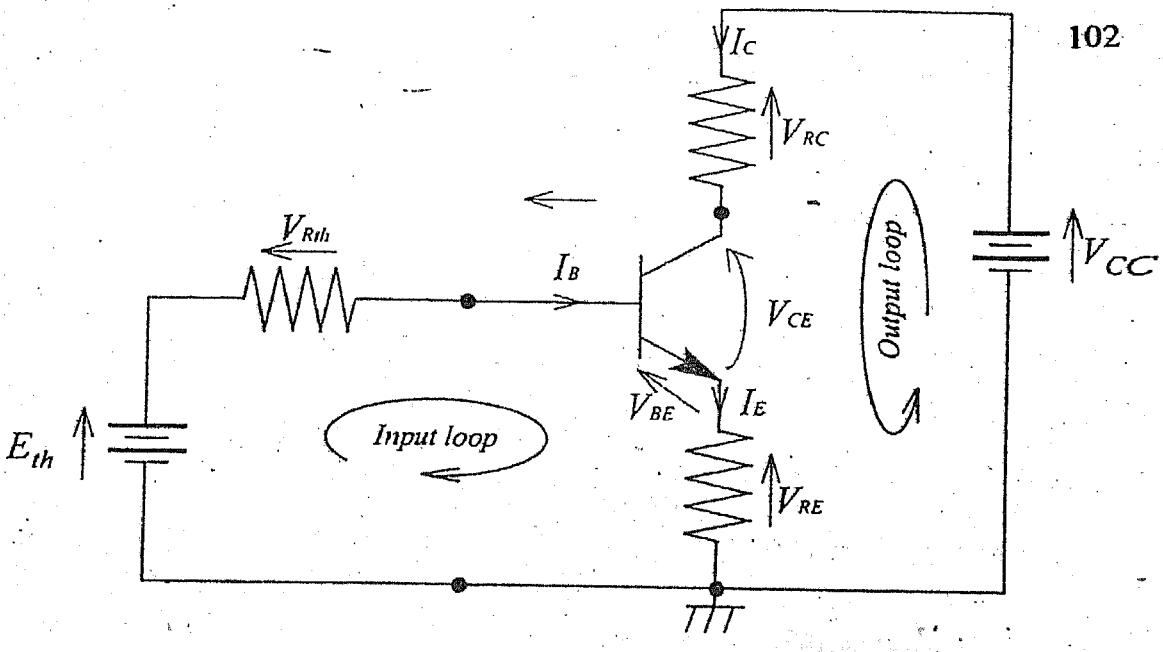


Fig 4. 25

The input loop and output loop equations can now be formed from Fig 4. 25.

Input Loop equation :

$$\overrightarrow{E_{th}} = \overleftarrow{V_{Rth}} + \overleftarrow{V_{BE}} + \overleftarrow{V_{RE}}$$

or

$$E_{th} = I_B R_{th} + V_{BE} + I_E R_E$$

Output Loop equation :

$$\overrightarrow{V_{CC}} = \overleftarrow{V_{RC}} + \overleftarrow{V_{CE}} + \overleftarrow{V_{RE}}$$

or

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

The approach in solving the voltage divider biasing circuit using Thevenin's theorem as discussed above is known as the *Exact* approach. This approach must be used if $\beta R_E < 10R_2$, where I_B is not negligible.

In the case where $\beta R_E \geq 10R_2$, another approach known as the *Approximate* approach can be apply, where I_B is negligible. This approach, V_B can be obtained by voltage divider rule.

$$V_B = \frac{R_2}{R_1 + R_2} V_{CC}$$

and

$$V_B = V_E + V_{BE}$$

Another type of bias arrangement is dc bias with voltage feedback circuit. This type of circuit is a negative feedback connection that provides a relatively stable Q-point by reducing the effect of variations in β_{dc}. Fraction of I_C is fedback to the input through R_B as in Fig 4. 26.

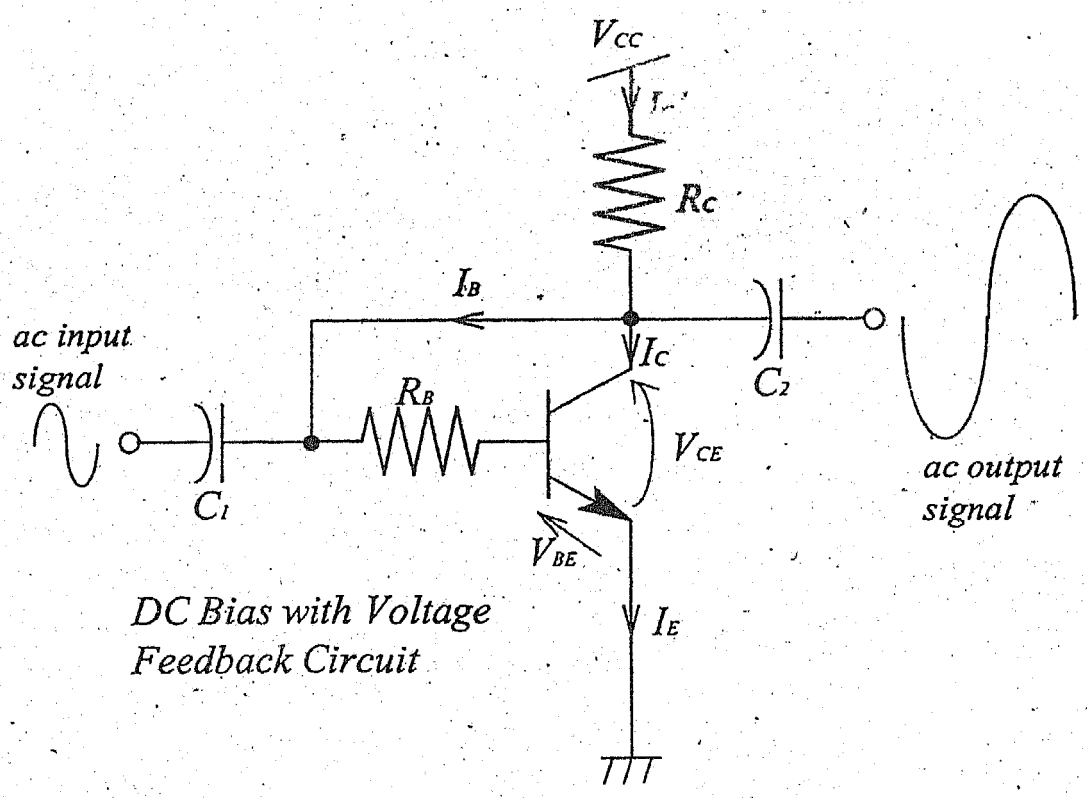


Fig 4. 26

By removing the coupling capacitors, the circuit is simplified into the next circuit shown in Fig 4. 27.

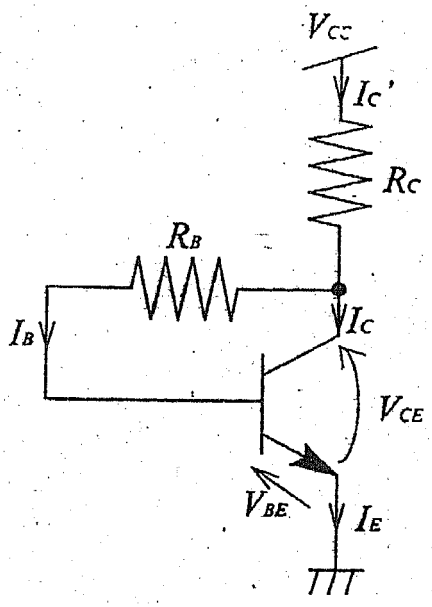


Fig 4. 27

We would like to redraw the circuit to form input & output loop equations. Therefore, the circuit is further re-arranged as shown in Fig 4. 28. Hence, the loop equations can easily be formed.

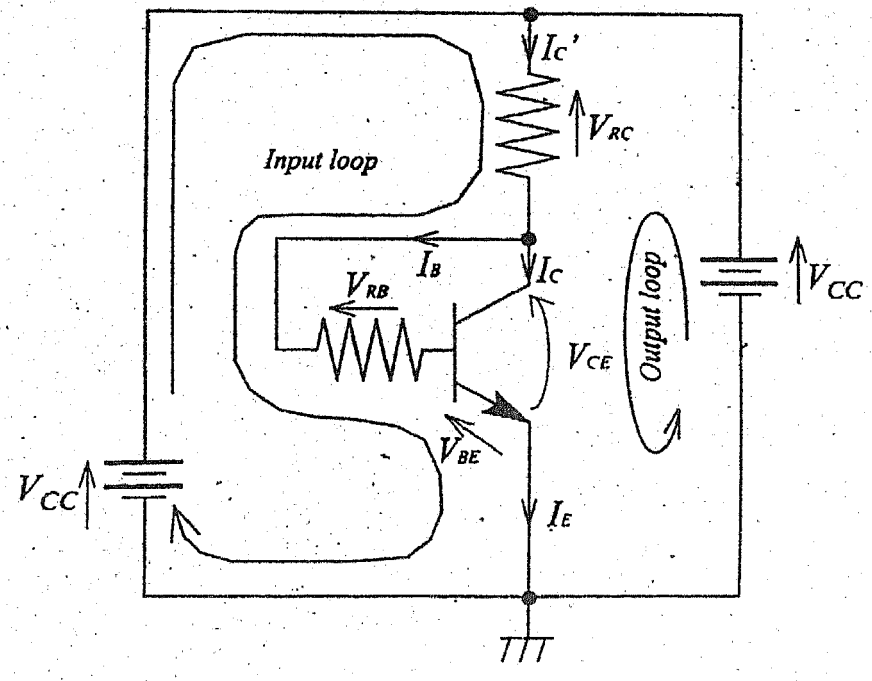


Fig 4. 28

Input Loop Equation :

$$\vec{V_{CC}} = \overleftarrow{V_{RC}} + \overleftarrow{V_{RB}} + \overleftarrow{V_{BE}}$$

or

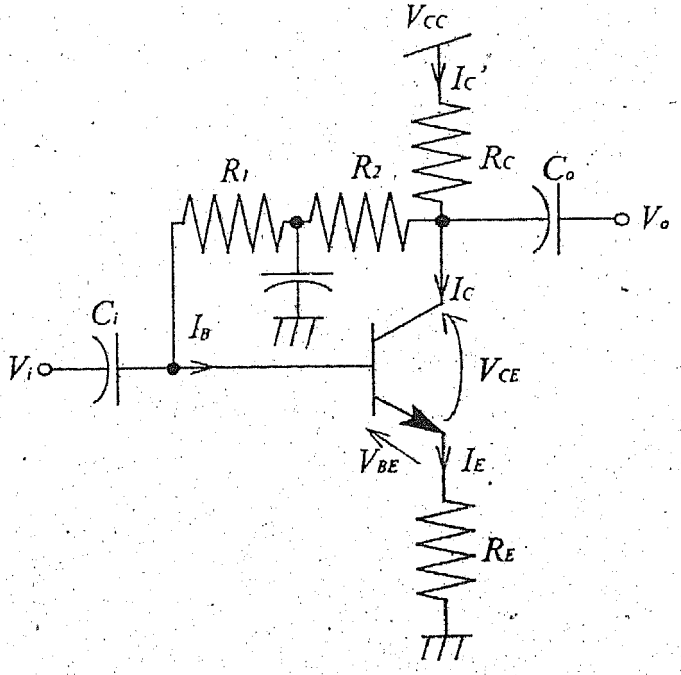
$$V_{CC} = I_C R_C + I_B R_B + V_{BE}$$

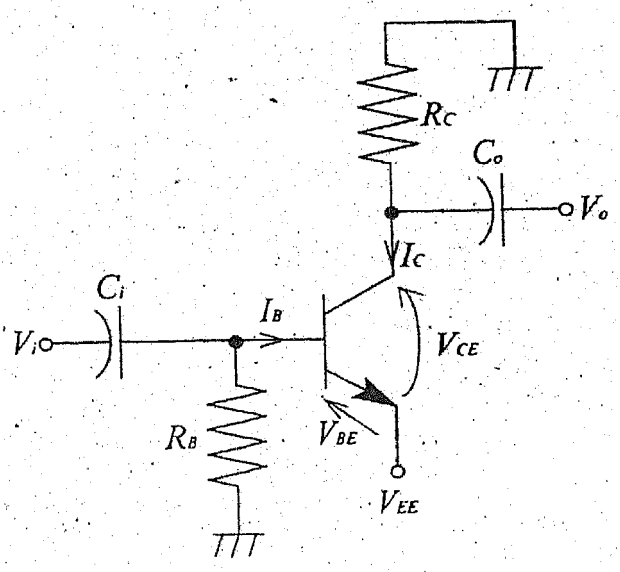
Output Loop Equation :

$$\vec{V_{CC}} = \overleftarrow{V_{RC}} + \overleftarrow{V_{CE}}$$

or

$$V_{CC} = I_C R_C + V_{CE}$$


V_{CC}
I_C'
R_C
C_o
R_1
R_2
V_o
I_C
C_i
I_B
V_i
V_{CE}
V_{BE}
I_E
R_E


R_C
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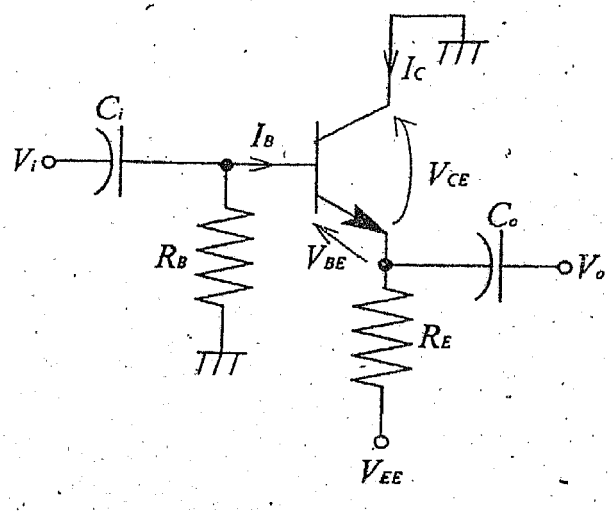
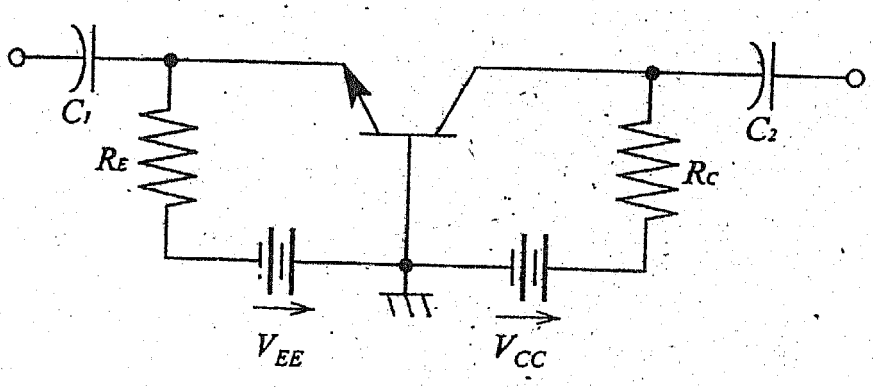
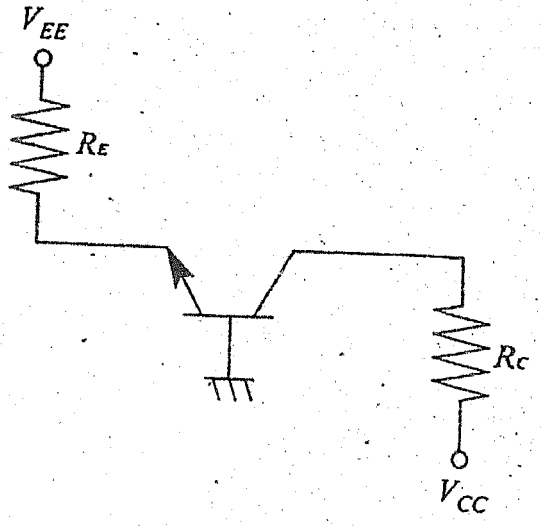
C_i
I_B
V_i
V_{CE}
R_B
V_{BE}
V_{EE}


I_C
C_i
V_i
I_B
V_{CE}
C_o
R_B
V_{BE}
V_o
R_E
V_{EE}


C_1
C_2
R_E
R_C
V_{EE}
V_{CC}


V_{EE}
R_E
R_C
V_{CC}