Advanced Micro Devices - AMD

- 1969 – Founded in Sunnyvale,CA with a budget of $100.000
- 1970 – First Proprietary Product: Am2501
- 1973 – First Overseas Manifacturing in Malaysia
- 1975 – Enters the RAM Market, produces Am2900 Family.
- 1987 – AMD merges with Monolithic Inc.
- 1991 – Introduces AMD 386® microprocessor family
- 1993 - AMD and Fujitsu Establishment
- 1993 – First AMD486® produced.
- 1997 – Introduces AMD-K6® processor.
- 1998 – Collaboration with Motorola.
- 1999 – Introduces AMD Athlon™ Processors
- 2000 – 1 GHz limit exceeded.
- 2000 – AMD-760™ Chipset with DDR Memory
- 2001 – First Multiprocessor Platform AMD Athlon™ MP
- 2002 – 0.13 Micron technology emerged
- 2002 – AMD opens AMD Development Center
- 2003 – AMD Opteron processor built on AMD64 Technology
- 2004 – 90nm, blade server, Sempron processor
- 2005 – Dual core, Turion
- 2006 – Spansion FLASH spin, 65nm, Merge w/ATI, quad-core
- 2007 – Barcelona, Opteron 2348 and 2350, Phenom
- 2008 – Phenom II, 45nm

AMD K5 (Wikipedia)

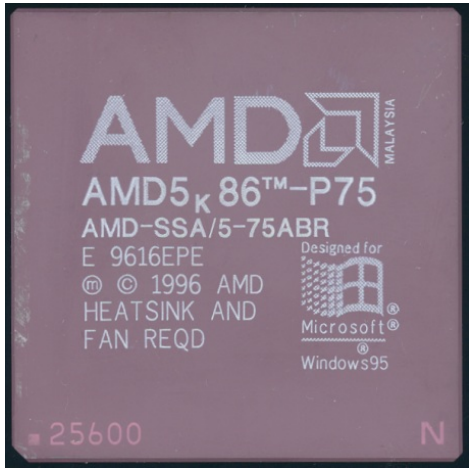
AMD's first in-house x86 processor was the K5 which was launched in 1996.[6] The "K" was a reference to "Kryptonite", which from comic book lore, was the only substance (radioactive pieces of his home planet) which could harm Superman, a clear reference to Intel, which dominated in the market at the time, as "Superman".

The K5 was based upon an internal highly parallel 29k RISC processor architecture with an x86 decoding front-end. The K5 offered good x86 compatibility.

All models had 4.3 million transistors, with five integer units that could process instructions out of order and one floating point unit. The branch target buffer was four times the size of the Pentium's and register renaming improved parallel performance of the pipelines. The chips speculative execution of instructions reduced pipeline stall. It touted an instruction cache of 16 KiB, which was double that of the Pentium. Further, the primary cache was a "4-way" set associative, instead of the Pentium's "2-way" set.

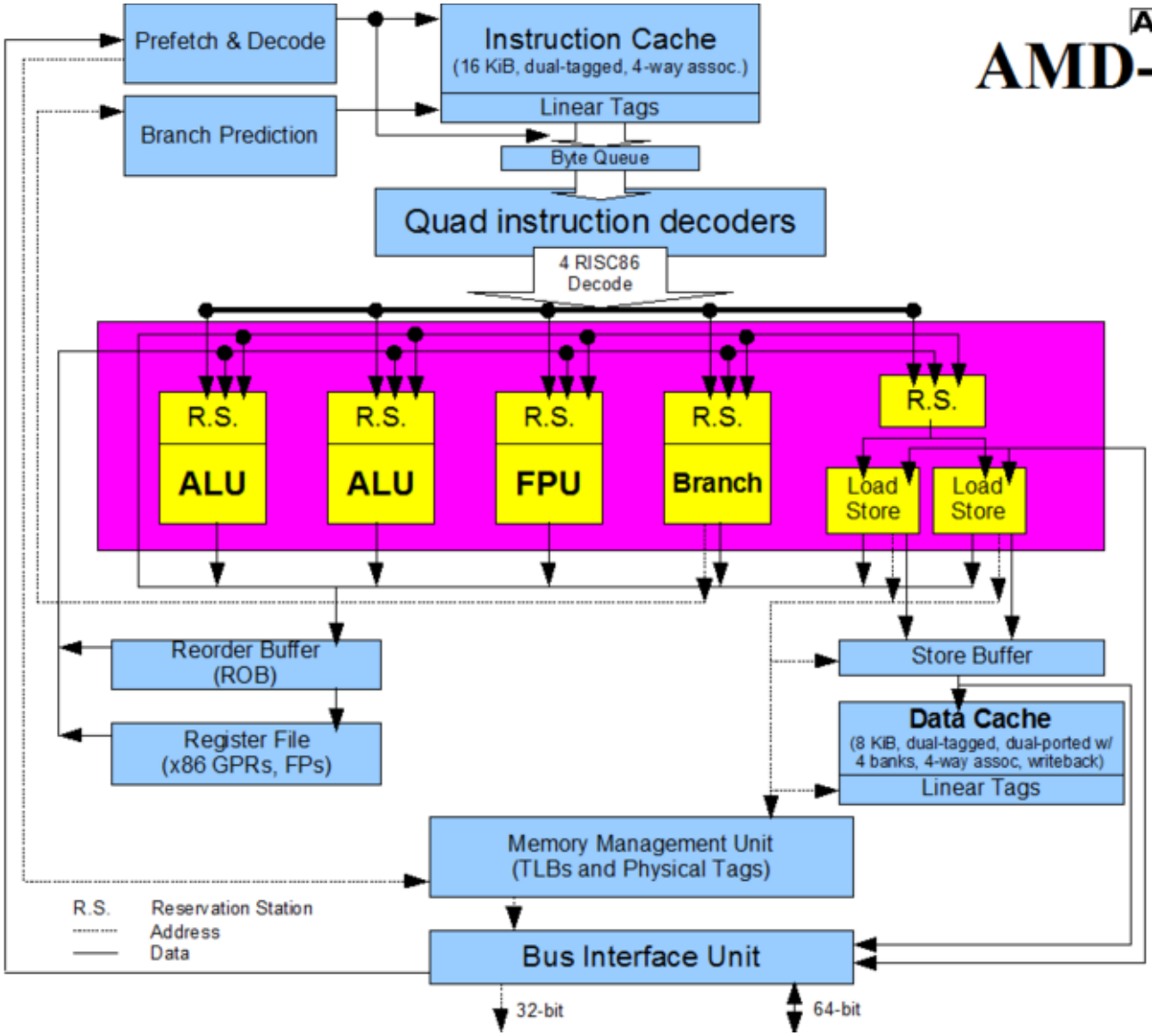
The K5 lacked MMX instructions, which Intel started offering in its Pentium MMX processors that were launched in early 1997. Compared to the Pentium the K5's floating point unit had around 10% less performance clock for clock.

AMD K5



- AMD SSA/5 (K5)
  - March 1996
  - Built by AMD from the ground up
    - Superscalar architecture
    - out of-order speculative execution
    - branch prediction
    - integrated FPU
    - power-management
  - 75-117MHz
  - Ran “hot”
  - 34KB L1 cache
  - 4.5 million transistors
  - .35 micron process

AMD K5 (Wikipedia)



Duron (K6)

- AMD K6 (1997)
  - Based on NexGen's RISC86 core (in the Nx586)
  - Based on Nx586 core
  - 166-300MHz
  - 84KB L1 Cache
  - 8.8 million transistors
  - .25 micron process
  - Advantages of K6 over K5:
    - RISC86 core translates x86 complex instructions into shorter ones, allowing the AMD to reach higher frequencies than the K5 core.
    - Larger L1 cache.
    - New MMX instructions.
- AMD produced both desktop and mobile K6 processors. The only difference being lower processor core voltage for the mobile part

Duron

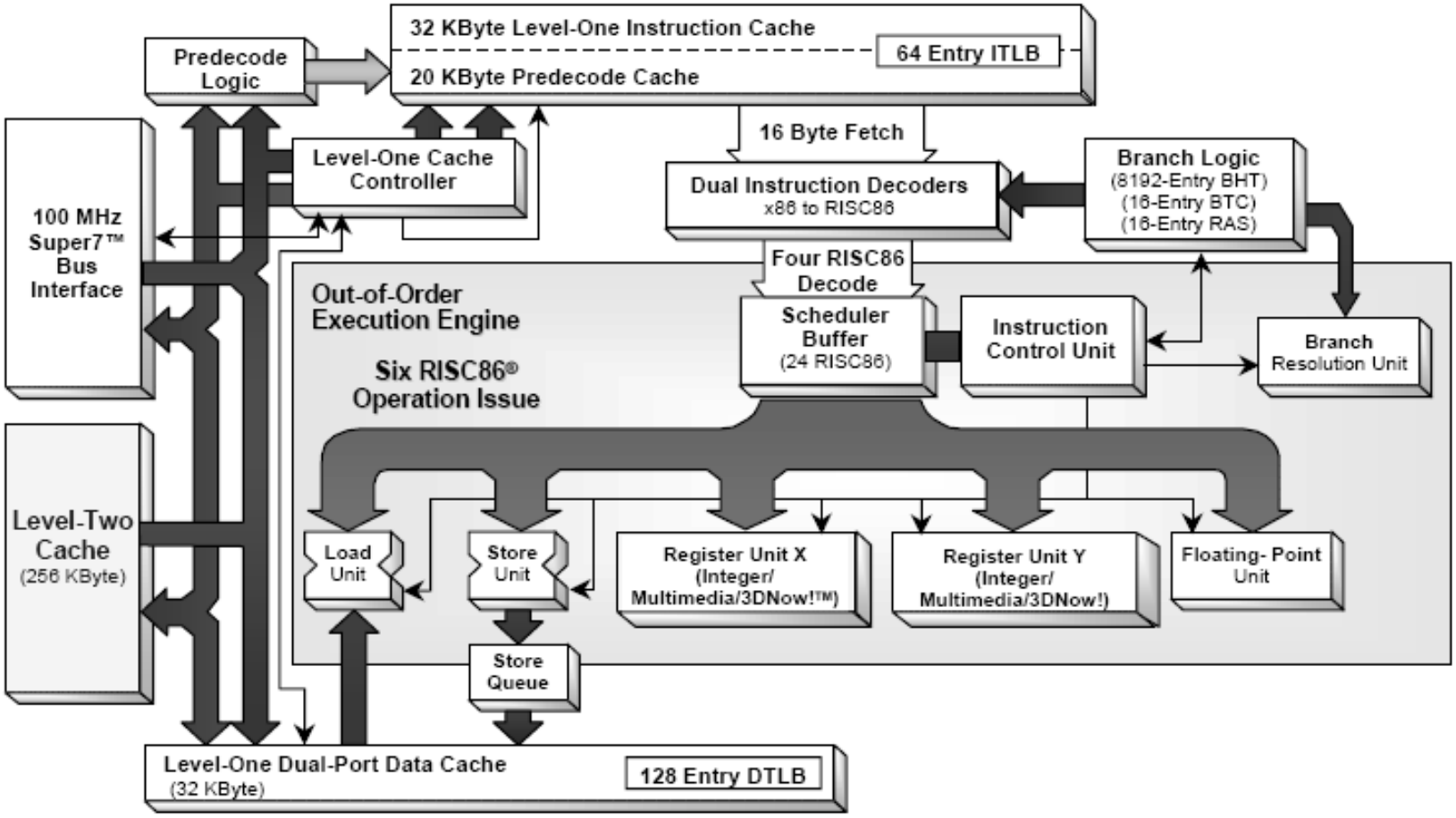
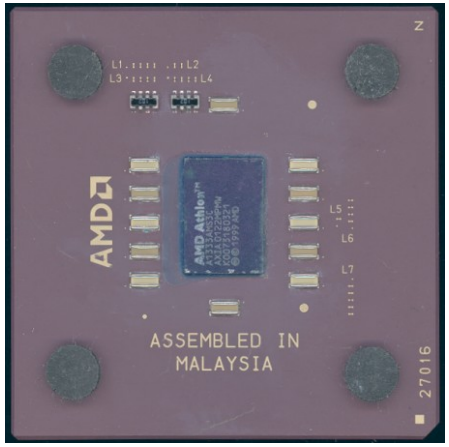


Figure 1. AMD-K6®-III Processor Block Diagram

Athlon K7



- First AMD Athlons, K7 (June 23, 1999)
  - Based on the K6 core
  - improved the K6's FPU
  - 128 KB (2x64 KB) L1 cache
  - Initially 500-700MHz
  - 8.8 million transistors
  - .25 micron process
  - 1999-2002 held fastest x86 title off and on
  - First to 1GHz clock speed
  - Intel suffered a series of major production, design, and quality control issues at this time.
  - Changed from slot to socket format
  - Athlon XP – desktop
  - Athlon XP-M – laptop
  - Athlon MP – server
  - Final (5th) revision, the Barton
  - 400 MHz FSB (up from 200 MHz)
  - Up to 2.2 GHz clock
  - 512 KB L2 cache, off-chip
  - 54.3 million transistors
  - .13 micron process
    - In 2004 AMD began using 90nm process on XP-M

Athlon

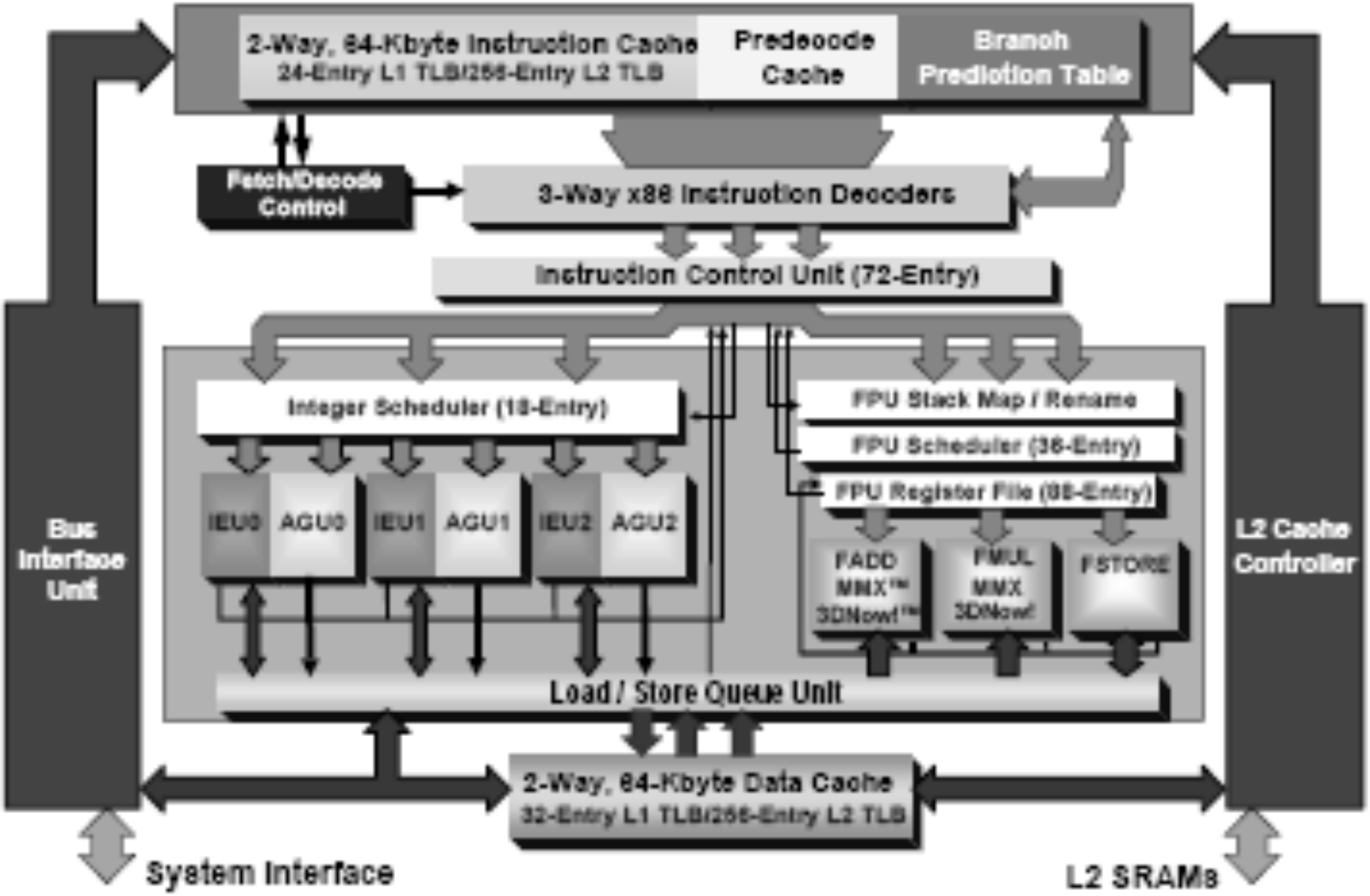


Figure 1. AMD Athlon™ Processor Block Diagram

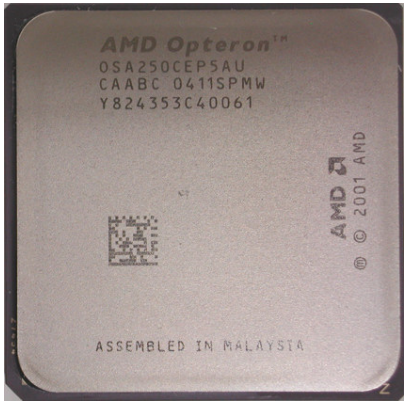
Athlon vs Pentium III

Table 1: Processor Architecture/Technology – Competitive Comparison

	AMD Seventh Generation	Intel Previous Generation
Feature	AMD Athlon™ Processor	Pentium® III * Processor
Operations per clock cycle	9	5
Integer pipelines	3	2
Floating point pipelines	3	1
Full x86 decoders	3	1
L1 cache size	128KB	32KB
L2 cache size	Internal, 256KB	Internal, 256KB
System bus speed	200 MHz – 400+ MHz	100MHz to 133 MHz
Peak bus bandwidth	1.6 to 3.2 GB/s+	533 MB/s to 1.06 GB/s
Bus outstanding transactions	24 per processor	4-8 per processor
Clock technology	Source synchronous (Clock forwarding)	Common clock
3D enhancement instructions	Enhanced 3DNow!™ technology	SSE
- Total no. of instructions	45	71
- Single-precision FP SIMD	Yes	Yes
- 4 FP operations per clock	Yes	Yes
- Cache/prefetch controls	Yes	Yes
- Streaming controls	Yes	Yes
- DSP/comm extensions	Yes	No
Multiprocessing support	Yes, point-to-point	Yes, shared
Max. system processors	Unlimited (by chipset)	Unlimited (by chipset)
No. of transistors per die	~37 million	Up to ~28 million

* Includes estimates for the Intel 0.18-micron Pentium III processors.

The AMD Opteron



- Built on the K8 Core
  - Released April 22, 2003
  - AMD's AMD64 (x86-64) ISA
- Direct Connect Architecture
  - Integrated memory controllers
  - HyperTransport interface
- Native execution of x86 64-bit apps
- Native execution of x86 32-bit apps with no speed penalty!

Direct Connect Architecture

- I/O Architecture for Opteron and Athlon64
- Microprocessors are connected to:
  - Memory through an integrated memory controller.
  - A high performance I/O subsystem via Hypertransport bus
  - To other CPUs via HyperTransport bus

Onboard Memory Control

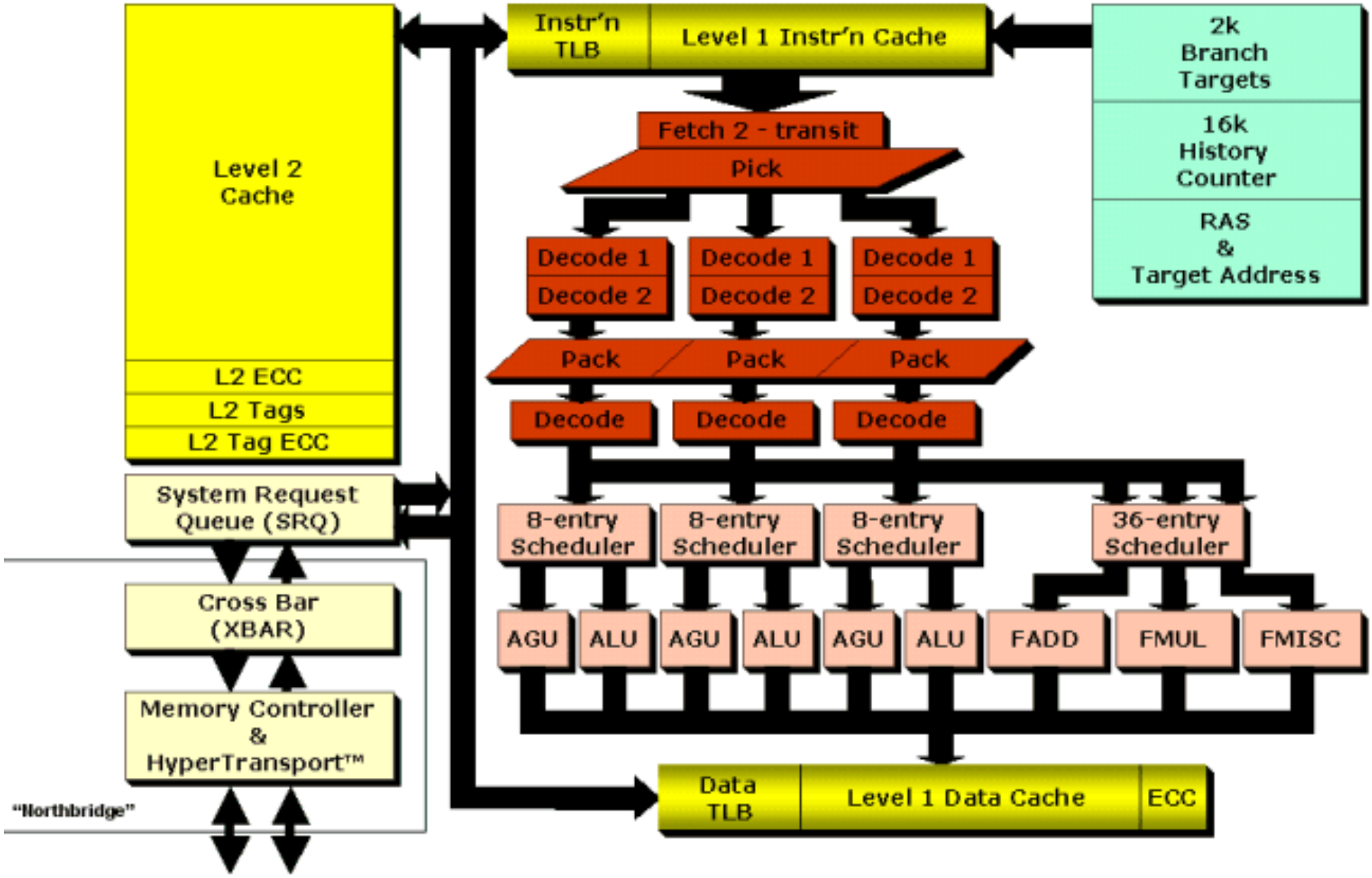
- Processors do not have to go through a northbridge to access memory
- 128-bit memory bus
- Latency reduced and bandwidth doubled
- Multicore: Processors have own memory interface and own memory
- Available memory scales with the number of processors
- DDR-SDRAM only
- Up to 8 registered DDR DIMMs per processor
- Memory bandwidth of up to 5.3 Gbytes/s (with PC2700) per processor.
- 20% improvement over Athlon just due to integrated memory

Changes From K7 to K8

The K8 was the first implementation of the AMD64 64-bit extension to the x86 processor architecture.

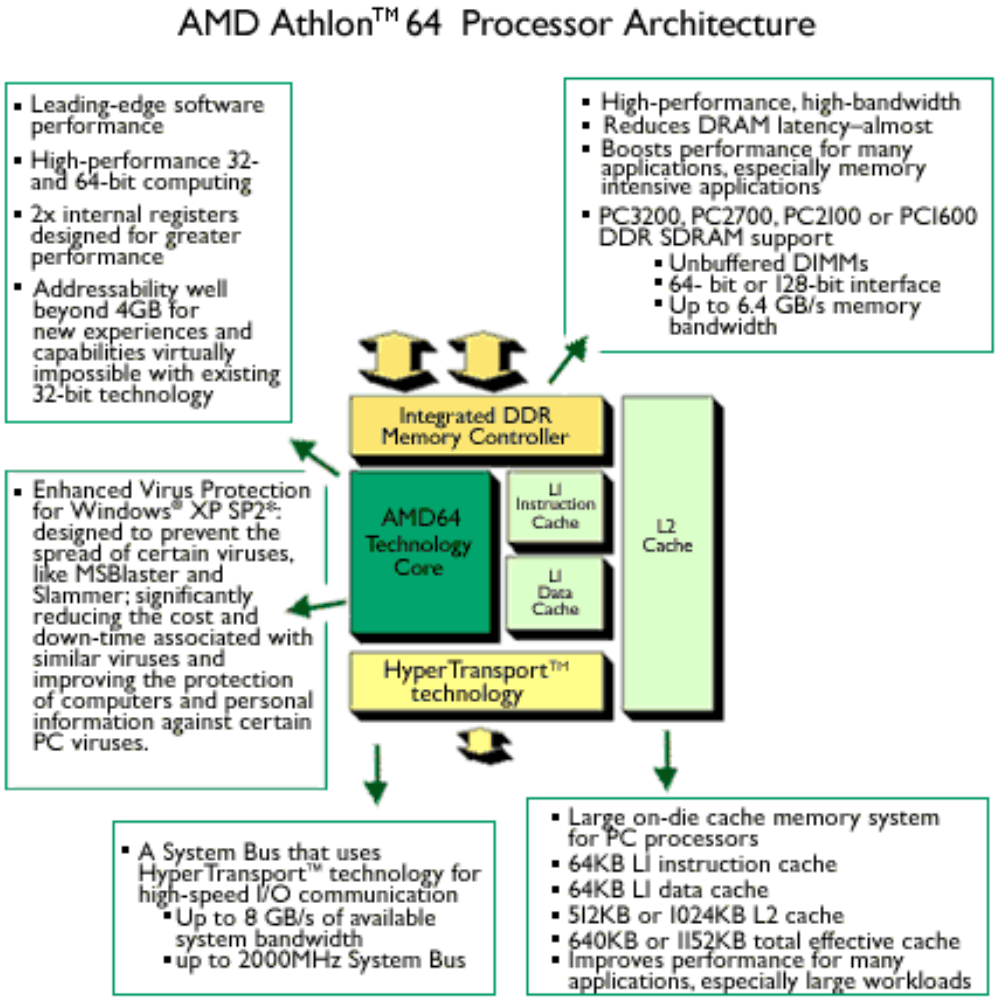
- Deeper & Wider Pipeline
- Better Branch Predictor
- Large workload TLB
- HyperTransport capabilities eliminate Northbridge and allow low latency communication between processors as well as I/O
- Larger L2 cache with higher bandwidth and lower latency
- AMD 64 ISA allowing for 64-bit operation

The K8 Core


Level 2 Cache
L2 ECC
L2 Tags
L2 Tag ECC
System Request Queue (SRQ)
Cross Bar (XBAR)
Memory Controller & HyperTransport™
"Northbridge"
Instr'n TLB
Level 1 Instr'n Cache
2k Branch Targets
16k History Counter
RAS & Target Address
Fetch 2 - transit
Pick
Decode 1
Decode 2
Decode 1
Decode 2
Decode 1
Decode 2
Pack
Pack
Pack
Decode
Decode
Decode
8-entry Scheduler
8-entry Scheduler
8-entry Scheduler
36-entry Scheduler
AGU
ALU
AGU
ALU
AGU
ALU
FADD
FMUL
FMISC
Data TLB
Level 1 Data Cache
ECC

A64

AMD Athlon™ 64 Processor
Key Architectural Features



The AMD64 core provides leading-edge 32-bit performance and support for future 64-bit applications

A64

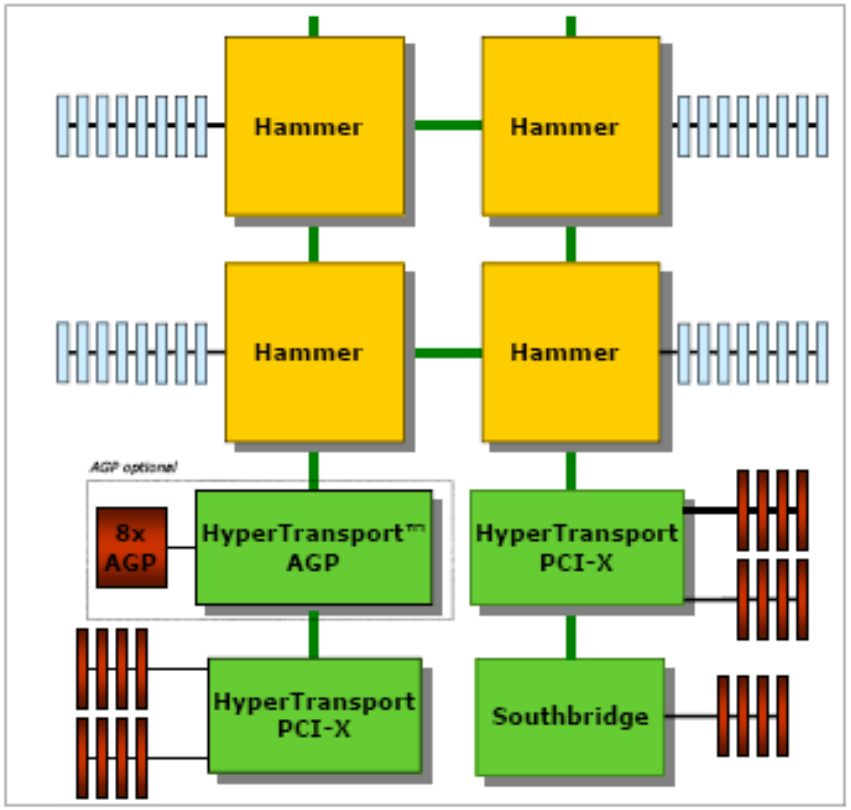


Figure 3: Four-Processor Hammer Processor System Architecture

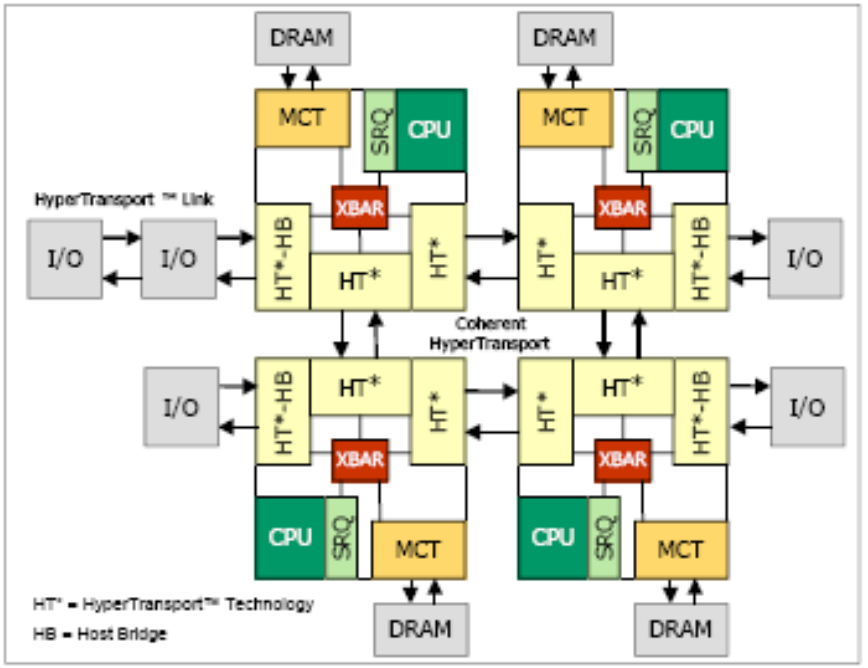


Figure 4: Four-processor Hammer Processor System with Northbridge Blocks

The integrated memory controller results in much higher bandwidth when compared to AMD's previous processor generations and significantly lowers latencies from processor to memory, and yields a considerable increase in delivered performance as advances are made in memory technology.

HyperTransport

- Bidirectional, serial/parallel, scalable, high-bandwidth low-latency bus
- Packet based
  - 32-bit words regardless of physical width
- Facilitates power management and low latencies
- 16 CAD HyperTransport (16-bit wide, CAD=Command, Address, Data)
  - processor-to-processor and processor-to- chipset
  - bandwidth of up to 6.4 GB/s (per HT port)
  - 50% more than what the latest Pentium 4 or Xeon processors
- 8-bit wide HyperTransport for components such as normal I/O-Hubs
- Number of HyperTransport channels

  (up to 3) determined by number of CPUs
  - 19.2 Gbytes/s of peak bandwidth per proccessor
- All are bi-directional, quad-pumped
- Low power consumption (1.2 W) reduces system thermal budget

Opteron – PhenomK10

AMD released the first dual core Opteron, an x86-based server CPU, on April 21, 2005.[11] The first desktop-based dual core processor family — the Athlon 64 X2 — came a month later.[12] In early May 2007, AMD had abandoned the string "64" in its dual-core desktop product branding, becoming Athlon X2, downplaying the significance of 64-bit computing in its processors while upcoming updates involves some of the improvements to the microarchitecture, and a shift of target market from mainstream desktop systems to value dual-core desktop systems. AMD has also started to release dual-core Sempron processors in early 2008 exclusively in China, branded as Sempron 2000 series, with lower HyperTransport speed and smaller L2 cache, thus the firm completes its dual-core product portfolio for each market segment.

The AMD microprocessor architecture, known as K10, became the successor to the K8 microarchitecture. The first processors released on this architecture were introduced on September 10, 2007 consisting of nine quad-core Third Generation Opteron processors. This was followed by the Phenom processor for desktop. K10 processors come in dual, triple-core,[13] and quad-core versions with all cores on one single die.

Improvements

In April 2010, AMD released a new Phenom II hexa-core (6-core) processor codenamed "Thuban". This was a totally new die based on the hexa-core “Istanbul” Opteron processor. It included AMD's “turbo core” technology, which allows the processor to automatically switch from 6 cores to 3 faster cores when more pure speed is needed. AMD's Enthusiast platform, codenamed “Leo”, utilized the new Phenom II, a new chipset from the AMD 800 chipset series and an ATI “Cypress” GPU from the Evergreen (GPU family) GPU series.

The Magny Cours and Lisbon server parts were released in 2010. The Magny Cours part came in 8 to 12 cores and the Lisbon part came in 4 and 6 core parts. Magny Cours is focused on performance while the Lisbon part is focused on high performance per watt. Magny Cours is an MCM (Multi-Chip Module) with two hexa-core “Istanbul” Opteron parts. This will use a new G34 socket for dual and quad socket processors and thus will be marketed as Opteron 61xx series processors. Lisbon uses C32 socket certified for dual socket use or single socket use only and thus will be marketed as Opteron 41xx processors. Both built on a 45 nm SOI process.

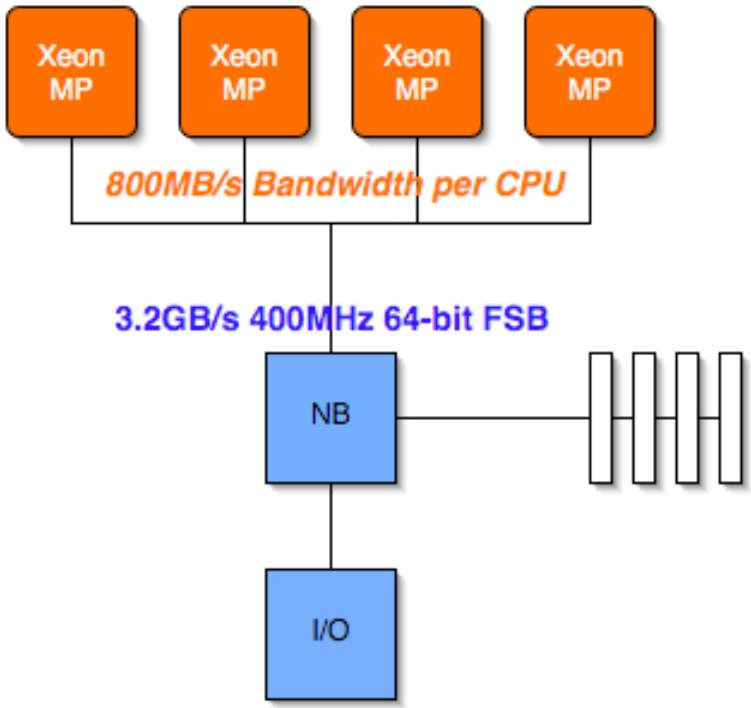
Improvements

Fusion, Llano and ARM:
After the merger between AMD and ATI, an initiative codenamed Fusion was announced that merges a CPU and GPU on some of their mainstream chips, including a minimum 16 lane PCI Express link to accommodate external PCI Express peripherals, thereby eliminating the requirement of a northbridge chip completely from the motherboard. Some of the processing originally done on the CPU (e.g. floating-point unit operations) moved to the GPU, which is better optimized for calculations such as floating-point unit calculations. This is referred to by AMD as an accelerated processing unit (APU).

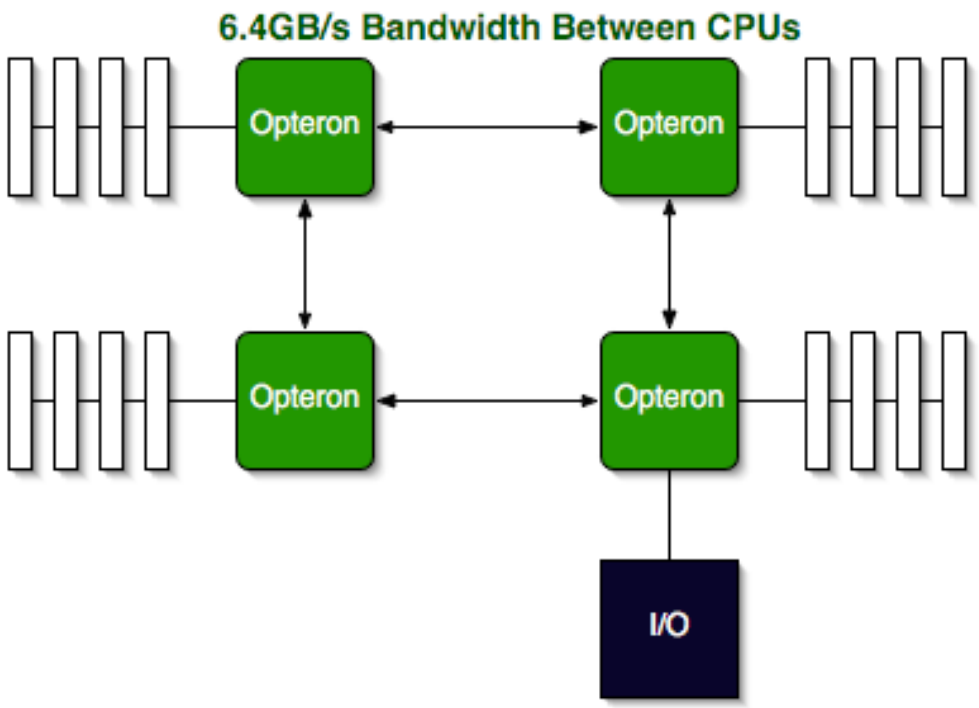
Llano is the second APU released. This incorporates a CPU and GPU on the same die, as well as the northbridge functions, and labeled on AMD's new timeline as using "Socket FM1" with DDR3 memory. This is, however, not based on the new bulldozer core and is in fact be similar to the current Phenom II "Deneb" processor serving as AMD's high-end processor. On September 28, 2011, AMD said that the third quarter of 2011 won't have a 10% revenue increase as AMD planned before, because of the manufacturing problem with the 32 nm Llano Fusion chips.

ARM architecture-based chip:
AMD intends to release an ARM chip in 2014 for use in servers as a low-power alternative to current x86 chips as part of a strategy to regain lost market share in the server chip business.

FSB Bottleneck



Intel's Xeon



AMD's Opteron

AMD Athlon™ Processors
Technical Specifications

AMD

Features	AMD Athlon™ 64 FX	AMD Athlon™ 64	AMD Athlon™ XP
Architecture Introduction	2003	2003	1999
Infrastructure	Socket 940	Socket 754	Socket A
Process Technology	0.13 Micron, SOI	0.13 Micron, SOI	0.13 Micron
Number of transistors	105.9 Million	105.9 Million	54.3 Million
64-bit instruction set support	Yes, AMD64 technology	Yes, AMD64 technology	No
32-bit instruction set support	Yes	Yes	Yes
System Bus Technology	HyperTransport™ technology Full duplex, independent	HyperTransport™ technology Full duplex, independent	Front Side Bus (FSB) Single duplex, bi-directional
Integrated DDR Memory Controller (MCT)	Yes, 128-bit + 16-bit ECC PC3200, PC 2700, PC 2100, or PC1600	Yes, 64-bit + 8-bit ECC PC3200, PC 2700, PC 2100, or PC1600	No, Discrete logic device on motherboard
Total Processor-to-System Bandwidth	HT: 6.4 GB/s @ 1.6GHz MCT: 6.4 GB/s @ 400MHz Total: 12.8 GB/s	HT: 6.4 GB/s @ 1.6GHz MCT: 3.2 GB/s @ 400MHz Total: 9.6 GB/s	Total: 3.2 GB/s @ 400MHz
Integrated Northbridge	Yes, 128-bit data path @ CPU core frequency	Yes, 128-bit data path @ CPU core frequency	No, Discrete logic device on motherboard, 64-bit data path @ 200MHz
High-Performance, On-chip Cache	L1: 128KB L2: 1024KB (exclusive) Total Effective Cache: 1152KB	L1: 128KB L2: 1024KB (exclusive) Total Effective Cache: 1152KB	L1: 128KB L2: 512KB (exclusive) Total Effective Cache: 640KB
3-D and Multimedia Instructions	3DNow!™ Professional technology, SSE2	3DNow! Professional technology, SSE2	3DNow! Professional technology

Links to AMD processors:

K5
http://datasheets.chipdb.org/upload/Unzlbunzl/AMD/18522F%20AMD-K5.pdf

K6
http://www.cs.albany.edu/~sdc/CSI404/20695h.pdf

K7 – Athlon
http://www.fh-sw.de/sw/fachb/et/halbl/rechnertechnik/K7_2.pdf

K8 – Athlon 64
http://vidcat.org/user_data/4751b1919985d9be22250e0705f5c929e72091c0.pdf

Newest processors
http://developer.amd.com/resources/documentation-articles/developer-guides-manuals/