# Sequential circuit

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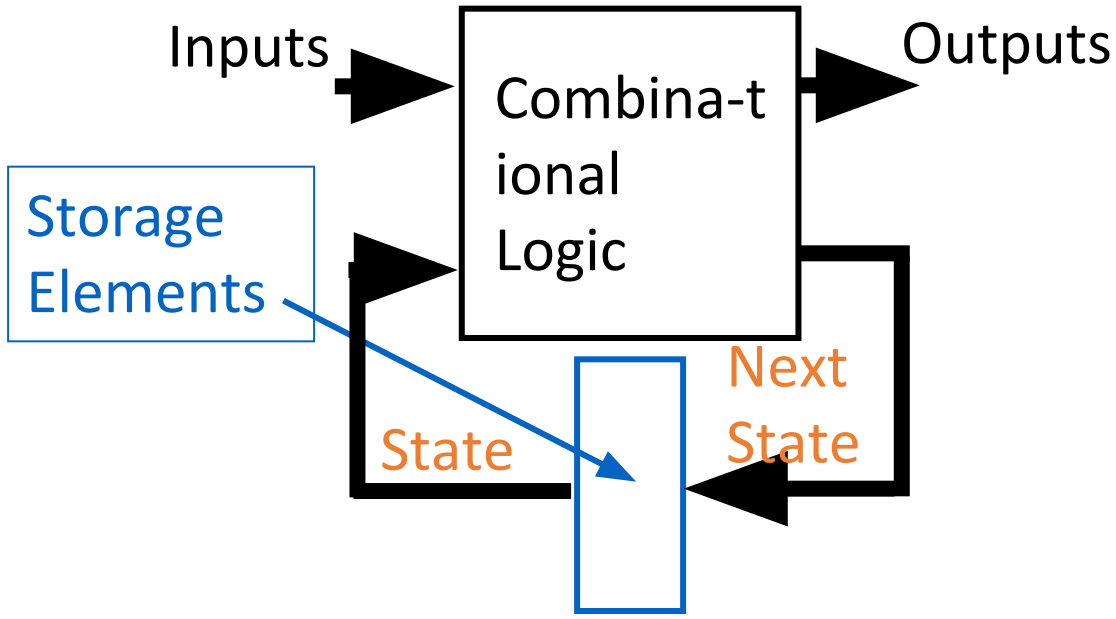
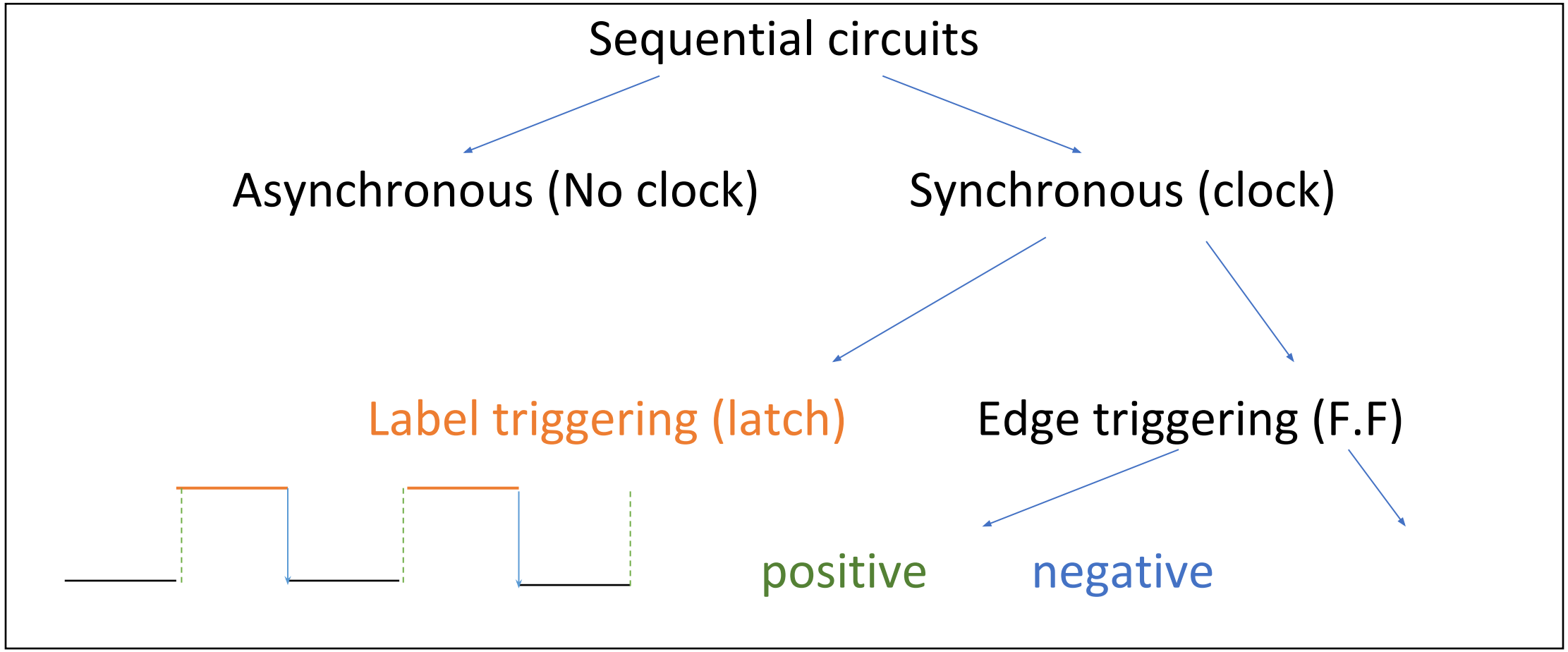
# Concept of sequential circuits

- Next state depends on current state
- Stores current state in a memory (Latch / Flipflop)

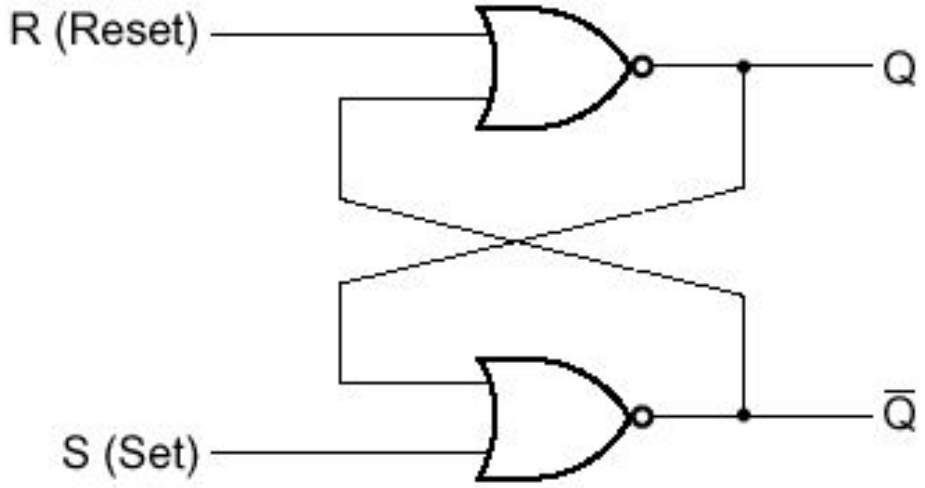


# Types of sequential circuits



# Basic (NOR) S-R Latch

- When S=0 and R=0, the SR-Latch is in *Memory state*
- When S=1 and R=0, the SR-Latch is in the *Set state*
- When S=0 and R=1, the SR-Latch is in the *Reset state*
- S=1 and R=1 generates illogical results




(a) Logic diagram

| S | R | Q | $\overline{Q}$ | |
|---|---|---|---|---|
| 1 | 0 | 1 | 0 | Set state |
| 0 | 0 | 1 | 0 | Memory |
| 0 | 1 | 0 | 1 | Reset state |
| 0 | 0 | 0 | 1 | Memory |
| 1 | 1 | 0 | 0 | Undefined |

(b) Function table

| S | R | Q | $\overline{Q}$ | |
|---|---|---|---|---|
| 1 | 0 | 1 | 0 | Set state |
| 0 | 0 | 1 | 0 | |
| 0 | 1 | 0 | 1 | Reset state |
| 0 | 0 | 0 | 1 | |
| 1 | 1 | 0 | 0 | Undefined |

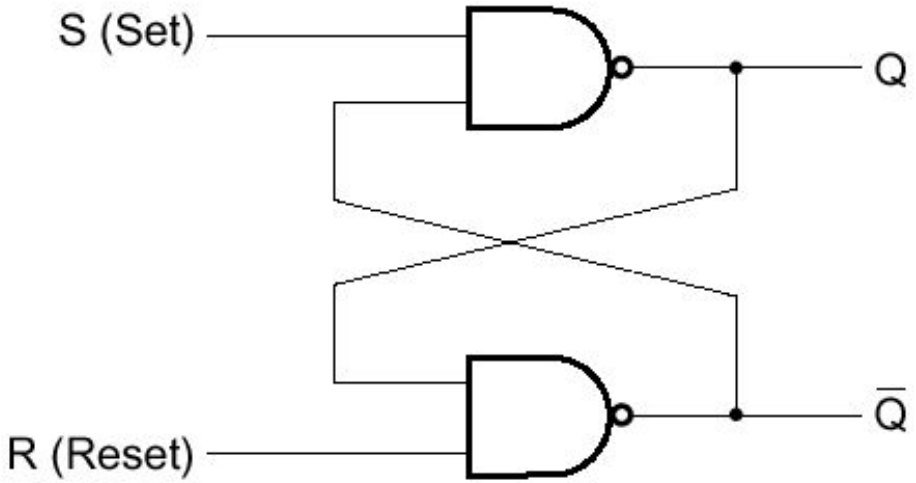
(b) Function table

Time

| R | S | Q | $\overline{Q}$ | Comment |
|---|---|---|---|---|
| 0 | 0 | ? | ? | Stored state unknown |
| 0 | 1 | 1 | 0 | “Set” Q to 1 |
| 0 | 0 | 1 | 0 | Now Q “remembers” 1 |
| 1 | 0 | 0 | 1 | “Reset” Q to 0 |
| 0 | 0 | 0 | 1 | Now Q “remembers” 0 |
| 1 | 1 | 0 | 0 | Both go low |
| 0 | 0 | ? | ? | Unstable! |

# Basic (NAND) S-R Latch / $\overline{S}\,\overline{R}$ Latch

- When S=1 and R=1, the SR-Latch is in *Memory state*
- When S=0 and R=1, the SR-Latch is in the *Set state*
- When S=1 and R=0, the SR-Latch is in the *Reset state*
- S=0 and R=0 generates illogical results

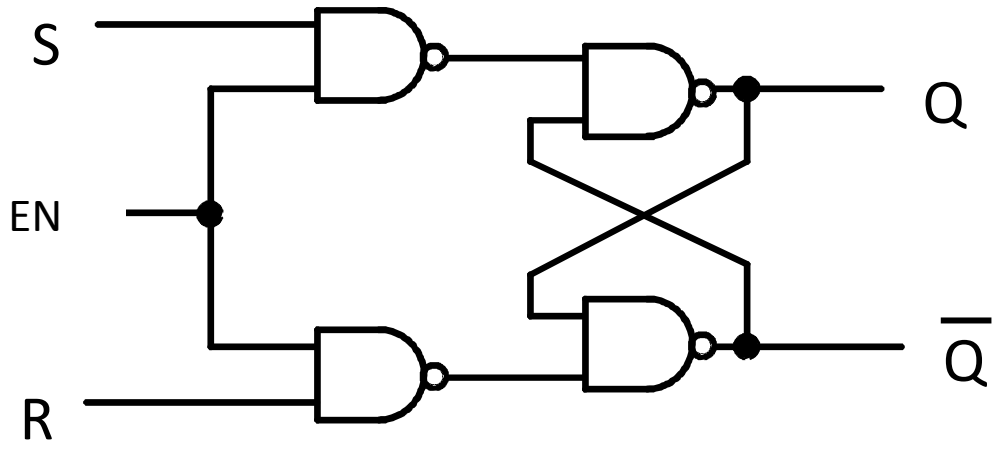



(a) Logic diagram

| S | R | Q | $\overline{Q}$ | |
|---|---|---|---|---|
| 0 | 1 | 1 | 0 | Set state |
| 1 | 1 | 1 | 0 | Memory |
| 1 | 0 | 0 | 1 | Reset state |
| 1 | 1 | 0 | 1 | Memory |
| 0 | 0 | 1 | 1 | Undefined |

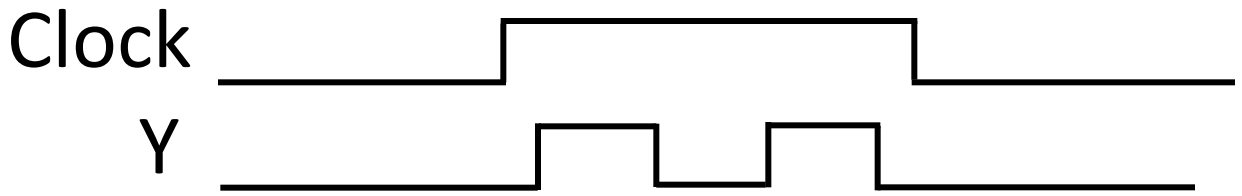
(b) Function table

# S-R latch with control (Enable)




| Enable | S | R | Q | $\overline{Q}$ |
|---|---|---|---|---|
| 0 | 0 | 0 | Memory | |
| 0 | 0 | 1 | Memory | |
| 0 | 1 | 0 | Memory | |
| 0 | 1 | 1 | Memory | |
| 1 | 0 | 0 | Memory | |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | Not Used | |

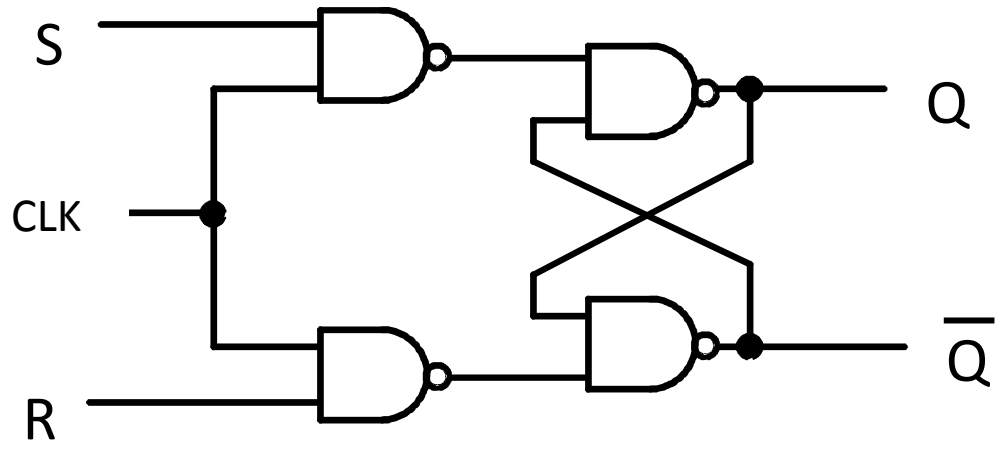
# Latch timing problem




- Solution:

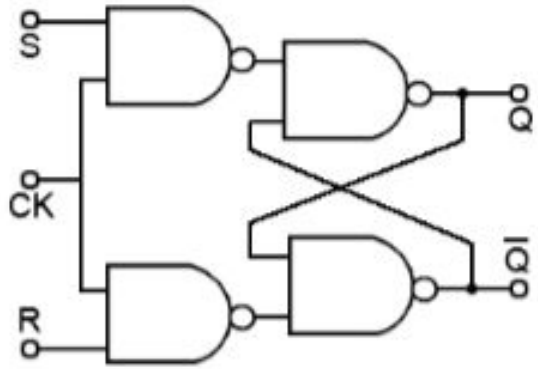
-- Flipflop (Edge triggered)

# S-R flipflop with clock




| CLK | S | R | Q | $\overline{Q}$ |
|---|---|---|---|---|
| 0 | 0 | 0 | Memory | |
| 0 | 0 | 1 | Memory | |
| 0 | 1 | 0 | Memory | |
| 0 | 1 | 1 | Memory | |
| 1 | 0 | 0 | Memory | |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | Not Used | |

# Truth table of S-R flipflop




**TRUTH TABLE**

| S | R | $Q_N$ | $Q_{N+1}$ |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | - |
| 1 | 1 | 1 | - |

# D-flipflop

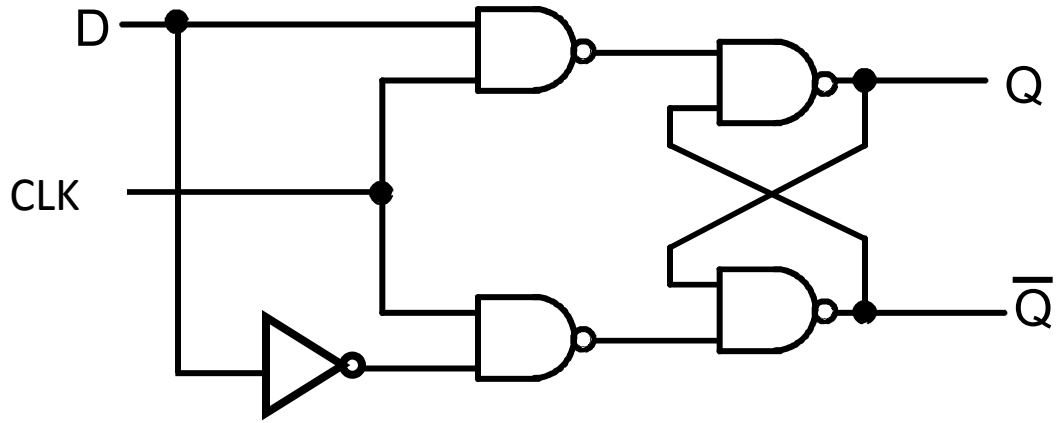
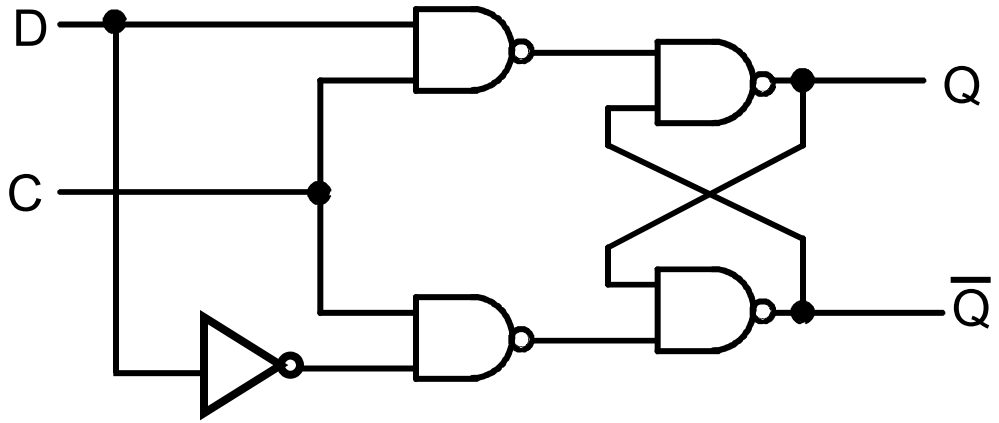



Table of truth:

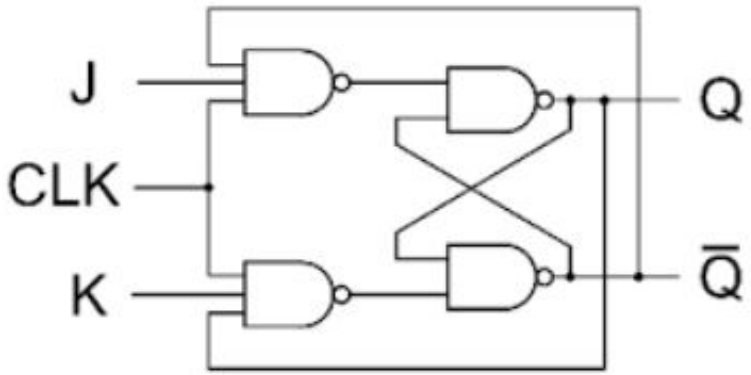
| clk | D | Q | $\overline{Q}$ | |
|---|---|---|---|---|
| 0 | 0 | Q | $\overline{Q}$ | Memory |
| 0 | 1 | Q | $\overline{Q}$ | Memory |
| 1 | 0 | 0 | 1 | Reset |
| 1 | 1 | 1 | 0 | Set |

# Truth table of D flipflop




| Q | D | Q(t+1) |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

# J-K flipflop with truth table



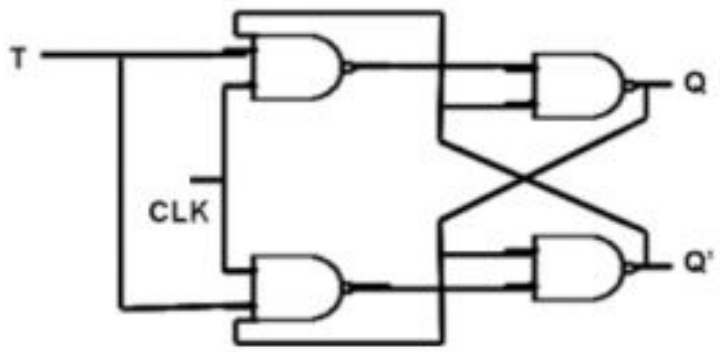

A JK flip-flop has the characteristic table below:

| J | K | Q(t+1) |
|---|---|---|
| 0 | 0 | Q(t) |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | Q(t)' |

**TRUTH TABLE**

| J | K | $Q_N$ | $Q_{N+1}$ |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

# T flipflop with truth table




| $T$ | $Q_n$ | $Q_{n+1}$ |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |