BiCMOS

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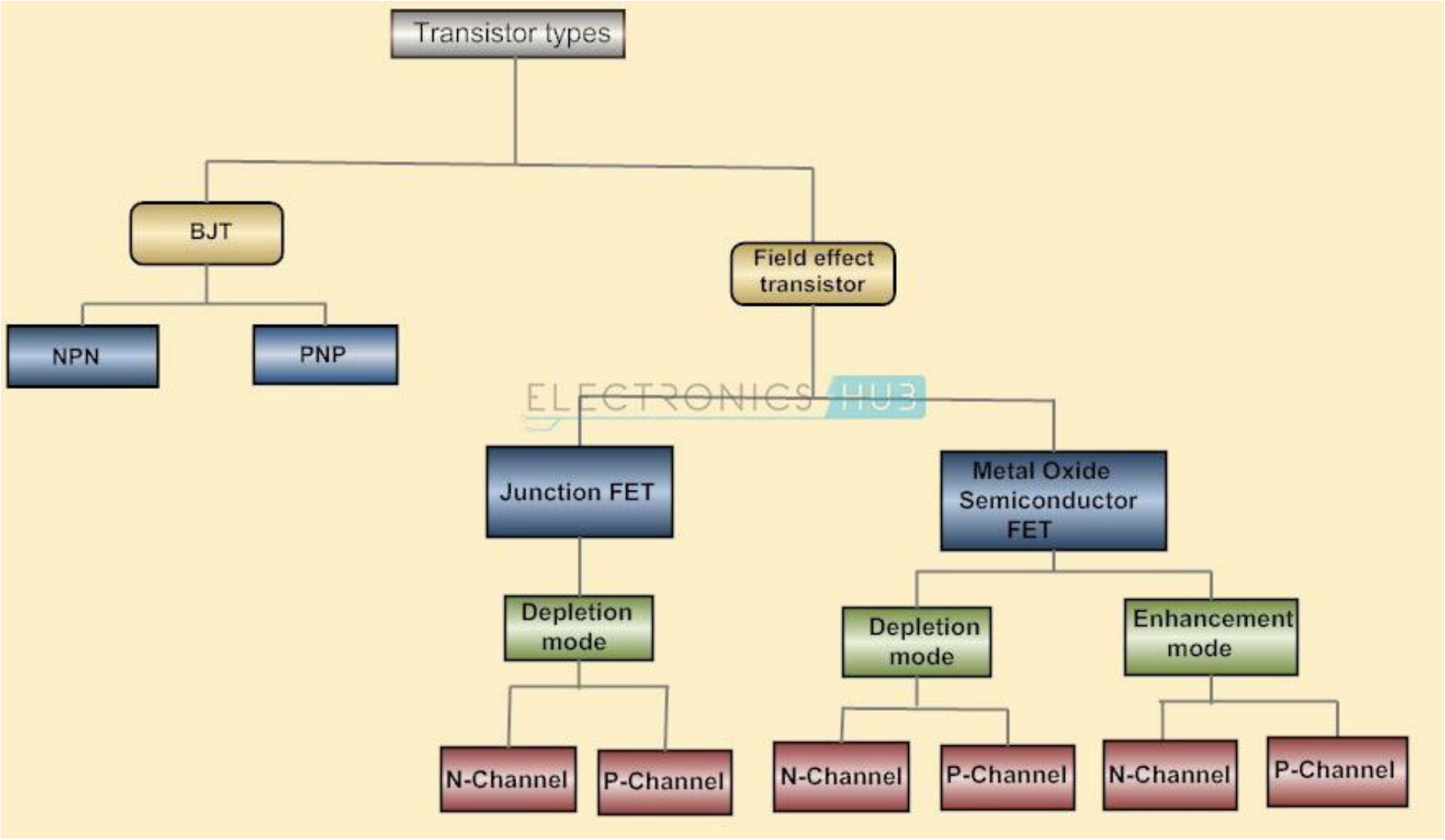
Introduction

- **BiCMOS** is a semiconductor technology that integrates **Bipolar Junction Transistor (BJT)** and **CMOS** transistor in a single integrated circuit device.

- The **objective** of the **BiCMOS** is to combine **BJT** and **CMOS** so as to exploit the advantages of both the technologies.

Types of Transistors



BJT

- **BJT** is a semiconductor device constructed with three doped semiconductor regions (Base, Collector and Emitter) separated by two p-n Junctions.

- In an **NPN** transistor, a thin and lightly doped P-type base is sandwiched between a heavily doped N-type emitter and another N-type collector.

- In a **PNP** transistor, a thin and lightly doped N-type base is sandwiched between a heavily doped P-type emitter and another P-type collector.

*http://fourier.eng.hmc.edu/e84/lectures/ch4/node3.html

BJT…

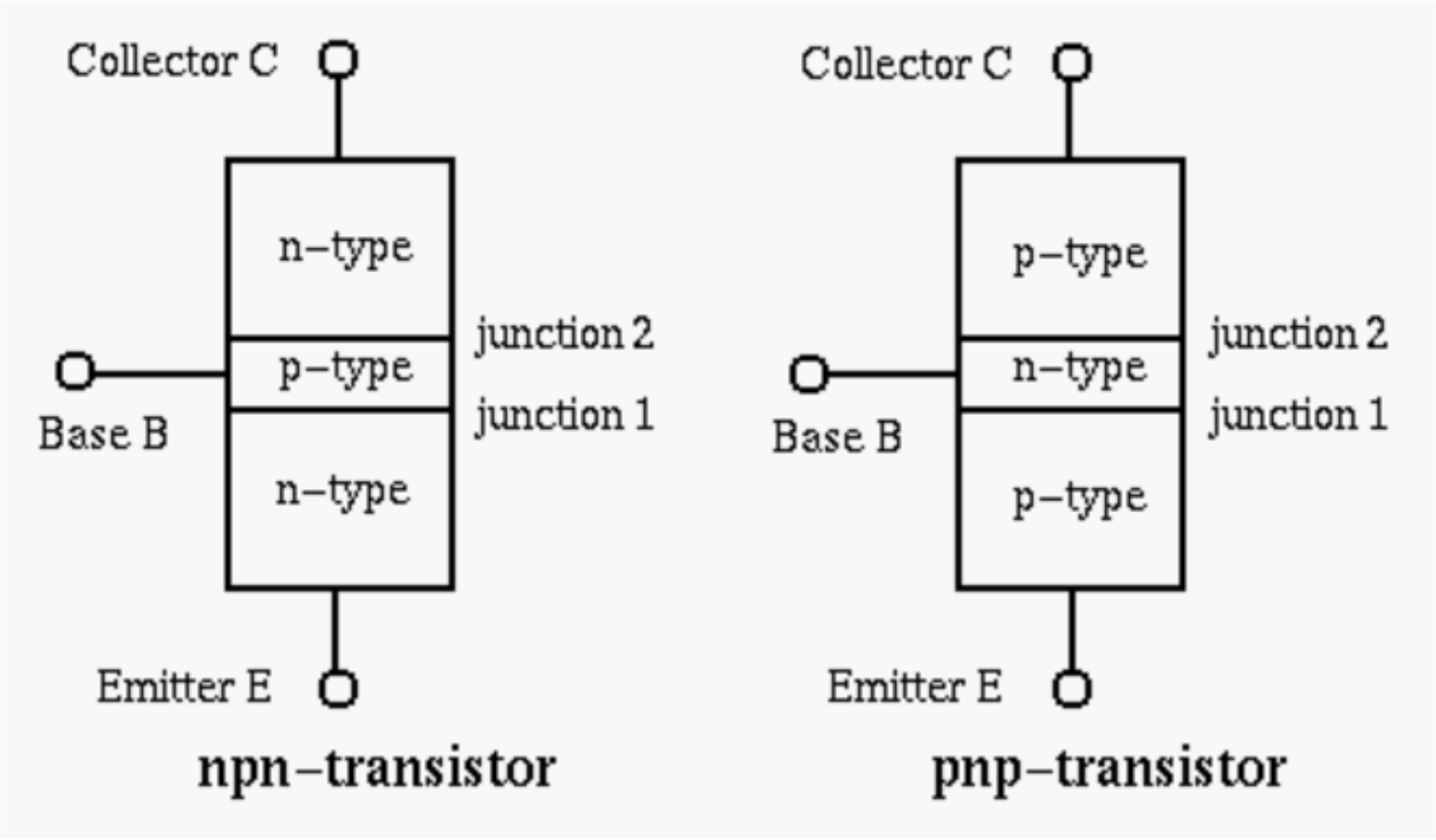


Figure 01: npn and pnp transistor

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Characteristics of CMOS Technology

Lower static power dissipation
Higher noise margins
Higher packing density – lower manufacturing cost per device
High yield with large integrated complex functions

Advantages of CMOS over bipolar

High input impedance (low drive current)
Scaleable threshold voltage
High delay sensitivity to load (fan-out limitations)
Low output drive current (issue when driving large capacitive loads)
Low transconductance, where transconductance, $g_{m} \alpha V_{in}$
Bi-directional capability (drain & source are interchangeable)
A near ideal switching device

Other CMOS Advantages

*http://ggn.dronacharya.info/ECEDept/Downloads/QuestionBank/VIsem/VLSI_Design/Section-A/VLSI_Lecture_9.pdf

Characteristics of Bipolar Technology

Advantages of Bipolar over CMOS

Higher switching speed
Higher current drive per unit area, higher gain
Generally better noise performance and better high frequency characteristics
Better analogue capability
Improved I/O speed (particularly significant with the growing importance of package limitations in high speed systems).

high power dissipation
lower input impedance (high drive current)
low voltage swing logic
low packing density
low delay sensitivity to load
high g_m ($g_m \alpha$ Vin)
high unity gain band width (f_t) at low currents
essentially unidirectional

Other Bipolar Advantages

*http://ggn.dronacharya.info/ECEDept/Downloads/QuestionBank/VIsem/VLSI_Design/Section-A/VLSI_Lecture_9.pdf

Advantages of BiCMOS Technology

- Resulting benefits of BiCMOS technology over solely CMOS or solely bipolar :
  - Improved speed over purely-CMOS technology
  - Lower power dissipation than purely-bipolar technology (simplifying packaging and board requirements)
  - Flexible I/Os (i.e., TTL, CMOS or ECL) –
    BiCMOS technology is well suited for I/O intensive applications.
    ECL, TTL and CMOS input and output levels can easily be generated with no speed or tracking consequences
  - high performance analogue

*http://ggn.dronacharya.info/ECEDept/Downloads/QuestionBank/VIsem/VLSI_Design/Section-A/VLSI_Lecture_9.pdf

BiCMOS Fabrication

The **BiCMOS Fabrication** combines the process of fabrication of **BJT** and **CMOS**:

Step1: P-Substrate is taken as shown in the below figure

P-substrate

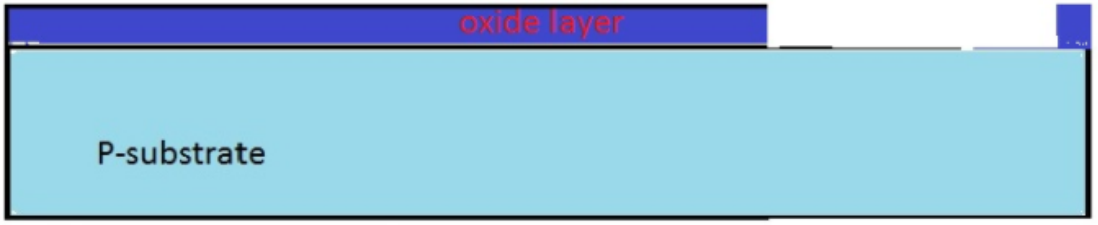
*https://www.elprocus.com/bicmos-technology-fabrication-and-applications/

BiCMOS Fabrication…

Step2: The p-substrate is covered with the oxide layer

P-substrate with oxide layer

Step3: A small opening is made on the oxide layer



Opening is made on the oxide layer

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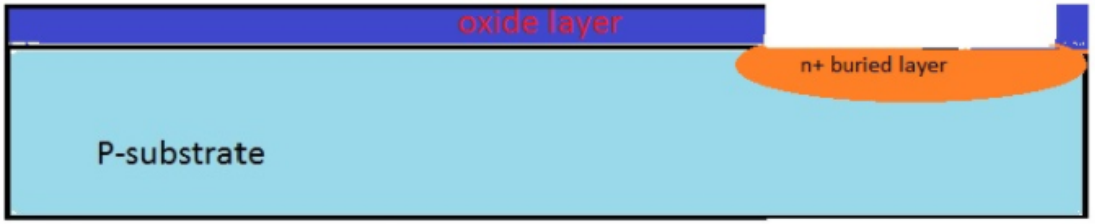
BiCMOS Fabrication…

Step4: N-type impurities are heavily doped through the opening



N-type impurities are heavily doped through the opening

Step5: The P – Epitaxy layer is grown on the entire surface

Epitaxy refers to the deposition of a crystalline over-layer on a crystalline substrate. The over-layer is called an **epitaxial** film or **epitaxial** layer

Epitaxy layer is grown on the entire surface

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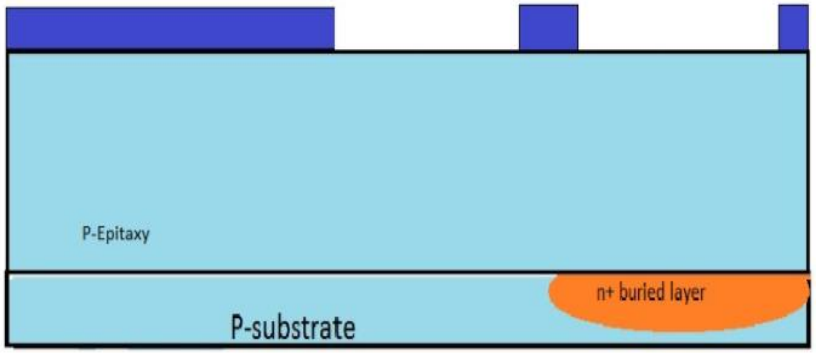
BiCMOS Fabrication…

Step6: Again, entire layer is covered with the oxide layer and two openings are made through this oxide layer.



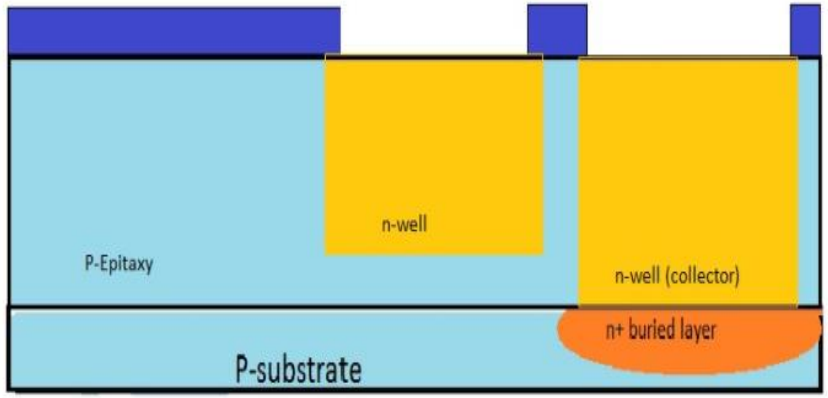
two openings are made through the oxide layer

****Buried layers** are formed within a semiconductor. Metallic or insulating buried layers are produced several microns within a semiconductor substrate. The buried layer can confine current to the buried layer itself by using a conductive material to create the buried layer. The buried layer can also confine current to a specified area of the semiconductor, by using an insulating material inside of the buried layer or by leaving a created void within the material.

*https://www.elprocus.com/bicmos-technology-fabrication-and-applications/
**https://patentimages.storage.googleapis.com/ba/35/66/754cf8a5a35c57/US6208007.pdf

BiCMOS Fabrication…

Step7: From the openings made through oxide layer n-type impurities are diffused to form n-wells



n-type impurities are diffused to form n-wells

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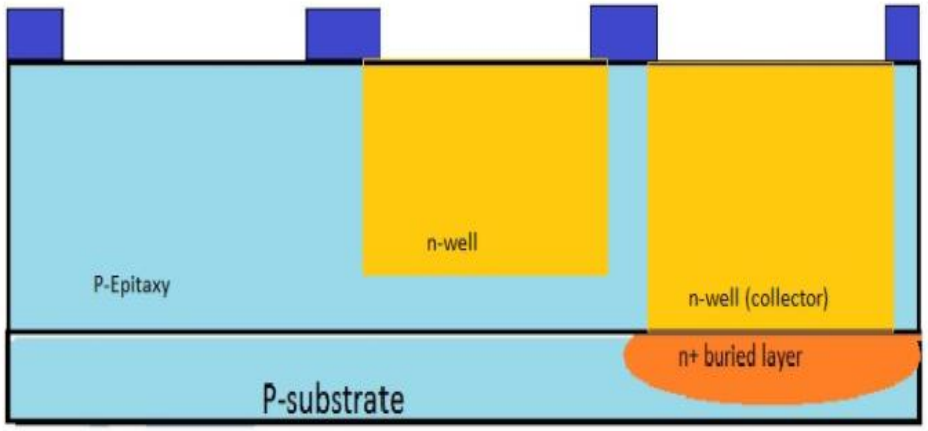
BiCMOS Fabrication…

Step8: Three openings are made through the oxide layer to form three active devices.



Three openings are made through the oxide layer to form three active devices

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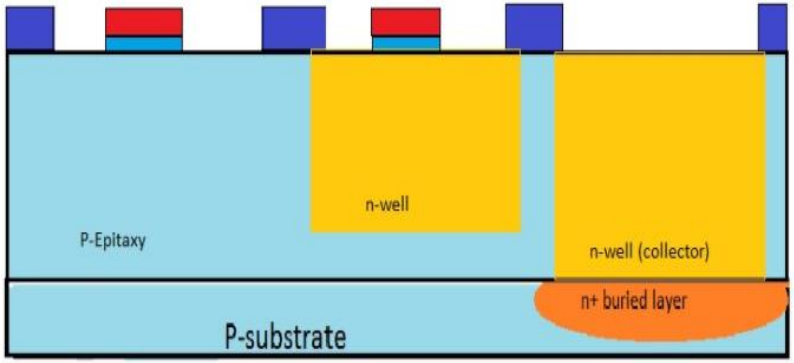
BiCMOS Fabrication…

Step9: The gate terminals of NMOS and PMOS are formed by covering and patterning the entire surface with Thinox and Polysilicon.



The gate terminals of NMOS and PMOS are formed with Thinox and Polysilicon

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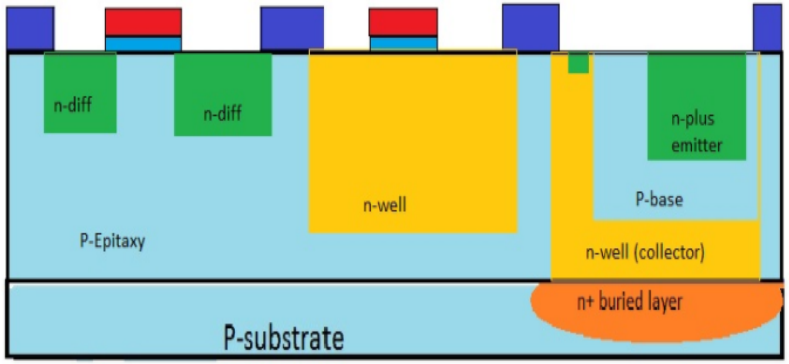
BiCMOS Fabrication…

Step10: The P-impurities are added to form the base terminal of BJT and similar, N-type impurities are heavily doped to form emitter terminal of BJT, source and drain of NMOS and for contact purpose N-type impurities are doped into the N-well collector.



P-impurities are added to form the base terminal of BJT

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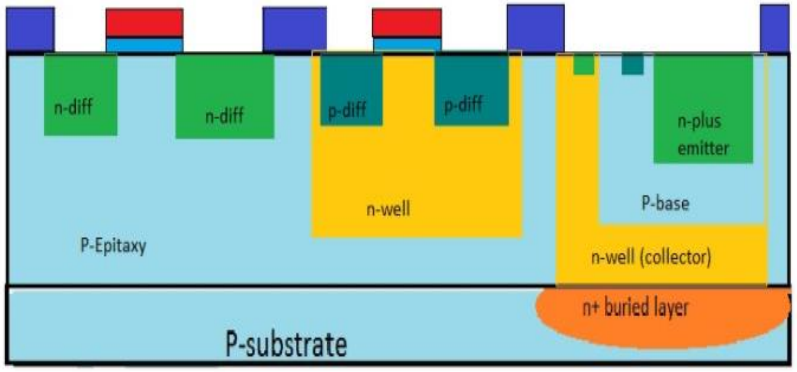
BiCMOS Fabrication…

Step11: To form source and drain regions of PMOS and to make contact in P-base region the P-type impurities are heavily doped.



P-type impurities are heavily doped to form source and drain regions of PMOS

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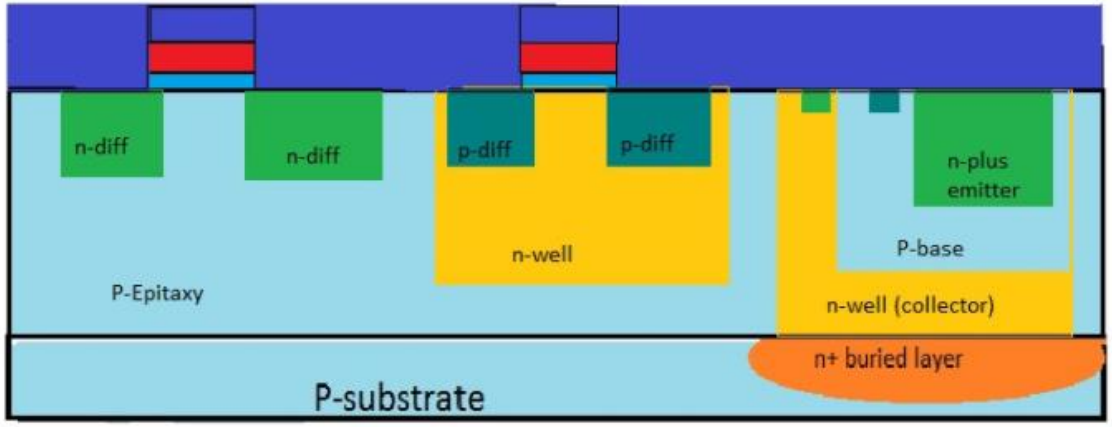
BiCMOS Fabrication…

Step12: Then the entire surface is covered with the thick oxide layer.



Entire surface is covered with the thick oxide layer

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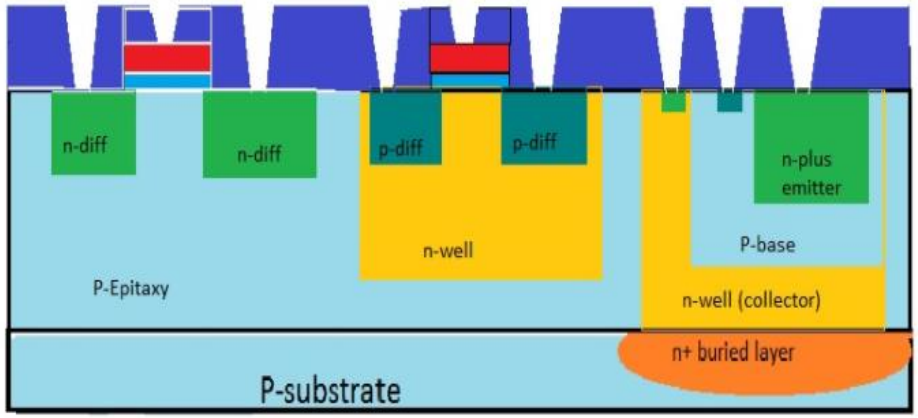
BiCMOS Fabrication…

Step13: Through the thick oxide layer the cuts are patterned to form the metal contacts.



The cuts are patterned to form the metal contacts

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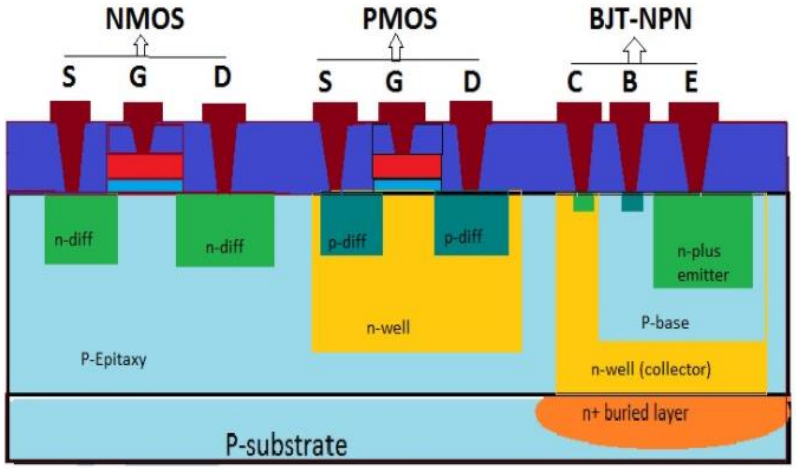
BiCMOS Fabrication…

Step14: The metal contacts are made through the cuts made on oxide layer and the terminals are named as shown in the below figure.



Metal contacts are made through the cuts and terminals are named

*https://www.elprocus.com/bicmos-technology-fabrication-and-applications/

Thank You