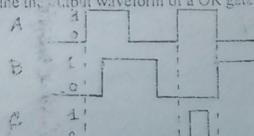


N.B. Answer six questions, taking three from each section.  
The questions are of equal value.  
Use separate answer script for each section.

SECTION-A

- Q1. (a) What are the differences of digital system and analog system? Give two examples of them. 2
- (b) Demonstrate by means of truth tables the validity of the following theorems of Boolean algebra. 4
- (i) The associative laws (ii) De Morgan's theorem for three variables.
- (c) Most calculators use BCD to store the decimal values as they are entered into the keyboard and to 3 drive the digit displays.
- (i) If a calculator is designed to handle 8-digit decimal numbers, how many bits does this require?
  - (ii) What will be the output when the number 375 is entered into the calculator? 6x2
- (d) In many cases binary subtraction is done in a special way by binary addition, why? 3x2

- Q2. (a) Determine the output waveform of a OR gate having the inputs shown in below figure. 2



- (b) Draw the circuit diagram to implement the expression  $x = (A+B)(\bar{B}+C)$  and also draw the circuit after simplification of this Boolean expression. 4
- (c) Draw the simplified circuit of part (b) using only NOR gate. 3
- (d) Prove that NAND gate works as universal gate. 2x2

- Q3. (a) What is mean by fan in and fan out of a logic family? 2

- (b) Explain the propagation delay of a TTL family. 3

- (c) Draw and explain the operating principle of a 2 input NOR gate using TTL. 4

- (d) What is noise margin? Draw the typical noise margin level of TTL logic family 3

- Q4. (a) Design a binary counter having the following repeated binary sequence. Use JK, D and T flip-flop. 6  
 $0 \rightarrow 1 \rightarrow 2 \rightarrow 3 \rightarrow 4 \rightarrow 0$

- (b) Design MOD-60 counter using 74LS293 IC. 4

- (c) If the input frequency of the counter part(b) is 100MHz then what is the frequency of the output of the last flip-flop? 1x2

SECTION-B

- Q5. (a) How can you overcome the race condition of a latch? 1x2
- (b) Mention the characteristics table of JK flip-flop, D flip-flop and T flip-flop. Also write its characteristics equation from their characteristics. 4x2
- (c) Convert a RS flip-flop to a D flip-flop. 3x2
- (d) Mention the basic sequential circuit design procedure. 2

- Q6. (a) Design a  $8 \times 1$  multiplexer by using two  $4 \times 1$  multiplexers and one  $2 \times 1$  multiplexer. 1x2

- (b) Implement the full adder by using decoder and basic gates. 4

- (c) Draw the circuit diagram of a 4-bit parallel adder/subtractor. Explain the operation. 4

- Q7. (a) What do you mean by SOP and POS? 2

- (b) Simplify the following expression by using k-map. 6

$$(i) \overline{ABC} + \overline{ABC} + BC + \overline{ABC} + \overline{ABC}$$

$$(ii) \overline{C} + \overline{D} + \overline{ACD} + \overline{ABC} + \overline{ABCD} + \overline{ACD}$$

- (c) Implement the following function with a multiplexer  $F(4, B, C, D) = \sum (0, 1, 3, 4, 8, 9, 15)$  3

- A/ Q8. (a) What are the necessary steps to determine output expression from a diagram? 4x2

- (b) Read the statement below concerning an OR gate. At first they may appear to be valid, but after some thought you should realize that neither one is always true. Prove this by showing a specific example to refute each statement. 7

- (i) If the output waveform of an OR gate is the same as the waveform at one of its inputs,

the other input is being held permanently low.

(ii) If the output waveform from an OR gate is always HIGH, one of its inputs is being held permanently HIGH.

N.B. Answer six questions. Taking three from each section.

The questions are of equal value.

Use separate answer script for each section.

### SECTION-A

- Q1. (a) What are the differences of digital system and analog system? Give two examples of them. 2
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- (i) The associative laws (ii) De Morgan's theorem for three variables.
- (c) Most calculators use BCD to store the decimal values as they are entered into the keyboard and to drive the digit displays. 3
- (i) If a calculator is designed to handle 8-digit decimal numbers, how many bits does this require? 3
  - (ii) What will be the binary representation of the number 375 if entered into the calculator? 3
- (d) In many cases time of subtraction is done in a special way by binary addition, why? 2
- Q2. (a) Determine the output waveform of a OR gate having two inputs shown in below figure. 2
- 
- Q3. (a) Draw the circuit diagram to implement the expression  $x = (A+B)(\bar{B}+C)$  and also draw the circuit after simplification of this Boolean expression. 4
- (b) Draw the simple logic circuit of part (b) using only NOR gate. 3
- (c) Prove that NOT gate works as universal gate. 3

- Q3. (a) What is meant by fan in and fan out of a logic family? 2
- (b) Explain the propagation delay of a TTL family. 1
- (c) Draw and explain the operating principle of a 2 input NOR gate using TTL. 4
- (d) What is noise margin? Draw the typical noise margin level of TTL logic family. 3

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- $0 \rightarrow 1 \rightarrow 2 \rightarrow 3 \rightarrow 4 \rightarrow 0$
- (b) Design MOD-60 counter using 74LS293 IC. 4
- (c) If the input frequency of the counter part(b) is 100MHz then what is the frequency of the output of the last flip-flop? 2

### SECTION-B

- Q5. (a) How can you overcome the race condition of a latch? 1
- (b) Mention the characteristics table of JK flip-flop, D flip-flop and T flip-flop. Also write its characteristics equation from their characteristics. 4
- (c) Convert a RS flip-flop to a D flip-flop. 3
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- Q6. (a) Design a  $8 \times 1$  multiplexer by using two  $4 \times 1$  multiplexers and one  $2 \times 1$  multiplexer. 3
- (b) Implement the full adder by using decoder and basic gates. 4
- (c) Draw the circuit diagram of a 4-bit parallel adder/subtractor. Explain the operation. 4

- Q7. (a) What do you mean by SOP and POS? 1
- (b) Simplify the following expression by using k-map. 6
- (i)  $\overline{ABC} + \overline{A}BC + A\overline{BC} + A\overline{B}C$
  - (ii)  $C + \overline{D} + \overline{A}\overline{C}\overline{D} + A\overline{B}C + A\overline{B}D$
  - (iii) Implement the following function with a multiplexer  $F(A, B, C, D) = \sum(0, 1, 3, 4, 8, 9, 15)$  3

- Q8. (a) What are the necessary steps to determine output expression from a diagram? 4
- (b) Read the statement below concerning an OR gate. At first they may appear to be valid, but after some thought you should realize that neither one is always true. Prove this by showing a specific example to refute each statement. 7
- (i) If the output waveform of an OR gate is the same as the waveform of one of its inputs, the other input is being used permanently. 2
  - (ii) If the output waveform from an OR gate is always HIGH, one of its inputs is being used permanently. 2

N.B. Answer six questions, taking three from each section.

The questions are of equal value.

Use separate answer script for each section.

### SECTION-A

Q1. (a) What are the differences of digital system and analog system? Give two examples of them. 2

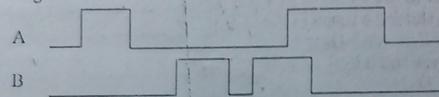
(b) Draw and explain basic digital system structure. 4

(c) A binary code uses ten bits to represent each of the ten decimal digits. Each digit is assigned a code of nine 0's and a 1. The code for digit 6, for example, is 0001000000. Determine the binary code for the remaining decimal digits. 3

(d) A process control computer uses hexadecimal codes to represent its 16-bits memory address. 2

- i) How many hex digits are required?
- ii) What are the ranges of address in hex?

Q2. (a) Determine the output waveform of a NAND gate having the inputs shown in below figure. 2



(b) Express the boolean function  $F = A + \bar{B}$  in a sum of min terms. 3

(c) Convert the following to other canonical form. 4

$$F(A,B,C,D) = \prod (0,1,2,3,4,6,12)$$

(d) Design a logic circuit whose output will be HIGH when all three inputs are in the same state. 2

Q3. (a) Simplify the following boolean function, F with the don't care function, d. 5

$$F(A, B, C, D) = \sum (0, 1, 2, 4, 6, 8, 11)$$

$$d(A, B, C, D) = \sum (3, 7, 9, 10, 12)$$

(b) Show how a two-input NAND gate can be constructed from two input NOR gate? 2

(c) A combination I circuit is defined by the following three functions: 4

$$F_1 = \bar{x} \bar{y} + xy\bar{z}$$

$$F_2 = \bar{x} + y \quad \left. \right\}$$

$$F_3 = xy + \bar{x} \bar{y}$$

Design the circuit with a decoder and external gates.

Q4. (a) Implement the following function with a multiplexer. 4

$$F(A, B, C, D) = \sum (0, 1, 3, 4, 8, 9, 15)$$

(b) Draw a parallel subtractor which subtract a number 1001 from 1101. Verify your answer with your circuit. 4

(c) Implement a 8:1 multiplexer by using two 4:1 multiplexers and one 2:1 multiplexer. 2

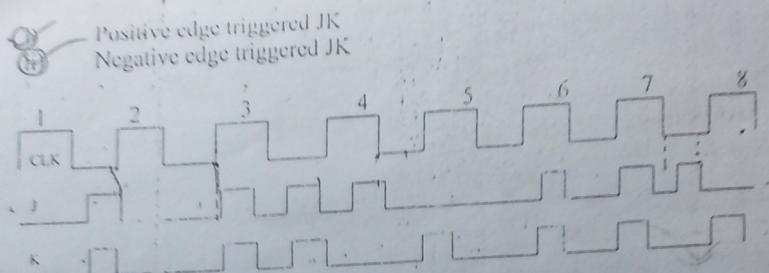
### SECTION-B

Q5. (a) What are the differences between latch and a Flip-Flop? 2

(b) Mention the characteristics table of Jk flip-flop, D flip-flop and T flip-flop. Also write its characteristics equation from their characteristics. 3 1/2

(c) Convert a D flip-flop to a T flip-flop. 4

(d) The waveforms shown in the below figure are to be applied to two different flip-flops: 3 1/2



Draw the output Q waveform response for each of these flip-flops, assuming that  $Q=0$  initially and  $t_{pd}=0$ .

- Q6. (a) Design the binary counter having the following repeated binary sequence. Use 6  
JK flip-flops.

$$0 \rightarrow 1 \rightarrow 2 \rightarrow 3 \rightarrow 4 \rightarrow 0$$

- (b) How many states in a ring counter having 5 flip flop?

- (c) If  $t_{pd}$  for each flip-flop is 50 ns and  $t_{pd}$  for each AND gate is 20 ns then calculate 3  
the total propagation delay and  $f_{max}$  for MOD-16 ripple counter.

- Q7. (a) Show how to connect the 74 ALS 174 so that it operates as a serial shift register 2  $\frac{2}{3}$   
with data shifting on each PGT of CP as follows:

$$D_3 \rightarrow D_4 \rightarrow D_3 \rightarrow D_2 \rightarrow D_1 \rightarrow D_0$$

- (b) What do you mean by TTL? Briefly describe low and high state circuit operation 4  
of basic TTL NAND gate.

- (c) Initially register A contains 1010 and register B contains 0010. If both of 5  
registers are connected in series then how much clock pulses are needed to  
transfer their data each other. Also draw the circuit diagram.

- Q8. (i) What factors determine CMOS fan out? 1  $\frac{2}{3}$

- (ii) Implement the following boolean function by using CMOS transistor,  $Y = A + BC$ . 4

- (iii) Prove that CMOS acts as inverter. 3

A certain logic family has the following voltage parameters:

$$V_{IH(\min)} = 3.5 \text{ V} \quad V_{IL(\max)} = 1.0 \text{ V}$$

$$V_{OH(\min)} = 4.9 \text{ V} \quad V_{OL(\max)} = 0.1 \text{ V}$$

- (i) What is the largest positive going noise spike that can be tolerated?

- (ii) What is the largest negative going noise spike that can be tolerated?

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$$V_{NH} = V_{OH(\min)} - V_{TH(\min)}$$

N.B. Answer six questions, taking three from each section.

The questions are of equal value.

Use separate answer script for each section.

### SECTION-A

Q1. (a) Draw and explain the operation of a basic digital system structure. 04

(b) A typical PC uses a 20-bit address code for its memory locations. 03

(i) How many hex digits are needed to represent a memory address?

(ii) What is the range of address?

(iii) What is the total number of memory locations?

(c) What about the alphabet of the digital system? Why is a binary alphabet used in computer system? 03

(d) Convert the following hex number to binary, octal and decimal. 03

$(B6F.4)_{16}$

Q2. (a) Draw the circuit diagram to implement the expression  $x = (A + B)(\bar{B} + C)$ . 03

(b) Implement the logic circuit that has the expression  $x = AB(C + D)$  using only NOR and NAND gates. 03

(c) Determine the output expression for the following circuit and simplify it using DeMorgan's theorems. 03

$$x = \overline{ABC} = (\overline{A} + \overline{B} + C)$$

(d) Express the boolean function  $f = -A + \bar{B}C$  in a sum of minterms. The function has three variables A, B, and C. 03

Q3. (a) Simplify the following Boolean function to a minimum number of literals. 03

$$xyz + xy + xyz$$

(b) Use k-map to simplify  $y = \overline{C}(\overline{ABD} + D) + \overline{AB}\overline{C} + \overline{D}$ . 04

(c) Design a logic circuit that will allow a signal to pass to the output only when control inputs B and C are both HIGH, otherwise the output will stay LOW. 03

(d) Design the logic circuit corresponding to the truth table shown below. 03

A	B	Y
0	0	0
✓0	1	1
✓1	0	1
1	1	0

Q4. (a) Simplify the Boolean function 04

$$F(A, B, C, D) = \Sigma(1, 3, 7, 11, 15) \text{ and don't care condition}$$

$$d(A, B, C, D) = \Sigma(0, 2, 5)$$

(b) Design a full adder by using its truth table. 03

(c) A certain memory location holds the hex data 77. If this represents an unsigned number, what is its decimal value? If this represents a sign number, what is its decimal value? 02

(d) Implement half adder circuit with a decoder and two OR gates. 02

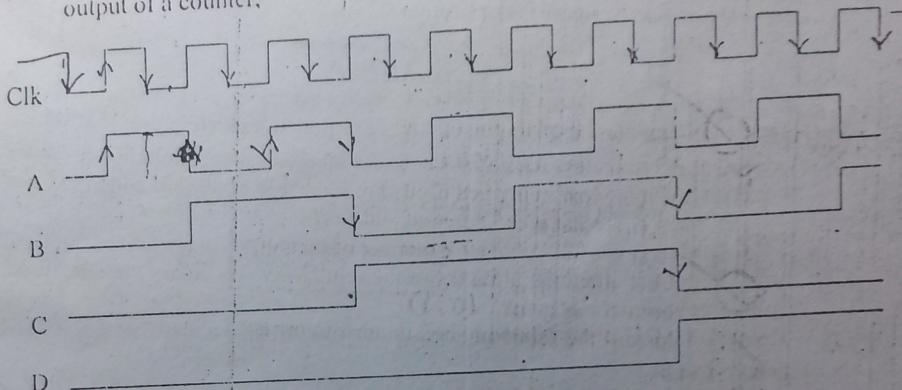
SECTION-B

Q5. (a) Distinguish between asynchronous and synchronous counter.

2  $\frac{2}{3}$

(b) The following timing diagram represent the clock signal of a counter and the output of a counter.

09



(i) Draw the block diagram of that counter.

(ii) If the clock pulse is 30KHz, determine the frequency at the D output.

(iii) Convert it to MOD 8 counter.

Q6. (a) Show how to connect the 74ALS174 so that it operates as a serial shift register with data shifting on each PGT of CP as follows:  $D_3 \rightarrow D_4 \rightarrow D_5 \rightarrow D_2 \rightarrow D_1 \rightarrow D_0$ .

3  $\frac{2}{3}$

(b) Convert a JK flip flop to a T flip flop.

3  $\frac{2}{3}$

(c) Determine the setup time and hold time requirements of a clocked flip flop.

02

(d) What are difference between latches and flip flop.

03

Q7. (a) Explain the operation of a 4-bit universal shift register.

3  $\frac{2}{3}$

(b) Explain the operating principle of a TTL 2 input NAND gate.

04

(c) Define the following terms:

04

- { (i) Fan in
- (ii) Fan out
- (iii) Noise Margin
- (iv) Propagation Delay

Q8. (a) Draw 3 input OR gate by using NMOS transistor.

04

(b) Implement the following Boolean function by using CMOS transistor.

04

$$Y = AB + C$$

3  $\frac{2}{3}$

(c) Prove that CMOS acts as inverter.

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N.B. Answer six questions, taking three from each section.

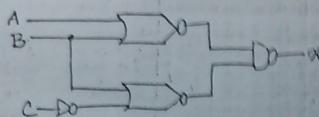
The questions are of equal value.

Use separate answer script for each section.

### SECTION-A

- Q1. (a) Draw and explain the operation of a basic digital system structure. 1  
 (b) A process-control computer uses hexadecimal codes to represent its 16-bit memory address. 2  
 (i) How many hex digits are required? 1  
 (ii) What are the ranges of address in hex? 1  
 (c) Represent each of the following values as an eight-bit signed number in the 2's complement system. 3  
 (i) +13 (ii) -128 1  
 (d) How can you tell when a correction is needed in BCD addition? 2

- Q2. (a) Draw the circuit diagram that implements the expression  $X = \overline{ABC}(\overline{A} + \overline{D})$  using gates with no more than three inputs. 1  
 (b) Implement the logic circuit that has the expression  $X = AB(C + D)$  using only NOR and NAND gates. 2  
 (c) Use DeMorgan's theorems to simplify the expression for the output of the following figure. 4

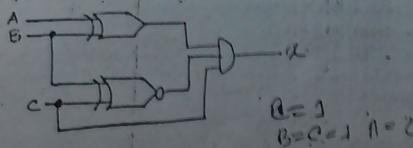


- Q3. (a) Simplify the following logic circuit. 4



- (b) Design a logic circuit with three inputs to produce a HIGH output only when all three inputs are at the same logic level. Use only EX-NOR gates and one other gate. 4  
 (c) Use a K-map to simplify  $Y = \overline{C}(\overline{ABD} + D) + \overline{ABC} + D$  4

- Q4. (a) Determine the input conditions needed to produce  $X=1$  in figure below. 4



- (b) A manufacturing plant needs to have a horn sound to signal quitting time. The horn should be activated when either of the following conditions is met:  
 (i) It's after 5 O'clock and all machines are shut down.  
 (ii) It's Friday, the production run for the day is complete and all machine are shut down. 5

Design a logic circuit that will control the horn.

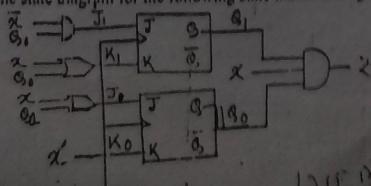
- (c) What is meant by sum-of-products and product-of-sums form? 3

### SECTION-B

- Q5. (a) Design a 8X1 multiplexer by using two 4X1 multiplexer and one 2X1 multiplexer. 5

- (b) Implement the full adder by using decoder and basic gates. 5  
 (c) Design 5X32 decoder by using 74LS158 and 74LS139 IC chips. 4

- Q6. (a) Draw the state diagram for the following state machine diagram. 5



(b) Convert a RS flip-flop to a JK flip-flop.

(c) What is the normal resting state of the NOR latch inputs? What is the active state?

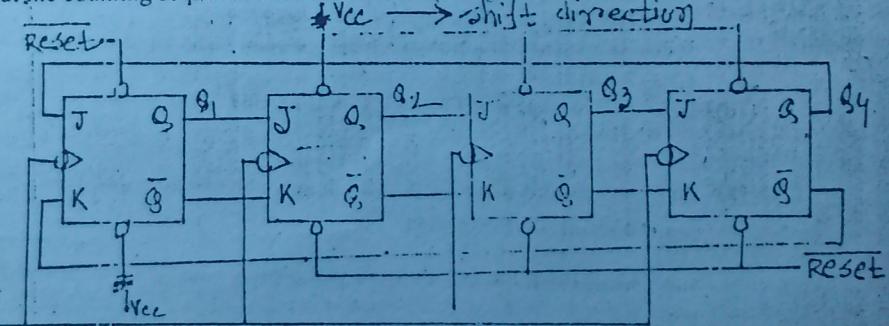
Q7. (a) Show how to wire 74LS293 ICs as a MOD60 counter.

(b) Design a counter that counts the following sequences:

$$0 \rightarrow 1 \rightarrow 2 \rightarrow 3 \rightarrow 4 \rightarrow 0$$

(c) Determine  $f_{max}$  for the 4 bit synchronous counter if  $t_{PLH}$  for each FF is 50 ns and  $t_{PHL}$  for each AND gate is 20 ns. Compare this value with  $f_{max}$  for a MOD-16 ripple counter.

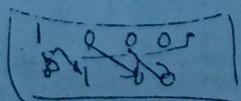
Q8 (a) Find out the counting sequence from the following diagram



(b) Show that 74LS194 IC acts as a 4-bit universal shift register.

(c) Draw a circuit diagram for the synchronous parallel transfer of data from one three-bit register to another using J-K flip-flops.

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N.B. Answer six questions, taking three from each section.  
 The questions are of equal value.  
 Use separate answer script for each section.

SECTION-A

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SECTION-B

8 + 3

Q5. (a) Reduce by 3-variable K-mapping:

$$f = \overline{ABC}E + \overline{ABC} + \overline{ABC}F + \overline{ABC} + \overline{AB}CD + ABC\overline{F}$$

(b) Use an 8-input multiplexer, implement the logic function  $f = A \oplus B \oplus C$

Q6. (a) Construct a binary counter that will convert a 64KHz pulse signal into a 2KHz square wave.  
 (b) Design a synchronous counter that will counts the following sequences:

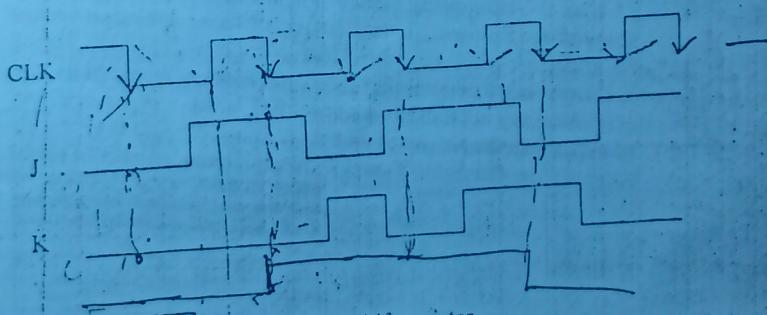
0 → 1 → 3 → 5 → 7 → 0

(c) Implement the following function with a multiplexer.

$$F(A, B, C, D) = \sum(0, 1, 3, 4, 8, 9, 15)$$

Q7. (a) Explain how one bit of data is stored in computer's memory.

(b) The following wave forms are applied to a negative edge-triggered J-K flip-flop. Draw the output wave form.



00  
00  
10  
11

Q8. Draw and design a 4-bit parallel in serial output shift register.

Draw and explain 2-input TTL NAND gate.

For the logic families, explain following terms briefly.

i) Propagation Delay      ii) Fanout and iii) Noise Margin

Draw circuit diagram of CMOS inverter and write its truth table.

\*\*\* The End \*\*\*

"Heaven's light is our guide"

Rajshahi University of Engineering & Technology  
B.Sc. Engineering 2<sup>nd</sup> Year 3<sup>rd</sup> Semester Examination, 2009  
Department of Computer Science and Engineering  
Course no: CSE-307 Course Title: Digital Techniques  
Full marks: 70 Time: Three (03) hours

N.B. Answer six questions, taking three from each section.

The questions are of equal value.

Use separate answer script for each section.

### SECTION-A

Q1. (a) Prove the following identities by using the method of induction

$$(i) x + \bar{x}y = x + y. (ii) (x + y)(\bar{x} + z)(y + z) = (x + y)(\bar{x} + z)$$

(b) Differentiate between combinational circuit and sequential circuit.

(c) Use De-Morgan's theorem to convert  $y = \overline{A + \bar{B} + \bar{C}\bar{D}}$  to an expression containing only single variable inversion.

(d) What are the universal gates? Why are they called so?

Q2. (a) Simplify the following Boolean function using k-map and finally draw its equivalent circuit diagram.

$$F(A, B, C, D) = \sum(0, 1, 4, 5, 8, 10, 13, 15)$$

$$d(A, B, C, D) = \sum(2, 3, 6, 7, 9)$$

Marks

03  $\frac{2}{3}$

02

03

03

06  $\frac{2}{3}$

20

Q3. (b) Implement a full adder circuit with the help of half adder/adders and other necessary logic gate and finally verify that it operates properly as a full adder circuit.

(a) Construct a  $5 \times 32$  decoder with four  $3 \times 8$  decoders and a  $2 \times 4$  decoder. Use only block diagram construction.

(b) Draw the logic diagram of a 2-line to 4-line demultiplexer using NOR gates only.

(c) What do you mean by

(i) Encoder and multiplexer and

(ii) Decoder and demultiplexer

Q4. (a) Simplify the following Boolean expression using Quine-McClusky method

$$f(x_1, x_2, x_3, x_4) = \sum m(0, 2, 5, 7, 8, 9, 10, 13, 15)$$

05

04  $\frac{2}{3}$

03

04

04  $\frac{2}{3}$

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03

### SECTION-B

Q5. (a) What is race condition? Why race condition must be avoided, explain?

Marks

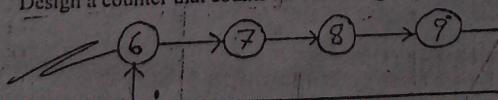
03  $\frac{2}{3}$

(b) What do you mean by ripple counter? Why is it so called?

02

(c) Is there any advantage of synchronous counter? Explain in brief. Design a counter that counts the following sequence.

06



Q6. (a) What do you mean by propagation delay of a gate? How can it affect the operation of a logic system?

03  $\frac{2}{3}$

(b) For operation amplifier(OP-Amp), prove that

$$\text{Voltage gain, } A_v = \frac{A}{1+AB} \text{ and feedback gain, } B = \frac{R_f}{R_1 + R_f},$$

where the symbols represent usual meaning.

Write down the characteristic for the followings

- (i) TTL, (ii) DTL, (iii) ECL and (iv) C-MOS.

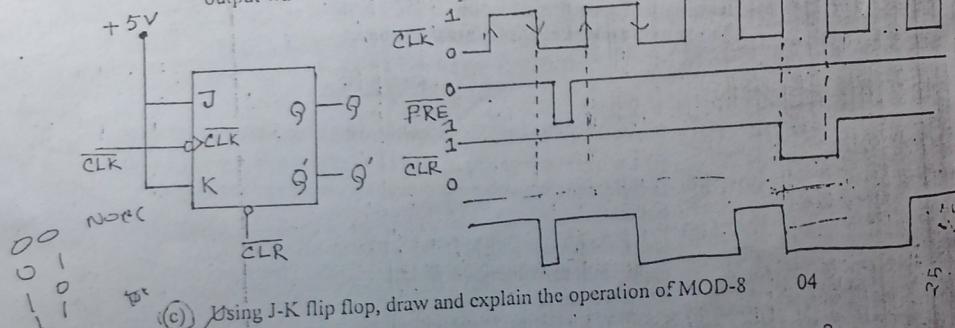
Q7. (a) Design a subtractor circuit using OP-Amp.

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(b) For the following J-K flip flop and the waveforms, find the output waveform Q.



(c) Using J-K flip flop, draw and explain the operation of MOD-8 binary counter.

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45  
CY

Q8. (a) Why is 555 IC called timer IC?

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(b) Draw the circuit diagram of a 3 input TTL NAND gate and explain its operation.

(c) Calculate  $T_{on}$ ,  $T_{off}$ ,  $T_i$  and % duty cycle for the following figure.

