Heaven's Light is Our Guide

Rajshahi University of Engineering & Technology

B.Sc. Engineering 3rd Year Even Semester Examination, 2016

Department of Computer Science & Engineering

Course No. CSE 3203 Course Title: **Computer Architecture**

Full Marks: 70 Time: **THREE** (03) hours

N.B:

Answer **SIX** questions taking **THREE** from each section.
The questions are of equal value.
Use separate answer script for each section.

SECTION A

		Marks
Q.1(a)	Discuss the data flow of fetch and interrupt cycles with neat sketch.	05
(b)	Explain the different addressing modes with examples.	04
(c)	Write the code to execute y = (A*B/C)+(D-E) using one address instructions.	03
Q.2(a)	Briefly describe the Von Neumann Architecture with neat sketch.	04
(b)	What do you mean by (i) SISD (ii) SIMD (iii) MIMD and (iv) MISD?	04
(c)	Define (i) WAR and (ii) RAW. Explain why is it necessary to know about WAR and RAW?	04
Q.3(a)	Write down about Flynn's classical Taxonomy. What is the main advantage of using cache memory in computing system?	05
(b)	Why is an instruction pipelining necessary?	02
(c)	Write the differences between instruction level parallelism (ILP) and parallel processing.	03
(d)	What are the ILP challenges to achieve parallelism?	02
Q.4(a)	Define (i) Thread (ii) Task (iii) shared memory and (iv) Process.	02
(b)	Explain the statement-"parallelism is the future computing".	03
(c)	What is the advantage of very long instruction word (VLIW)?	02
(d)	In general, how much general purpose registers are available in a computing system and why?	05

SECTION B

Q.5(a)	What are the problems of sign magnitude representation?	02
(b)	Define (i) 1's complement and (ii) 2's compliment with examples.	02
(c)	Explain how pipelining is used to enhanced performance of a computing system?	04
(d)	Draw and explain the hardware structure for addition and subtraction with an example.	04
Q.6(a)	What do you mean by computer architecture? What is the difference between computer architecture and computer organization?	04
(b)	Describe the basic functions of the major structural components of CPU.	04
(c)	Specify the significance of the following CPU registers: (i) PC (ii) IR (iii) MAR and (iv) MDR.	04
Q.7(a)	What is the advantage of using expansion bus in multiple-bus architecture?	02
(b)	What are the benefits of using high speed bus architecture compared to single bus architecture?	04
(c)	What do you mean by RISC and CISC architecture? How do they differ from each other?	04
(d)	Between RISC and CISC, which architecture shortens execution time by reducing the clock cycles per instruction?	02
Q.8(a)	Define (i) Multiprocessor Organization (ii) Cluster Computing (iii) VGA and (iv) HDMI.	06
(b)	Represent the decimal values 100, 128, -128, -127, -28 as signed, 8-bit numbers in the following binary formats: (i) sign-magnitude representation (ii) 1's complement representation and (iii) 2's complement representation.	06

*** The End***

Heaven's Light is our Guide

Rajshahi University of Engineering & Technology

B.Sc. Engineering 3rd Year Even Semester Examination, 2016

Department of Computer Science & Engineering

Course No. CSE 3201 Course Title: Operating System

Full Marks: 72 Time: THREE (03) hours

N.B:

Answer **SIX** questions taking **THREE** from each section.
The questions are of equal value.
Use separate answer script for each section.

SECTION A

		Marks
Q.1(a)	What is an Operating System? Distinguish between the client-server and peer-to-peer models of system using suitable example.	04
(b)	Consider the following table:	08

Process	Burst Time(ns)	Priority
P_1	19	3
P_2	7	2
P_3	9	1
P_4	5	4
P_5	4	5

(i) Draw the Gantt chart showing the case of execution using FCFS, SJF, Priority and RR (time slice = 4ns) scheduling algorithms.

(ii) Compute the turn around time and average waiting time for each of the above algorithms.

Q.2(a)	Describe the actions taken by a kernel to context-switch between processes.	03
(b)	Define the producer consumer problem and show how the deadlock happens when using semaphore.	05
(c)	Explain the address translation mechanism used in paging system with a suitable example.	04
Q.3(a)	Define inter process communication using mailbox system.	03
(b)	Solve the producer problem using message passing system and write the appropriate code segment.	05
(c)	Define critical section with an example and describe how monitor can be used to manage critical section.	04
Q.4(a)	What is deadlock? What are the necessary conditions for deadlock?	03
(b)	Consider the following snapshot of a system:	06

Process	Allocation			Max			Available		
	A	B	C	A	B	C	A	B	C
P_0	0	1	0	7	5	3	3	3	2
P_1	2	0	0	3	2	2			
P_2	3	0	2	9	0	2			
P_3	2	1	1	2	2	2			
P_4	0	0	2	4	3	3			

Answer the following queries using Banker's algorithm-

(i) What is the content of matrix need? And (ii) Is the system in a safe state?

(c)	Define virtual memory. Why is virtual memory important in process management?	03

SECTION B

Q.5(a)	Define paging. What are the differences between traditional and demand paging system?	03
(b)	Consider a logical address space of 32 pages of 2048 words each, mapped onto a physical memory of 8 frames. Then answer the following questions:	03
	(i) How many bits are needed for addressing the total logical address space?	
	(ii) How many bits required to indicate page number?	
	(iii) How many bits required for addressing the physical address?	
	(iv) What is the total number of bits required for addressing the physical memory?	
(c)	How can the external and internal fragmentation be removed?	03
(d)	Paging has some internal fragmentation. Prove this statement with a suitable numeric example.	03
Q.6(a)	Define Belady's Anomaly with a suitable example.	04
(b)	Define page replacement. Consider the following page-reference string: 1, 2, 3, 4, 2, 1, 5, 6, 2, 1, 2, 3, 7, 6, 3, 2, 1, 2, 3, 6, how many page faults occur for the following replacement algorithms, assuming four frames. Remember that all pages are initially empty. (i) Optimal replacement and (ii) LRU replacement.	06
(c)	Write down the benefits of multithreaded programming.	02
Q.7(a)	Distinguish between the following terms (i) Distributed and multiprocessor system and (ii) Time sharing VS Multiprogramming.	05
(b)	Under what circumstances would a user be better off using a time sharing system, rather than a PC or single user workstation?	03
(c)	Suppose you are given the responsibility to configure the network system of CSE dept.lab, RUET. What network configuration would best suit the environment and why?	04
Q.8(a)	What is context switch? Show the CPU switching from process to process with a diagram.	04
(b)	How does producer-consumer process work? Can you illustrate the idea of cooperating process with producer-consumer concept? If so, how?	05
(c)	Provide two examples of multithreading that improve performance over a single-threaded solution.	03

Heaven's Light is Our Guide

Rajshahi University of Engineering & Technology

B.Sc. Engineering 3rd Year Even Semester Examination, 2016

Department of Computer Science & Engineering

Course No. CSE 3207 Course Title: **Peripherals & Interfacings**

Full Marks: 72 Time: **THREE** (03) hours

N.B:

Answer **SIX** questions taking **THREE** from each section.
The questions are of equal value.
Use separate answer script for each section.

SECTION A

		Marks
Q.1(a)	If you want to transfer data between I/O and microprocessor using IN, INS, OUT, OUTS instructions, then which interfacing technique will you choose and why?	03
(b)	Is it possible to access 32-bit I/O port using 8-bit I/O ports?	02
(c)	Many I/O devices accept or release information at a much slower rate than the microprocessor. How can you synchronize these I/O devices with microprocessor? Explain with example.	04
(d)	Can 82C55 interface any TTL-compatible I/O device to the microprocessor? How many ports are there in 82C55? What are the purposes of these ports?	03
Q.2(a)	What do you mean by programmable peripheral device? Why are the port lines of programmable port devices automatically put in the input mode when the device is first powered up or reset?	04
(b)	In mode 2 operation of 8255A which pins are used as input pin and output pin?	02
(c)	Write down the Mode-Set control word format for 8255A.	04
(d)	Write the instruction to send the control word 8Eh. Explain.	02
Q.3(a)	Explain why is a modem required to send digital data over standard switched phone lines?	04
(b)	What logic levels on BHE and A_0 is required to write a word to address 04300H?	02
(c)	Draw the block diagram of 8086 memory banks.	03
(d)	Explain the working of a hand shake input port and output port.	03
Q.4(a)	Draw a circuit that uses 2764 EPROMs for a 64k x 8 section of memory in an 8086 microprocessor system using 74LS138 decoder.	04
(b)	What are functions of A_0, A_1, and GATE input in 8254 programmable timer?	03
(c)	How does the main processor distinguish its instruction from those for 8087 as it fetches instruction from memory?	02
(d)	Convert the decimal number 178.25 to 8087 short real data format.	03

SECTION B

Q.5(a)	What is resolution of a five-bit D/A converter that produces V_{out} = 0.2V for a digital input of 00001? Describe the staircase signal out of this DAC.	03
(b)	Describe the operation of a DAC using an OP-AMP summing amplifier with binary weighted registors.	04
(c)	Write down the application of DAC in signal reconstruction.	02
(d)	What is the problem of using a high-resolution DAC that has large difference in registor values between the LSB and MSB? What is the solution of this problem?	03
Q.6(a)	Draw the architecture of a 32 x 8 ROM.	04
(b)	What is mask-program ROM? MROMs can be used to store tables of mathematical function. Show how MROM can be used to store the function, $y = x^2+3$, where the input address supplies the value for x and the value of the output data is y.	05
(c)	Draw the architecture of PAL for the following functions: $O_0 = A + B\bar{D} + C\bar{D}$ $O_1 = A\,B\,\bar{C}\,\bar{D} + \bar{A}\,\bar{B}\,C\,D$ $O_2 = A\,\bar{B}\,C$ $O_3 = A\,B + \bar{C}\,\bar{D}$	03
Q.7(a)	How many 8259As are required to have 64 interrupt inputs and why?	03
(b)	Assume that IR inputs in 8259A are in fixed priority. If it receives interrupt signal on IR2 and IR4 inputs at the same time, then how will it response?	03
(c)	How can you configure 8255A PPI if its control register contains 8Ch? Explain with necessary figure.	04
(d)	What is the purpose of using in-service register in 8259A?	02
Q.8(a)	What is DMA operation? Write the advantages and applications of DMA operation.	03
(b)	How can you interface a 4 x 4 keyboard with 8086 microprocessor using 8255A PPI? Explain with necessary diagram and assembly instructions.	05
(c)	Write the differences between synchronous and asynchronous data communication.	02
(d)	How can you perform interfacing through memory mapped I/O technique? Write with example.	02

Rajshahi University of Engineering & Technology
B.Sc. Engineering 3rd Year Even Semester Examination, 2016
Department of Computer Science & Engineering
Course No. CSE 3205 Course Title: **Computer Networks**
Full Marks: 72 Time: **THREE** (03) hours

N.B:

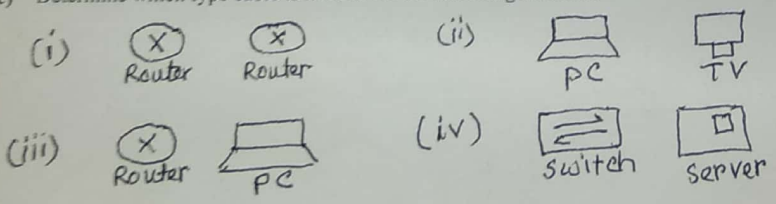
Answer **SIX** questions taking **THREE** from each section.
The questions are of equal value.
Use separate answer script for each section.

SECTION A

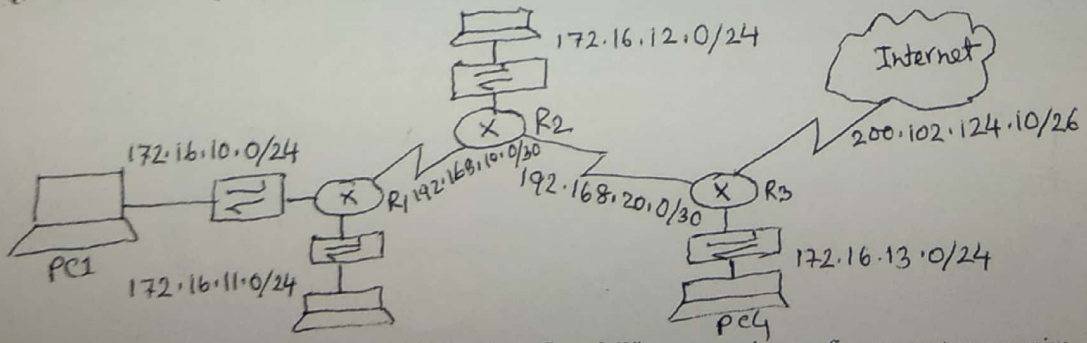
		Marks
Q.1(a)	Why the network layer must never be given any part of the frame header? Explain briefly.	02
(b)	What should you consider for creating layer in OSI model?	03
(c)	Consider a stop-wait protocol where the frame header contains sequence number of the frame. What is the minimum number of bits needed for the sequence number? Justify your answer.	02
(d)	A bit stream 10010011 is transmitted using the standard CRC method. The generator polynomial is x^3+1. Show the actual bit string transmitted. Suppose the third bit from the left is inverted during transmission. Show that this error is detected at the receiver's end.	05
Q.2(a)	Briefly explain the followings: (i) Transport entity (ii) Transport service provider and (iii) Transport service user.	03
(b)	Data link protocols almost put the CRC in a trailer rather than in a header, why?	03
(c)	In transport layer "establishing a connection sounds easy, but it is actually tricky". Justify the statement.	03
(d)	Why does the maximum packet lifetime, T have to be large enough to ensure that not only the packet but also its acknowledgement have vanished?	03
Q.3(a)	Briefly explain single bit sliding window protocol.	04
(b)	Why does UDP exist? Would it not have been enough to just user processes send raw IP packets.	03
(c)	Briefly explain different fields of TCP segment header.	03
(d)	Mention the misconception about public key crypto-system.	02
Q.4(a)	Why is a security necessary in computer networks?	03
(b)	Bob wants to set up his own private and public keys for RSA crypto-system. He choose p = 7 and q = 11. Calculate the key pair. Encrypt message M = 5 using public key.	4.5
(c)	Construct a palyfair matrix with key "COMPUTER". Encrypt the message "COMPUTER NETWORK".	4.5

SECTION B

Q.5(a)	What is an IP address? What are the differences between IPv4 and IPv6?	03
(b)	Suppose your network address is 117.10.0.0/12. Now answer the following questions: (i) How many IP addresses can be generated? And (ii) If you have four different LANs of 100, 2810, 5 and 3000 hosts, then design VLSM scheme.	06
(c)	What is the principle difference between connectionless communications and connection oriented communication?	03
Q.6(a)	Show the comparison between datagram subnet and virtual-circuit subnet.	03
(b)	How do we remove magnetic field effect in copper cabling?	02
(c)	Determine which type cable is needed for the following situation:	04



(d)	What do you mean by propagation delay and transmission delay?	03
Q.7	For the following diagram, answer the below questions:	



(i)	How many stub networks are present in the above figure? When we need to configure a port as a passive interface?	03
(ii)	If you want to communicate from PC1 to PC4, what are necessary steps to ensure this connection?	04
(iii)	What do you mean by routing table? After achieving convergence, what entries are available for R_1, R_2 and R_3 routers?	05
Q.8(a)	"When too much traffic is offered, congestion sets in and performance degrades sharply"-Justify your answer.	03
(b)	What do you mean by routing loop? How can routing loop be broken?	03
(c)	A system has an n-layer protocol hierarchy. Application generates message of length M bytes. At each of the layer, an h-byte header is added. What fraction of the network bandwidth is filled with headers?	04
(d)	Describe (i) IGP and (ii) BGP	02

Heaven's Light is Our Guide

Rajshahi University of Engineering & Technology

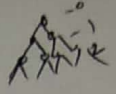
B.Sc. Engineering 3rd Year Even Semester Examination, 2016

Department of Computer Science & Engineering

Course No. CSE 3209 Course Title: Artificial Intelligence

Full Marks: 72 Time: THREE (03) hours

N.B: Answer SIX questions taking THREE from each section.
The questions are of equal value.
Use separate answer script for each section.



SECTION A

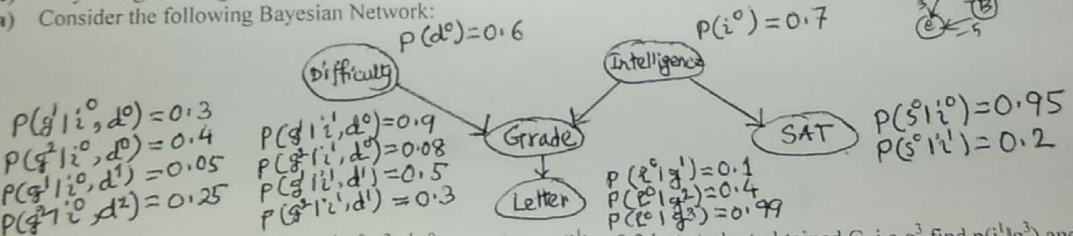
		Marks
Q.1(a)	Define Artificial Intelligence (AI). Briefly describe applications of AI.	03
(b)	What do you mean by 'learning'? Explain with suitable example.	03
(c)	Differentiate between MAP and MLE.	03
(d)	Compare between human intelligence and virtual intelligence for problem solving by searching.	03
Q.2(a)	When comparing tree-search algorithms, we measure the number of nodes expanded. How many nodes are expanded (in the worst case) by each of the following search techniques when searching a tree with branching factor, b to find a goal at a depth of d? Do not use big-Oh notation. (i) Breadth-first search (ii) Depth-first search (iii) Iterative deepning depth-first search.	06
(b)	What is the definition of an admissible heuristic?	02
(c)	What is an example of when IDA* becomes inefficient?	04
Q.3(a)	Represent the following sentence in first-order logic: (i) All dogs are mortal (ii) No person bugs an expensive policy.	04
(b)	Define first-order logic with an example.	03
(c)	Let C1 be the clause ¬republican (Mother(x)) V Republican(x) and let C2 be the clause ¬Republican(y) V likes (y, sarah) V ¬Resident(y, Alaska). What is the result of applying the resolution rule of inference to C1 and C2?	05
Q.4(a)	Given p(A|B) = 0.4, P(B) = 0.2. P(A) = 0.5, Compute P(B|A).	04
(b)	Given the following network A→B→C, where all variables are binary, write down the minimum number of (conditional) probabilities that define the CPTs.	04
(c)	Define joint probability distribution with suitable example.	04

SECTION B

Q.5(a)	Give example of learning algorithm that has greedy choice property. What is the affect of this property on your example algorithm, discuss details.	04
(b)	Differentiate between JDE and NDE. Estimate the JDE and NDE for the dataset for the following figure:	04

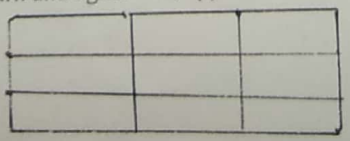
Age	Education	Income	Marital-status	Purchase
36-55	Master's	High	Single	Yes
18-35	High School	Low	Single	No
36-55	Master's	Low	Single	Yes
18-35	Bachelor's	High	Single	No
<18	High School	Low	Single	Yes
18-35	Bachelor's	High	Married	No
36-55	Bachelor's	Low	Married	No
<18	High School	High	Single	No
<18	High School	Low	Married	Yes

(c)	Why is negative edge costs not allowed in UCS? Explain.	04
Q.6(a)	Consider the following Bayesian Network:	07

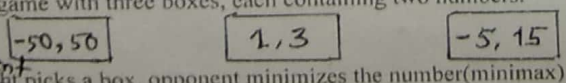


(i) Find the Joint probability $p(i^1,d^0,g^2,s^1,l^0)$ (ii) Given $p(i^1) = 0.3$ but student obtained C, i,e g^3 find $p(i^1|g^3)$ and $p(d^1|g^3)$ (iii) since the student performed poorly, he received a weak recommendation letter. Find $p(i^1|g^3,l^0)$ and (iv) ~~But~~ the student has good SAT score. Will the probability that he/she has higher intelligence increase?

(b)	Describe the properties of minimum algorithm.	02
(c)	Differentiate between UCS and A* search algorithms.	03
Q.7(a)	Given the following board position in the tic-tac-toe game, predict the game value using minimax algorithm (Assume it is the agent's turn and agent = X, opponent = O).	04



(b)	In the constraint satisfaction problem(CSP), which variable(Q) to assign next and what values to try for Q?	03
(c)	Consider a game with three boxes, each containing two numbers.	05



Case 1: Aghi picks a box, opponent minimizes the number(minimax)
Case 2: A coin is tossed. If it is head, aght picks first otherwise opponent picks first(Expeetiminimax).
Draw the game trees for both cases.

Q.8(a)	If P(A|B) is three times the value of P(B|A) and P(A) = 0.123, what is P(B)?	04
(b)	Compute the joint probability P(~A, ~B, ~C) for the following Bayesian Network A→B→C with binary random variables, where CPTs are P(A) = 0.3, P(B|A) = 0.4, P(B|~A) = 0.5, P(C|B) = 0.2, P(C|~B) = 0.1. Here "~" stands for negation.	05
(c)	Define Bayes Theorem.	03