

Microprocessors and Assembly Language

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Ref. Book:

Charles Marret

BIOS → software
→ ROM → RAM

Execution memory → Primary Memory

(RAM)

Instruction

↓
Array of resistors

Access → read + write

Intel 8086 / 8088

base start) register available program ← RAM

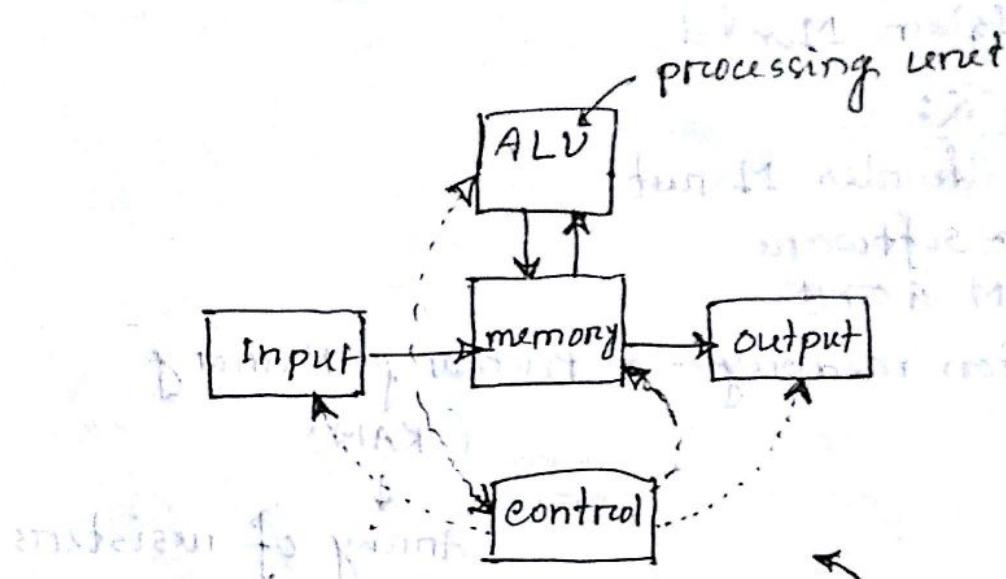
• \$ start • 114 → RAM

register to apply on → program area
(area a recording)

2(A)-Day

Date: 7/6/2017

von Neumann Architecture:



→ Sequential operation (sequential machine)

MAR → Memory Address Register (Data read + write)

MDR → Data

Cache Memory → one type of register
(processor a भूक)

Basic Performance Equation

$$T = \frac{N \times S}{R}$$

Intel 4004 → 4 bit

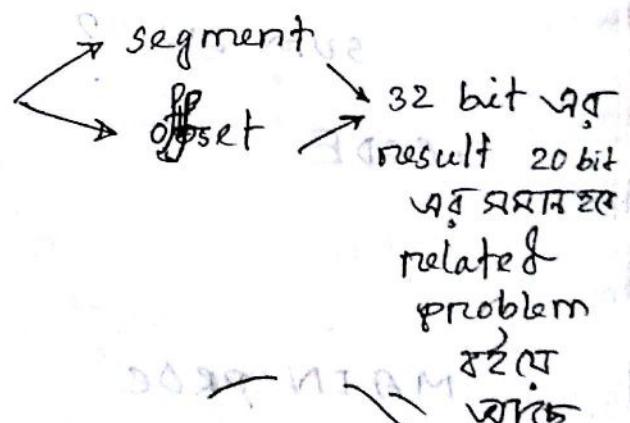
- Difference between multi-core and many-core processor

Instruction → Intel 8086

Address bus - 20 bit

Data bus - 16 bit

Control bus -



Flags register

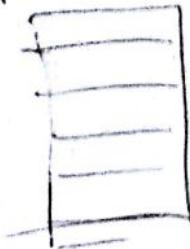
16-bit register w/ 9 flag

Op code → operation for 20 bit data

Operands → 16 bit data for operation

- MODEL SMALL
- 100H
- Data

D2 1111 1111
0000 0010 FF



Ex 4th chapter → 4.9

- MODEL SMALL
- STACK 100H
- DATA

AL → Accumulation Register

A DW 2

BL → Base Register

B DW 3

CL → counter

sum DW ?

DL → Data

• CODE

AH →

MAIN-PROC

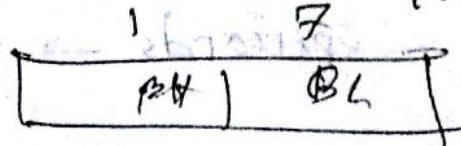
AX 8 7 17 0
AH AL

MOV DL, AL

P - 16 Bit

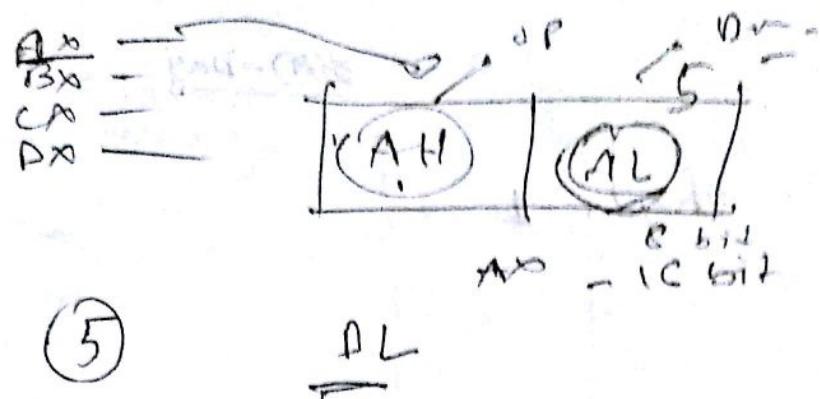
INT 21H

MOV AH, 2 → w/p
1 → L/p

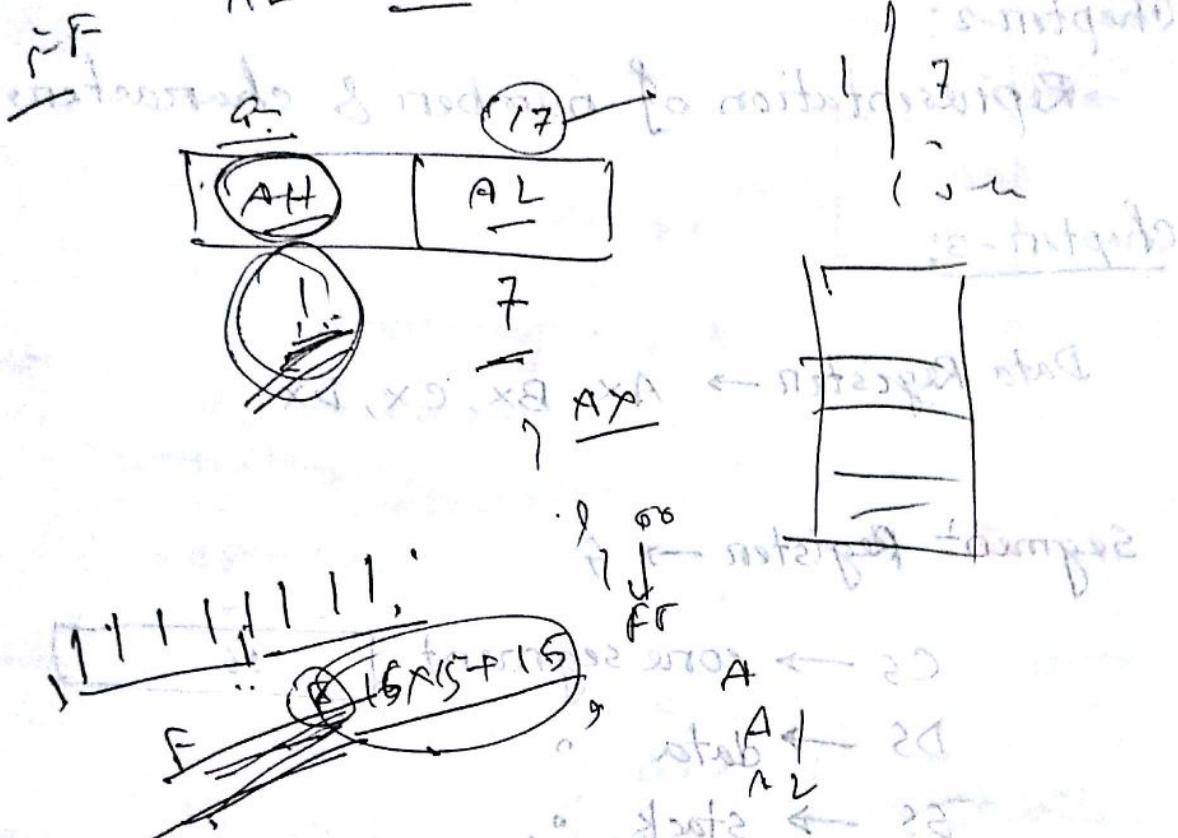


ADD AH, AL

ADD AL, —

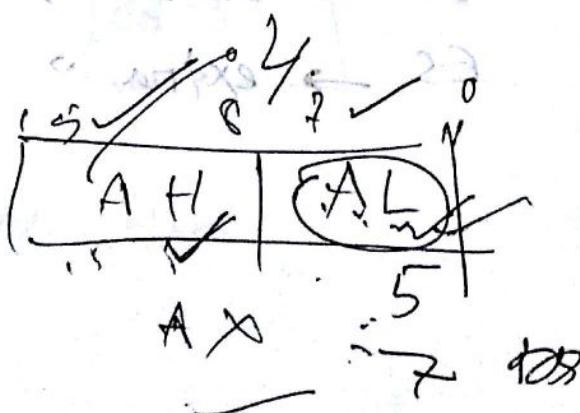


AL → 017



11111111
16x(5+15)

AL
010



S(A)-Day

Date: 15/5/2017

Chapter-2

Chapter-2:

→ Representation of numbers & characters.

Chapter-3:

Data Register → AX, BX, CX, DX

Segment Register → 4

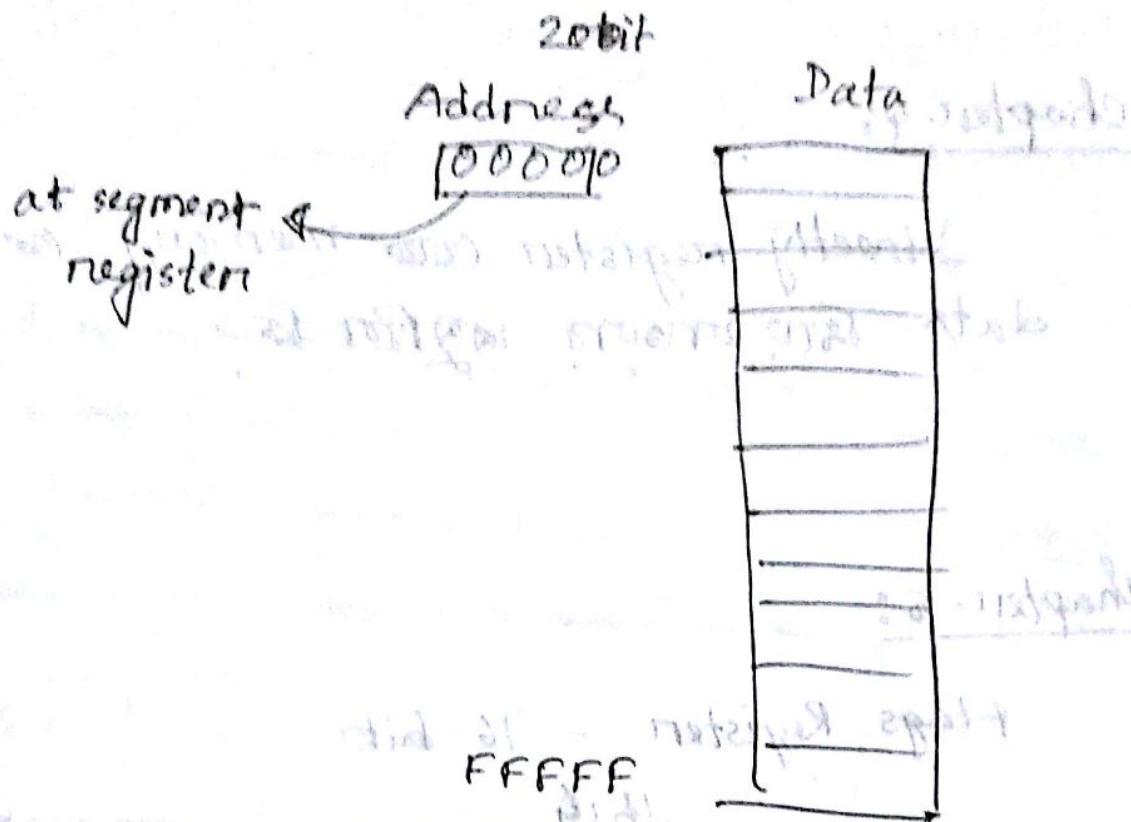
CS → code segment

16

DS → data

SS → stack

ES → extra



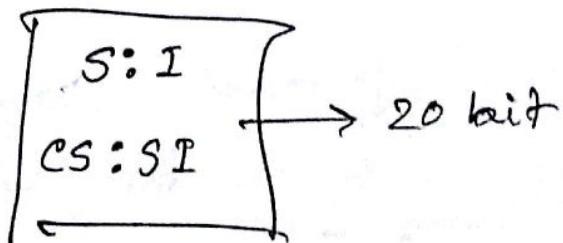
→ Indexing register

SI → Source Index

DI → Destination

SP →

DP →



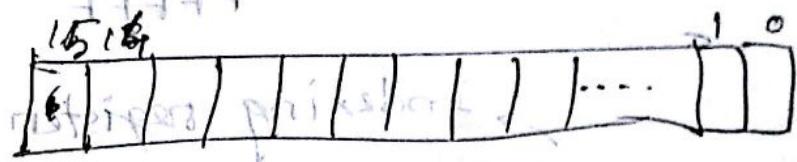
Startup operation

Chapter - 4:

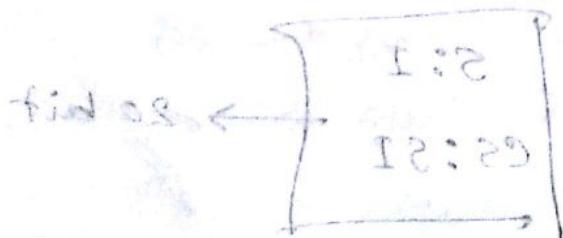
Directly register or memory
data ഫോറ്മാറ്റ് എന്താണ?

Chapter - 5:

Flags Register - 16 bit



control flag - 3 (operation control)
status " - 6



multiple outputs

4(B)-Day

Date: 03/7/2017

Chapter-6

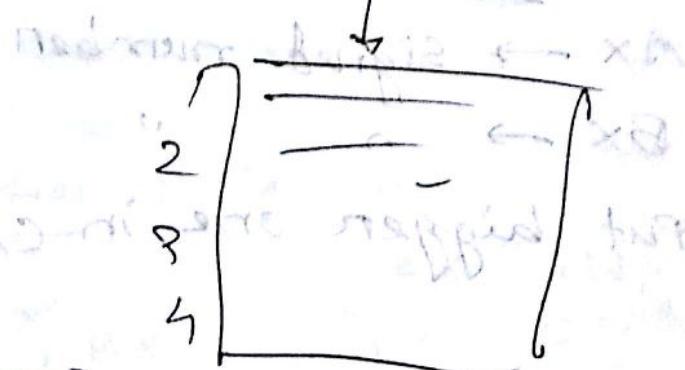
1 —
2 —
3 —

break

Br

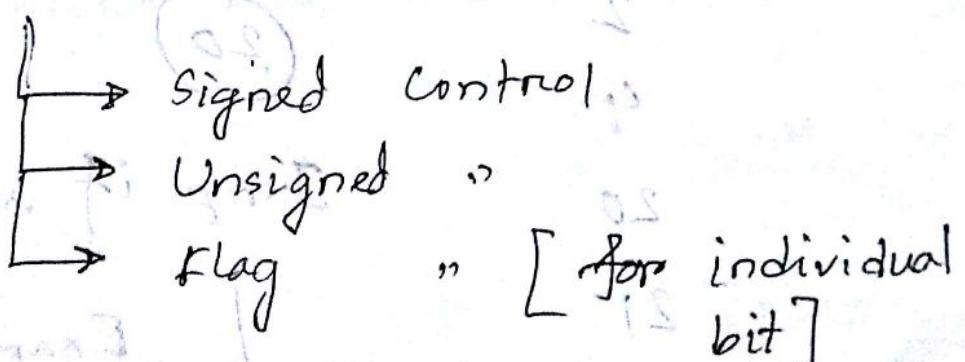
6.

10



Control Instructions:

1. Conditional control



2. Unconditional control

CMP → compare
dest, src

CMP AX, BX

JLE Room 5

Example - 6.1

AX → signed number

BX → " "

Put bigger one in CX

JA

Data

5

10

2

4

20

21

20

Jump if above

20

JZ → Jump if zero
if zero flag = 0

Example

$\frac{6 \cdot 3}{6 \cdot 4}$

Unconditional

MOV AX, BX

SUB AX, BX

JMP Next

Next:

Plug Conditional Contour

AND AX, BX

OR AX, BX

XOR AX, BX

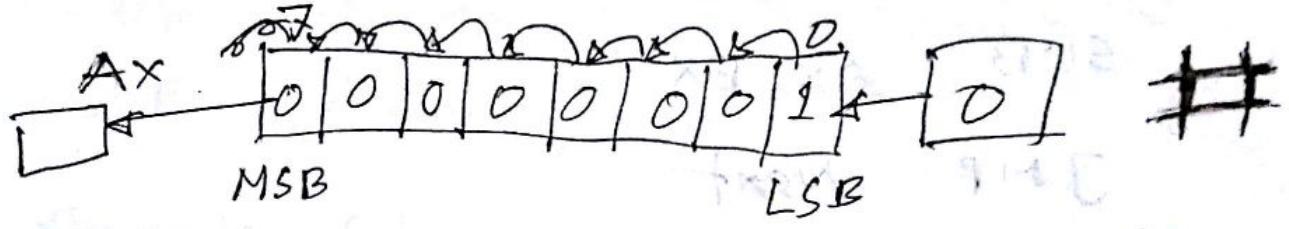
$$\begin{array}{r} \text{AX} \\ \text{BX} \\ \hline \text{AND} \xrightarrow{\leftarrow} \text{0000} \end{array}$$

original trace (XOR AX, AX)

8.7 segment

JXA JA2

chapter-7



00000010
00000100
00001000

} left shift
SHL

SHR → wrong value (5)

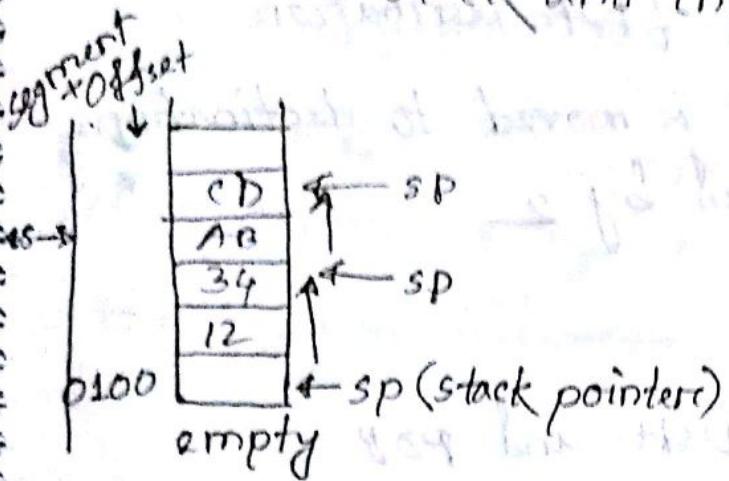
NOT → Negative करें (5 to -5)

Example 7.8

MOV CL, 3

SAL AX, CL

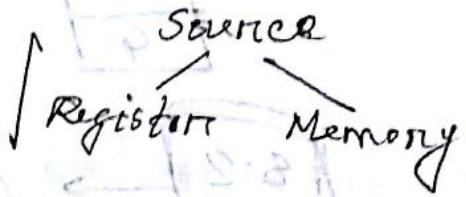
The stack and introduction to procedure



SS + SP
32 bit

- STACK 100H is stack if empty word top address 0100.

PUSH Source



- PUSH AX; $AX = 1234$
- PUSH BX; $BX = ABCD$

1. SP is decreased by 2
2. A copy of source content is moved to the address specified by SS:SP source unchanged

• PUSHF

| F → Flag

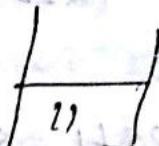
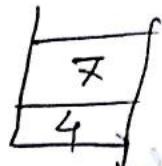
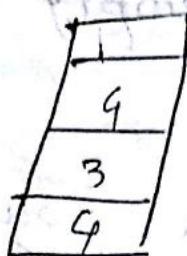
• POP AX

| POP destination

1. SS:SP \Rightarrow content is moved to destination
2. SP is decreased by 2

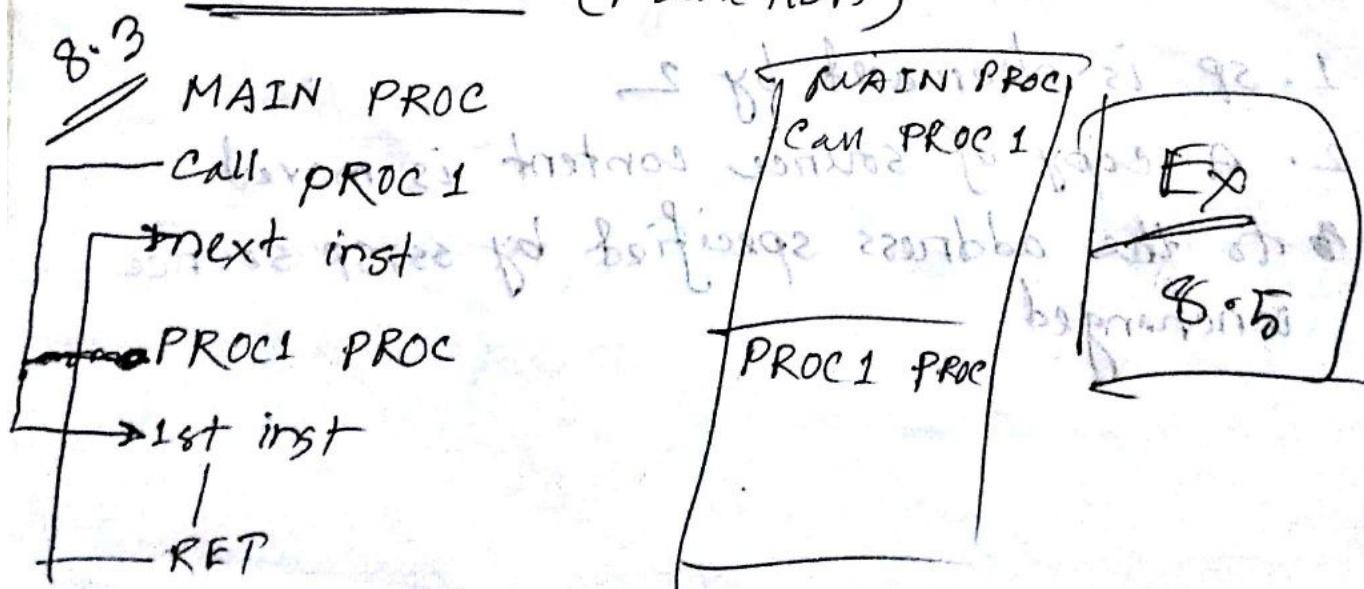
POPF

Addition using PUSH and POP



8.2

Procedure (Function)



Chapter-9

Multiplication and Division Instructions

MUL Source → Unsigned Ex. MUL BX
IMUL Source → Signed IMUL BX

for byte multiplication:

1. One number is contained in source
2. Other number is assumed to be in AL
3. Product in AX

For word multiplication:

1. One number is contained in source
2. Other is assumed to be in AX
3. Product in DX:AX

$n \text{ byte} \times n \text{ byte} = \max 2n \text{ byte}$

" + " = $2n + 1 \text{ byte}$

DIV Source

IDIV Source

CT-2

Chapter 4

Introduction to IBM PC Assembly Language

statement

Instruction

Assembly directive

which the assembler

translates into
machine code

which instructs the
assembler to perform
some specific tasks.

Both ~~asse~~ & instructions and directives have
up to four fields:

name operation operand(s) comment

START: MOV CX, 5 ; initialize counter

Operation

for an instruction →

Symbolic operation code (opcode)

→ The assembler translates a
symbolic opcode to a machine
language.

Example: MOV, ADD, SUB

For an assembler directive →

→ Pseudo-operation code (pseudo-op)

→ are not translated into machine code.

Example: PROC

Operand

For instruction

NOP ; No operand, does nothing

INC AX ; one operand

ADD WORD1,2 ; two operands

↙
destination
operand

↘
source
operand

For Assembler directive

The operand field usually contains more information about the directive.

Comment

The comment field of a statement is used by the programmer to say something

Binary \rightarrow 1001B (or B)

Decimal \rightarrow 123d (or D)

Hexadecimal \rightarrow 0A8h (or H)

→ must be decimal
digit. Otherwise
assembler would be
unable to differentiate
between variable and
hexadecimal numbers.

Characteris

'Hello' / 'A'

Pseudo-op stands for

DB \rightarrow define byte

DW \rightarrow " word "

DD \rightarrow double word

DQ \rightarrow " quad word " (four words)

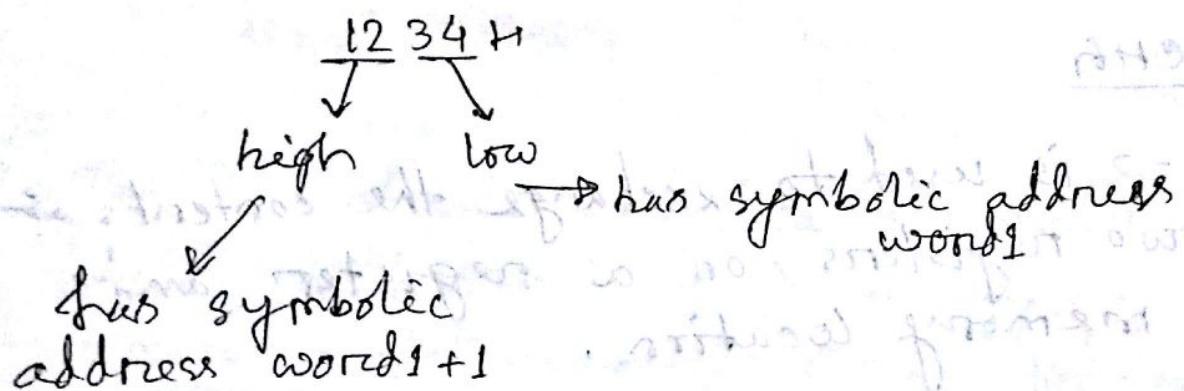
DT \rightarrow " ten bytes "

→ translate to binary form into 16-bit words
for example 10000000000000000000000000000000

* In assembly language, an array is just a sequence of memory bytes or words.

B_array DB 10h, 20h, 30h

* High and low bytes of a word



* EQU (Equates)

name EQU constant

LF EQU 0AH

[0AH → line feed character]

The name LF may now be used in place of 0AH anywhere in the program.

→ assigns the name LF to 0AH.

* MOV

→ MOV instruction is used to transfer data between registers.

MOV dest, source

* XCHG

→ is used to exchange the contents of two registers, one register and a memory location.

XCHG AH, BL

* MOV and XCHG between memory location is not allowed.

Move word1, word2

* ADD and SUB

ADD dest, source

SUB dest, source

* INC and DEC

INC destination

DEC destination

* NEG

→ is used to negate the contents of the destination.
NEG dest.

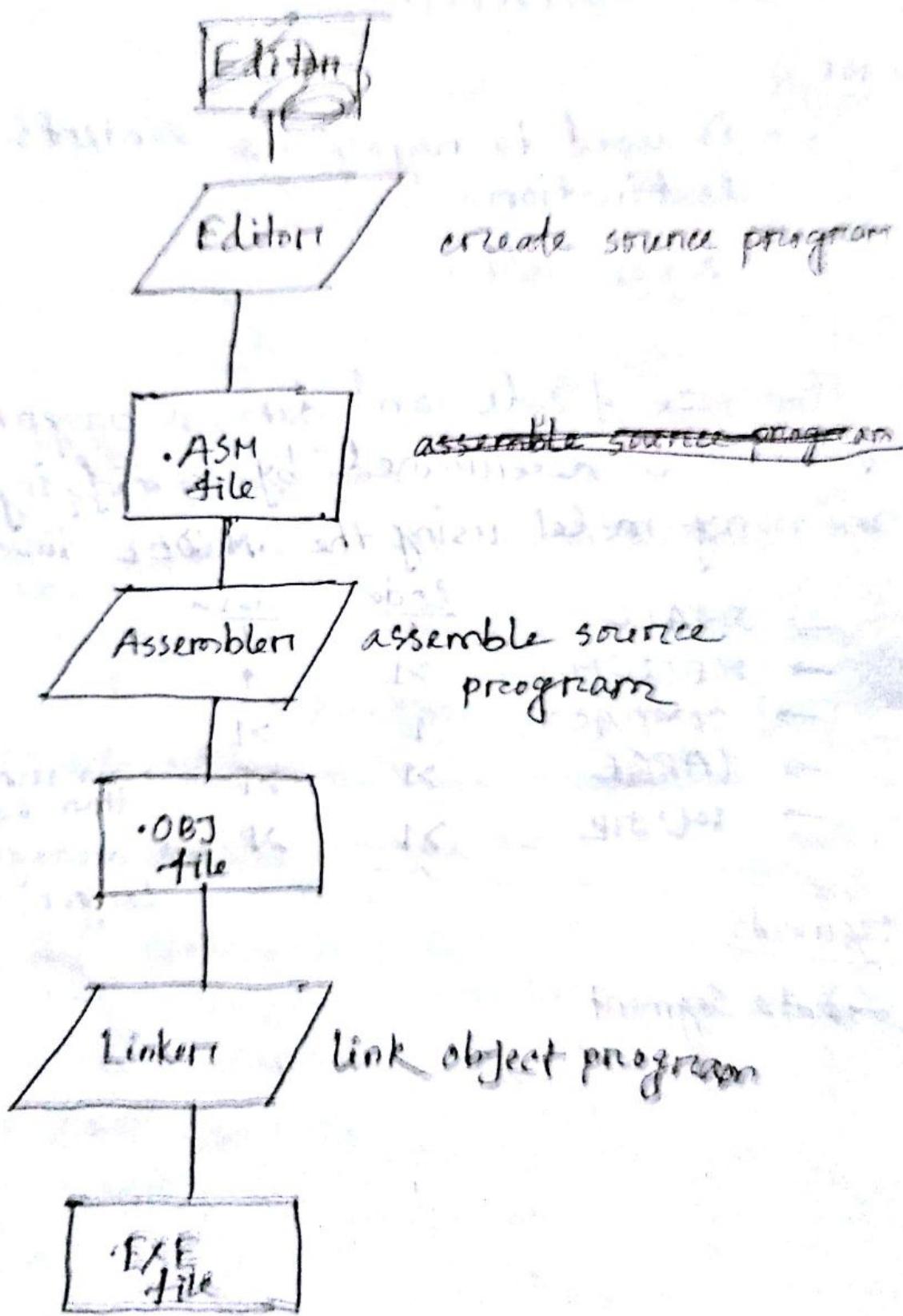
* The size of code and data a program can have is determined by specifying a memory model using the .MODEL directive.

	<u>Code</u>	<u>Data</u>
→ SMALL	1	1
→ MEDIUM	>1	1
→ COMPACT	1	>1
→ LARGE	>1	>1 → no arrays larger than 64K bytes
→ HUGE	>1	>1 → arrays may be larger than 64K bytes.

Segments

→ Data Segment

Programming Steps

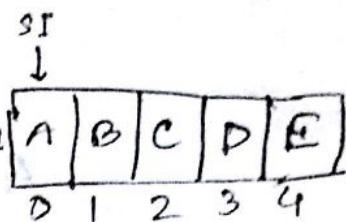


9(A) - Day

Date: 13/8/2017

The String Instruction

STR1 DB 'ABCDE'
↓
1 byte



DB →
Seg: OFF

0200	A
0201	B
0202	C
0203	D
0204	E

DW →

0200	A
0202	B



DF (Direction Flag) → storing operation

DF = 0, Left to right

DF = 1, Right to left

CLD → clear Direction Flag

STD → Set " "

SI
Source DI
Destination

~~DS:SI~~ → Source

~~ES:DI~~ → Destination

~~MOV~~ ~~MOVSB~~ MOVSB

MOV AX, @ DATA

MOV DS, AX

MOV ES, AX

LEA SI, STR1

LEA DI, STR2

CLD

MOVSB

MOVSB

MOVSB

MOVSB

MOVSB

CLD

LEA SI, STR1

LEA DI, STR2

MOV CX, 5

REP MOVSB

After MOVSB

SI

↓ →

STR1	A	B	C	D	E
	0	1	2	3	4

DI

↓ →

STR2	A	B	C	D	E
	5	6	7	8	9

Offset add. handle

MOVS B SI DI

fhcv. MOVS B

(Copy of main)

Reverse

LEA SI STR1+4

LEA DI STR2
STD
MOV CX, 5

MOVE:

MOVSB

ADD DI, 2

Loop MOVE

Store String

STOSB

Move the content of AX to the address ES:DI

LODSB (Mem to reg →)

[load string]

DS:SI → AX

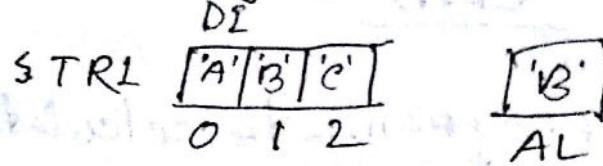
DS:SI ← AX

DS:SI ← AX

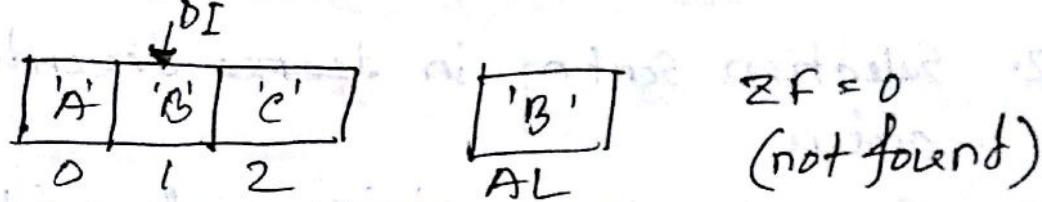
DS:SI ← AX

DS:SI ← AX

SCASB (Scan string)



After SCASB



CMPSB (Compare string)

(C-W)(W-W)W

W

W

9(b)-Day

Date: 20/8/2017

. LAB

1. Write a program to calculate factorial N where $N < 10$
2. Selection sorting in ~~decreasing~~ descending order
3. From 4×4 by matrix. find out the maximum and minimum element.

(Printed program) 829MS

ΘX , ΘN

$$N(N+1)(N-2)$$

~~M2L~~ $\Theta X, \Theta X-1$

$N \times N$

.MODEL SMALL

.DATA

x dw 5

POP DX

DIT DL

.

'code

mov ax, @data

mov ds, ax → counter

mov cx, x }
5 }

mov ax, x } → result
5 }

HERE:

DEC X ; x = 9

MUL x ; ax = (x * ax)

DEC CX ax = 5 * 4 = 20

JNZ HERE

[cx = ?]

mov ax, 4CH

int 81H

end

Prob

CSE14

i input: WE ARE CSE14

Output: 41ESC ERA EW

ii search for CSE14

11(A) - Day Date : 22/8/2018

Direct Memory Access (DMA)

Addressing mode → chapter 10

Interrupt structure } → after End
RISC CISC }

Memory → RAM

Process → computing (ALU)

DMA विरुद्ध I/O विरुद्ध CPU विरुद्ध

Acknowledgement → Data flow साथि
कर्तव्य

Control Instruction

→ Opcode
→ Operand

Data bus

Address bus

DMA → improvement performance in
terms of time.

11(D)-Day

Date: 11/9/2017

Use of RISC Today

Cache memory \rightarrow RAM of Processor

Address mapping \rightarrow { unit cache for instruction
DDIO address

RISC PowerPC CISC \leftarrow From here

\hookrightarrow RISC \rightarrow Reduced Instruction Set Computer

RISC architecture \rightarrow no cache needed.

PowerPC \rightarrow Improved version of RISC

\rightarrow integer 40 bit ALU

\rightarrow float 40 bit ALU

Storage \downarrow

CISC \rightarrow Complex Instruction Set Computer

Like \rightarrow

ADD AX, BX, CX, DX, EX (सिर्फ़ यह)

(i) Implementing datapath \rightarrow AND
 \rightarrow with the help of registers