Heaven's light is our guide

Rajshahi University of Engineering & Technology

Department of Computer Science & Engineering

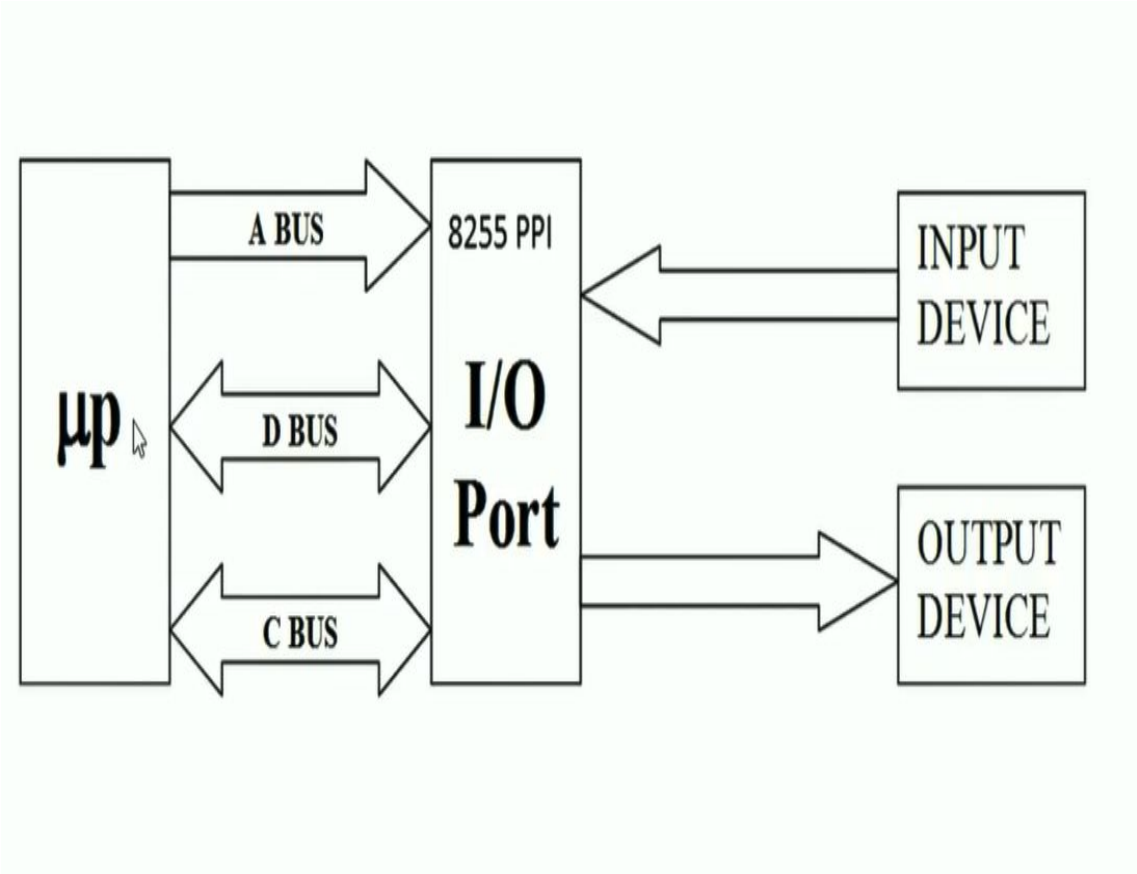
Course Title: Peripherals & Interfacings

Topic : 8255 Programmable Peripheral Interface

Can we connect input/output device to 8086 microprocessor directly?

Can we connect input/output device to 8086 microprocessor directly?

- The reason is 8086 microprocessor has no input output ports. If we want to connect any input or output device to the 8086 microprocessor we need an interfacing device, that interfacing device is programmable peripheral interfacing device.



8255 Programmable Peripheral Interface

Features of 8255:

- General purpose programmable device.
- It is programable means can transfer data under various conditions from simple I/O to interrupt I/O.
- Flexible, commercial, versatile and internal circuitry is somewhat complex.
- It has 24 input-output lines.

i. Port A(PA0-PA7) – 8 Lines

ii. Port B(PB0-PB7) – 8 Lines

iii. Port C(PC0-PC7) – 8 Lines. Port C further divided into two groups.

- Upper(pc4-pc7).
- Lower(pc0-pc3).
- Each port can be programmed as an input port and output port.
- These ports are further divided into two groups.
    1. Group A (Port A and Port C upper). Group A has 12 lines.
    2. Group B (Port B and Port C lower). Group B has 12 lines.

- The two groups can be programmed in different modes.

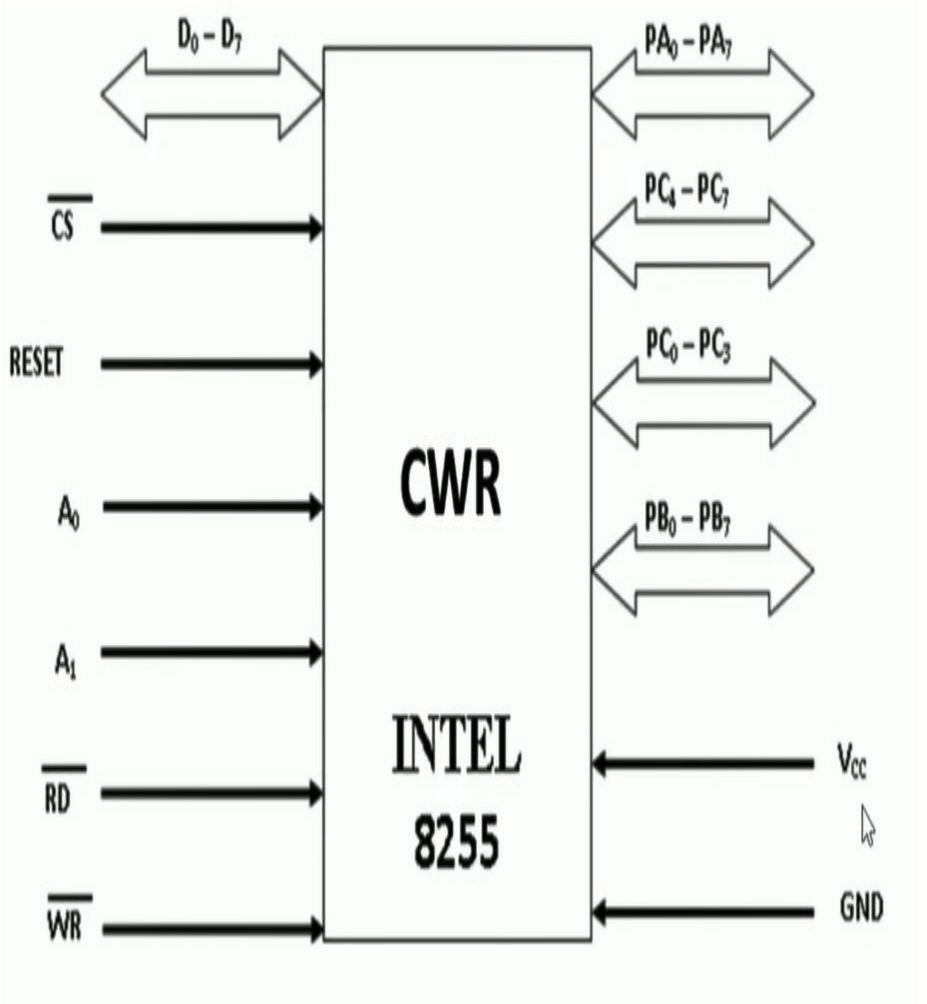
1. **Bit set reset mode**- It decides which bits are to set and reset.

2. **Input output mode**- Which port is going to be used as input port or output port. Input output mode is further divided into three modes.

i. **Mode 0**

ii. **Mode 1**

iii. **Mode 2**



Pin Description of 8255

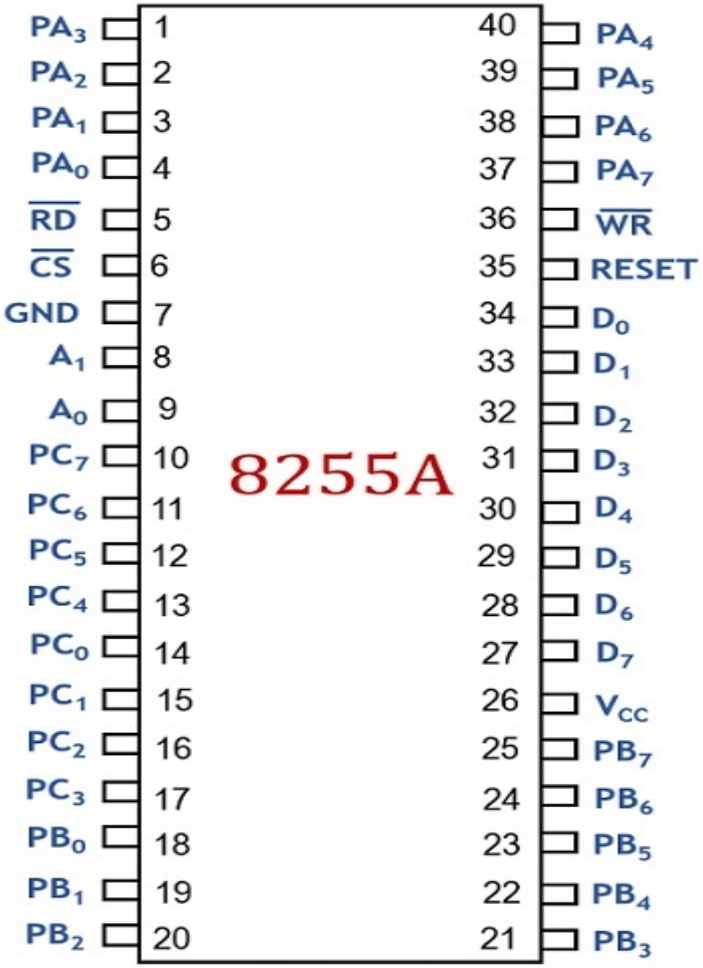
CS (Chip Select): A low on this input selects the chip and enables the communication between 8255 and microprocessor.

RD (Read Input): when this signal is low, 8255 will send out data or status information to the microprocessor through the data bus.

WR (Write Input): A low on this input enables the microprocessor to write data or control words to the 8255.

Reset: This is an active high signal. It clears the control register and sets all ports in the input mode. There are various modes in 8255, so which mode is going to be selected it is decided by the control word that is written in the control register.

Data bus buffer: It is a tri-state 8-bit buffer, which is used to interface the microprocessor to the system data bus. Data is transmitted or received by the buffer as per the instructions by the CPU. Control words and status information and data is also transferred using this bus.



Pin Diagram of 8255 PPI

Electronics Desk

Pin Description of 8255

A1 and A0: These two pins are used to select the port. These input signals work with RD, WR, and one of the control signal.

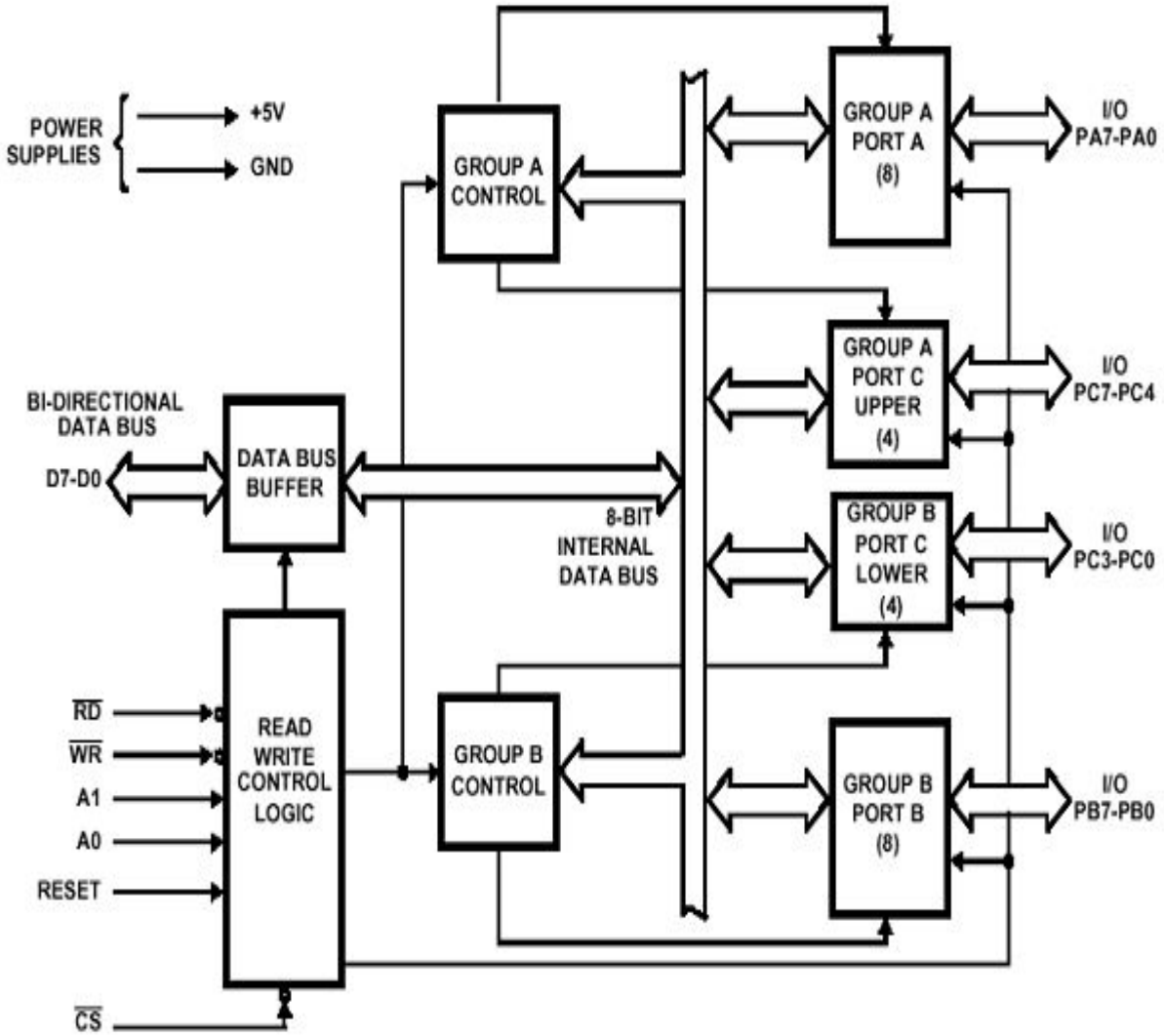
Following is the table showing their various signals with their result.

A_1	A_0	RD	WR	CS	Result
0	0	0	1	0	Input Operation PORT A → Data Bus
0	1	0	1	0	PORT B → Data Bus
1	0	0	1	0	PORT C → Data Bus
0	0	1	0	0	Output Operation Data Bus → PORT A
0	1	1	0	0	Data Bus → PORT B
1	0	1	0	0	Data Bus → PORT C
1	1	1	0	0	Data Bus →Control register

Block Diagram and Functional Description of 8255

Port A, Port B and Port C:

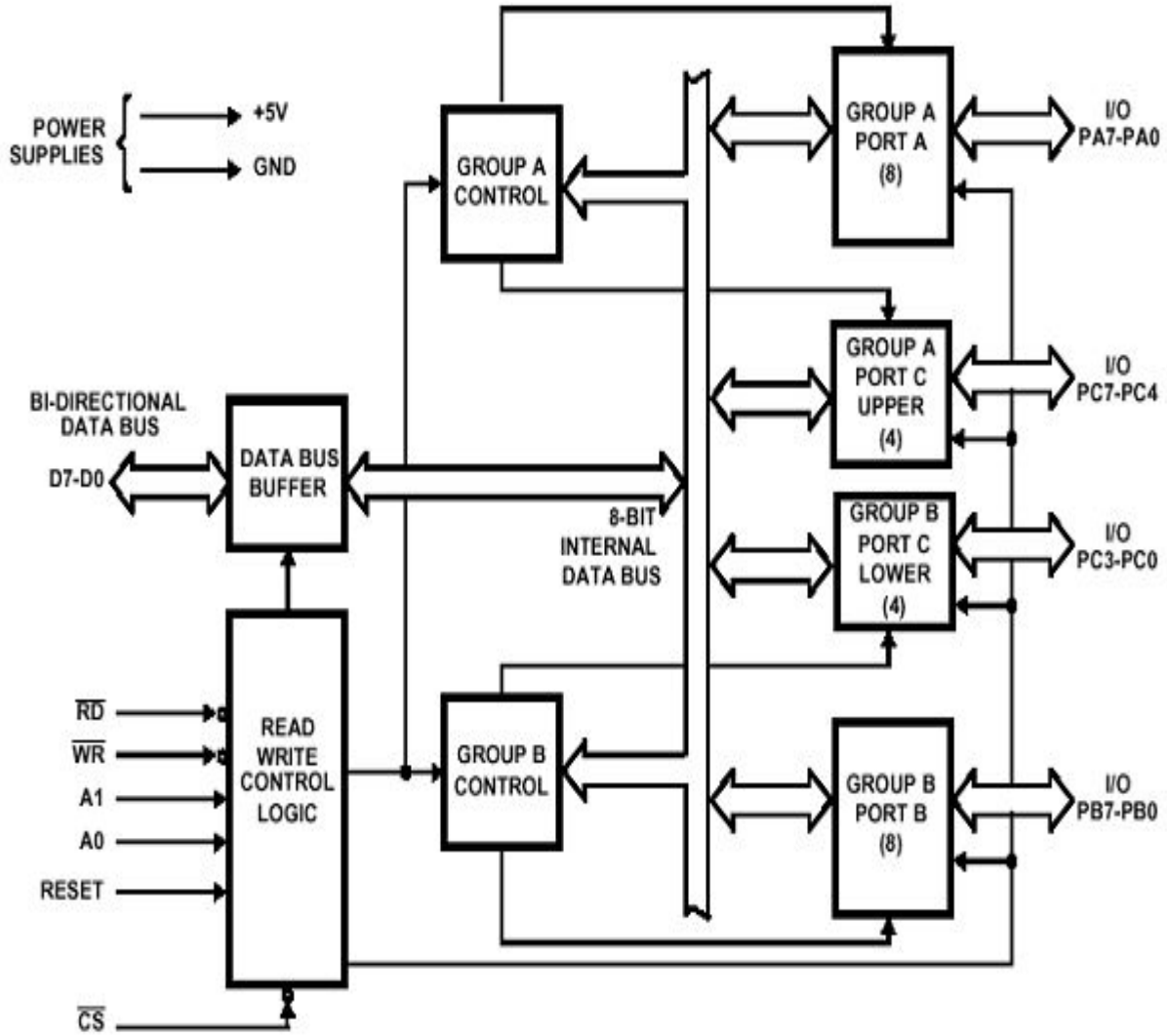
- 8-bit ports and work as input output port. Port A has one 8-bit output latch/buffer (when it works as output port) and one 8-bit input latch (when it works as input port).
- Port B has one 8-bit output latch/buffer (when it works as output port) and one 8-bit input latch (when it works as input port).
- Port C has one 8-bit output latch/buffer (when it works as output port) and one 8-bit input latch (when it works as input port).



Block Diagram and Functional Description of 8255

Group A and Group B Control:

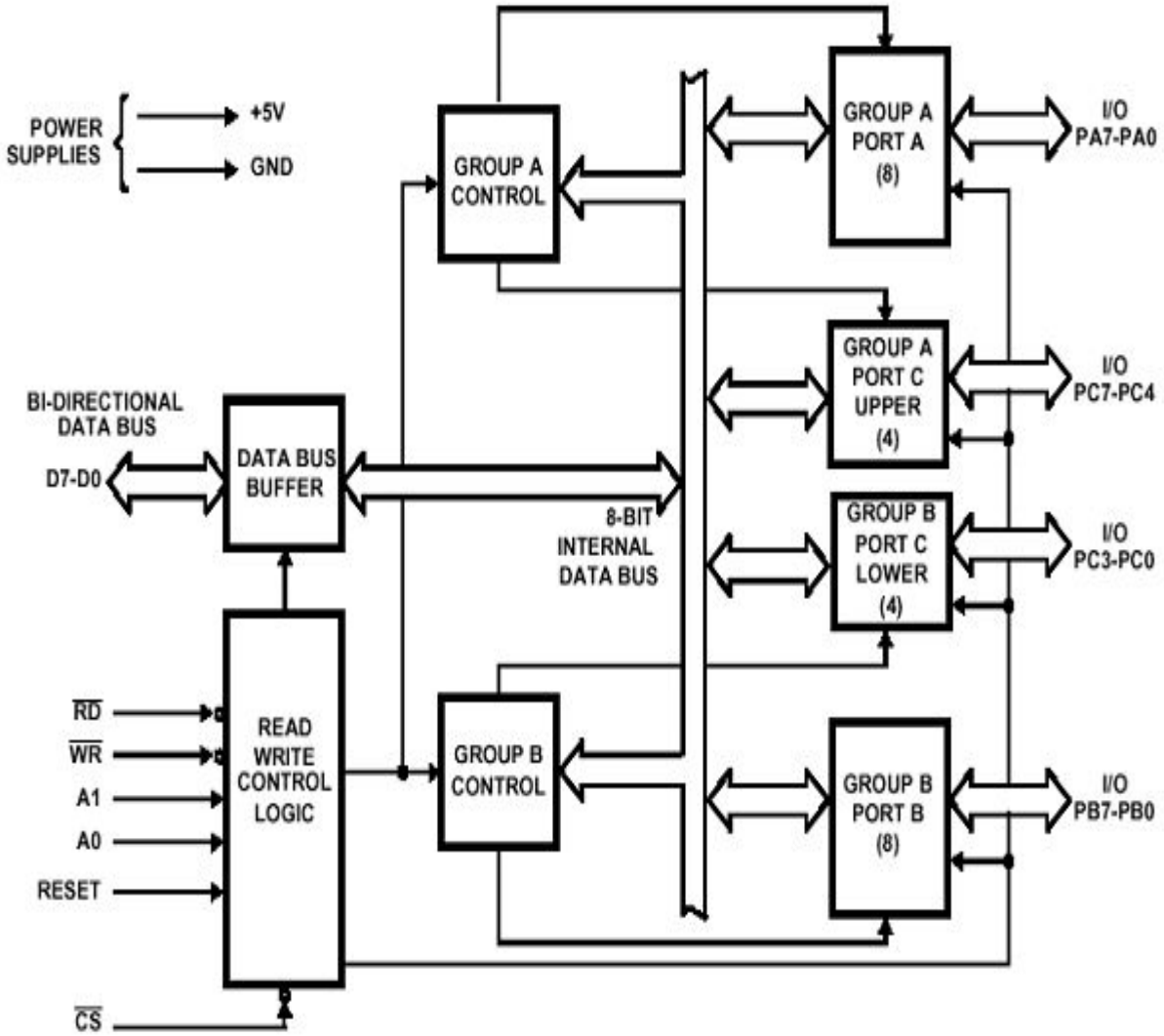
- The functional configuration of each port is programmed by the system software.
- The control words are outfitted by the CPU. Configure the associated ports of the each of the two groups.
- The control word contains information like mode set reset bits, which mode is going to be selected, which port will act as an input, which port will act as an output, which group is going to be activated. The control word initializes the functional configuration of 8255.
- Control word is written into the control register by the microprocessor. No read operation is associated with it.



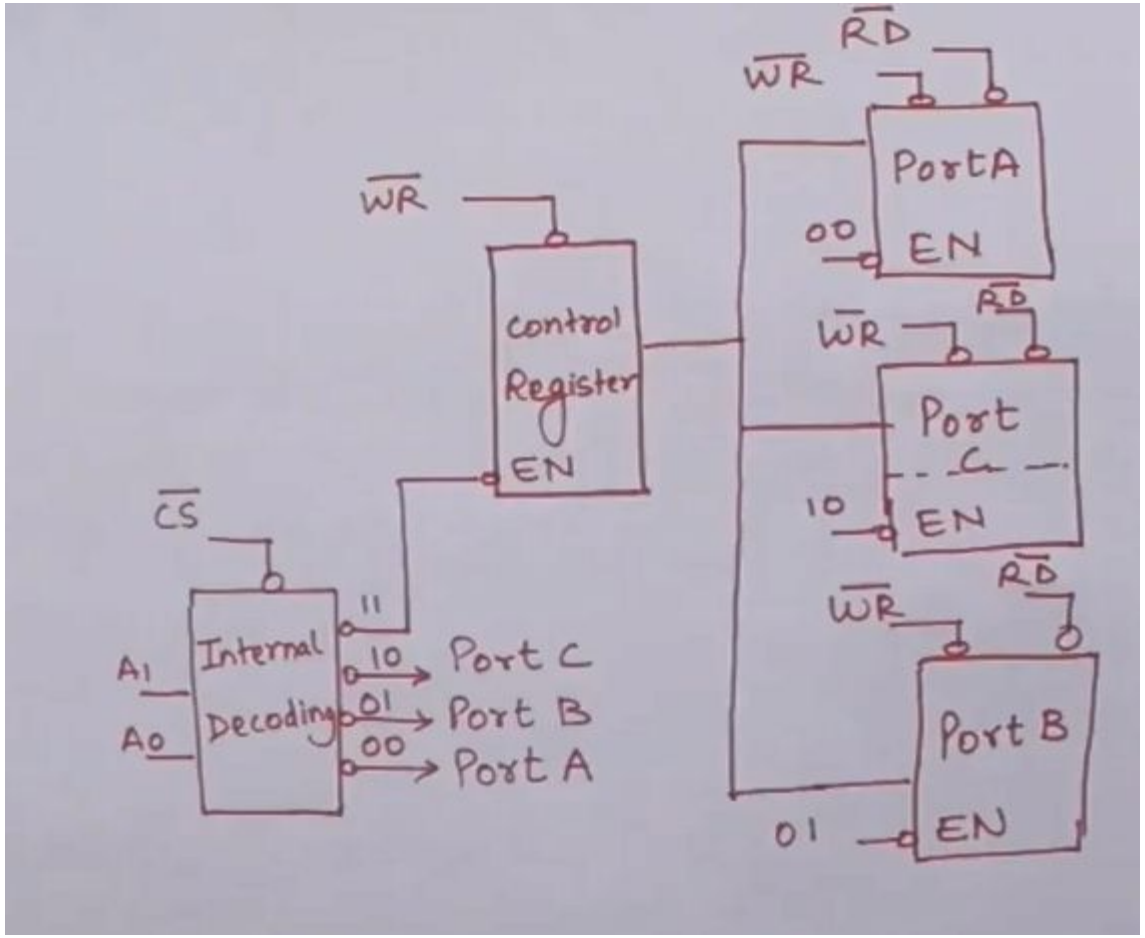
Block Diagram and Functional Description of 8255

Read Write control logic:

- Its function is to control the internal operation of the device and to control the transfer of data and control or status words.
- It accepts inputs from the CPU address and control buses and in turn issues commands to both the control groups.



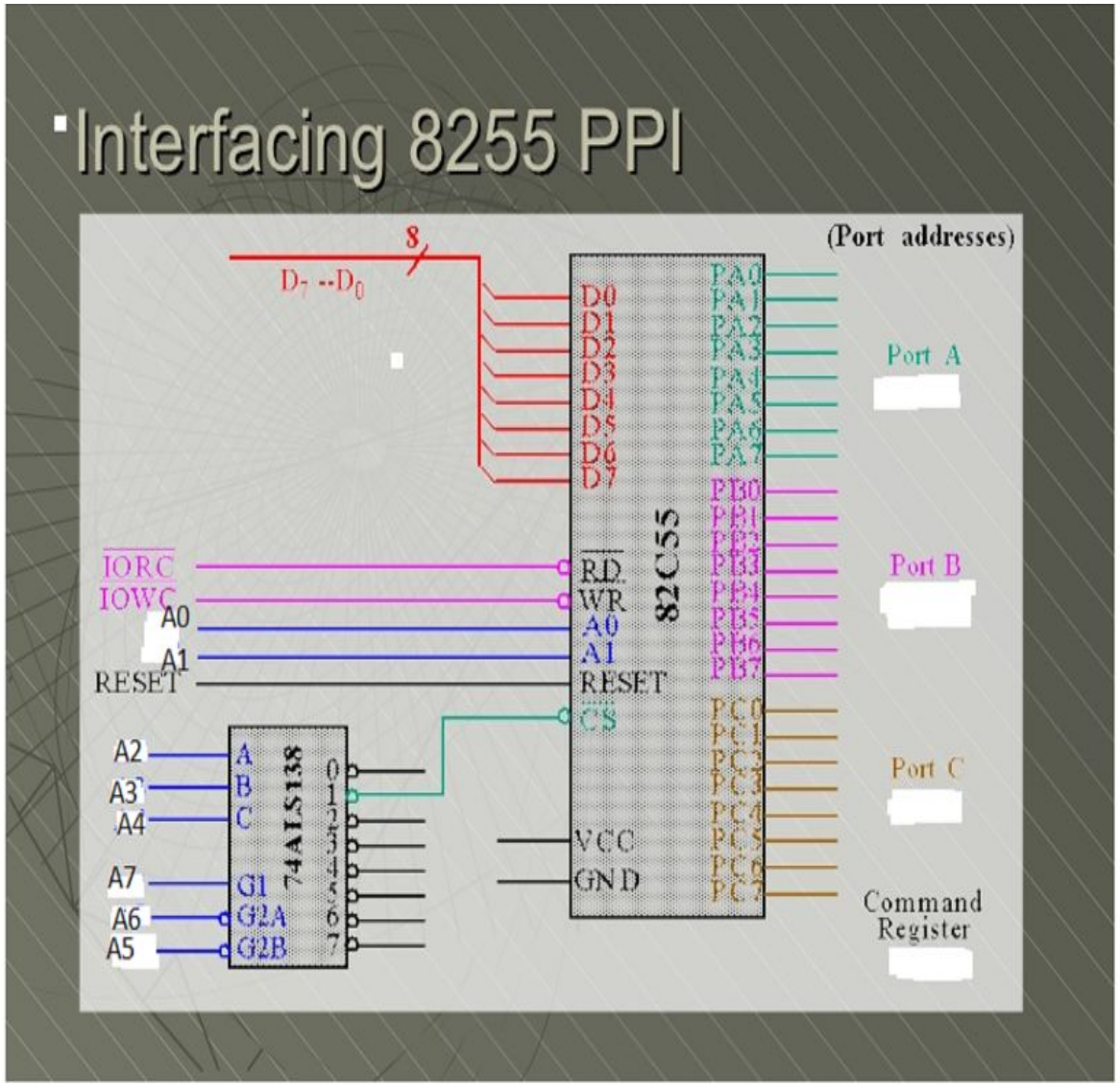
Operational Modes of 8255



Interfacing 8255 with 8086 microprocessor

Chip Select (CS)						Port Selection		
A7	A6	A5	A4	A3	A2	A1	A0	Port
1	0	0	0	0	1	0	0	A
1	0	0	0	0	1	0	1	B
1	0	0	0	0	1	1	0	C
1	0	0	0	0	1	1	1	Control Register

To communicate with 8255 input/output device microprocessor activate the device by sending the address that is showing in the address generation table.



Two modes of operation of 8255

1. **Bit set reset mode**
2. **Input output mode**

Control Word

D7	D6	D5	D4	D3	D2	D1	D0
1 / 0							

1 = Input Output Mode

0 = Bit Set Reset Mode

Two modes of operation of 8255

Bit Set Reset Mode:

- This mode is used to set or reset the bits of port C.
- BSR mode does not affect the function of PORT A and PORT B.
- Bit D7 of control word is reset to zero.

Control Word

D7	D6	D5	D4	D3	D2	D1	D0
0	Don't care bits, usually set to zero.			Bit select of Port C			Set/Reset

D3	D2	D1	Port C
0	0	0	PC0
0	0	1	PC1
0	1	0	PC2
0	1	1	PC3
1	0	0	PC4
1	0	1	PC5
1	1	0	PC6
1	1	1	PC7

- **Here, the D3, D2, D1 selects the particular bit of port C to set or reset it.**
- **To set or reset the particular bit it depends on D0 bit.**
- **If D0 bit is 0 then the selected bit of port C is set to zero.**
- **If D0 bit is 1 then the selected bit of port C is set to 1.**

Two modes of operation of 8255

Input Output Mode:

1. Mode 0 – Simple input output mode
2. Mode 1 – Input output mode with handshake
3. Mode 2 – Bidirectional mode

Control Word

D7	D6	D5	D4	D3	D2	D1	D0
	Group A				Group B		
1	Mode selection 00 – Mode 0 01 – Mode 1 1X (Don't care) – Mode 2		Port A 1 – input 0 – Output	Port C Upper (pc4-pc7) 1 – input 0 – Output	Mode selection 1 – Mode 1 0 – Mode 0	Port B 1 – input 0 – Output	Port C Lower (pc0-pc3) 1 – input 0 – Output

Input Output mode of 8255

Mode 0:

1. Port A and Port B are used as 8-bit i/o ports.
2. Port C is used as two 4-bit i/o ports.
3. Each port can be programmed as an input port or an output port.
4. Output are latched.
5. Input are not latched.
6. Ports do not have interrupt or handshaking capability.

Input Output mode of 8255

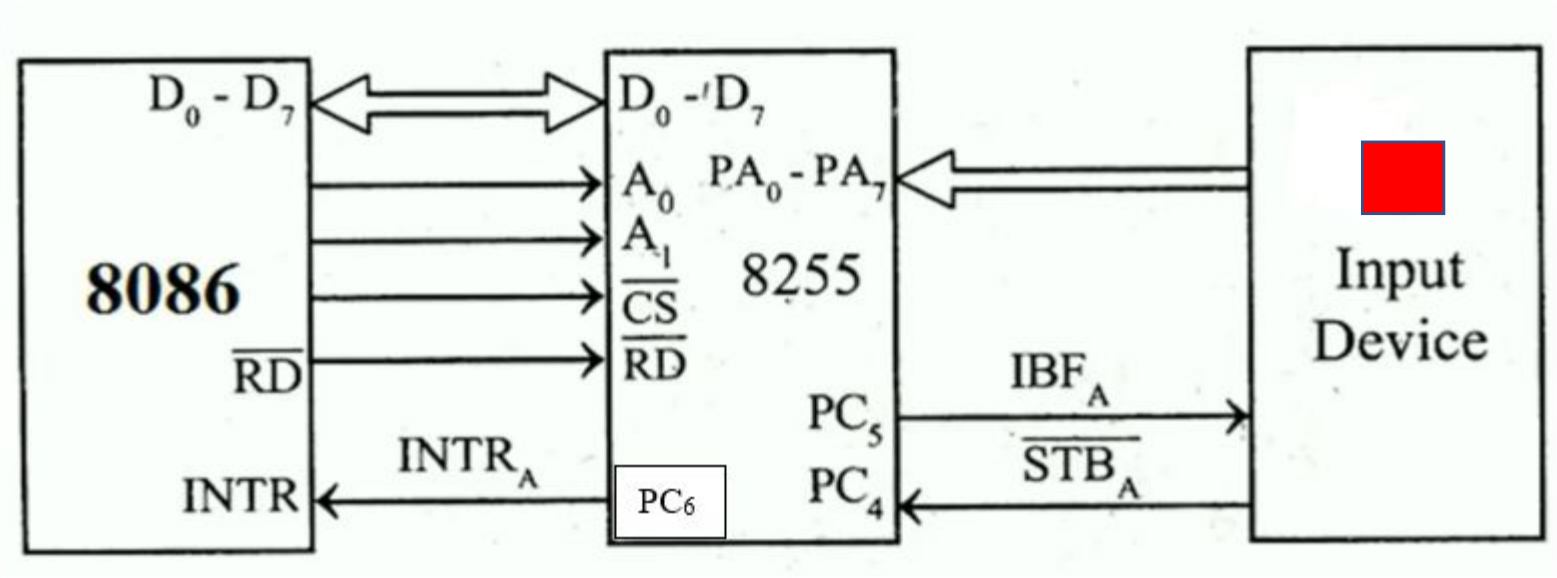
Mode 1 Input Operation:

1. Input or output with handshake (use some lines of other port for itself).
2. Handshake signals are exchanged between microprocessor and peripherals for data transfer.
3. Port A and Port B function as 8-bit i/o ports.
4. Each port (A and B) use 3 lines from port C as handshake signals.
5. Remaining lines can be used as I/O functions.
6. Input and output data are latched.
7. Interrupt logic is supported.

Input Output mode of 8255

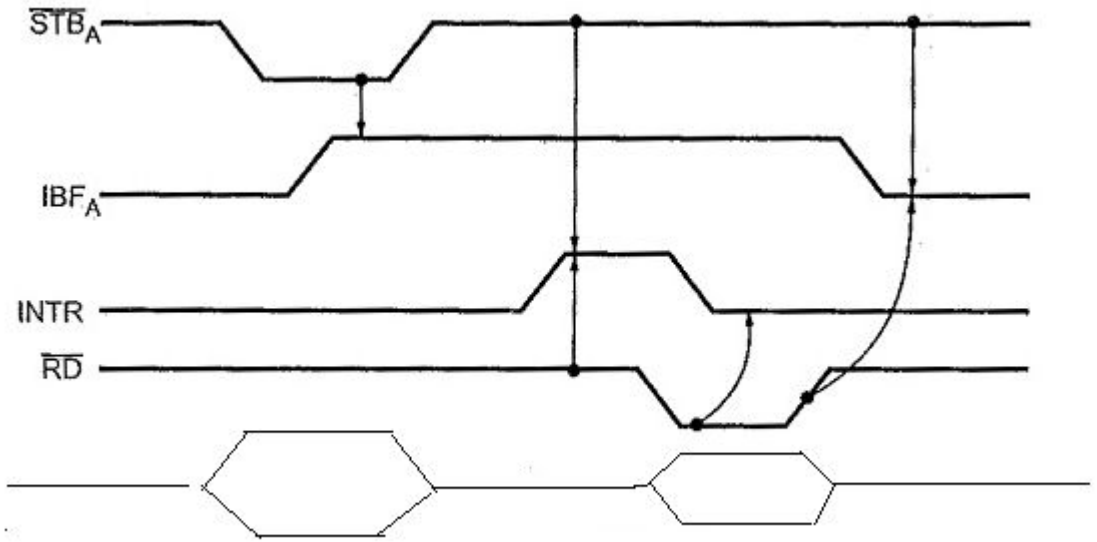
❖ **Mode 1 Input Operation:**

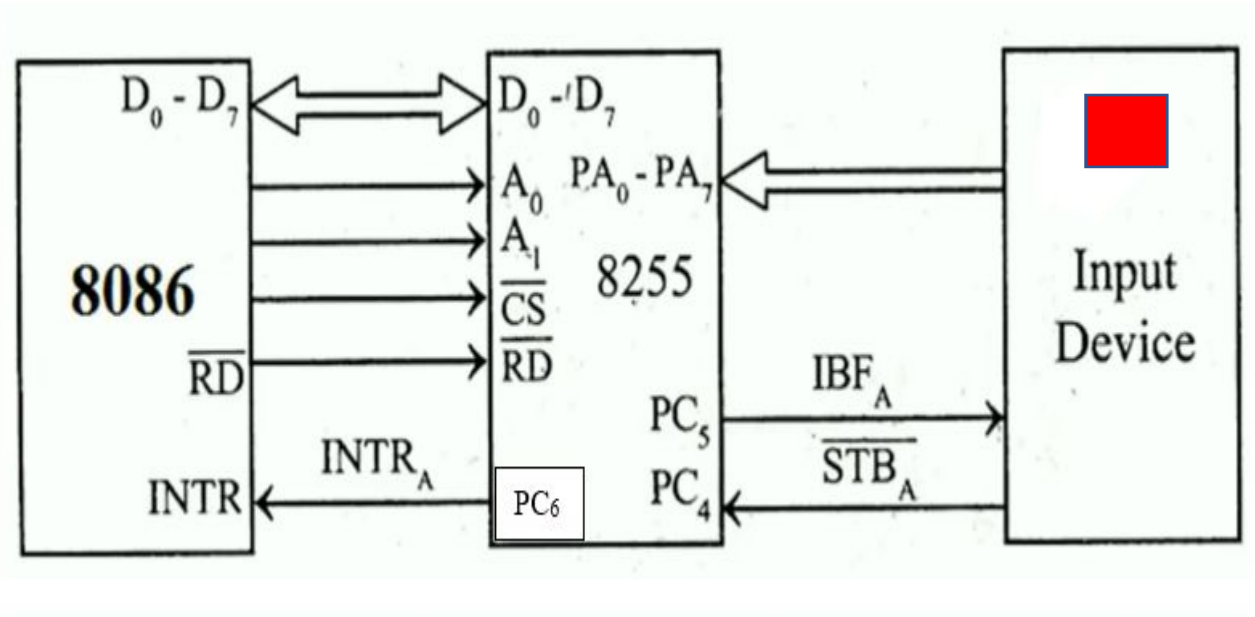
1. At first, the input device will send active low strobe signal to 8255 and then data is sent to the port A of 8255.
2. In response, the 8255 will send a active high signal through IBF to the input device.
3. Then the 8255 will send a interrupt request signal to the INTR pin of the 8086 microprocessor.
4. Then the 8086 microprocessor will read the data from port A through the data bus.



Input Output mode of 8255

Timing waveform of Mode 1 input operation:





Input Output mode of 8255

Mode 1 Input Operation:

Strobe Input (STB):

1. Active low signal.
2. Generated by a peripheral device and sends to the 8255 and 8-bit data is transmitted to 8255.
3. In response, 8255 generates IBF and INTR signal.

Input buffer full (IBF):

1. Acknowledgement by 8255 that the input latch has received the data byte.
2. Reset when microprocessor reads the data.

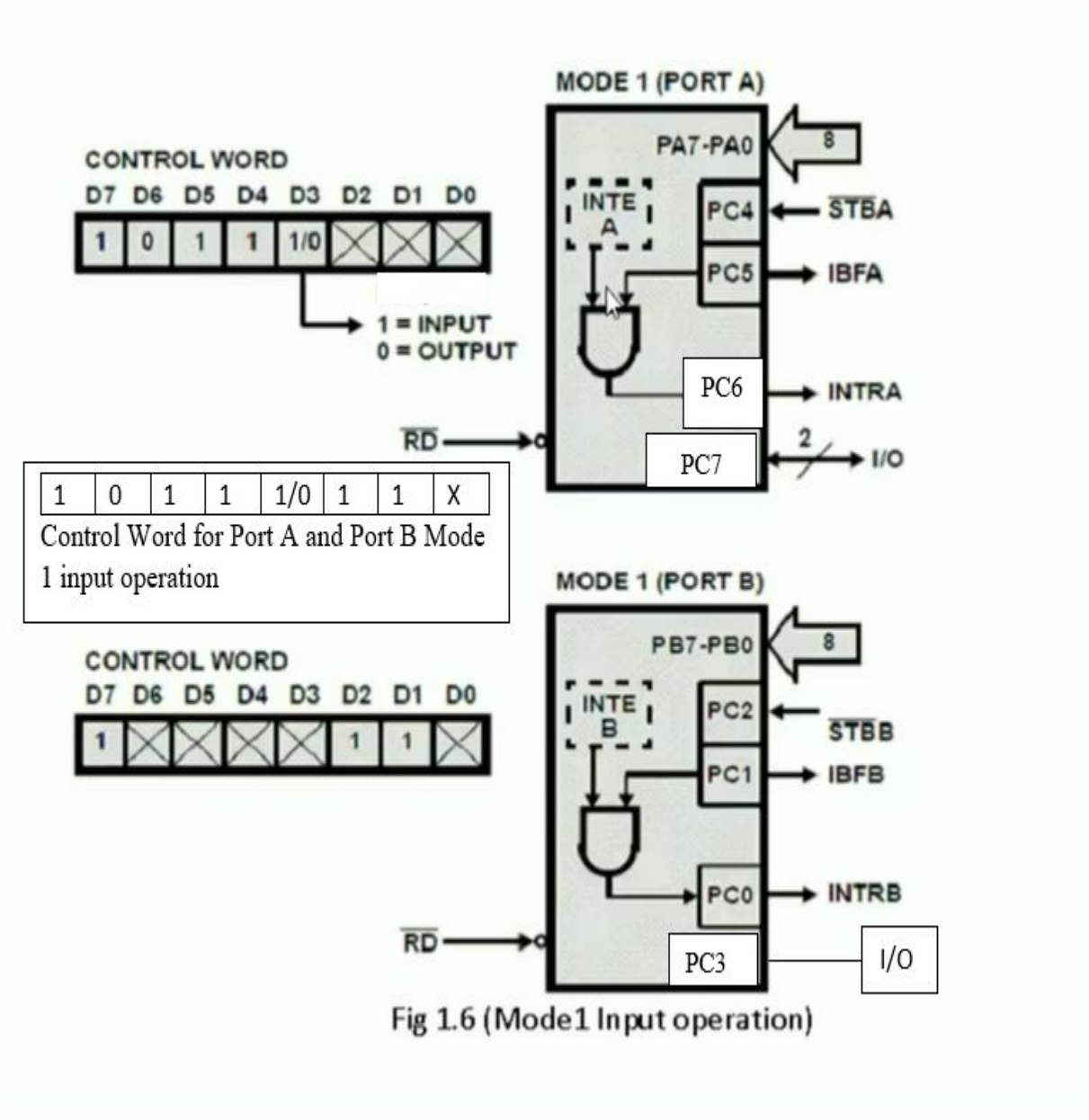


Fig 1.6 (Mode1 Input operation)

Input Output mode of 8255

INTR (Interrupt Request):

1. Output signal is used by the 8255 to interrupt the microprocessor.
2. It is generated if STB, IBF and INTE are active high.

INTE (Interrupt Enable):

1. It is in logic 1 and used to set the INTR.

Input Output mode of 8255

Mode 1 Output Operation:

Output Buffer Full ($\overline{OBF}$):

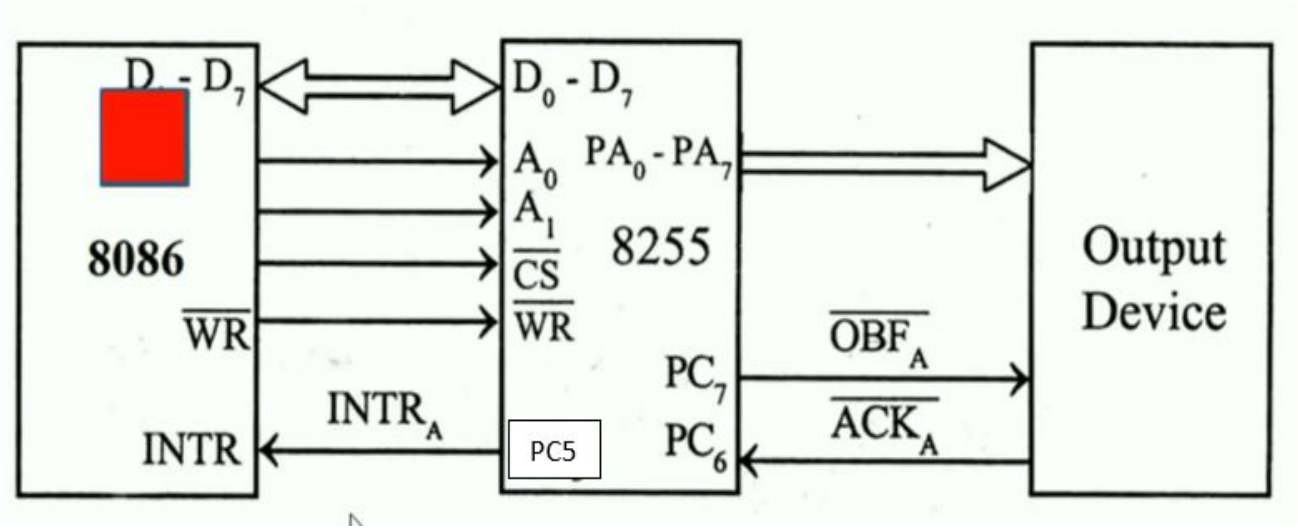
1. $\overline{OBF}$ goes low, when the microprocessor writes data into the output latch of the 8255.
2. Indicates that new data is ready.

Acknowledgement ($\overline{ACK}$):

1. This signal is generated by the peripheral device and sends the acknowledgement to the 8255 that it already received the data.

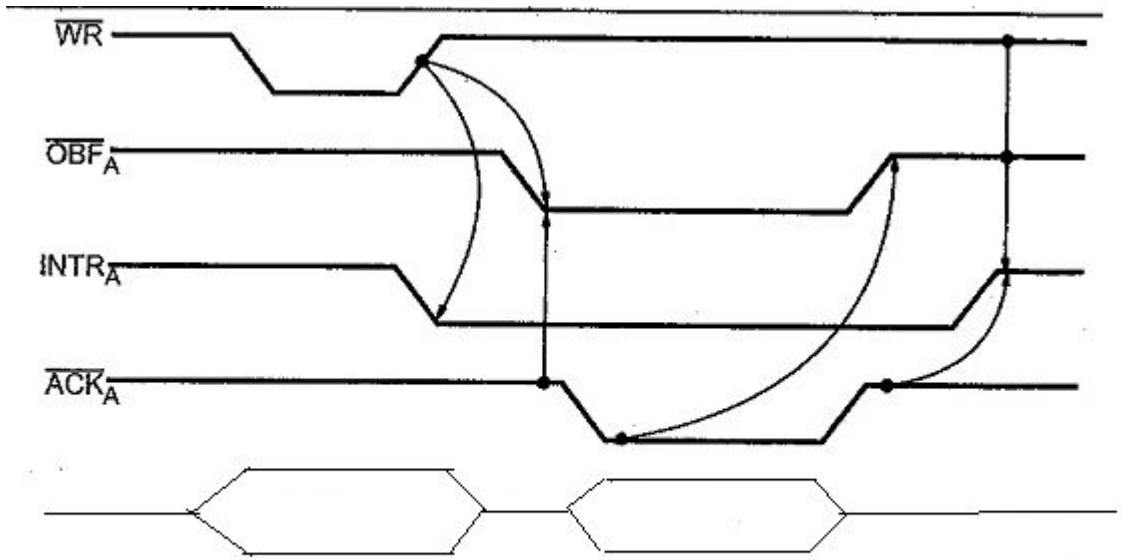
INTR (Interrupt Request):

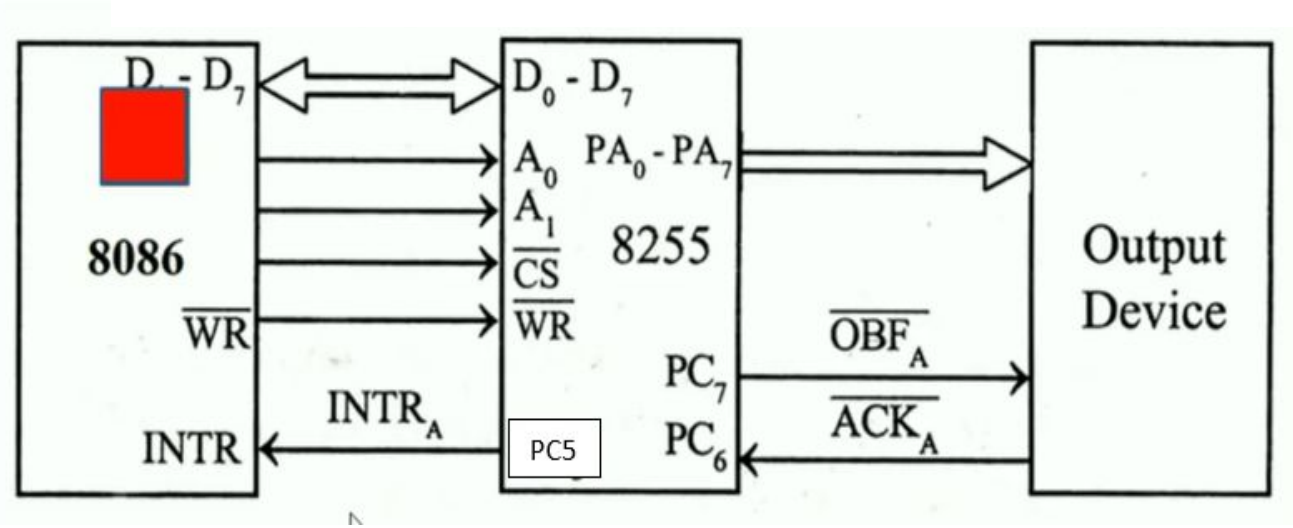
1. It is in logic 1 when the INTE, $\overline{ACK}$, $\overline{OBF}$ are all in logic 1.
2. It interrupts the microprocessor to get ready to write the next byte of data.



Input Output mode of 8255

Mode 1 Output Operation:





Input Output mode of 8255

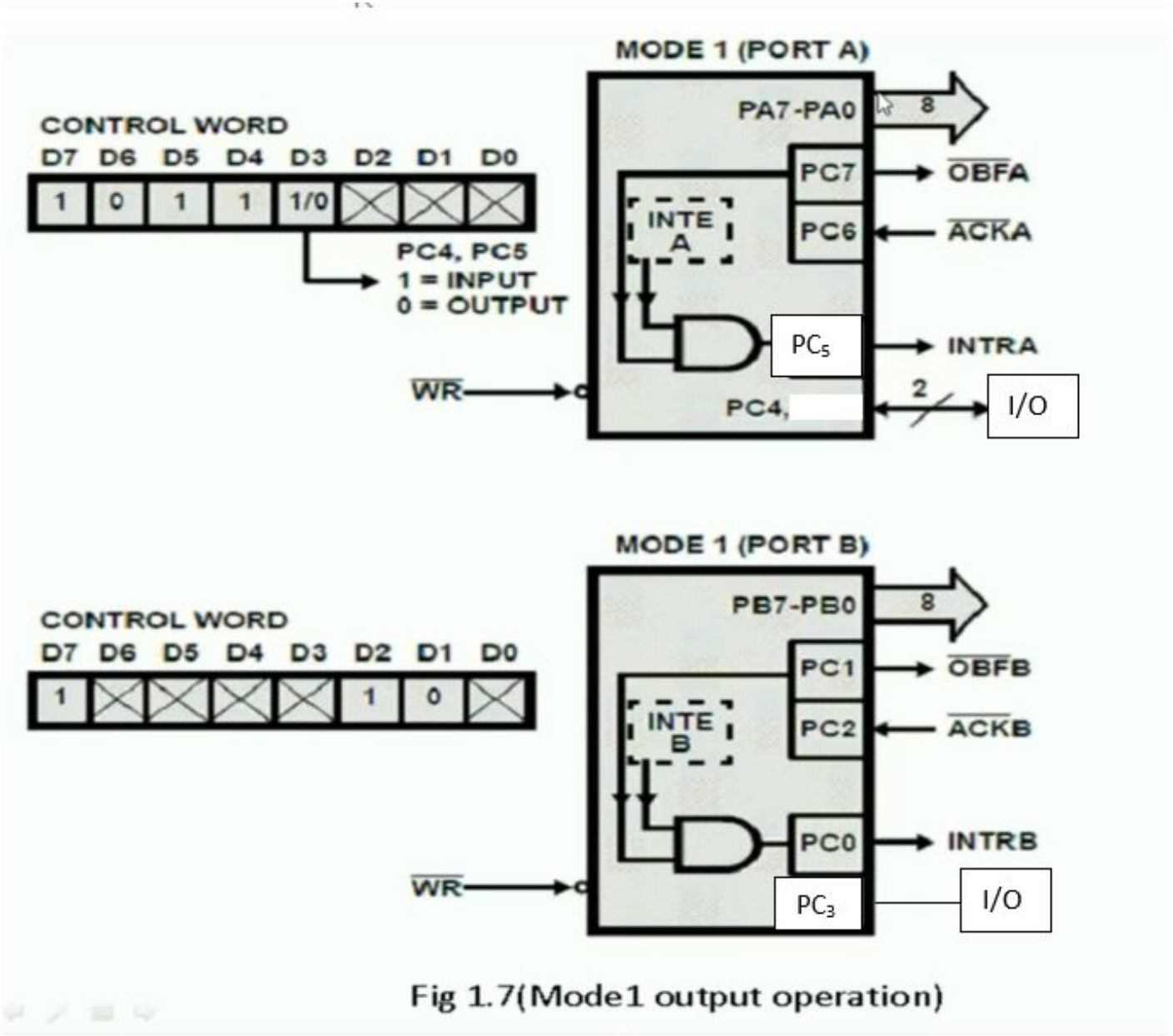


Fig 1.7(Mode1 output operation)

Input Output mode of 8255

Mode 2 (Bidirectional Data Transfer):

1. Port A works as bidirectional port.
2. Port B works in either mode 0 or mode 1.
3. Port A uses five signals of Port C as handshake signals.
4. Remaining three lines can be used as simple i/o or handshake signals for port B.

Input Output mode of 8255

Mode 2 (Bidirectional Data Transfer):