Experiment No : 5.1

Name of the experiment : A/D conversion

Objectives of experiment :

1. To understand converting process of Analog Digital.
2. To understand the method of counter type A/D conversion.

Theory : Analog to digital conversion is the process of transforming the signal from the analog domain to the digital domain. This process could take place at baseband, as it is the case of direct conversion receivers, or at intermediate frequency (IF) or low IF depending on the requirements and consequently on the receiver architecture pursued by the designers. In A/D conversion, there are various hardware architectures in which an analog-to-digital converter (ADC) can be implemented. The main building blocks of ADCs, namely track-and-hold amplifiers and comparators.

Topics such as aperture time acuracy, clock feed through and charge injection and their impact on the signal-to-ration (SNR) arce very important in A/D conversion.

Analog to digital conversion is a multi-step process. Analog-to-digital conversion can be viewed as imposing a grcid on a continuous signal. The signal becomes discrete both in amplitude and time. It is obvious that the grcid must be sufficiently fine and must covere the full extent of the signal to avoid a significant loss of information.

Requiring Equipments:

1. Power supply
2. signal source
3. Pulse code Modulation
4. Digital Storage Oscilloscope
5. Digital Multimeter.

Experiment Procedure:

1. Module and measuring equipment were prepared. All ADJ control terminals were set to MIN repectively and the power was provided to all devices.

2. Frequency selector was set in signal source to 8 [kHz].

3. CLK, RAMP, SINE terminal output of signal source was connected to CLK, RAMP, AUDIO INPUT terminal of PCM 1 module.

4. 32 [kHz] of signal generator was connected from signal source to CLKX4 terminal and 128 [kHz] was connected to CLKX16 terminal of PCM 1 module.

5. Oscilloscope was set as followings:

TIME/DIV	0.25 [ms]
CH-1 VOLT/DIV	5 [v]
CH-2 VOLT/DIV	5 [v]
TRIGGER MODE	AUTO
TRIGGER SOURCE	CH-1
VERTICAL MODE	DUAL
INPUT COUPLING	DC
SLOPE	+

6. CH-1 input probe of oscilloscope was connected to TP1 of PCM 1, the frequency was set to 1 [kHz] by adjusting frequency ADJ control terminal of audio generator and amplitude was set to 8 [V] by adjusting Amplitude ADJ. control terminal

7. CH-1 ~~wa~~ input probe of oscilloscope was connected to TP2 of PCM 1, ramp voltage was set to 9 [V] by adjusting Amplitude ADJ. control terminal in ramp generator.

8. As CH-1, 2 input probe of oscilloscope was connected to TP1 and J1 of PCM module, two wave forms was appeared as Fig. 1.

9. CH-1, 2 was removed ~~and~~ connected to TP1 and J1 terminal of PCM 1 module and J1 & J2 terminal were connected.

10. It was checked whether wave form of oscilloscope as fig. 2 appears on the screen or not, when input probe of oscilloscope CH-1 was connected to TP3 of PCM 1 module. At that time, TIME/DIV of oscilloscope was set to 0.1 [mS].

11. As input probe of oscilloscope CH-1, 2 were connected to SYNC, CLK and PCM OUTPUT terminal of PCM 1 module, wave form of oscilloscope as Fig. 3 was appeared. At that time, TIME/DIV of oscilloscope was set to 50 [μS].

12. As input probe of oscilloscope CH-1,2 were connected to J1 and PCM OUTPUT terminal of PCM 1 module, wave form of oscilloscope as Fig. 4 was appeared. At that time, TIME/DIV was adjusted to 50[MS] for making the size of quantization phase to appear on the oscillo-scope screen with about four pieces.
But PCM direct output signal was appeared with delay as much as one cycle of quantization phase. It would be appeared by delaying with one cycle toward right side in oscilloscope.

13. AUDIO INPUT of PCM 1 module was removed connected to SINE input of SIGNAL SOURCE temporarily and also connection line connecting J1 terminal and J2 terminal ~~temp~~ was removed temporarily.

14. DC VOLTAGE ±5[V] output terminal of POWER SUPPLY was connected to J2 terminal of PCM 1 module.

15. Lighting status of ENCODER DISPLAY Diode was made to equal with Table-1 by adjusting DC VOLTAGE ADJ. control terminal.
At that time, the voltage range of J2 terminal was measured and it was recorded to Table-1.

ENCODE DISPLAY				Voltage Range [V]
D3	D2	D1	D0	
ON	ON	ON	ON	4.21
ON	ON	ON	OFF	3.82
ON	ON	OFF	ON	3.20
ON	ON	OFF	OFF	2.54
ON	OFF	ON	ON	1.87
ON	OFF	ON	OFF	1.21
ON	OFF	OFF	ON	0.49
ON	OFF	OFF	OFF	-0.06
OFF	ON	ON	ON	-0.28
OFF	ON	ON	OFF	-0.73
OFF	ON	OFF	ON	-1.42
OFF	ON	OFF	OFF	-2.08
OFF	OFF	ON	ON	-2.71
OFF	OFF	ON	OFF	-3.39
OFF	OFF	OFF	ON	-4.01
OFF	OFF	OFF	OFF	-4.70

Discussion: In this experiment, the conversion process of counter type A/D converter was discussed. General cause of noise and distorsion within time domain was also discussed. This experiment demonstrate how the number of quantizing interval effects of quantizing noise within time domain.