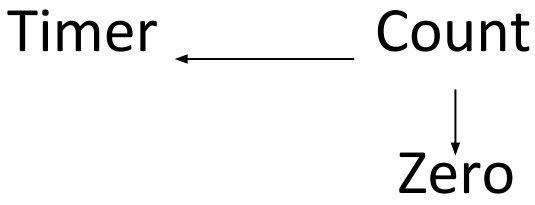
Why Timer is needed?

- Suppose a microprocessor is performing n tasks. In between these n tasks it wants a time delay of fixed T seconds. Now every time this microprocessor wants this time delay, through software we can provide a time delay by writing a subroutine. After completing one task microprocessor is going to execute the subroutine of time delay and come again and execute the 2^{nd} task. Every time the microprocessor has to call the subroutine and execute the subroutine and load the count. In this way, microprocessor is busy for performing those task. Therefore, the solution is using external IC 8253/8254.

Applications of Programmable Interval Timer

- Interrupt a time sharing microprocessor operating system at evenly spaced intervals so that it can switch the program. At first, a count is set to the timer. When the count becomes zero, then it will generate a pulse or interrupt the microprocessor.



- It can be used as a programmable one shot generator. It is used to generate a pulse after a delay of desired period.
- It can be used as a programmable baud rate (bits per second) generator. It can be used to generate high frequency pulse train for setting baud rate in serial communication.

Applications of Programmable Interval Timer

- It measures time delays between external events. It can also be used to measure the time interval between two events.
- It counts the number of times an event has been occurred. It can be used as a counter if external system is generating a pulse every time an event occurs.
- It causes the processor to be interrupted after a programmed number of external events have occurred. Suppose there are n number of tasks, and the processor needs to be interrupted after completing the half of the tasks.
- Complex waveform generator
- Square wave generator
- Minimize the overload on microprocessor

Features of 8253/8254 Programmable Interval Timer

1. The Intel 8253/8254 is a counter/timer device designed to solve the common timing control problems in microcomputer system design.
2. It is used to perform timing and counting operations.
3. It is used to interrupt the microprocessor at certain time intervals.
4. It has three independent 16-bit down counters.
5. These three counters can be programmed for either binary or BCD count.
6. It is compatible with almost all microprocessors.
7. 16 bits count is loaded into its register and on command, it begins to decrement until it reaches to zero. At the end of the count, it generates a pulse that can be used to interrupt the processor.
8. Each timer can be programmed in different modes.
9. It has six different modes- mode 0, mode 1, mode 2, mode 3, mode 4, mode 5 and which modes the timers are operating it is decided by the control word of 8254.

Applications of 8253/8254 Programmable Interval Timer

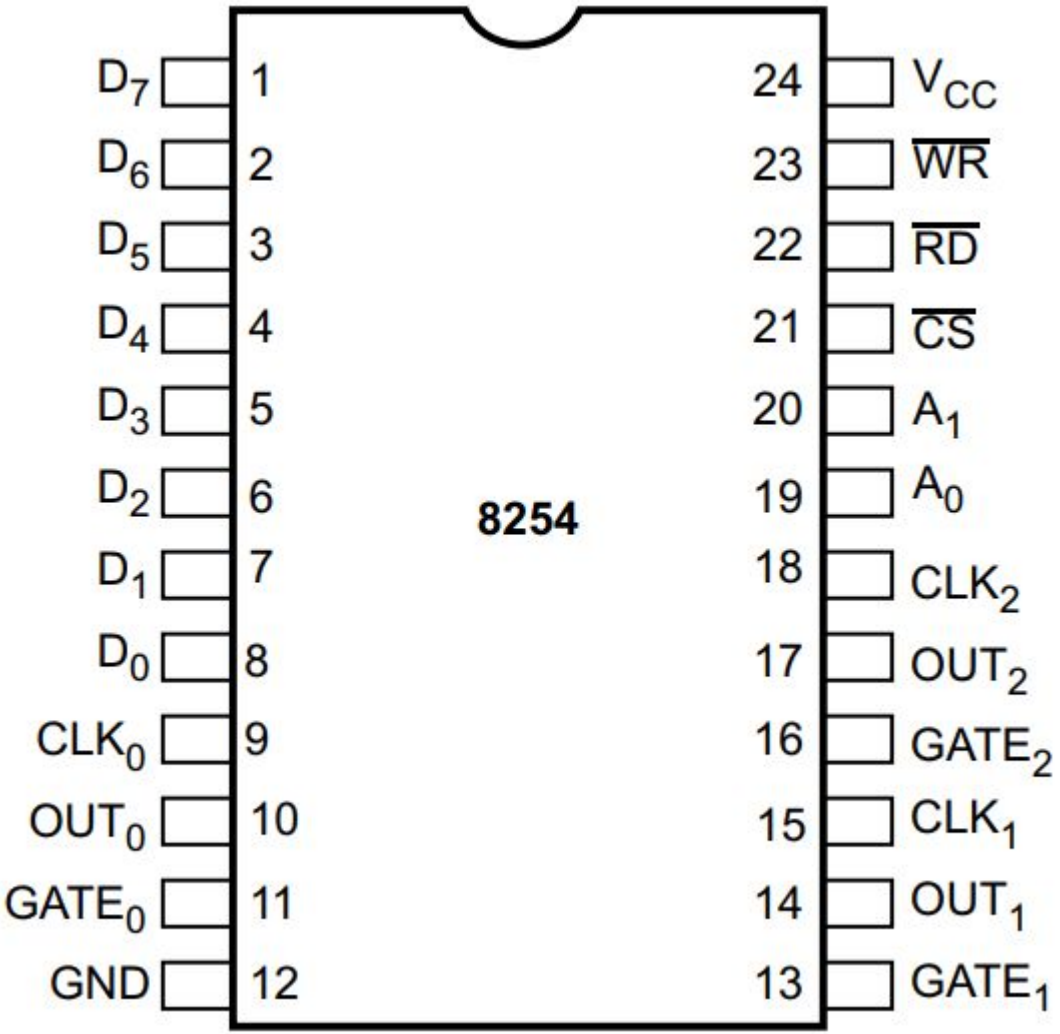
1. Real time clock
2. Event counter
3. Digital one shot
4. Programmable rate generator
5. Square wave generator
6. Complex waveform generator
7. Complex motor controller

Differences Between 8253 and 8254

8253	8254
Its operating frequency is 0 - 2.6 MHz.	Its operating frequency is 0 - 10 MHz.
It uses N-MOS technology.	It uses H-MOS technology.
Read-Back command is not available.	Read-Back command is available.
Reads and writes of the same counter cannot be interleaved.	Reads and writes of the same counter can be interleaved.

- 8254 has a powerful **command** called **READ BACK command**, which allows the user to check the count value, the programmed mode, the current mode, and the current status of the counter.

Pin Diagram of 8254



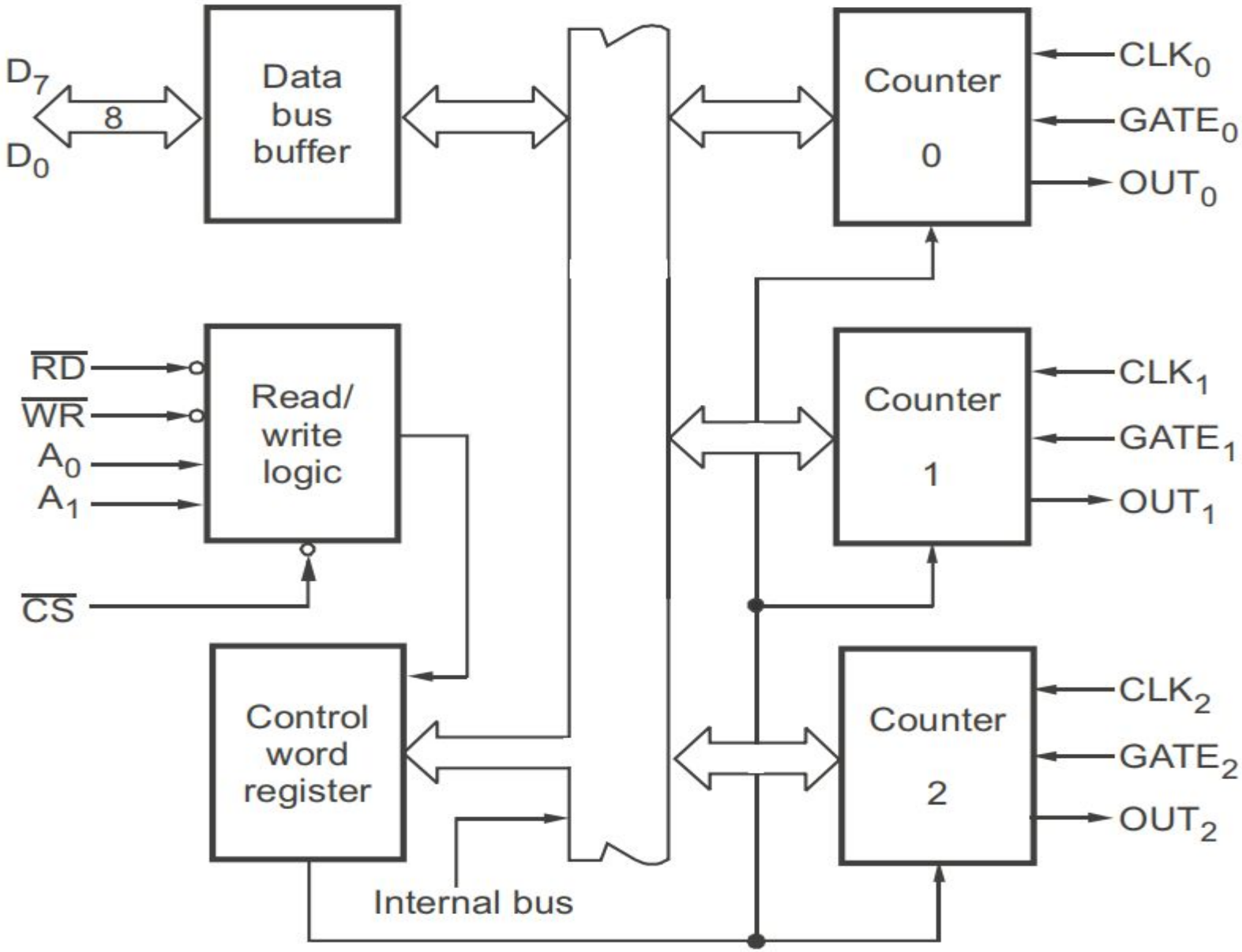
Pin Description of 8254

Symbol	Pin No.	Type	Name and Function
D_7–D_0	1–8	I/O	**DATA:** Bi-directional three state data bus lines, connected to system data bus.
CLK 0	9	I	**CLOCK 0:** Clock input of Counter 0.
OUT 0	10	O	**OUTPUT 0:** Output of Counter 0.
GATE 0	11	I	**GATE 0:** Gate input of Counter 0.
GND	12		**GROUND:** Power supply connection.
V_{CC}	24		**POWER:** +5V power supply connection.
$\overline{WR}$	23	I	**WRITE CONTROL:** This input is low during CPU write operations.
$\overline{RD}$	22	I	**READ CONTROL:** This input is low during CPU read operations.
$\overline{CS}$	21	I	**CHIP SELECT:** A low on this input enables the 8254 to respond to $\overline{RD}$ and $\overline{WR}$ signals. $\overline{RD}$ and $\overline{WR}$ are ignored otherwise.
A_1, A_0	20–19	I	**ADDRESS:** Used to select one of the three Counters or the Control Word Register for read or write operations. Normally connected to the system address bus.

A_1	A_0	Selects
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control Word Register

CLK 2	18	I	**CLOCK 2:** Clock input of Counter 2.
OUT 2	17	O	**OUT 2:** Output of Counter 2.
GATE 2	16	I	**GATE 2:** Gate input of Counter 2.
CLK 1	15	I	**CLOCK 1:** Clock input of Counter 1.
GATE 1	14	I	**GATE 1:** Gate input of Counter 1.
OUT 1	13	O	**OUT 1:** Output of Counter 1.

Block Diagram of 8254



Functional Description of 8254

- **Data Bus Buffer**

  This tri-state, bi-directional, 8-bit buffer is used to interface the 8254 to the system data bus.

- **Read/ Write logic**

The Read/Write Logic accepts inputs from the system bus and generates control signals for the other functional blocks of the 8254. A1 and A0 select one of the three counters or the Control Word Register to be read from/written into. A ‘‘low’’ on the RD input tells the 8254 that the CPU is reading one of the counters. A ‘‘low’’ on the WR input tells the 8254 that the CPU is writing either a Control Word or an initial count. Both RD and WR are qualified by CS; RD and WR are ignored unless the 8254 has been selected by holding CS low.

A_1	A_0	Selection
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control word Register

Functional Description of 8254

❖ **Control Word Register**

This register is accessed when lines A0 and A1 both are at logic 1. If the CPU then does a write operation to the 8254, the data is stored in the Control Word Register and is interpreted as a Control Word used to define the operation of the Counters. It is used to write a command word which specifies the counter to be used (binary or BCD), its mode, and either a read or write operation.

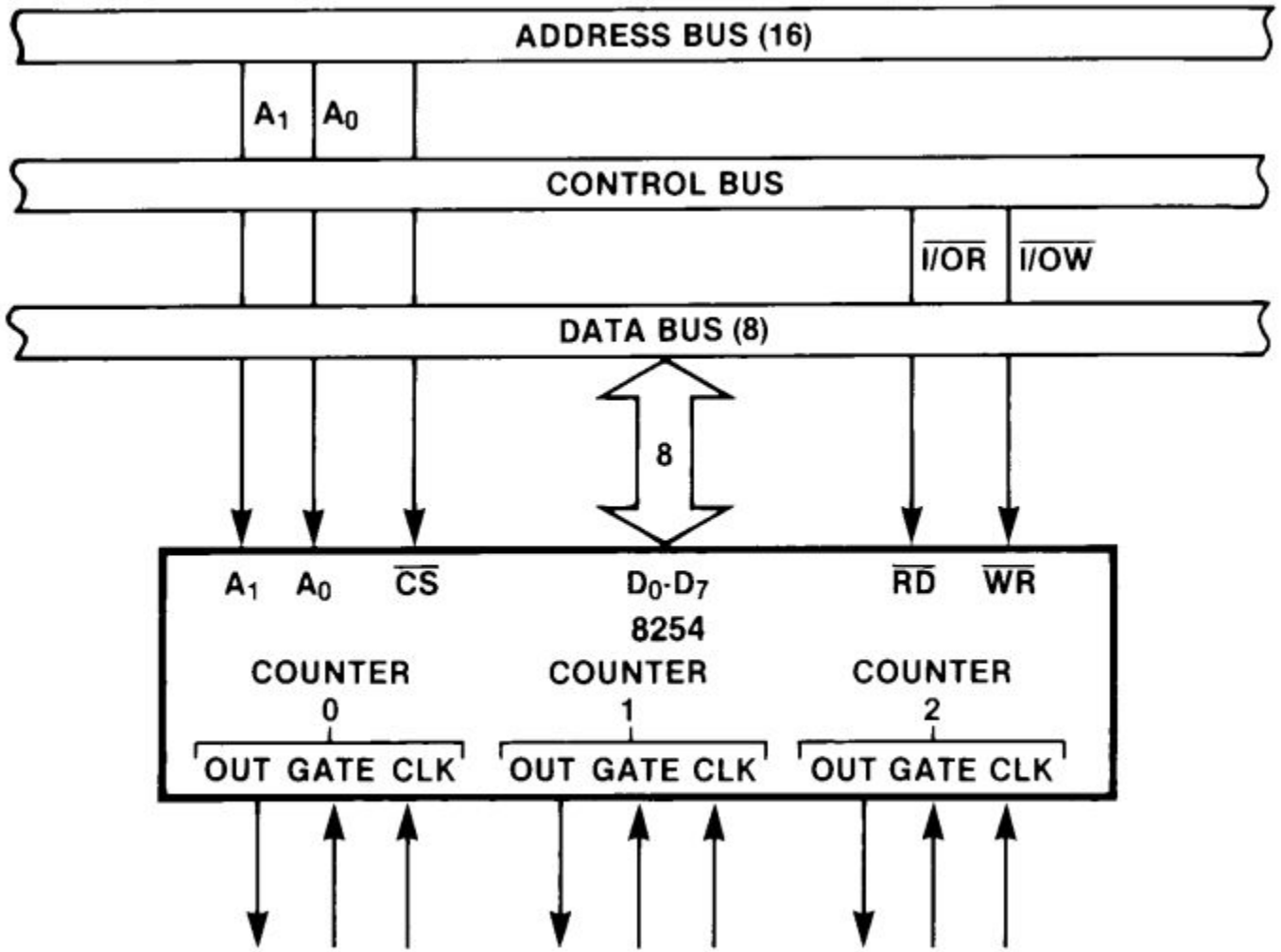
$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0	
0	1	0	0	0	Write into Counter 0
0	1	0	0	1	Write into Counter 1
0	1	0	1	0	Write into Counter 2
0	1	0	1	1	Write Control Word
0	0	1	0	0	Read from Counter 0
0	0	1	0	1	Read from Counter 1
0	0	1	1	0	Read from Counter 2
0	0	1	1	1	No-Operation (3-State)
1	X	X	X	X	No-Operation (3-State)
0	1	1	X	X	No-Operation (3-State)

Functional Description of 8254

- **Counters**

1. These three functional blocks are identical in operation.
2. Each counter consists of a single, 16 bit, pre-settable, down counter.
3. The counter can operate in either binary or BCD and its input, gate and output are configured by the selection of modes stored in the control word register.
4. The counters are fully independent.
5. The programmer can read the contents of any of the three counters without disturbing the actual count in process.

8254 system interface with 8086 microprocessor



Operational Description of 8254

After power-up, the state of the 8254 is undefined. The Mode, count value, and output of all Counters are undefined. How each Counter operates is determined when it is programmed. Each Counter must be programmed before it can be used. Unused counters need not be programmed.

Programming the 8254

Counters are programmed by writing a Control Word and then an initial count. The Control Words are written into the Control Word Register, which is selected when A1,A0 = 11. The Control Word itself specifies which Counter is being programmed.

❖ Write Operations

1. For each Counter, the Control Word must be written before the initial count is written.
2. The initial count must follow the count format specified in the Control Word (least significant byte only, most significant byte only, or least significant byte and then most significant byte).
3. If a Counter is programmed to read/write two-byte counts, the following precaution applies: A program must not transfer control between writing the first and second byte to another routine which also writes into that same Counter. Otherwise, the Counter will be loaded with an incorrect count.

Operational Description of 8254

- Initial counts are written into the Counters, not the Control Word Register. The A_1,A_0 inputs are used to select the Counter to be written into. The format of the initial count is determined by the Control Word used.

Control Word Format

A_1,A_0 = 11 $\overline{CS}$ = 0 $\overline{RD}$ = 1 $\overline{WR}$ = 0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC—Select Counter

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-Back Command (see Read Operations)

M—Mode

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

RW—Read/Write

RW1	RW0	
0	0	Counter Latch Command (see Read Operations)
0	1	Read/Write least significant byte only
1	0	Read/Write most significant byte only
1	1	Read/Write least significant byte first, then most significant byte

BCD

0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

NOTE:
Don't care bits (X) should be 0 to insure compatibility with future Intel products.

Operational description of 8254 Timer

❖ Modes of operation of 8254

1. It has 3 independent 16-bit counters which can be programmed to anyone of the six possible modes.
2. Each counter has a clock and gate input and counter output.
3. To operate a counter, count value has to be loaded in the count register, gate should be tied high, clock input should be applied through the clock.
4. The counter will decrement the count value by 1 for each cycle of clock signal.
5. Finally, generate output based on the modes of operation.

Operational description of 8254 Timer

❖ Modes of operation of 8254

1. Mode 0 – Interrupt on terminal count
2. Mode 1 – Hardware triggerable one shot
3. Mode 2 – Rate Generator
4. Mode 3 – Square wave mode
5. Mode 4 – Software triggered strobe
6. Mode 5 – Hardware triggered strobe

The initialization procedure for each mode is almost same, but the output of each mode will be different. To initialize a counter, the following steps are necessary:

1. Write a control word into the control register.
2. Write count value in the count register.

Operational description of 8254 Timer

The writing of count value depends on the control word and can be written in three ways:

1. If the control word is framed for writing LSB only then write LSB alone.
2. If the control word is framed for writing MSB only then write MSB alone.
3. If the control word is framed for writing LSB first then MSB then writing LSB first and then MSB.

In all operating modes, gate signal acts as a control signal to start, stop or maintain the counting process.

Operational description of 8254 Timer

Mode 0: Interrupt on terminal count

1. Mode 0 is typically used for event counting. After the control word is written, OUT is initially low, and remain low until the counter reaches zero. OUT then goes high and remains high until a new count or a new mode 0 control word is written into the counter.

2. GATE = 1 enables counting and GATE = 0 disables counting.

3. After the control word and initial count are written into the counter, the initial count will be loaded on the next clock pulse.

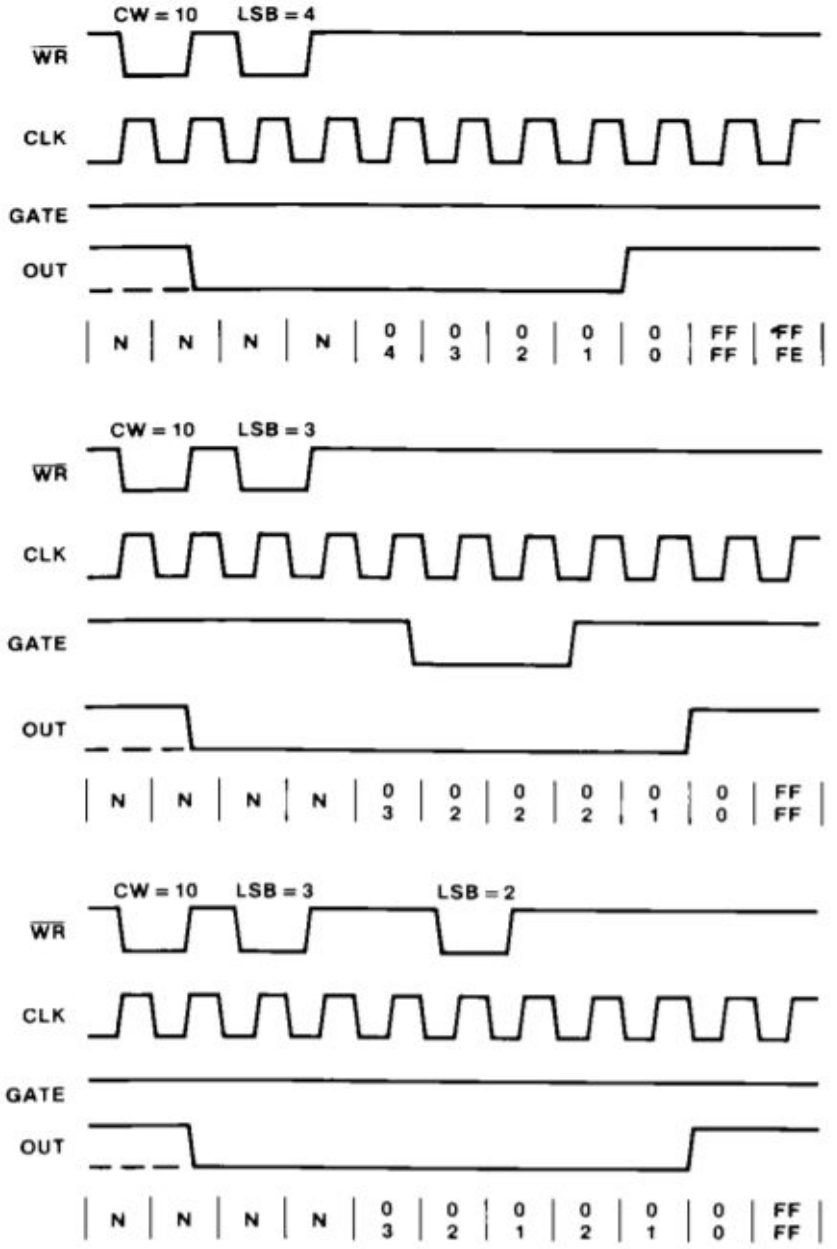
4. Therefore, in the first clock pulse after WR goes high, the 8254 loads the count value in the counter register and after each subsequent clock pulse, the count value is decremented by one. When count value becomes zero, the OUT asserted high.

5. If an initial count is written while GATE = 0, it will still be loaded on the next CLK pulse. When GATE goes high, OUT will go high N CLK pulses later; no CLK pulse is needed to load the Counter as this has already been done.

6. If a new count is written to the Counter, it will be loaded on the next CLK pulse and counting will continue from the new count.

Operational description of 8254 Timer

Timing diagram of Mode 0:



Operational description of 8254 Timer

Mode 1: Hardware Retriggerable One-Shot

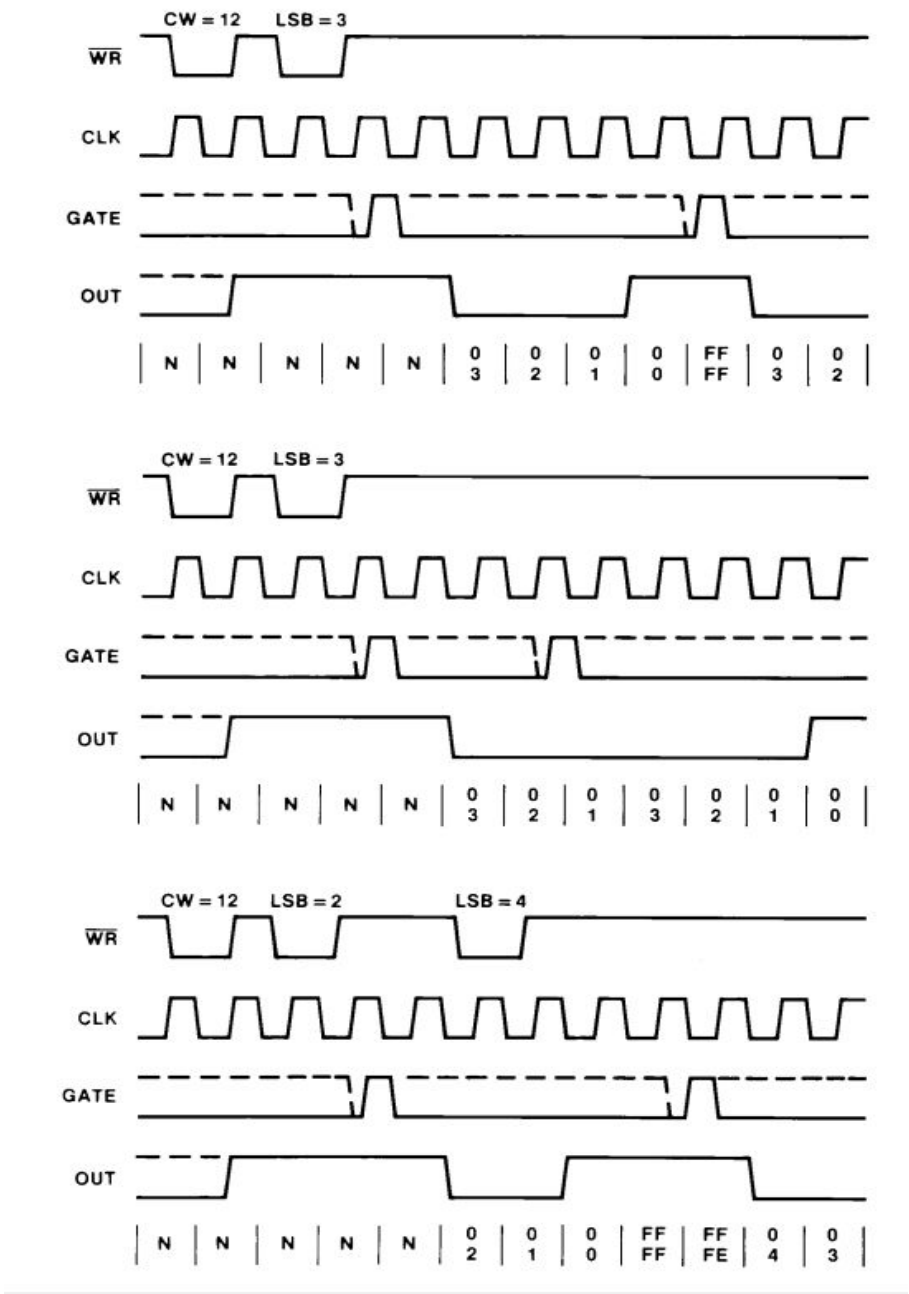
1. OUT will be initially high. OUT will go low on the CLK pulse following a trigger to begin the one-shot pulse, and will remain low until the Counter reaches zero. OUT will then go high and remain high until the CLK pulse after the next trigger.

2. The one-shot is retriggerable, hence OUT will remain low for N CLK pulses after any trigger. The one-shot pulse can be repeated without rewriting the same count into the counter. GATE has no effect on OUT.

3. If a new count is written to the Counter during a one shot pulse, the current one-shot is not affected unless the counter is retriggered. In that case, the Counter is loaded with the new count and the one shot pulse continues until the new count expires.

Operational description of 8254 Timer

Timing diagram of Mode 1:



Operational description of 8254 Timer

Mode 2: Rate Generator

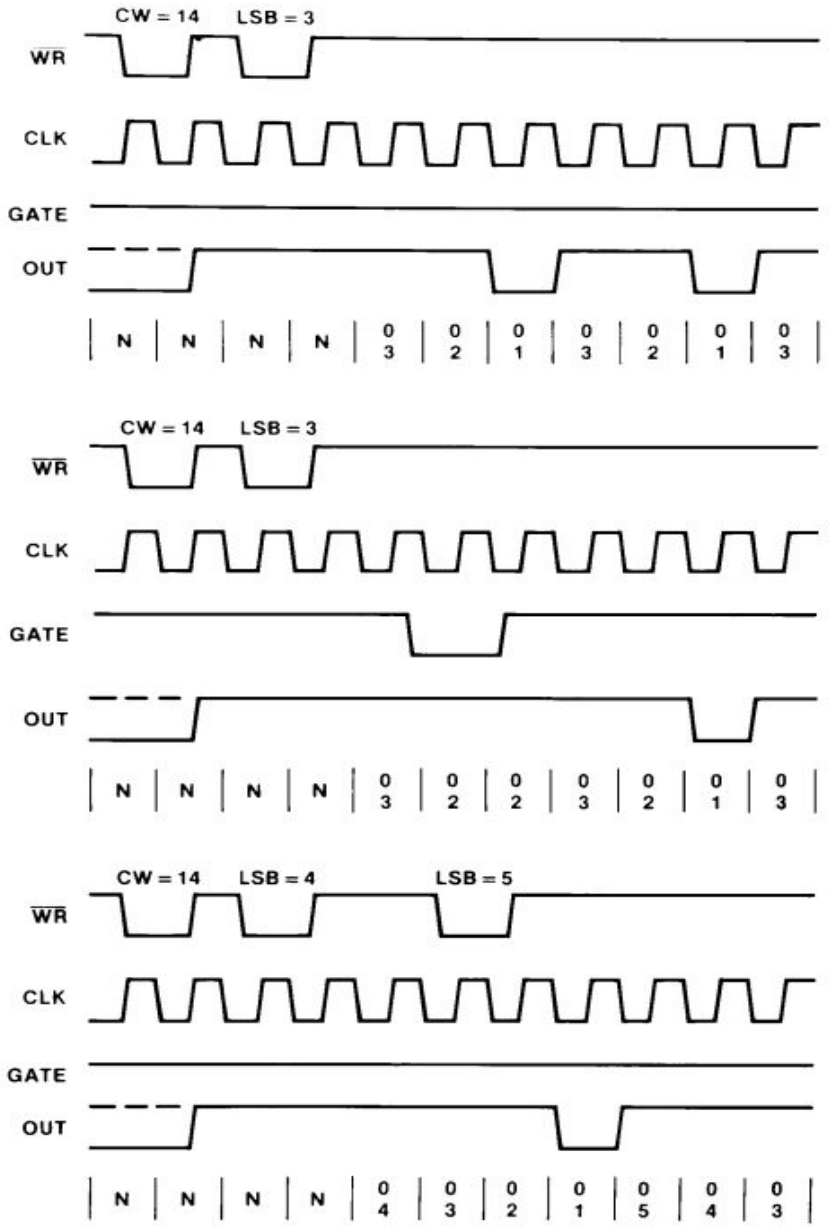
1. This Mode functions like a divide-by-N counter. It is typically used to generate a Real Time Clock interrupt. OUT will initially be high. When the initial count has decremented to 1, OUT goes low for one CLK pulse. OUT then goes high again, the Counter reloads the initial count and the process is repeated. Mode 2 is periodic; the same sequence is repeated indefinitely. For an initial count of N, the sequence repeats every N CLK cycles.

2. GATE e 1 enables counting; GATE e 0 disables counting. If GATE goes low during an output pulse, OUT is set high immediately. A trigger reloads the Counter with the initial count on the next CLK pulse; OUT goes low N CLK pulses after the trigger. Thus the GATE input can be used to synchronize the Counter.

3. Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current period, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current counting cycle.

Operational description of 8254 Timer

Timing diagram of mode 2:



Operational description of 8254 Timer

Mode 3: Square Wave Mode

1. Mode 3 is typically used for Baud rate generation.

2. Mode 3 is similar to Mode 2 except for the duty cycle of OUT. OUT will initially be high. When half the initial count has expired, OUT goes low for the remainder of the count. Mode 3 is periodic; the sequence above is repeated indefinitely. An initial count of N results in a square wave with a period of N CLK cycles.

3. GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low while OUT is low, OUT is set high immediately; no CLK pulse is required. A trigger reloads the Counter with the initial count on the next CLK pulse. Thus the GATE input can be used to synchronize the Counter.

4. After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This allows the Counter to be synchronized by software also.

5. Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current half-cycle of the square wave, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current half-cycle.

Operational description of 8254 Timer

Mode 3: Square Wave Mode

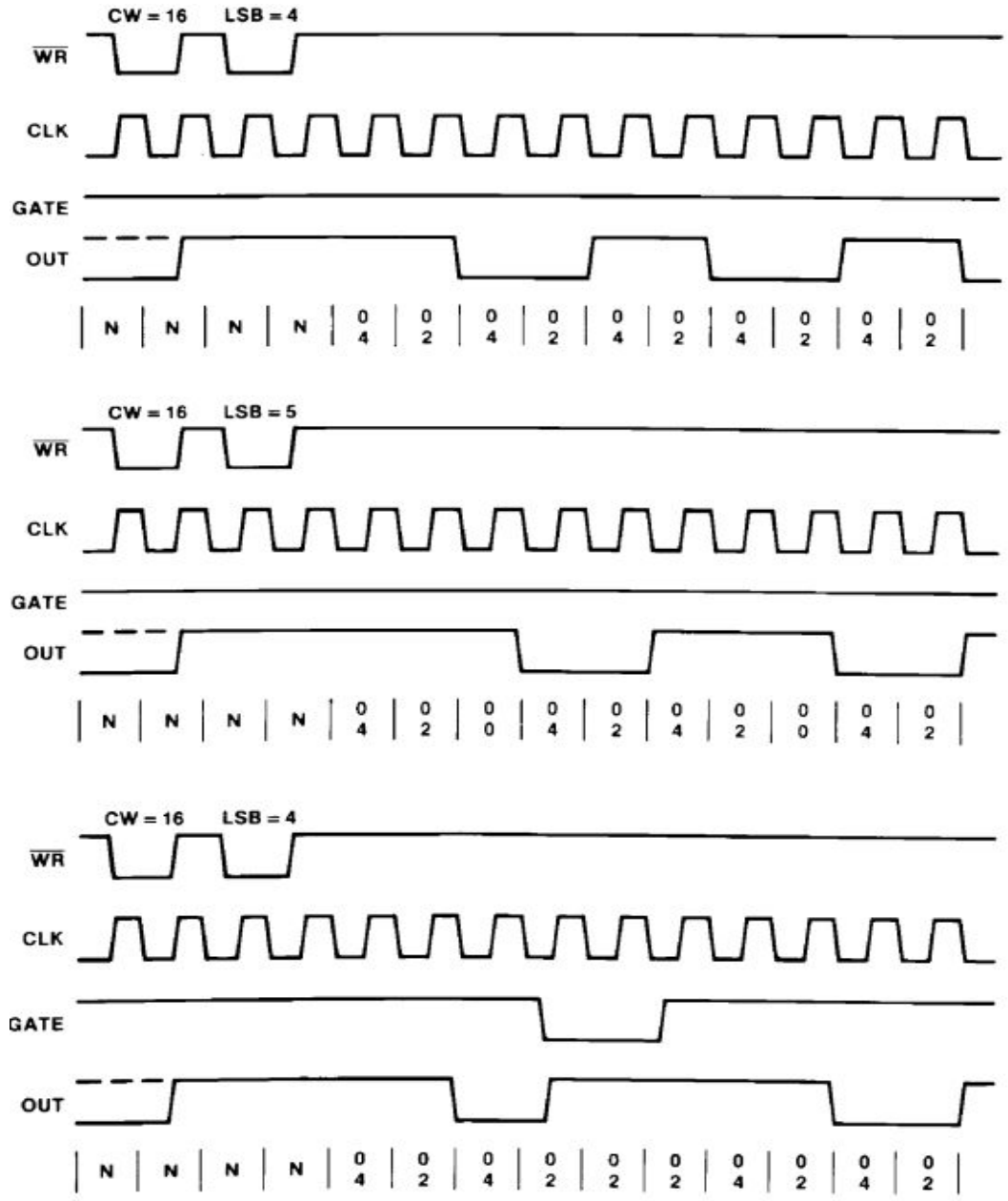
Mode 3 is implemented as follows:

1. Even counts: OUT is initially high. The initial count is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. When the count expires OUT changes value and the Counter is reloaded with the initial count. The above process is repeated indefinitely.

2. Odd counts: OUT is initially high. The initial count minus one (an even number) is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. One CLK pulse after the count expires, OUT goes low and the Counter is reloaded with the initial count minus one. Succeeding CLK pulses decrement the count by two. When the count expires, OUT goes high again and the Counter is reloaded with the initial count minus one. The above process is repeated indefinitely. So for odd counts, OUT will be high for (N + 1)/2 counts and low for (N - 1)/2 counts.

Operational description of 8254 Timer

Timing diagram of mode 3:



Operational description of 8254 Timer

Mode 4: Software triggered strobe

1. OUT will be initially high. When the initial count expires, OUT will go low for one CLK pulse and then go high again. The counting sequence is ‘‘triggered’’ by writing the initial count.

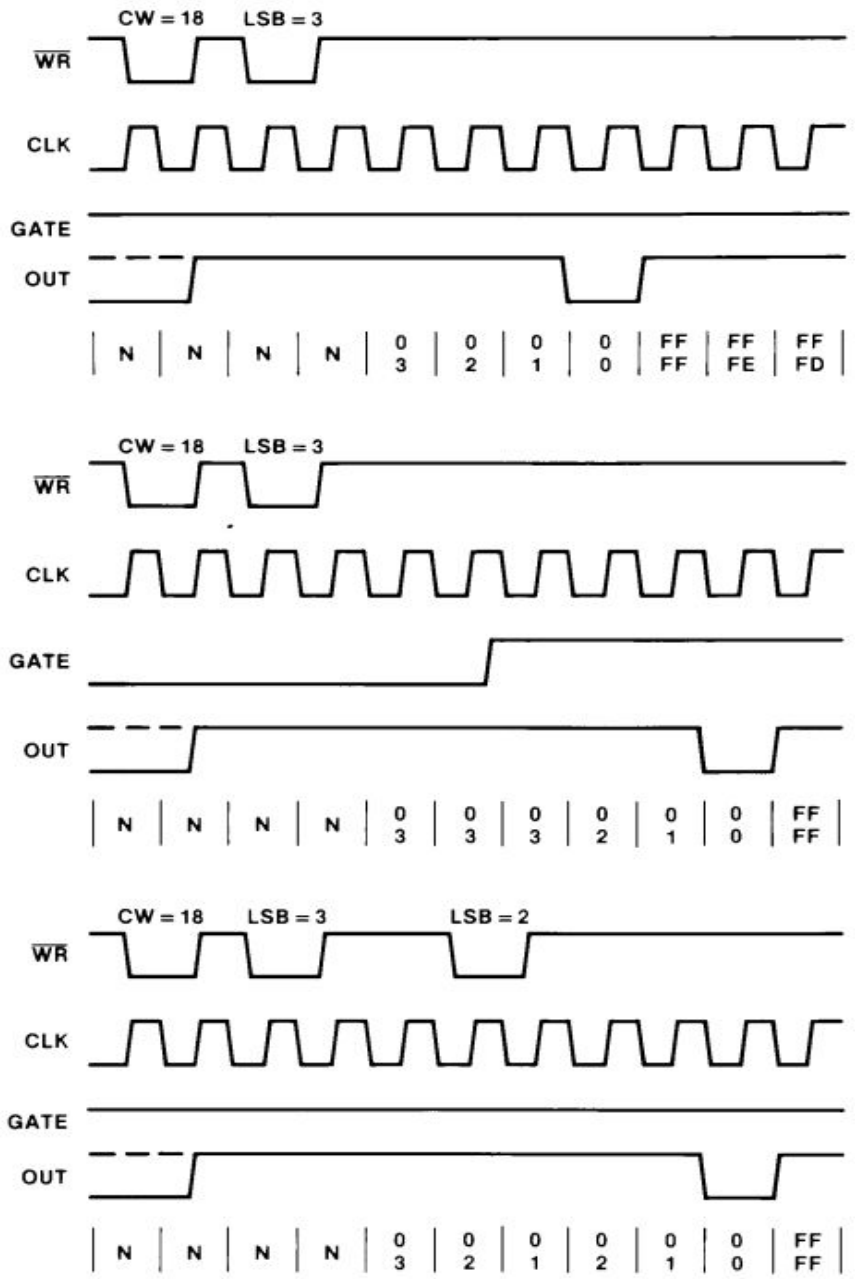
2. GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

3. After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N + 1 CLK pulses after the initial count is written.

4. If a new count is written during counting, it will be loaded on the next CLK pulse and counting will continue from the new count.

Operational description of 8254 Timer

Timing diagram of mode 4:



Operational description of 8254 Timer

Mode 5: Hardware triggered strobe

1. OUT will initially be high. Counting is triggered by a rising edge of GATE. When the initial count has expired, OUT will go low for one CLK pulse and then go high again.

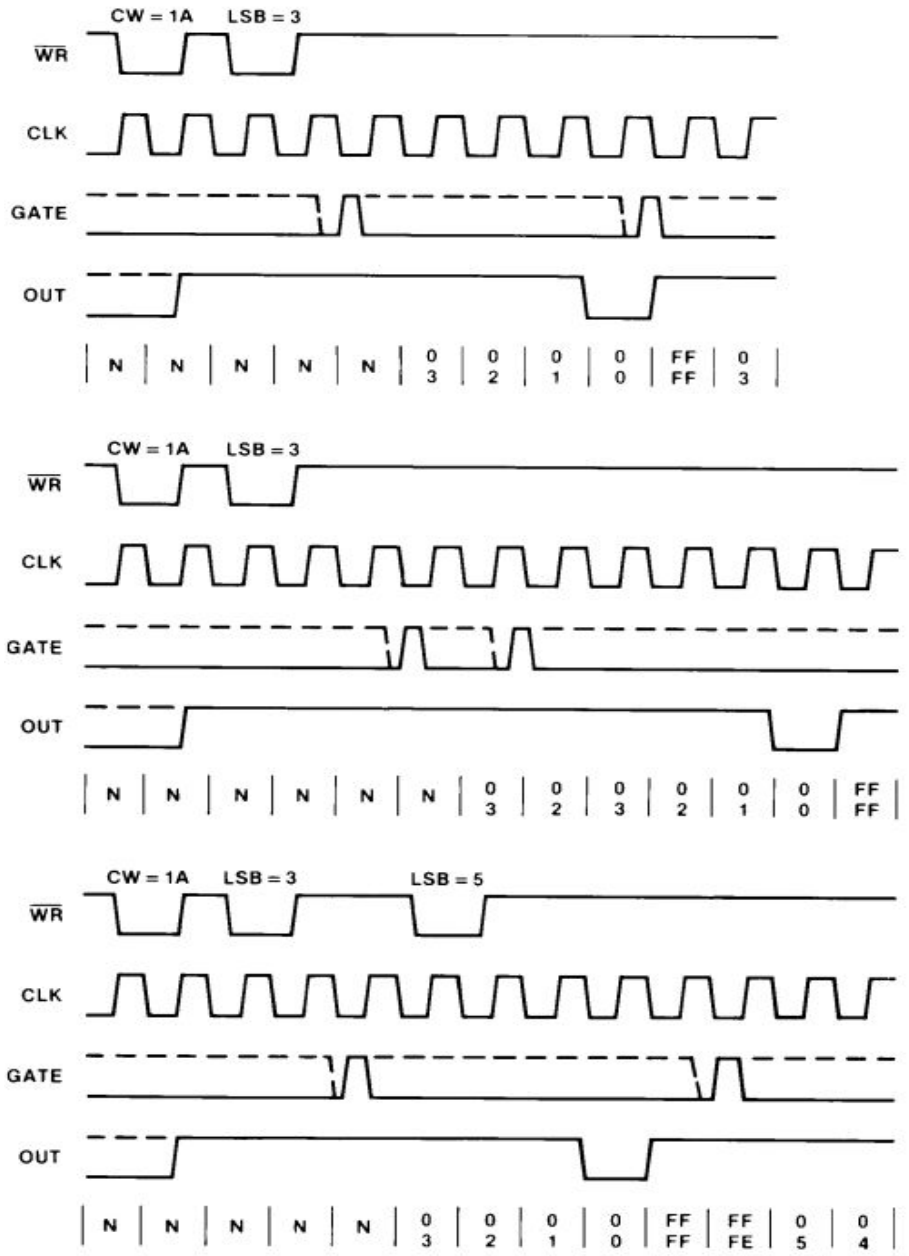
2. After writing the Control Word and initial count, the counter will not be loaded until the CLK pulse after a trigger. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N = 1 CLK pulses after a trigger.

3. A trigger results in the Counter being loaded with the initial count on the next CLK pulse. The counting sequence is retriggerable. OUT will not strobe low for N = 1 CLK pulses after any trigger.

4. If a new count is written during counting, the current counting sequence will not be affected. If a trigger occurs after the new count is written but before the current count expires, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from there.

Operational description of 8254 Timer

Timing diagram of mode 5:



Operational Description of 8254

❖ **Read Operations of 8254**

It is often desirable to read the value of a Counter without disturbing the count in progress. This is easily done in the 8254.

There are three possible methods for reading the counters:

- **Simple read operation:** To read the Counter, which is selected with the A1, A0 inputs, the CLK input of the selected Counter must be inhibited by using either the GATE input or external logic. Otherwise, the count may be in the process of changing when it is read, giving an undefined result.
- **Counter Latch Command.**
- **Read-Back Command.**

Operational Description of 8254

- **Counter Latch Command:**

1. The second method uses the ‘‘Counter Latch Command’’. Like a Control Word, this command is written to the Control Word Register, which is selected when A1,A0 = 11. Also like a Control Word, the SC0, SC1 bits select one of the three Counters, but two other bits, D5 and D4, distinguish this command from a Control Word.

2. The selected Counter’s output latch (OL) latches the count at the time the Counter Latch Command is received. This count is held in the latch until it is read by the CPU (or until the Counter is reprogrammed). The count is then unlatched automatically and the OL returns to ‘‘following’’ the counting element (CE). This allows reading the contents of the Counters ‘‘on the fly’’ without affecting counting in progress.

3. If a Counter is latched and then, some time later, latched again before the count is read, the second Counter Latch Command is ignored. The count read will be the count at the time the first Counter Latch Command was issued.

$A_1,A_0 = 11; CS = 0; RD = 1; WR = 0$

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	0	0	X	X	X	X

SC1,SC0—specify counter to be latched

SC1	SC0	Counter
0	0	0
0	1	1
1	0	2
1	1	Read-Back Command

D5,D4—00 designates Counter Latch Command

X—don’t care

NOTE:
Don’t care bits (X) should be 0 to insure compatibility with future Intel products.

Figure 9. Counter Latching Command Format

Operational Description of 8254

- **Read Back Command:**

1. This command allows the user to check the count value, programmed Mode, and current status of the OUT pin and Null count flag of the selected counter(s).

2. The Read-Back command may be used to latch multiple counter output latches by setting the COUNT bit D5 = 0 and selecting the desired counter (s). Each counter's latch count in held until it is read (or the counter is reprogrammed). That counter is automatically unlatched when read.

3. The following figure shows the format of the control word register for Read-Back command.

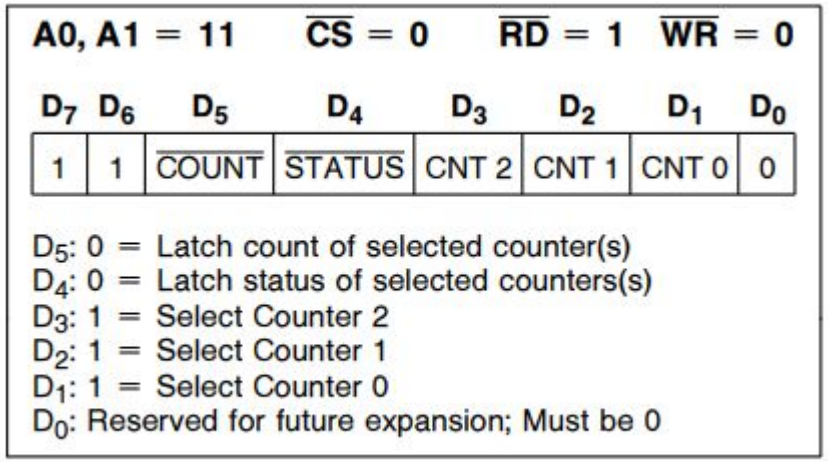


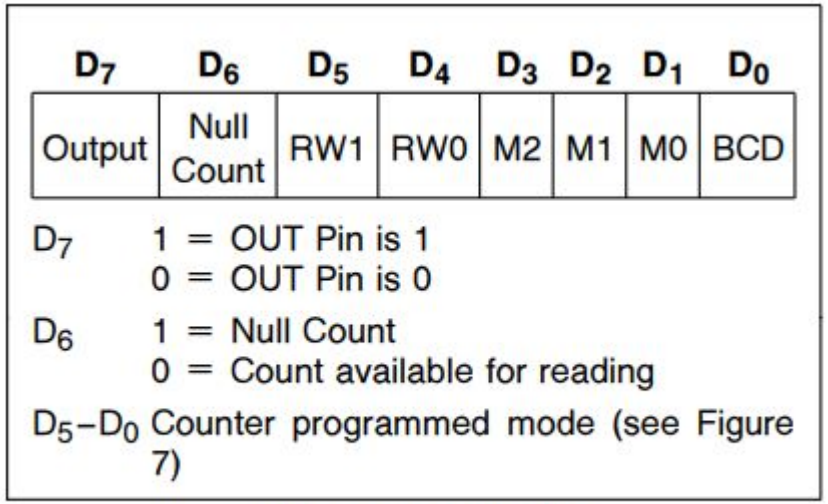
Figure 10. Read-Back Command Format

Operational Description of 8254

3. Read Back Command:

1. The Read-Back command may also be used to latch status information of selected counter(s) by setting STATUS bit D4 = 0. The contents of the counter must be latched before reading. The status of a counter is then accessed by a read from that counter.

2. Bit D5 - D0 contains the counter's programmed mode exactly as written in the last mode control word. Bit D7 contains the current status of the output. The Bit D6 indicates whether the counting element has count or not. If D6 = 0 count is available for reading.



D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Output	Null Count	RW1	RW0	M2	M1	M0	BCD

D_7 1 = OUT Pin is 1
0 = OUT Pin is 0

D_6 1 = Null Count
0 = Count available for reading

D_5–D_0 Counter programmed mode (see Figure 7)

Figure 11. Status Byte