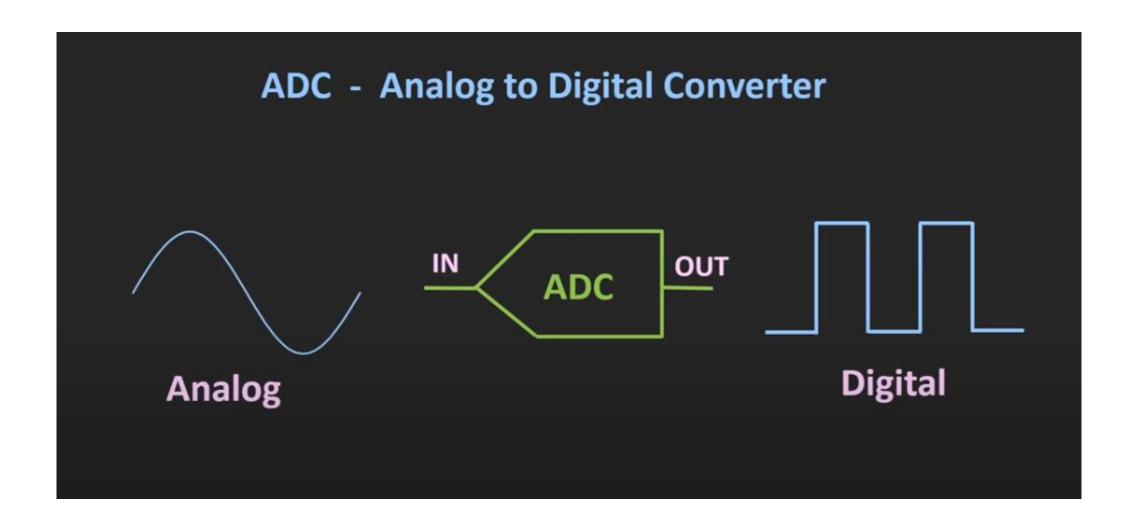
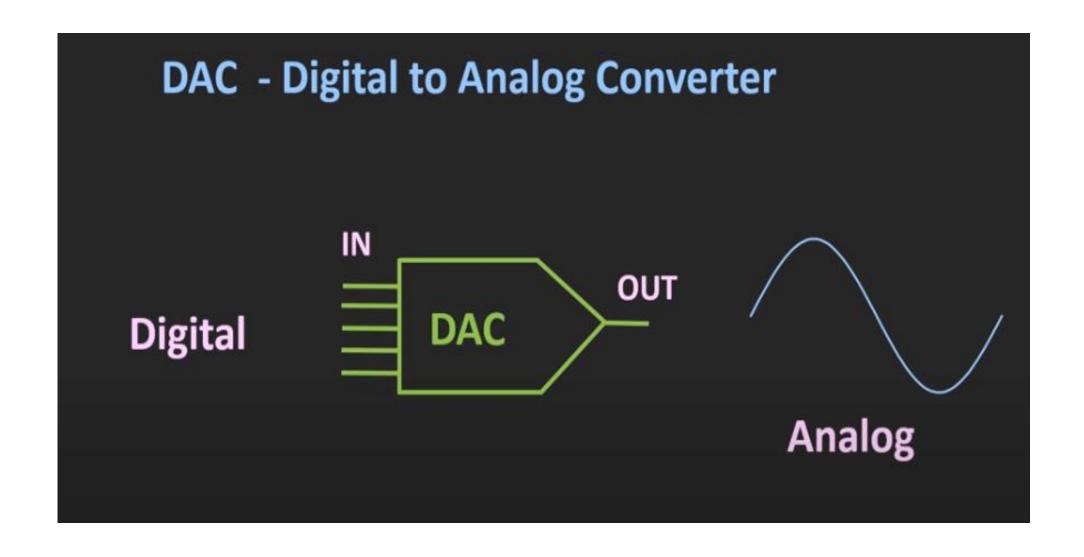
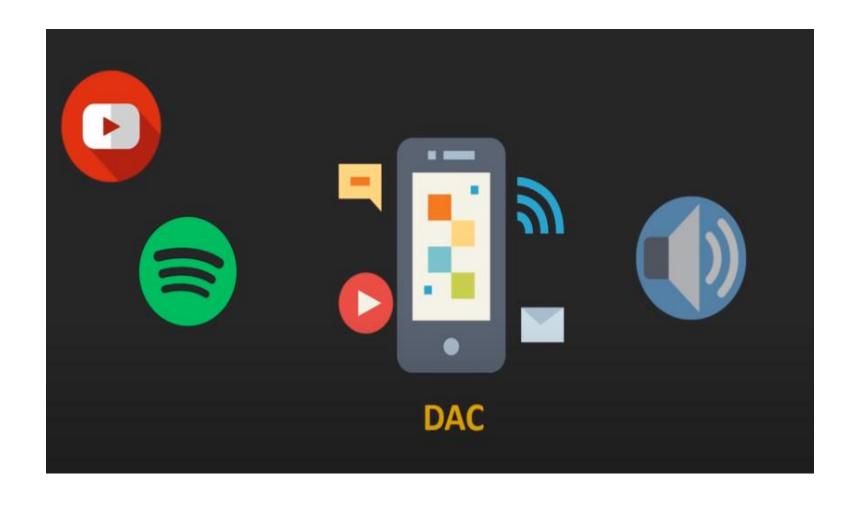
Introduction to ADC and DAC



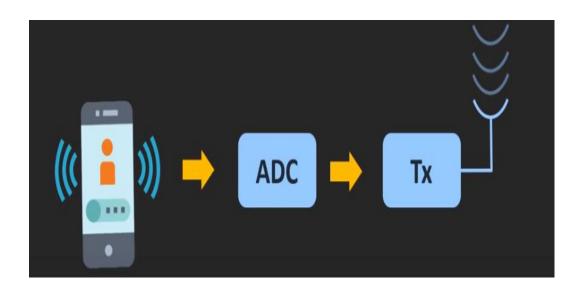
Introduction to ADC and DAC

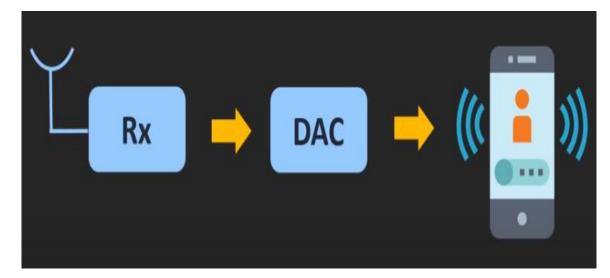


Uses of ADC & DAC



Uses of ADC and DAC





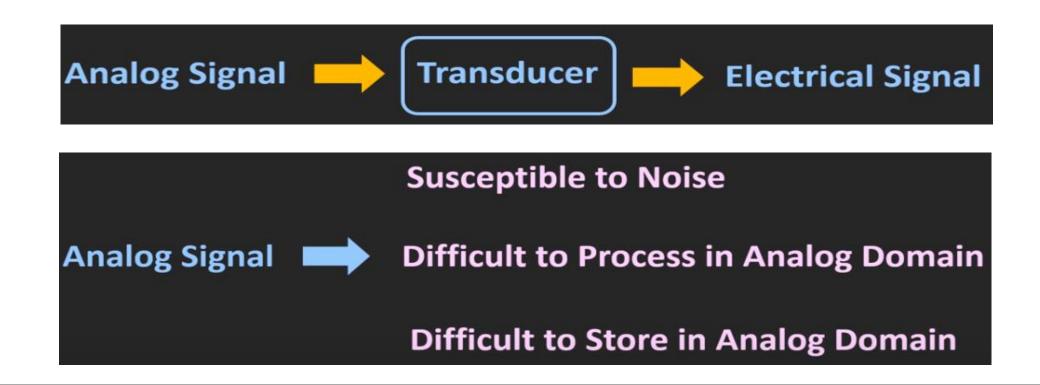
Sender site Receiver site

- 1. In sender site, while talking microphone converts our voice into the electrical signal, using this ADC this signal is digitized and transforms into the form of radio waves.
- 2. In receiver site, the received digital signal is converted into analog through the DAC and using this microphone we are able to hear it.

Why we use ADC and DAC

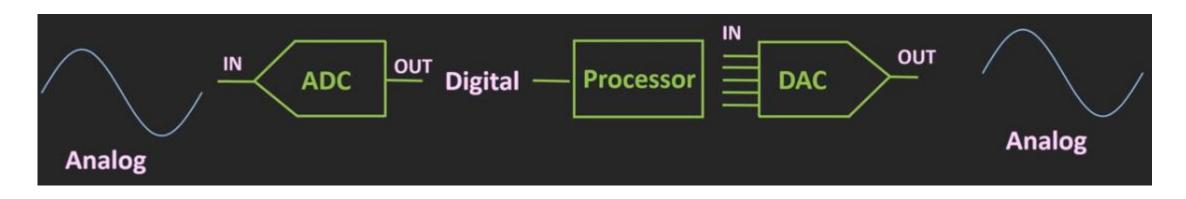
Analog signal

- Temperature
- Pressure
- Velocity
- Sound



Why we use ADC and DAC





Lossy Conversion

Introduction to ADC and DAC

Types of DAC

- 1. Binary weighted resistor DAC
- 2. R-2R Ladder type DAC

Types of ADC

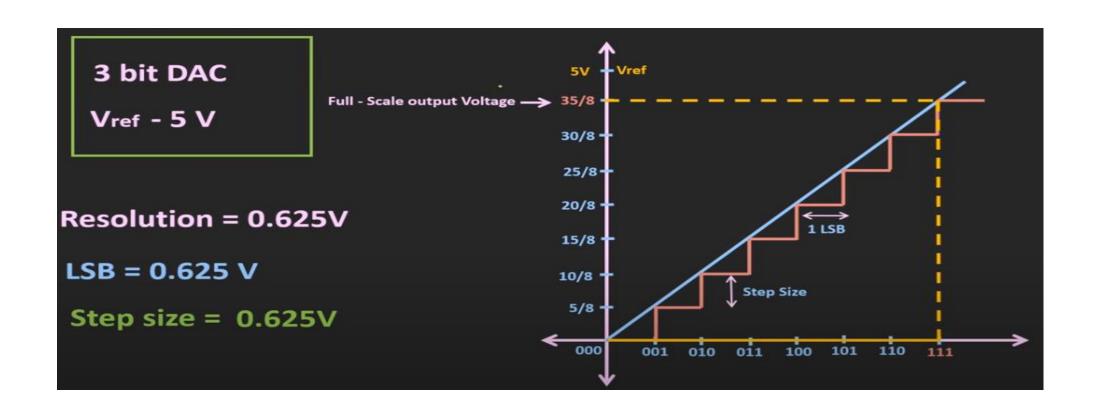
- 1. Counter type ADC/Digital Ramp ADC
- 2. Successive Approximation type ADC
- 3. Flash ADC

Digital to Analog Converter

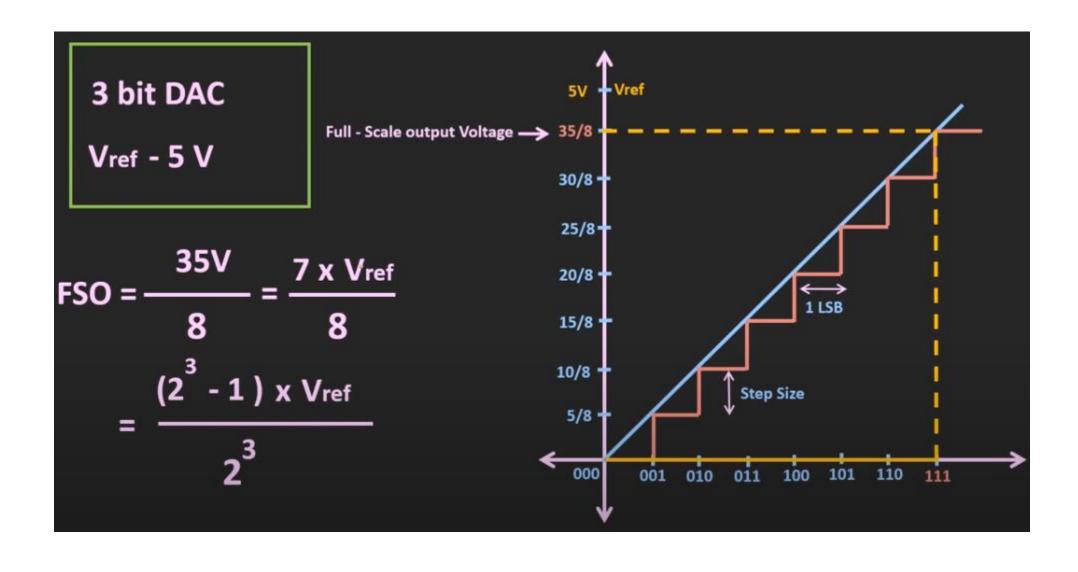
Suppose, there is 3-bit DAC, and it's reference voltage = 5v.

Resolution =
$$\frac{V_{ref*K}}{2^n} = \frac{5}{2^3} = 0.625v$$

Here, k is the multiplying factor of DAC and assume that for this 3 bit DAC k = 1.



Digital to Analog Converter



Digital to Analog Converter

$$FSO = \frac{(2^n - 1) * V_{ref}}{2^n}$$

$$Step \ size = \frac{V_{ref}}{2^n}$$

$$FSO = (2^n - 1) * Step size$$

$$Step \ size = \frac{FSO}{2^n - 1}$$

$$Resolution = LSB = step \ size = \frac{V_{ref}}{2^n}$$

$$FSO = V_{ref} - 1LSB$$

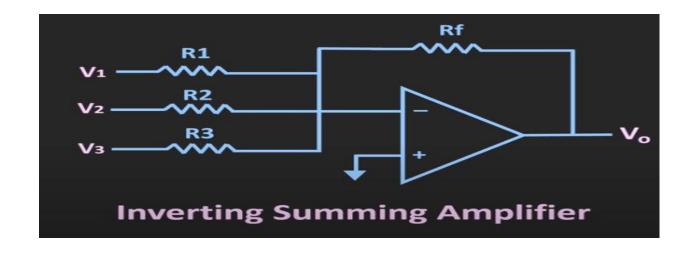
Let,

R1 = R

R2 = R

R3 = R

Rf = R



$$V_0 = -\left[\frac{R_f}{R_1} * V_1 + \frac{R_f}{R_2} * V_2 + \frac{R_f}{R_3} * V_3\right]$$

$$V_0 = -[V_1 + V_2 + V_3]$$

Here, the minus sign indicates that the output voltage will be the 180 degree phase of the input voltage.

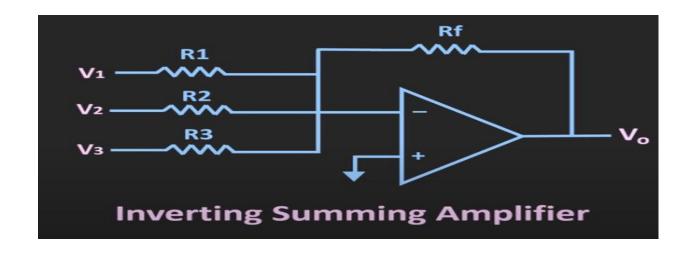
Let,

R1 = R

R2 = 2R

R3 = 3R

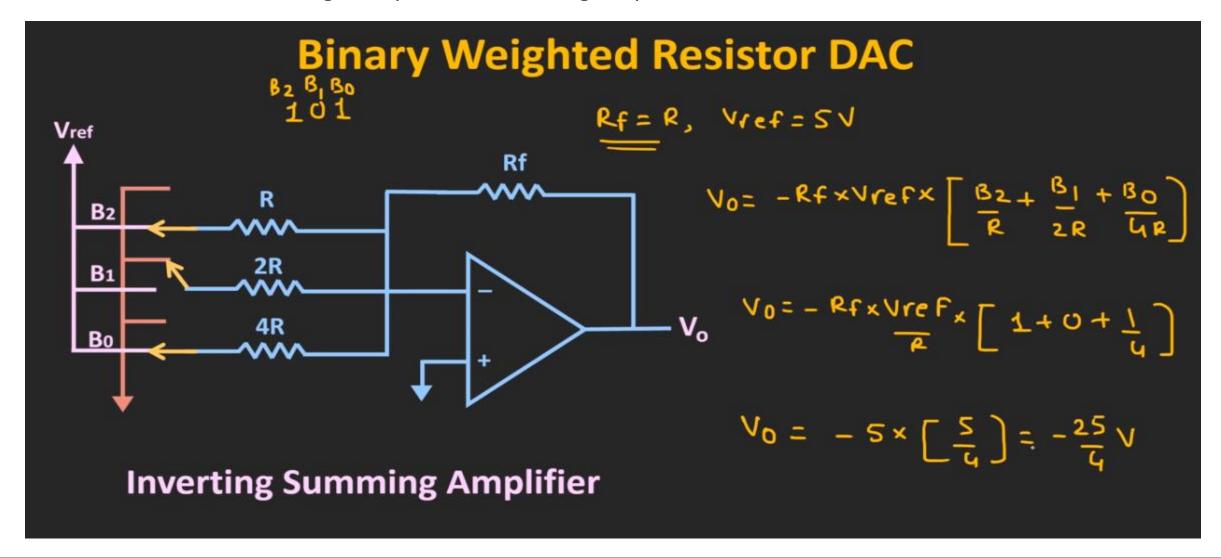
Rf = R

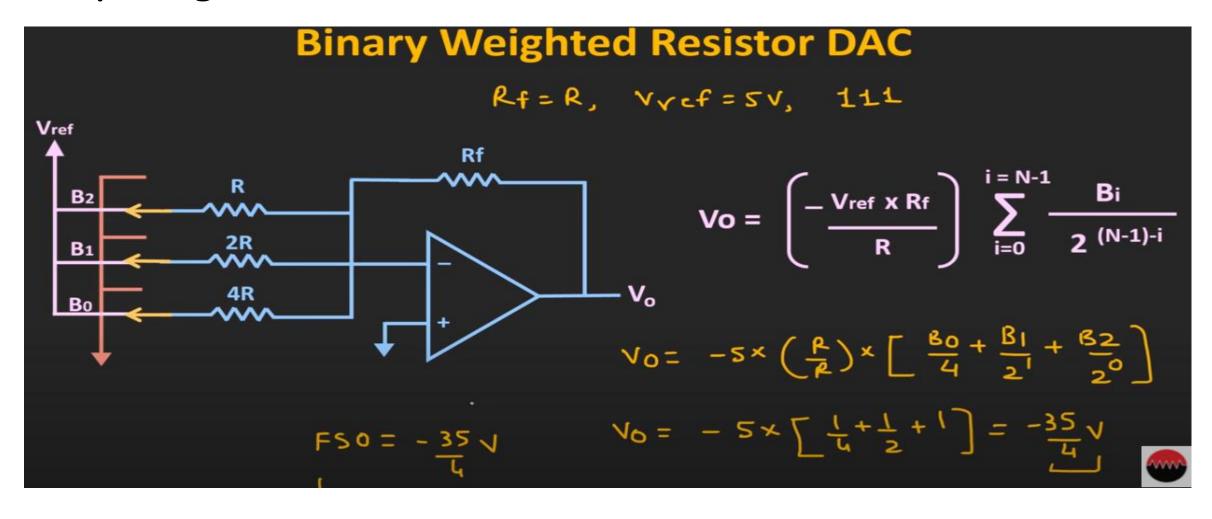


$$V_0 = -\left[\frac{R_f}{R_1} * V_1 + \frac{R_f}{R_2} * V_2 + \frac{R_f}{R_3} * V_3\right]$$

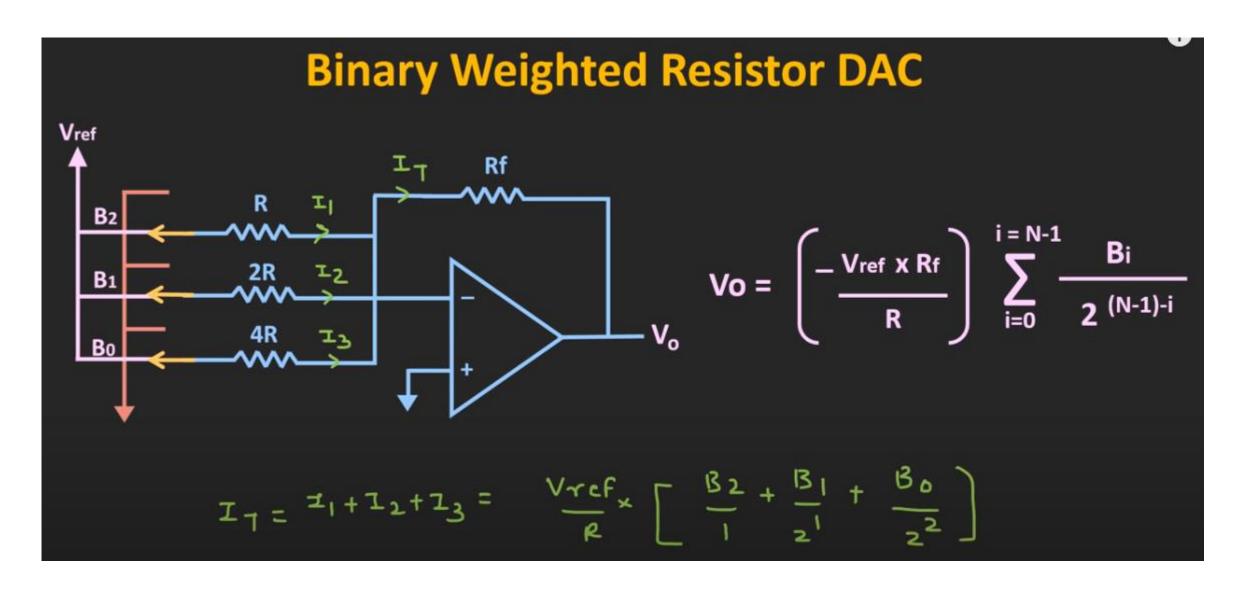
$$V_0 = -[V_1 + V_2/2 + V_3/3]$$

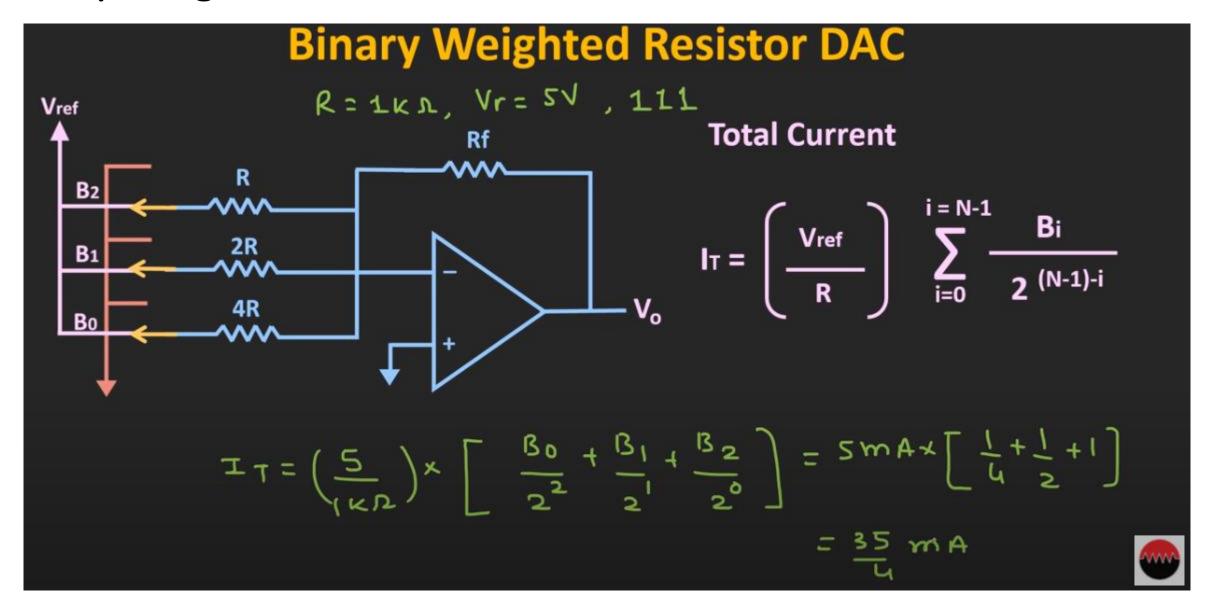
In this summing amplifier, if the inputs and the weight of each resistor is according to the binary number, then it can be used to convert the digital inputs to the analog outputs.



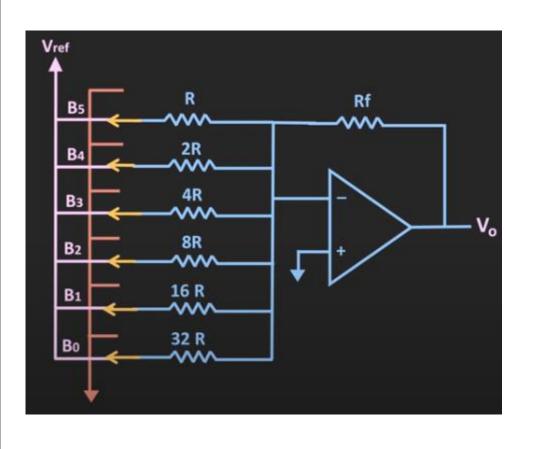


$$1LSB = \frac{FSO}{2^{N}-1} = \frac{-35/4}{2^{3}-1} = \frac{-35}{4\times7} = \frac{-5}{4}$$





Let us consider, Rf = R and find the V(max), V(min) for 111111, V(ref) = 5V



$$V_{0} = \left(-\frac{V_{ref} \times R_{f}}{R}\right)^{\frac{1}{2}} \sum_{i=0}^{N-1} \frac{B_{i}}{2^{(N-1)-i}}$$

$$V_{0} = \left(-5 \times \frac{R}{R}\right) \times \left[\frac{80}{32} + \frac{B_{1}}{16} + \frac{B_{2}}{8} + \frac{B_{3}}{4} + \frac{B_{4}}{2} + \frac{B_{5}}{2}\right]$$

$$V_{0} = -5 \times \left[\frac{1}{32} + \frac{1}{16} + \frac{1}{8} + \frac{1}{4} + \frac{1}{4} + \frac{1}{4}\right]$$

$$= V_{0} = -5 \times \frac{63}{32} \simeq -9 \cdot 84375 \times \Rightarrow FSO$$

$$2^{N} = -9 \cdot 84375 \times \Rightarrow FSO$$

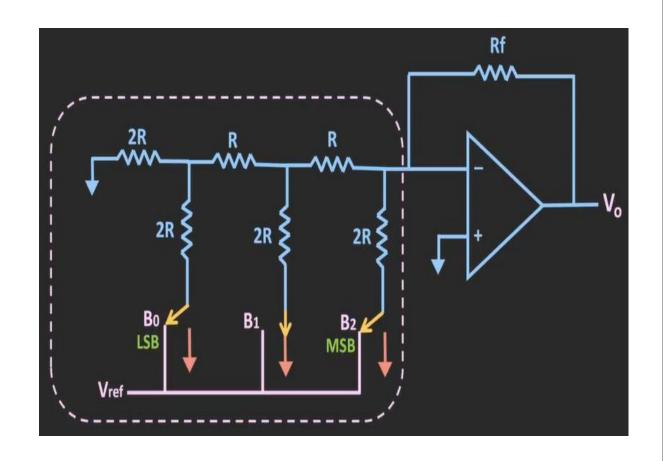
$$2^{N} = -9 \cdot 84375 \times \Rightarrow FSO$$

$$= -9 \cdot 84375 \times \Rightarrow FSO$$

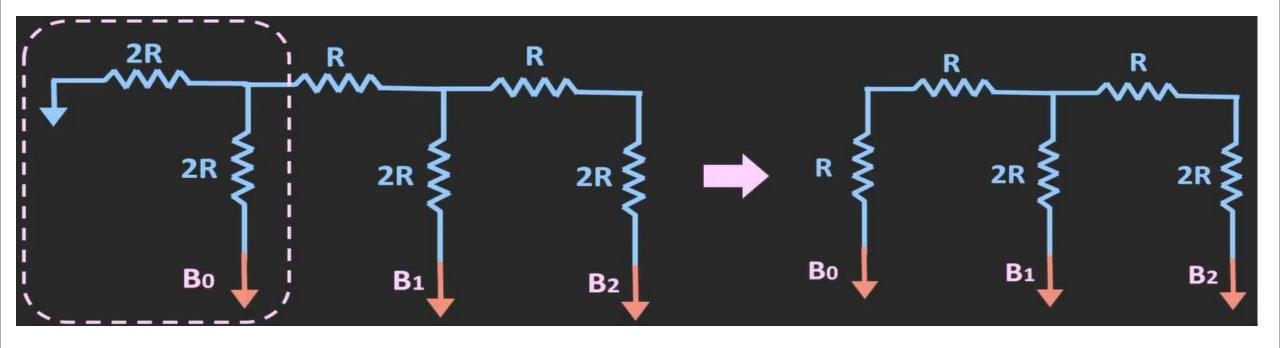
R-2R Ladder type DAC

Advantages of R-2R ladder type DAC

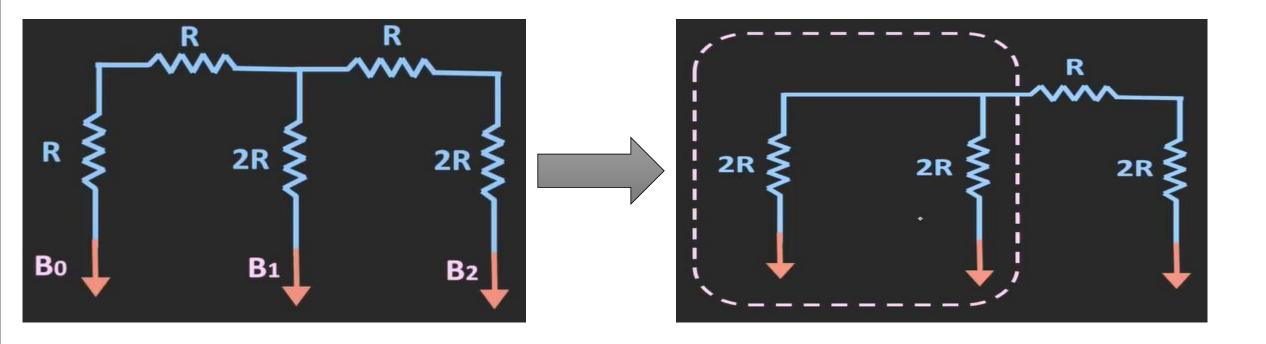
- Uses only two values of resistors that's why easy and accurate fabrication is possible.
- 2. Easily scalable to any desired number of bits.
- 3. Output impedance is R, regardless the number of bits.



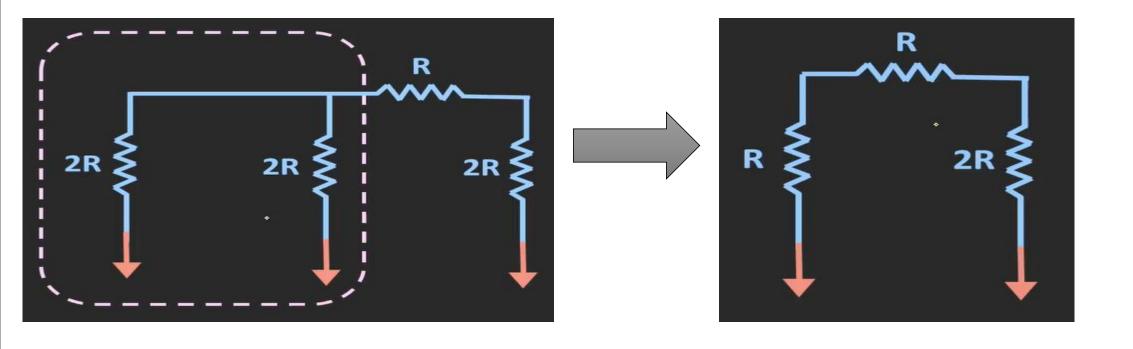
```
1/R = 1/2R + 1/2R
= 1 + 1/2R
= 2/2R
1/R = 1/R
R = R
```



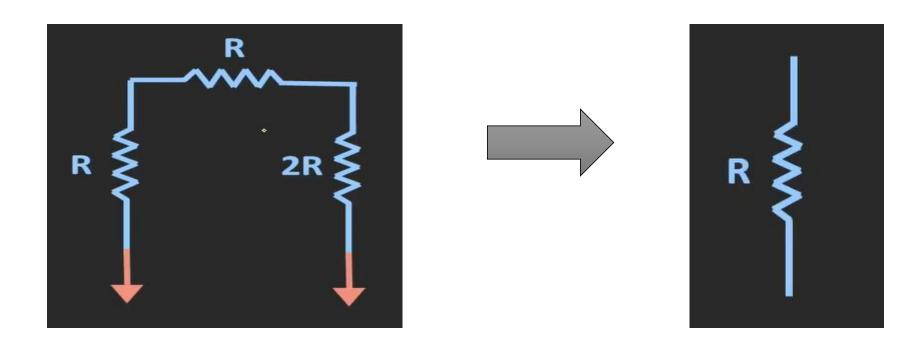
```
R = (R+R) \mid \mid (2R)
= (2R) \left| (2R)
= R
```



```
R = (2R) || (2R)
= R
```



```
R = (R+R) \mid \mid (2R)
= (2R) \left| (2R)
= R
```

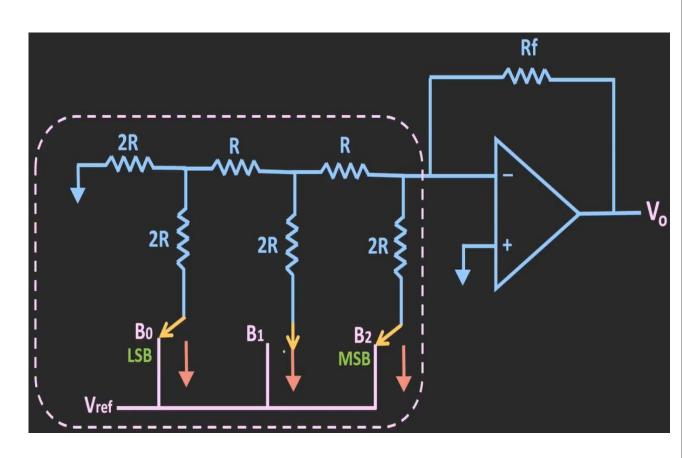


According to the binary number, this register are connected to the reference voltage or to the ground.

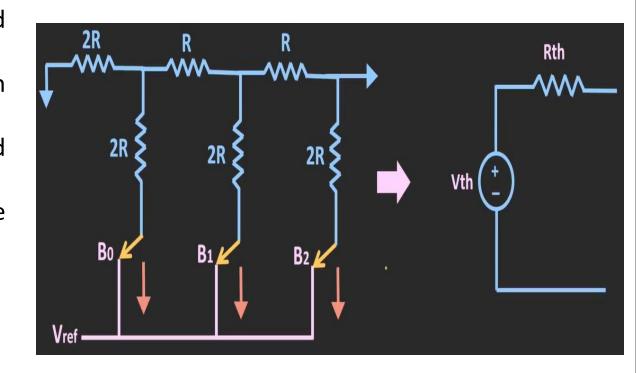
Here, B0 = 1

B1 = 0

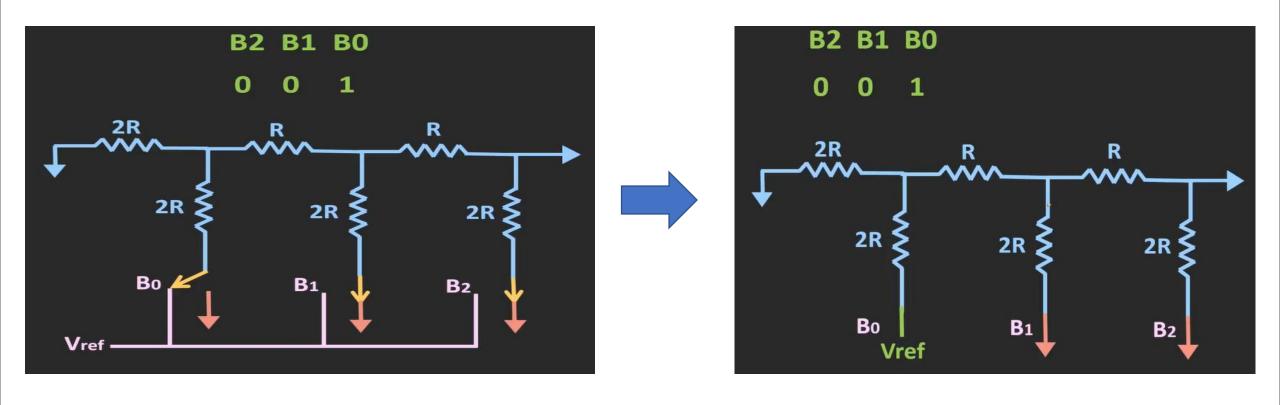
B2 = 1

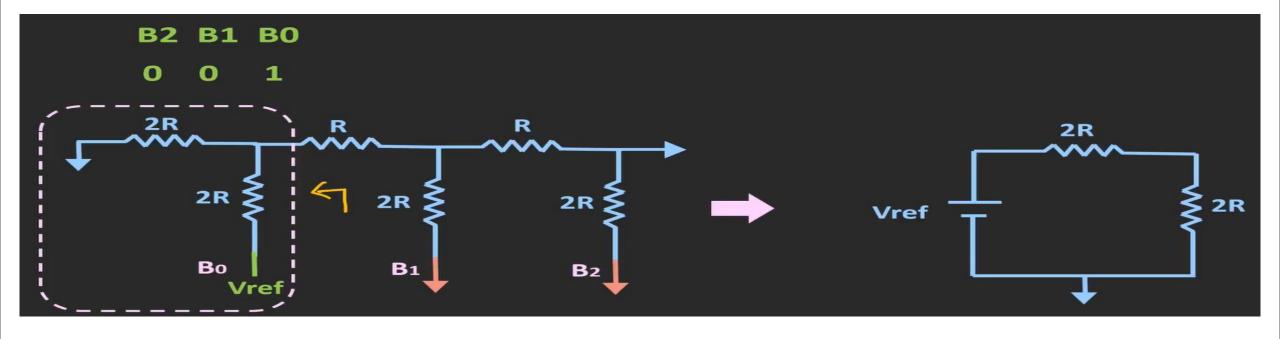


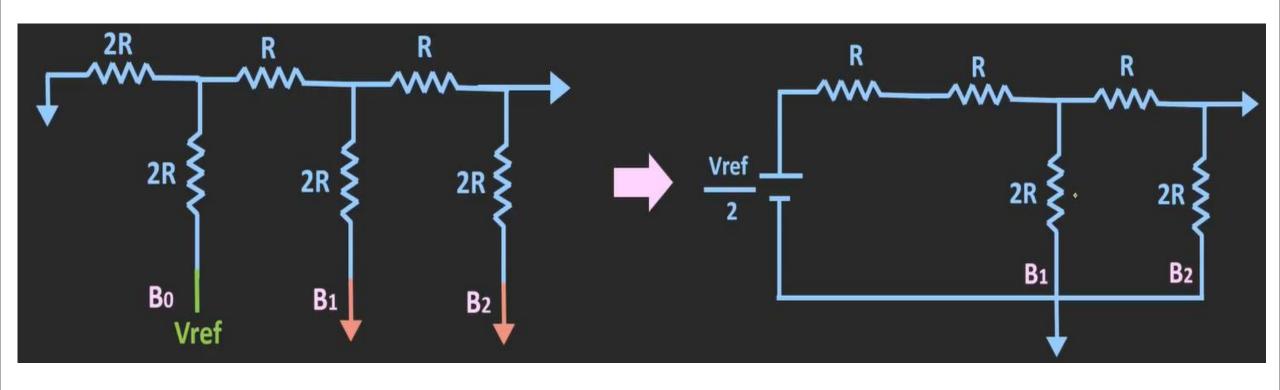
This is the Thevenin equivalent circuit of the R-2R ladder network. The value of the Thevenin's voltage will depend on the position of the switches. To find the Thevenin voltage we will consider one voltage source at a time and then by using the superposition theorem we will find the overall output voltage.

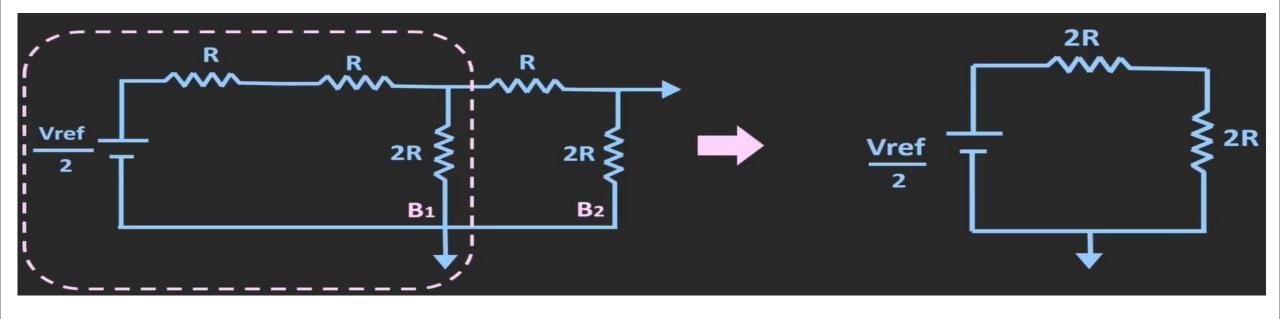


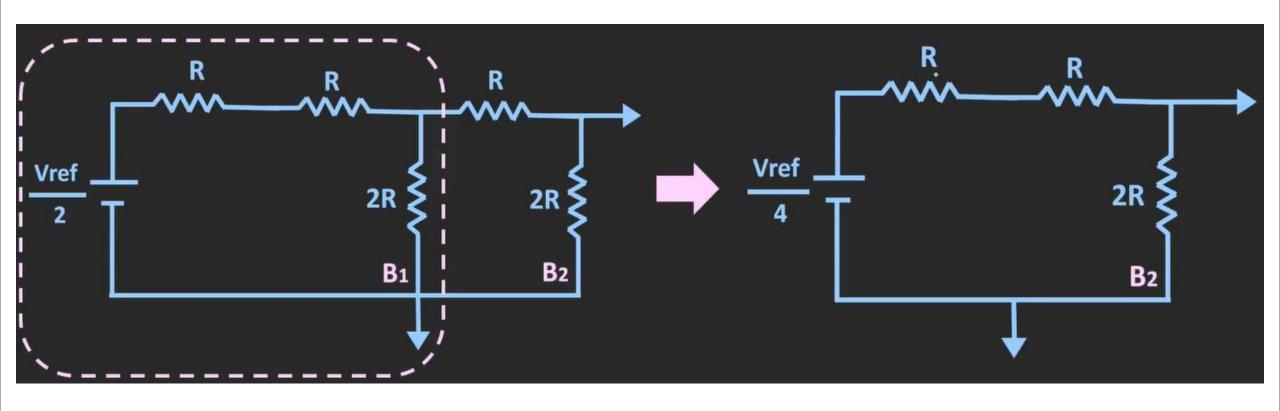
• Find out the output of the this 3 bit R-2R ladder circuit for the bit combination of B2 = 0, B1 = 0, B0 = 1.

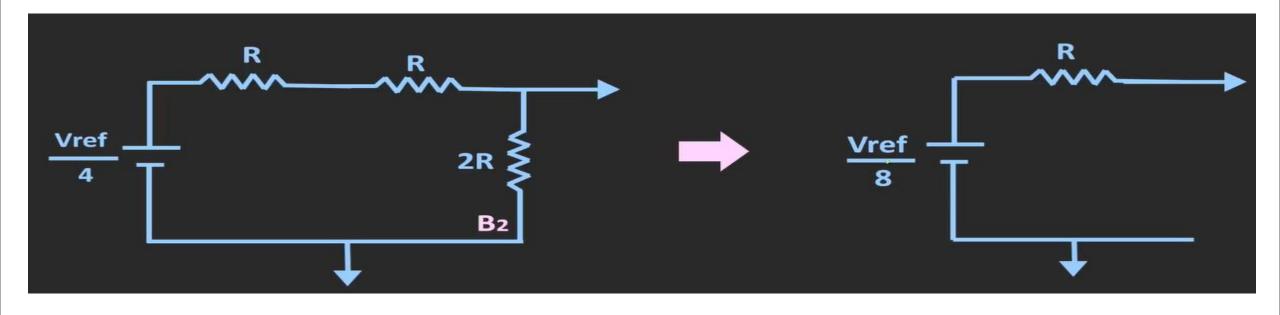




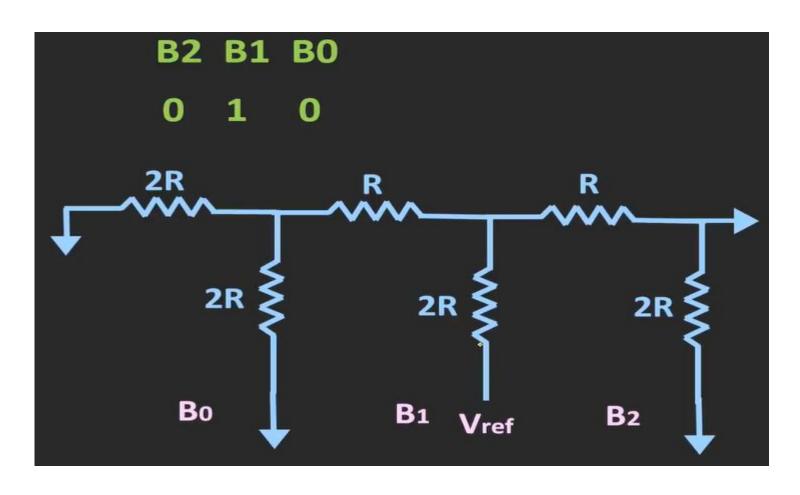


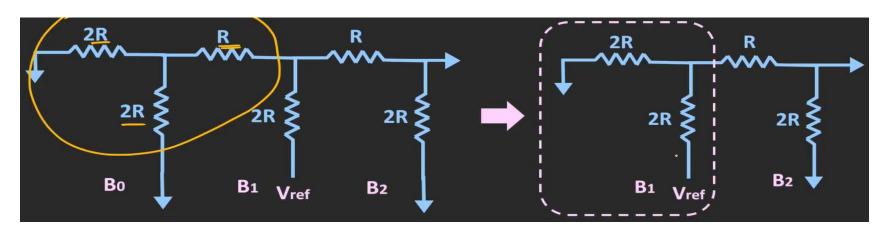


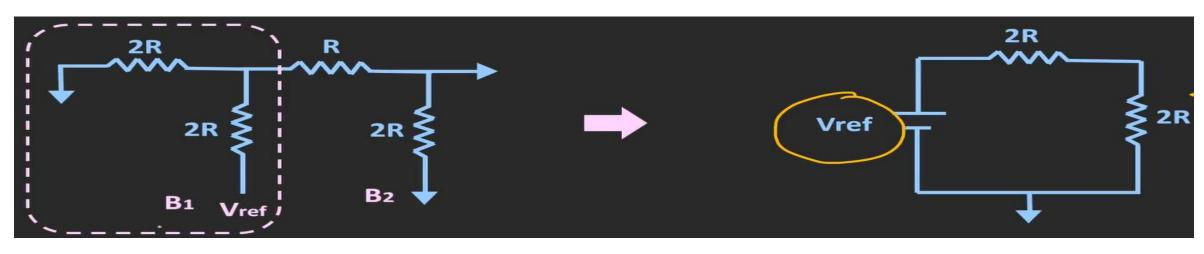


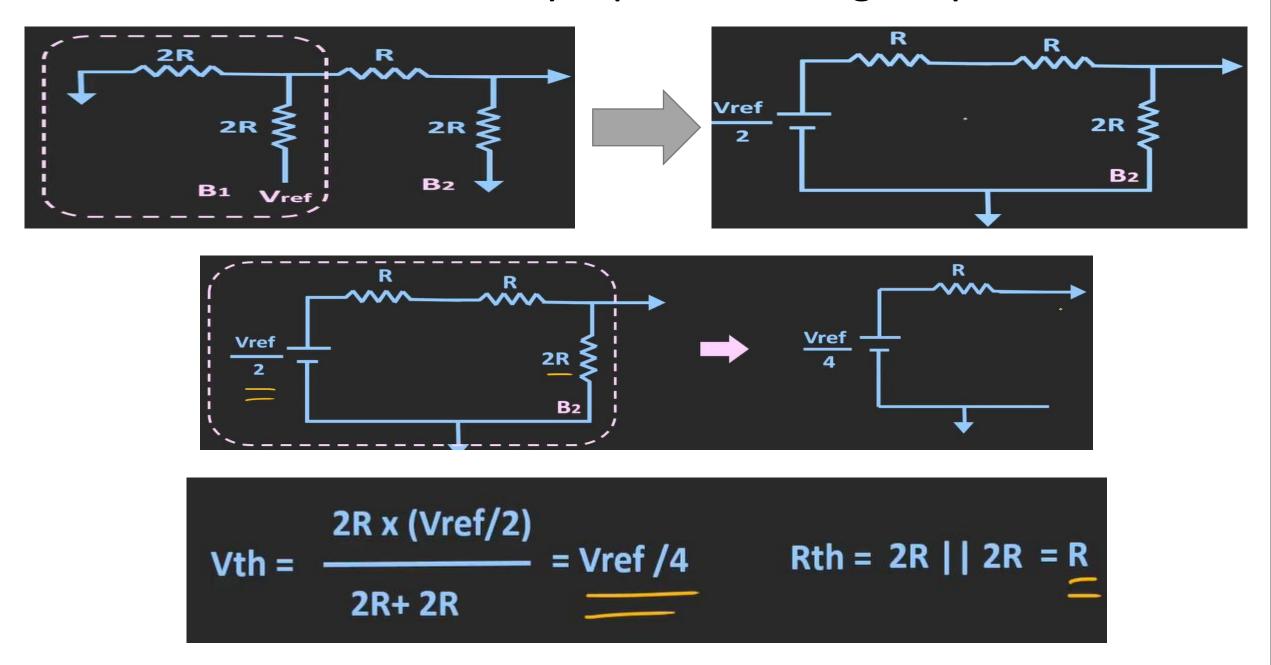


Find out the output of this R-2R ladder circuit







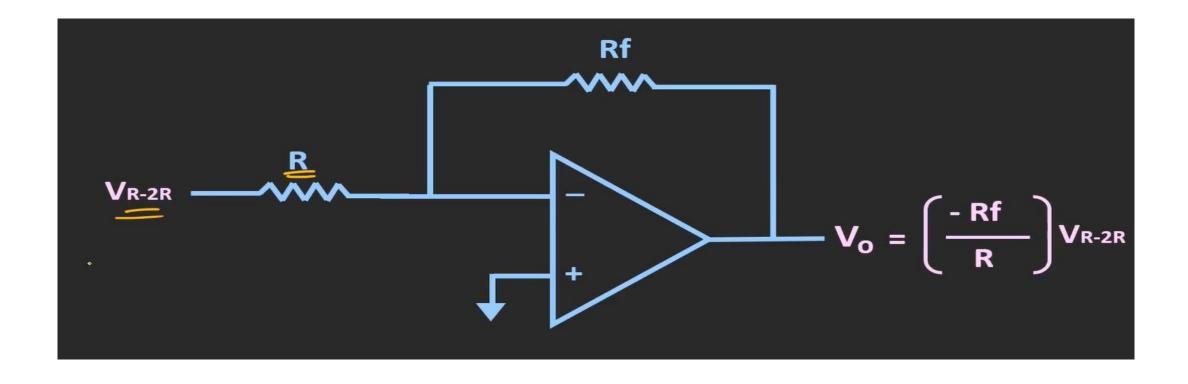


Output of 3 bit output Ladder

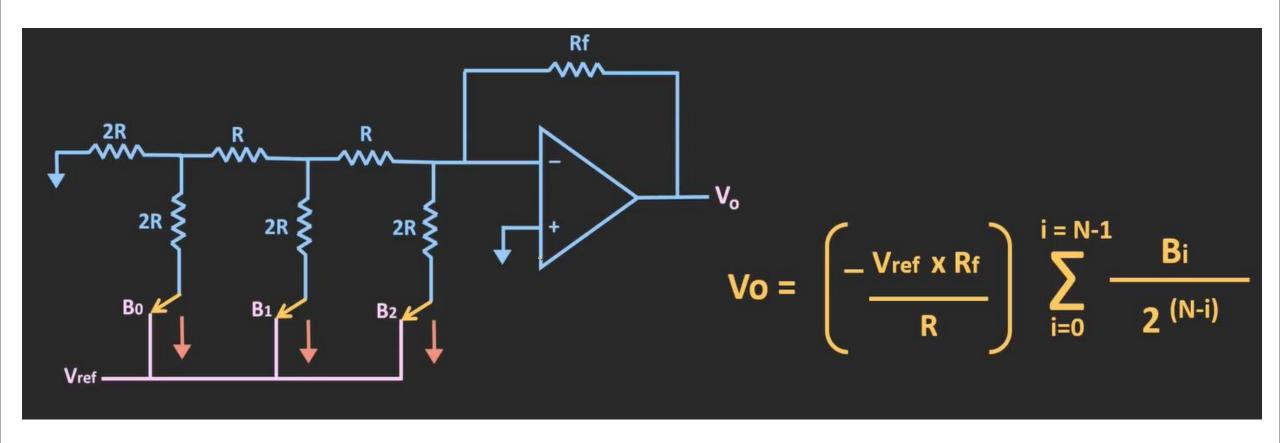
$$N = 3$$

$$Vref \left(\frac{B0}{8} + \frac{B1}{4} + \frac{B2}{2} \right)$$

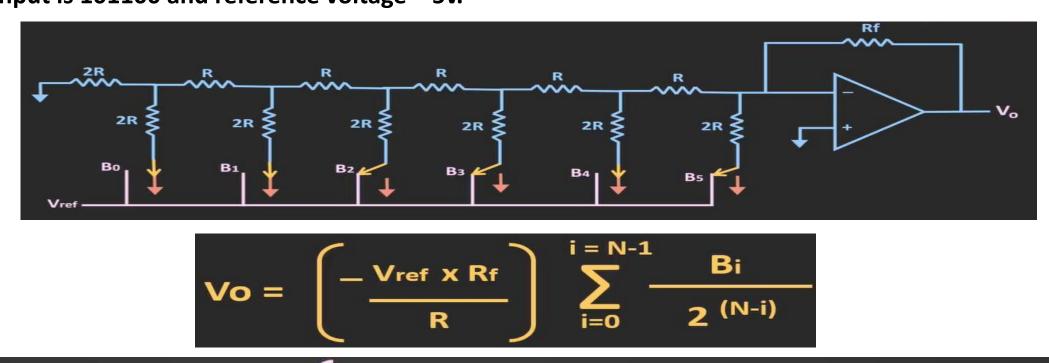
Final analog output:



Final analog output of N bit R-2R Ladder DAC:



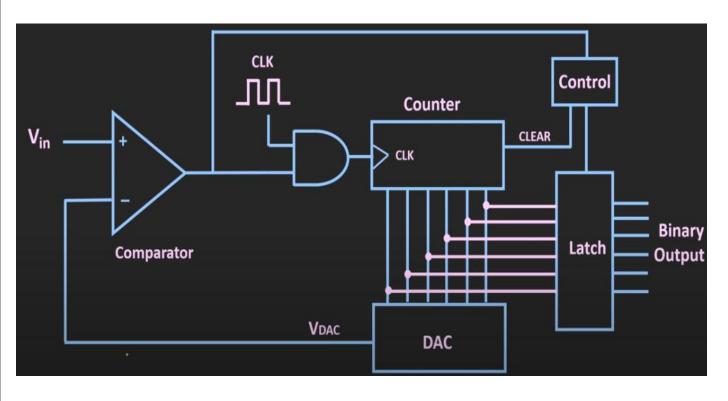
• For the given DAC find the full scale output voltage if Rf = $2k\Omega$ and R = $1k\Omega$. Find the output voltage when the input is 101100 and reference voltage = 5v.

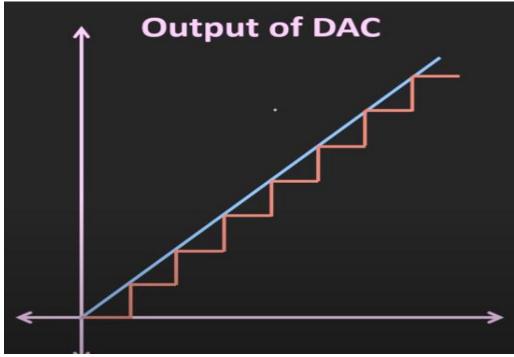


FSO = 5V
$$\left(\frac{-2}{1}\right)\left(\frac{1}{2^6} + \frac{1}{2^5} + \frac{1}{2^4} + \frac{1}{2^3} + \frac{1}{2^2} + \frac{1}{2^1}\right)$$

Counter Type ADC/Digital Ramp ADC

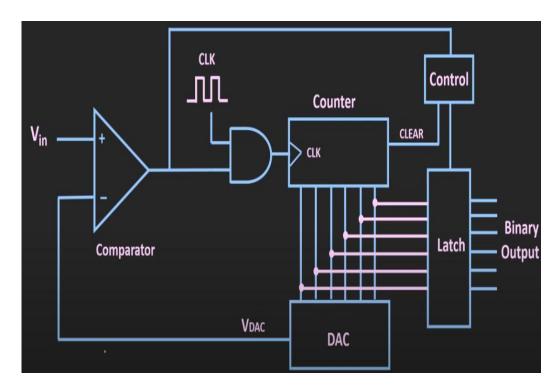
- It is called counter type ADC, because it uses a binary counter for the conversion.
- Here, the output of the counter is given to the DAC.
- As the counter increments it's count, the output of the DAC is incremented in a RAMP fashion.





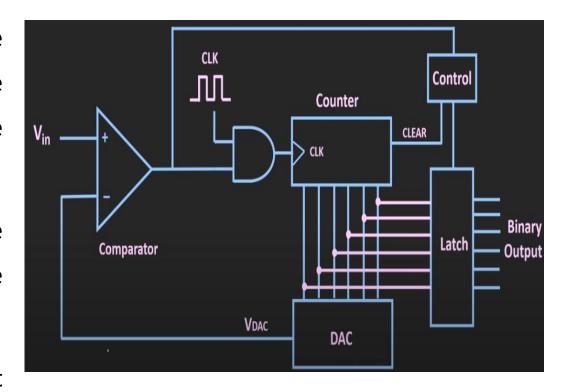
Working of Counter Type ADC/Digital Ramp ADC

- Here, the input voltage V_{in} is given to the non-inverting terminal of the comparator and the output of the DAC that V_{DAC} is given to the inverting terminal of the comparator.
- The output of the counter is given to the digital to analog converter.
- Initially, when the conversion starts, the counter is reset and the output of the DAC, $V_{DAC}=0$. Therefore, the input voltage is initially greater than the output of the DAC and the output of the comparator is high.
- When the comparator output is high then the clock pulse will be applied to the counter and starts counting.



Working of Counter Type ADC/Digital Ramp ADC

- As the counter increments its count, the output of the DAC will be increased in staircase form.
- The output of the DAC is continuously compared with the input voltage and as far as the $V_{in} > V_{DAC}$ the O/P of the comparator will be high and clock pulse is applied to the counter.
- When $V_{in} < V_{DAC}$ then the O/P of the comparator will be low and through the control circuit the output of the counter will be latched and this counter will get reset.
- The latched output is directly proportional to the input voltage.
- After this entire procedure the new conversion will start.



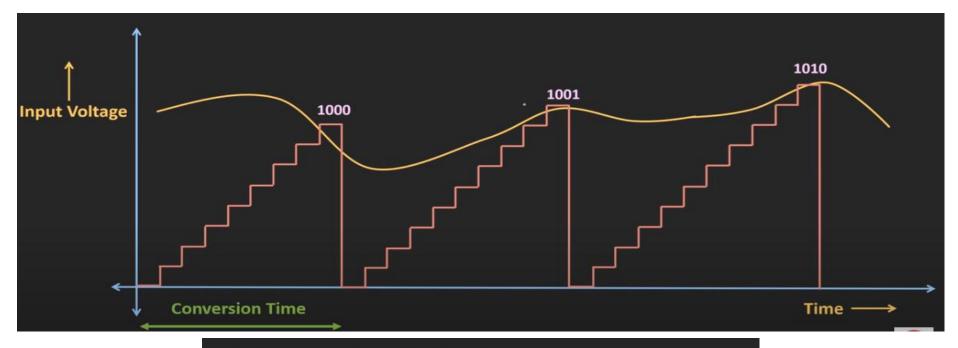
Counter Type ADC/Digital Ramp ADC

Disadvantage:

- Every time the new conversion starts, the counter will get reset and starts from 0.
- The conversion time depends on the magnitude of the input voltage.

Counter Type ADC/Digital Ramp ADC

Conversion Time:



Maximum Conversion Time:

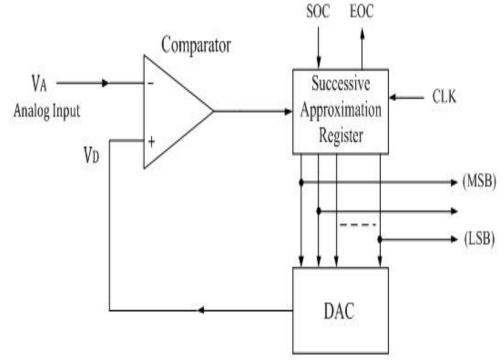
 $Tc (max) = (2^{N} - 1) Tclk$

TCLK: Duration of the clock pulse

N: Number of bits of ADC

Successive Approximation ADC

- At first, when the conversion starts, the SAR register clears all the bit to 0 and therefore, the output of the DAC is 0.
- Let's consider the input voltage V_A = 11.2v. Now, compare the input volage with the output of DAC.
- Here, $V_A = 11.2 > V_D = 0$ so, at first the MSB of the register is to 1 and rest of the bits set to 0. Let's consider this is a 4 bit ADC. So, the output of the **SAR will be 1000**.
- Now the output of V_D will be = 8V and V_A = 11.2 > V_D = 8 so, now the MSB of the SAR register will kept as it is and next bit will be set to 1. **SAR** = **1100**.
- Now V_D = 12 V and V_A = 11.2 < V_D = 12 so, now the 2nd bit will be 0 and the next bit will be set to 1. **SAR** = **1010**.



Successive Approximation ADC

- Now $V_D = 10$ V and $V_A = 11.2 > V_D = 10$ so, now the 3rd bit will be kept at it is and the next bit will be set to 1. SAR = 1011.
- Now $V_D = 11$ V and $V_A = 11.2 > V_D = 11$ so, now the 4th bit will be kept as it is and next bit will be 1 (but there is not next bit and all bits are checked so stop the conversion and the final value is the required result). **SAR = 1011.**

