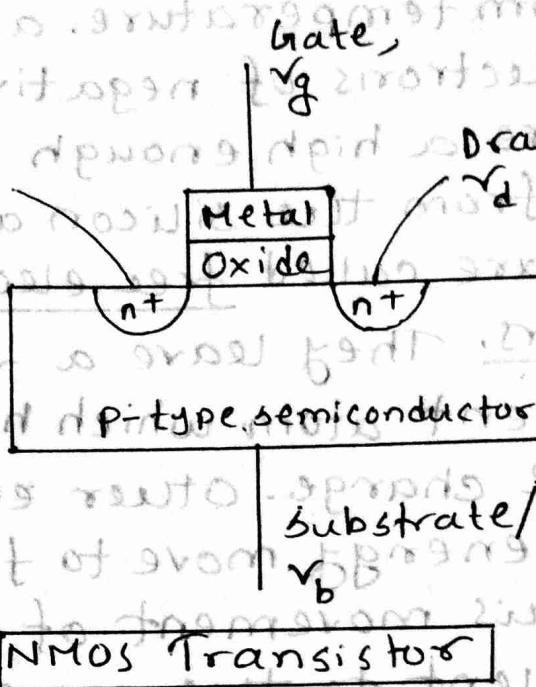


## Chapter-2

### MOS devices and basic circuits

**The MOS structure:** A n - doped semiconductor substrate.



- The basis of the transistor is a metal-oxide-semiconductor structure, hence the name MOS.

- The device input is called the gate. Originally it was a metal plate. Nowadays, it is usually made of poly silicon.

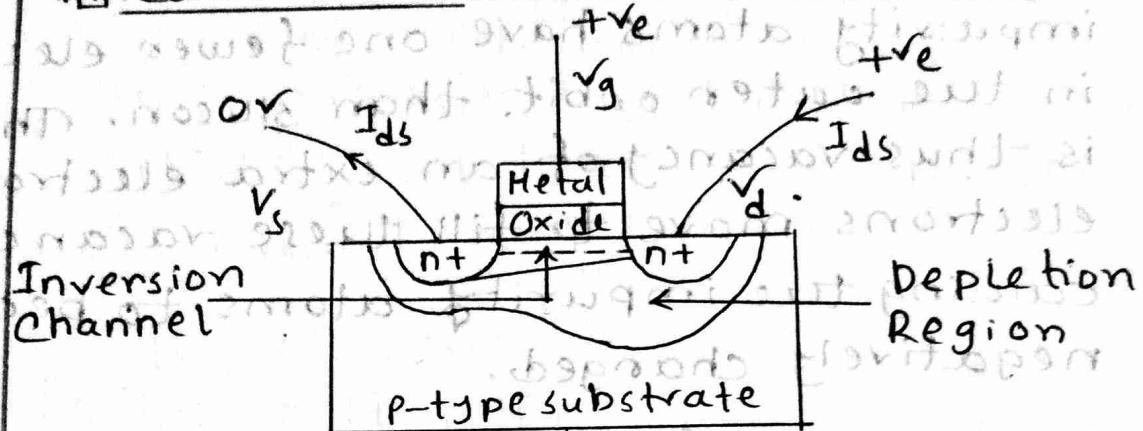
- The Oxide is very pure silicon dioxide. It acts as an insulator.

- The semiconductor is pure silicon which has been doped with relatively small amounts of an impurity.

- Pure silicon is not a good conductor at room temperature, as there are very few electrons of negative charge which acquire a high enough energy to break away from the silicon atoms. These electrons are called free electron / free charge carriers. They leave a vacancy or hole in parent atom which now has a net positive charge. Other electrons of lower energy move to fill these vacancies and this movement of free carriers is equivalent to the movement of holes of positive charge.
- An n-type semiconductor is obtained by doping pure silicon with an impurity possessing one more electron than silicon. This electron is loosely bound to the impurity atom and can easily break away leaving the atom positively charged. The freed electrons form the majority of free charges in the material, reducing the resistivity of the material.

- A p-type semiconductor arises when the impurity atoms have one fewer electron in the outer orbit than silicon. There is thus vacancy of an extra electron and electrons move to fill these vacancies, causing the impurity atoms to become negatively charged.
- The NMOS in figure consists of lightly doped p-type substrate and heavily doped n-type regions denoted and are called the source and the drain.
- Conventionally, the drain is the device output terminal.
- Input voltage  $V_{GS} \approx V_G - V_{SD}$   
Output voltage,  $V_{DS} = V_D - V_S$
- A terminal is connected to the bulk substrate and in NMOS, this is always connected to the most negative voltage available. This is so that the diodes formed by the substrate-source and substrate-drain pn junctions are always reverse biased and hence never conduct.

### 2) Conduction:



To make the transistor conduct, appropriate voltages have to be applied to the terminals.

$$V_g = +ve, V_d = +ve, V_s = 0, V_b = 0$$

- Although the conductivity of the semiconductor is less than that of the metal, it can be considered to be a conducting material. The oxide acts as an insulator between two conductors. So the structure resembles that of a capacitor.
- Applying positive gate bias wrt the source causes a positive charge to accumulate on the metal and an equal negative charge, supplied by the drain and the source, to be induced in the semiconductor surface just beneath

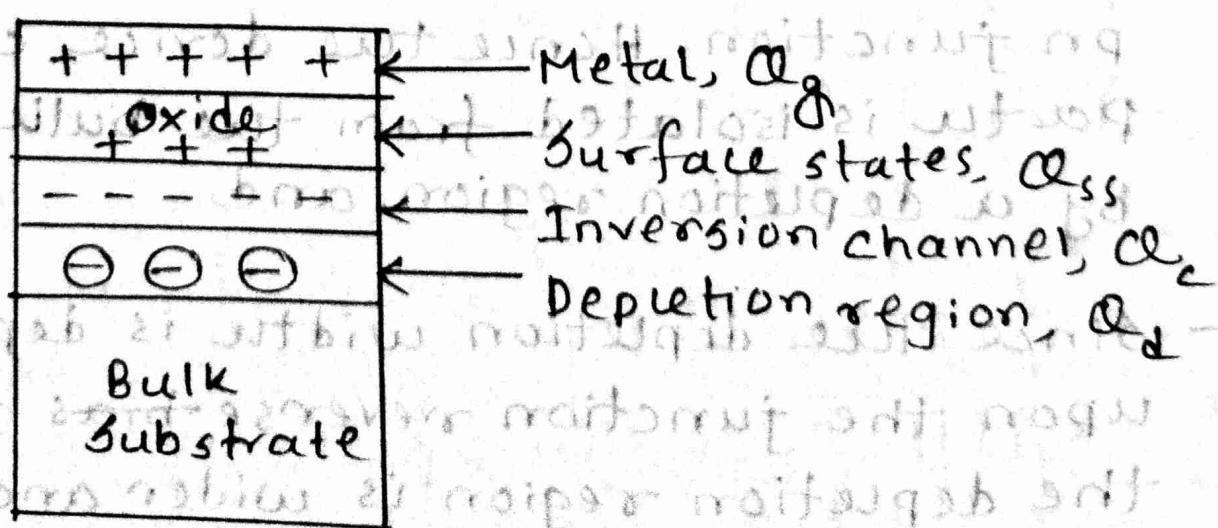
the oxide. This change is in addition to the existing charge.

- If the induced charge is small then it only causes the surface layer to become less p-type than the bulk.
- If the charge is large enough then the surface layer inverts from p-type to n-type. There is now continuous electron channel from the drain to the source, and current flows if there is a bias between them. In figure, current flows from the drain to the source as the drain potential is higher than that of source.
- A region depleted of free charge carriers separate all p-type region from n-type and prevents conduction of reverse biased pn junction. Hence the device conduction path is isolated from the bulk substrate by a depletion region.
- Since the depletion width is dependant upon the junction reverse bias voltage, the depletion region is wider around the drain than around the source.

- The device conduction path is also isolated from the gate by the oxide. Thus, all the current flowing into the drain must flow out of the source. This current is referred to as  $I_{ds}$ .

### Threshold Voltage:

- The input voltage at which the surface just becomes inverted is called the threshold voltage,  $V_t$ .
- Below the threshold voltage, an NMOS transistor is off and no current flows. Above the threshold, the inversion channel is established and the device conducts.



- $\sigma_{ss}$  represents positive charge trapped at the oxide-semiconductor interface as a result of imperfections at the surface. This, plus the gate charge  $\sigma_g$ , must be equal to the induced charge in the inversion channel  $\sigma_c$  plus the impurity atom charge  $\sigma_d$  in the depletion region.

$$\sigma_{ss} + \sigma_g = \sigma_c + \sigma_d$$

When the surface is just at the point of inversion,  $\sigma_c = 0$ .

$$\therefore \sigma_g = \sigma_d - \sigma_{ss}$$

If  $C_g$  = capacitance across the insulator-

$$\sigma_g = \frac{\sigma_d - \sigma_{ss}}{C_g}$$

- In practice,  $\sigma_g$  has to overcome some in-built potential differences before the transistor is brought to the edge of conduction. As a result, another two voltage terms have to be included.
- $V_{dif}$  represents the voltage arising as a result of the difference between the gate and the semiconductor material. Since, silicon gates are used nowadays,  $V_{dif}$  is small.

- $V_t$  is the voltage across the depletion region just at the point of inversion. It is usually less than 1V.

$$\therefore V_t = \frac{Q_d}{Cg} + V_p - \frac{Q_{ss}}{Cg} + V_{diff}$$

- The last three terms can be regarded as constant.
- $Q_d$  is dependent upon the impurity concentration of the semiconductor material beneath the oxide. This provides a mechanism for adjusting the threshold voltage.
- For NMOS transistor, the first two terms are positive and the last two negative. It allows the threshold to be made either positive or negative by suitable doping.
- The threshold is positive (usually 1V) if the semiconductor surface between the source and the drain is heavily doped with a p-type impurity. Such device is NMOS transistor.

- The threshold can be made negative (-4v) by doping the semiconductor surface with n-type impurity. Thus, even with  $V_{GS} = 0$  the device is on. Such transistor is called NMOS depletion mode transistor. It is necessary to apply a negative  $V_{GS}$  in order to repel the electrons from the surface and turn the device off.
- In PMOS, the substrate is n-type and the drain and source are heavily doped p-type regions. The substrate is connected to the most positive voltage available.
- A negative  $V_{GS}$  causes the holes to be attracted to and electrons to be ~~attracted by~~ repelled from the semiconductor surface just beneath the oxide.
- In PMOS, all four terms are negative. The threshold voltage can be adjusted by altering the impurity doping level. However, logic circuits require only PMOS enhancement type devices. These are fabricated with a negative threshold (-1v) and are off when  $V_{GS} = 0$ .

- Threshold are quoted for transistors assuming a source-substrate voltage of 0V. Changing the substrate voltage causes the threshold to change. It is known as the body effect.

$V_t$  is the threshold when  $V_{sb} = 0$ ,

$$\therefore V_t = V_t + r(V_{sb})^{1/2}$$

$r$  is a constant. Usually  $0.5$ .

## Characteristic Equation for NMOS Devices:-

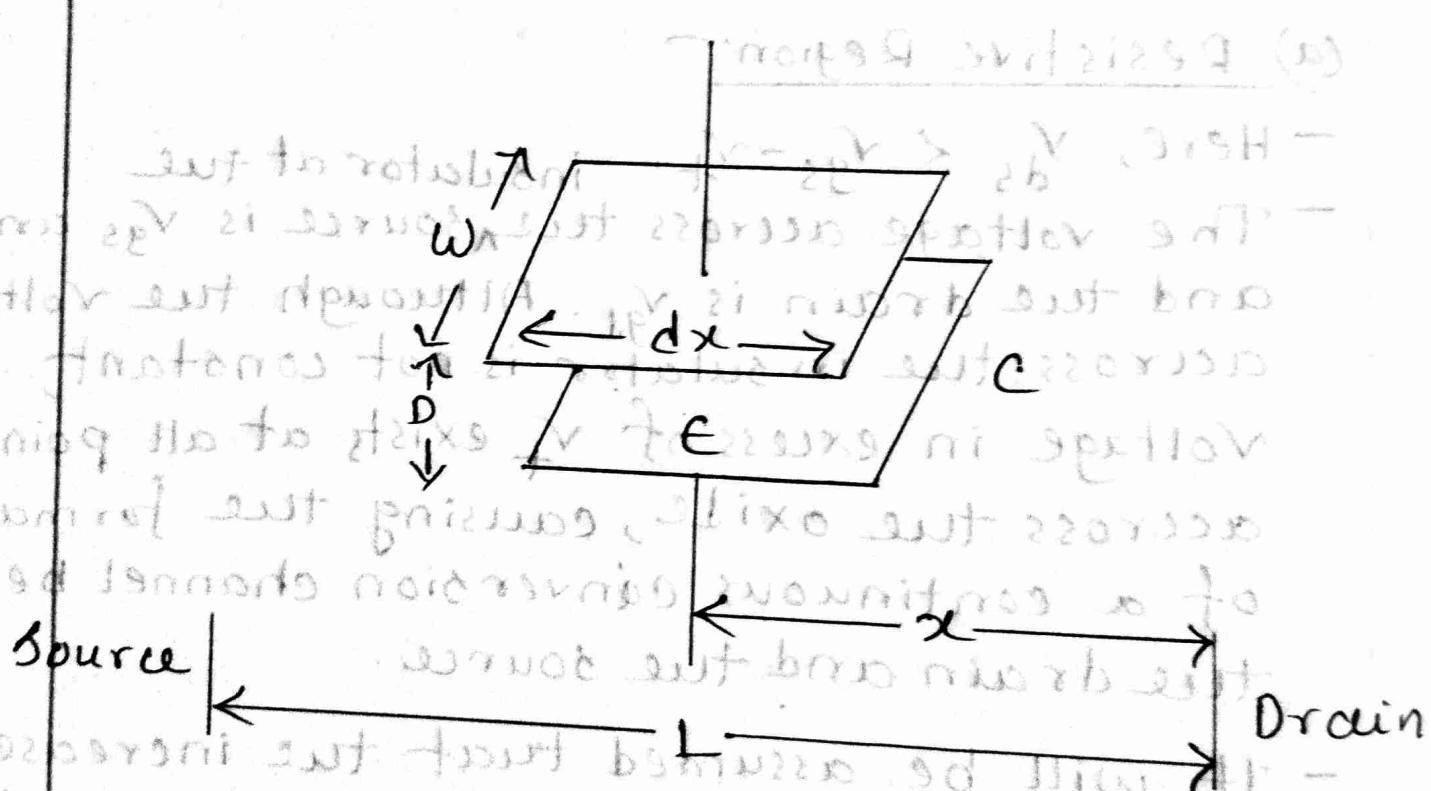
- when  $V_{GS} < V_t$ , the transistor is off, regardless of the drain voltage. The device does not conduct and no current flows.
- when  $V_{GS} > V_t$ , the device conducts. If a constant  $V_{GS}$  is applied then the resulting  $I_{DS}$  vs  $V_{DS}$  curve can be split into two regions - Resistive and Saturated.

### (a) Resistive Region:-

- Here,  $V_{DS} < V_{GS} - V_t$ . insulator at the
- The voltage across the source is  $V_{GS}$  and the drain is  $V_{DS}$ . Although the voltage across the insulator is not constant, a voltage in excess of  $V_t$  exists at all points across the oxide, causing the formation of a continuous conduction channel between the drain and the source.
- It will be assumed that the increase in voltage along the channel from drain to the source is linear with distance.
- The device structure therefore resembles an infinite number of capacitances between the drain and the source, each one having a different voltage across it.

and therefore a different charge from its neighbours. The total charge induced in the channel is the sum of the charge induced on each of these capacitances.

- Consider one of these capacitances of length  $dx$  situated at a distance  $x$  meters from the drain,



The channel width and length are w and L meters. Thus the capacitance, C farads, of the structure -

$$C = \frac{w \epsilon dx}{D}$$

where  $\epsilon$  is the permittivity of the insulator in farads/metre and  $D$  is the thickness of the oxide in meters.

- The voltage  $v$  in excess of  $v_t$  across the capacitor is -

$$v = \sqrt{g_d} + \frac{x}{L} \sqrt{d_s} - v_t$$

$$= v_{gs} - \sqrt{d_s} + \frac{x}{L} \sqrt{d_s} - v_t$$

$$v_{gs} = \sqrt{g_d} + \sqrt{d_s}$$

$$\therefore v_{gd} = v_{gs} - \sqrt{d_s}$$

- Thus the charge,  $q$  coulombs, induced on this capacitor is -

$$q = C \cdot v$$

$$= \frac{\omega \epsilon D x}{D} (v_{gs} - \sqrt{d_s} + \frac{x}{L} \sqrt{d_s} - v_t)$$

The total charge  $Q$  induced in this channel -

$$Q = \int_0^L \frac{\omega \epsilon}{D} (v_{gs} - \sqrt{d_s} + \frac{x}{L} \sqrt{d_s} - v_t) dx$$

$$= \frac{\omega \epsilon}{D} \int_0^L (v_{gs} \cdot dx - \sqrt{d_s} \cdot dx + \frac{x}{L} \sqrt{d_s} \cdot dx - v_t \cdot dx)$$

$$= \frac{\omega \epsilon}{D} \left[ v_{gs} \cdot x - \sqrt{d_s} \cdot x + \frac{x^2}{2L} \sqrt{d_s} - v_t \cdot x \right]_0^L$$

$$\text{displacement} = \frac{etw}{D} \left[ v_{gs} \cdot L - \frac{v_{ds}}{2} \cdot L + \frac{L}{2} \frac{v_t}{v_{ds}} - \frac{v_t \cdot L}{2} \right]$$

$$\therefore Q = \frac{etwL}{D} \left[ (v_{gs} - v_t) - \frac{v_{ds}}{2} \right]$$

- Now,  $Q = t I_{ds}$ , where it is the time in seconds for an electron to move across the channel and

$$t = \frac{\text{Channel length}}{\text{Electron velocity}} = \frac{L}{\mu n v_{ds}}$$

$$\therefore t = \frac{L}{\mu n v_{ds}}$$

$\mu n$  is the electron velocity per unit electron field (metre/volt-second) and is called the electron mobility.

- Hence,  $I_{ds}$  in amps ~

$$I_{ds} = \frac{Q}{t} = \frac{\frac{etwL}{D} \left[ (v_{gs} - v_t) - \frac{v_{ds}}{2} \right]}{\frac{L}{\mu n v_{ds}}} = \frac{etw \left[ (v_{gs} - v_t) - \frac{v_{ds}}{2} \right]}{D \mu n v_{ds}}$$

$$\Rightarrow I_{ds} = \frac{tW\mu n}{LD} [(V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2}]$$

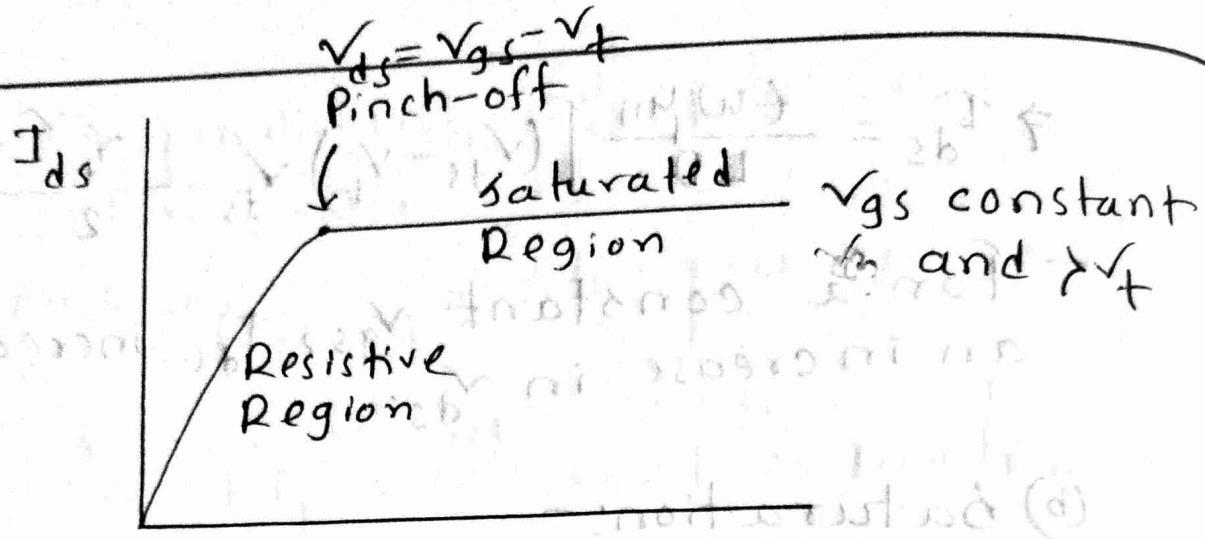
- For a constant  $V_{gs}$ ,  $I_{ds}$  increases with an increase in  $V_{ds}$ .

### (b) Saturation:

- Here,  $V_{ds} > V_{gs} - V_t$
- As the drain voltage rises, the voltage across the insulator at the drain drops, and at  $V_{ds} = V_{gs} - V_t$  it is  $V_t$ .
- This is the voltage necessary to just support the inversion, and this point is called pinch-off.
- At this point, the inversion channel ends just at the drain.
- At pinch off -  $V_{ds} = V_{gs} - V_t$

$$\therefore I_{ds} = \frac{tW\mu n}{LD} [(V_{gs} - V_t)V - \frac{(V_{gs} - V_t)^2}{2}]$$

$$\Rightarrow I_{ds} = \frac{tW\mu n}{2LD} (V_{gs} - V_t)^2$$



## Characteristic Equation for PMOS devices

### (a) Resistive region:-

-  $V_{ds} < V_{sg} - V_t$

$$- I_{sd} = \frac{\epsilon M_p}{D} \cdot \frac{w}{L} \left[ (V_{sg} - V_t) V_{sd} - \frac{\sqrt{V_{sd}}}{2} \right]$$

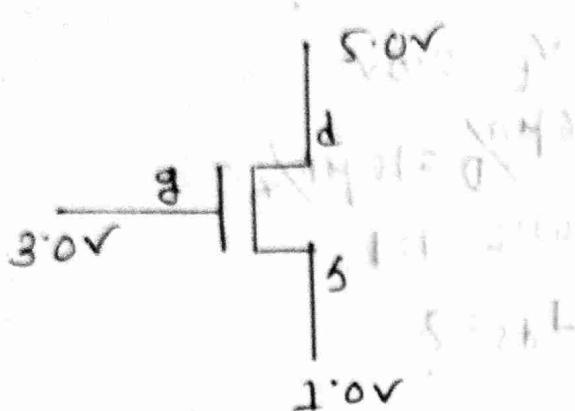
### (b) Saturated region:-

- Pinch off at  $V_{sd} = V_{sg} - V_t$

- Saturated at  $V_{sd} > V_{sg} - V_t$

$$- I_{sd} = \frac{\epsilon M_p}{2D} \cdot \frac{w}{L} (V_{sg} - V_t)^2$$

\*Exercise - 1:-



$$V_t = 1.0V$$

$$k_m \mu_D = 15 \mu A/V^2$$

$$w/L = 1/1$$

$$I_{ds} = ?$$

Soln:-

$$V_{gs} = (3 - 1)V \\ = 2V$$

$$\because V_{gs} > V_t$$

$\therefore$  Transistor on.

$$V_{ds} = 5 - 1 = 4V$$

$$V_{gs} - V_t = 2 - 1 = 1V$$

$$V_{ds} > V_{gs} - V_t$$

$\therefore$  Transistor in saturated region.

$$(V_{ds} - V_t) = 3V$$

$$\therefore I_{ds} = \frac{k_m \mu n}{2D} \cdot \frac{W}{L} (V_{ds} - V_t)$$

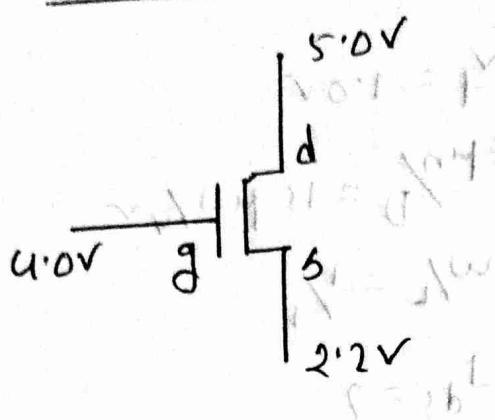
$$= 15/2 \cdot 1/1 \cdot 1V$$

$$= 15/2 \mu A$$

$$(Ans.) = 7.5 \mu A$$

(Ans.)

## \* Exercise-2:-



$$V_f = 2.0V$$

$$\epsilon \mu_n / D = 15 \mu A / \sqrt{m}$$

$$\omega:L=1:1$$

$$I_{ds} = ?$$

501<sup>n</sup>:—

$$\sqrt{g_s} = (4 - 2 \cdot 2) \sqrt{ }$$

$$= 1.8 \checkmark$$

$$\therefore \sqrt{g_s} < \sqrt{t}$$

∴ Transistor off

$$\therefore I_{ds} = 0 \mu A$$

## NMOS Inverter with a Resistor Load :-

\*  $V_p = +5V$

when  $V_g = 0V$

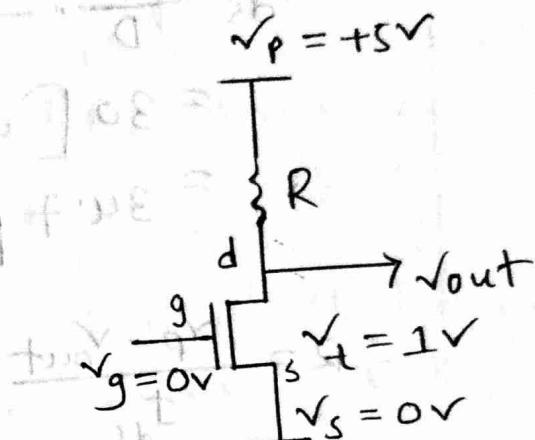
$$V_{gs} = V_g - V_s = 0V$$

$$V_{gs} < V_t$$

$\therefore$  Transistor off.

No current flows through the transistor.

$$\therefore V_{out} = V_p$$



$$V_{out} = \text{Logical 0}$$

$$\approx 0.3V_F \\ = 0.3$$

$$V_d = V_{out} \\ = 0.3$$

When  $V_g = 5V$  (resistive mode)

$$V_{gs} = V_g - V_s = 5V$$

$$V_{gs} \geq V_t$$

$\therefore$  Transistor on

$$V_{ds} = V_d - V_s$$

$$= 0.3 - 0$$

$$= 0.3$$

$$V_{gs} - V_t = 5 - 1 = 4V$$

$$\therefore V_{ds} < V_{gs} - V_t$$

$\therefore$  Transistor in resistive mode.

$$\therefore I_{ds} = \frac{E_M n}{D} \cdot \frac{w}{L} \left[ (V_{GS} - V_t) \sqrt{I_{ds}} - \frac{\sqrt{I_{ds}}}{2} \right] \text{mA}$$

$$= 30 \left[ 4 \times 0.3 - 0.3 \sqrt{I_{ds}} \right] \mu\text{A}$$

$$= 34.7 \mu\text{A}$$

for enhancement  
 type NMOS -  
 $\frac{E_M n}{D} = 30 \text{ mA}/\sqrt{\text{v}}$   
 we assume  
aspect ratio  
 $w/L = 1/1$

$$\therefore R = \frac{V_p - V_{out}}{I_{ds}}$$

$$= \frac{5 - 0.3}{34.7} \text{ k}\Omega$$

$$= 135.4 \text{ k}\Omega$$

Problem

- The silicon area required to implement this resistor is far larger than that for the transistor ( $\times 300$ ). Thus it is not practical to use a resistor as a load. Instead, MOS device is used.

## NMOS Inverter with an NMOS enhancement Transistor load:-

\*

When  $V_{in} = 0$ ,

$$V_{gs} = V_g - V_s = 0V$$

$$V_{gs} < V_{t_1}$$

i.e. Transistor  $T_1$  off

Let us take  $V_{out} = \text{Logical ON}$

$$\therefore V_s = V_{out} \text{ at } T_2$$

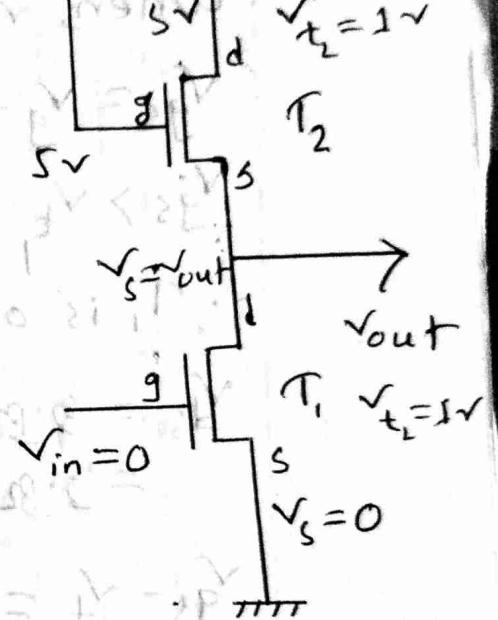
we cannot neglect the body effect of  $T_2$

$$V_{t_L} = V_{t_{20}} + r(V_{sb})^{1/2}$$

$$= V_{t_{20}} + r(V_{out})^{1/2}$$

$$= 1 + 0.5(V_{out})^{1/2}$$

$$r_p = 5\text{N}$$



Body effect constant,  
 $r = 0.5$

$$V_{out} = V_p - V_{t_2}$$

$$= 5 - (1 + 0.5V_{out})^{1/2}$$

$$= 5 - 1 - 0.5V_{out}^{1/2}$$

$$\Rightarrow V_{out} = 6 - 0.5V_{out}^{1/2}$$

$$\begin{aligned} 0.5V_{out}^{1/2} &= 6 - V_{out} \\ V_{out}^{1/2} &= 8 - 2V_{out} \\ V_{out} &= 64 - 32V_{out} + 4V_{out} \\ 4V_{out} - 33V_{out} + 64 & \end{aligned}$$

Solving ~

$$V_{out} = 3.12 \text{ V} \rightarrow \text{for this circuit}$$

$$\text{logic } Dn = 3.12 \text{ V}$$

$$V_p = 5 \text{ V}$$

\*

$$\text{When } V_{in} = 3.12 \text{ V}$$

$$V_{gs} = V_g - V_s = 3.12 \text{ V}$$

$$V_{gs} > V_t$$

$\therefore T_1$  is on.

$$V_{ds} = 0.3 - 0 \quad \begin{matrix} \nearrow \text{Because, we} \\ \text{want } V_{out} \text{ to} \\ \text{be off} \end{matrix}$$

$$= 0.3 \text{ V}$$

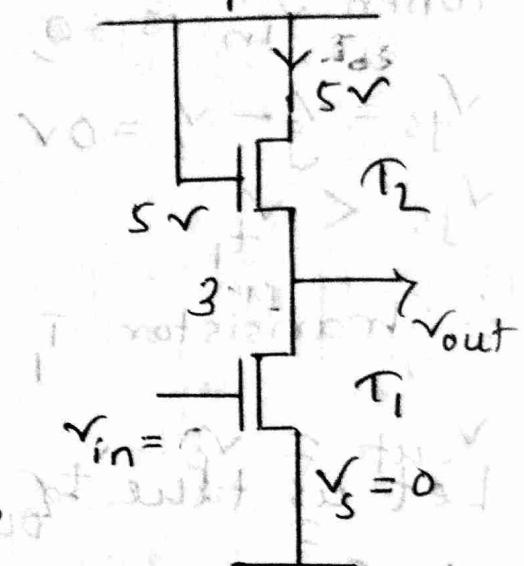
$$V_{gs} - V_t = 3.12 - 1 = 2.12 \text{ V}$$

$$V_{ds} < V_{gs} - V_t$$

$\therefore$  Resistive region

$$I_{ds1} = \frac{EMn}{2D} \cdot \frac{w_1}{L_1} \left[ (V_{gs} - V_t) V_{ds} - \frac{V_{ds}}{2} \right]$$

$$= 17.73 w_1 \text{ MA}$$



At  $T_L$  -

$$\sqrt{v_{gs}} = 5 - 0.3 \\ = 4.7 \text{ V}$$

$$\sqrt{v_{gs}} > \sqrt{T_L}$$

$\therefore T_L$  is on

$$\sqrt{v_{ds}} = 5 - 0.3 = 4.7 \text{ V}$$

$$\sqrt{v_{gs}} - \sqrt{T_L} = 4.7 - 1 = 3.7 \text{ V}$$

$\therefore v_{out} = \text{off, body effect}$

$\because \sqrt{v_{ds}} > \sqrt{v_{gs} - \sqrt{T_L}}$  (no saturation is neglected)

$\therefore T_L$  is in saturated region

$$\therefore I_{ds2} = N \frac{\epsilon \mu n}{2D} \cdot \frac{w_2}{L_2} (\sqrt{v_{gs}} - \sqrt{T_L})^{\sqrt{}} \\ = 15 \cdot \frac{w_2}{L_2} (3.7)^{\sqrt{}} \\ = 205.4 \frac{w_2}{L_2} \text{ mA}$$

Inverter ratio,  $k = \frac{w_1/L_1}{w_2/L_2}$

$$\therefore I_{ds1} = I_{ds2} \text{ web current of qsb is same}$$

$$\Rightarrow 17.73 \frac{w_1}{L_1} = 205.4 \frac{w_2}{L_2}$$

$$\Rightarrow \frac{\omega_1/L_1}{\omega_2/L_2} = \frac{205.4}{17.73}$$

$$\Rightarrow K = 11.6$$

$$\therefore K \approx 12$$

$$\rightarrow \omega_1/L_1 = 3/1$$

$$\omega_2/L_2 = 1/4$$

### \*Drawbacks:-

- Output voltage is only 3.12 V.
  - The speed of the rising edge of the gate is slow.
  - - - - -
- when  $V_{in} = 3.12 V$ ,  $V_{out} = 0.3 V$ . If  $V_{in}$  switches to 0.3 V,  $T_1$  turns off and  $V_{out}$  starts to rise. Initially,  $V_{gs}$  of  $T_2 = 4.7 V$ , but as  $V_{out}$  rises,  $V_{gs}$  of  $T_2$  decreases and  $V_{T2}$  rises because of the body effect. So, less current flows in  $T_2$ . This progressively slows down the rate of voltage rising.

$\hookrightarrow$  Soln n-channel depletion devices

## NMOS Inverter with an NMOS Depletion Transistor Load:-

Transistor Load:-

- The depletion threshold of  $T_2$  is always negative and since the gate source voltage of  $T_L$  is zero,  $T_2$  is always on.

\*

When  $V_{in} = 0V$

$$V_{gs} = 0V$$

$$V_{gs} < V_{t_1}$$

$\therefore T_1$  is off

$$V_{out} = 5V$$

The drain source voltage of  $T_L$  is very small (and negligible). Thus there is no high level voltage loss.

\*

When  $V_{in} = 5V$

$$V_{gs} = 5V > V_{t_1}$$

$\therefore T_1$  is on.

$$\text{Let } V_{out} = 0.3V$$



At  $T_1$

$$\sqrt{ds} = 0.3 \text{ V}$$

$$\sqrt{gs - \sqrt{t_1}} = 5 - 1 = 4 \text{ V}$$

$$\therefore \sqrt{ds} < \sqrt{gs - \sqrt{t_1}}$$

$\therefore T_1$  is in resistive region.

for enhancement type,  $\frac{\epsilon M_n}{D} = 30$

for depletion type,  $\frac{\epsilon M_n}{D} = 25$

$$\therefore I_{ds} = \frac{\epsilon M_n}{D} \cdot \frac{w_1}{L_1} \left[ (\sqrt{gs - \sqrt{t_1}}) \sqrt{ds} - \frac{\sqrt{ds}}{2\sqrt{D}} \right] = 28 \text{ V}$$
$$= 34.65 \frac{w_1}{L_1} \mu\text{A}$$

At  $T_2$

$$\sqrt{ds} = 5 - 0.3 = 4.7 \text{ V} \quad | \quad \sqrt{gs} = 0.3 - 0.3 = 0 \text{ V}$$

$$\sqrt{gs - \sqrt{t_2}} = 0 - (-u) = u \text{ V}$$

$$\sqrt{ds} \geq \sqrt{gs - \sqrt{t_2}}$$

$\therefore$  Saturated region.

$$\therefore I_{ds} = \frac{\epsilon M_n}{2D} \cdot \frac{w_2}{L_2} (V_{gs} - \sqrt{t_2})^2$$

$$= 200 \frac{w_2}{L_2} \text{ mA}$$

$$\therefore k = \frac{w_1/4}{w_2/L_2} = \frac{200}{34.65} = 5.8 \approx 6$$

$$\therefore \frac{w_1/4}{w_2/L_2} = 3/1$$

④ Advantage:

- Silicon area occupied by  $T_1$  and  $T_2$  are reduced.

⑤ The CMOS Inverter:

\* When  $V_{in} = 0V$

In  $T_1$  -

$$V_{gs} = 0V < V_{t1}$$

$\therefore T_1$  is off.

In  $T_2$  -

$$V_{sg} = 5V > V_{t2}$$

$\therefore T_2$  is on

The current flowing through  $T_1$  is leakage current and can be neglected.

$$\therefore V_{sd} = 0$$

$$\therefore V_d = 5V \text{ and } V_{out} = 5V.$$

\*

When  $V_{in} = 5V$  -

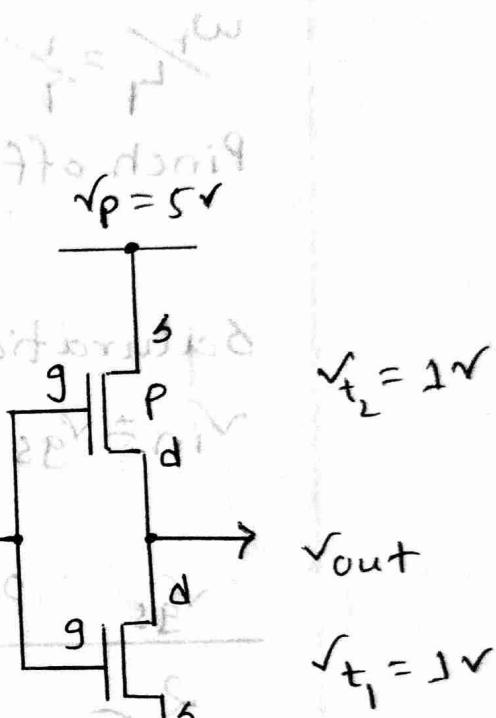
$$V_{gs} = 5V > V_{t1}$$

$\therefore T_1$  is on

Since,  $V_{sg} = 0V < V_{t2}$

$\therefore T_2$  is off.

$$\therefore V_{out} = 0V$$



$\otimes I_{ds}$  vs.  $V_{out}$  curves for  $T_1$  and  $T_2$ :

Transistor  $T_1$ :

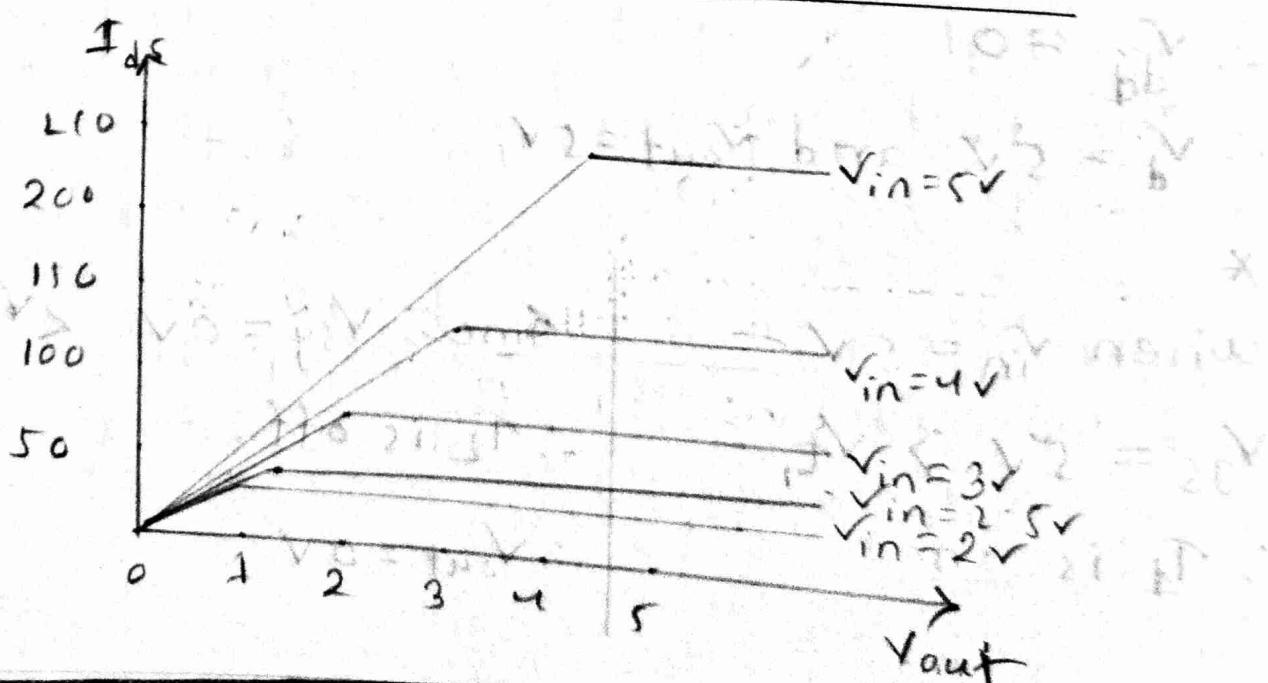
$$\frac{w}{l} = \frac{1}{1}, \frac{C_{mn}}{D} = 30 \mu A/V, V_{te} = 1V$$

$$\begin{aligned} \text{Pinch off occurs when } V_{ds} &= V_{gs} - V_{te} \\ &= V_{gs} - 1 \end{aligned}$$

$$\text{Saturation } I_{ds} = 1(V_{gs} - 1)^2$$

$$V_{in} = V_{gs}, V_{out} = V_{ds}, I = I_{ds}$$

$V_{gs}$	Pinch off $V_{ds}$	Saturation $I_{ds}$
2	1	15
2.5	1.5	33.8
3	2	60



## Transistor T2

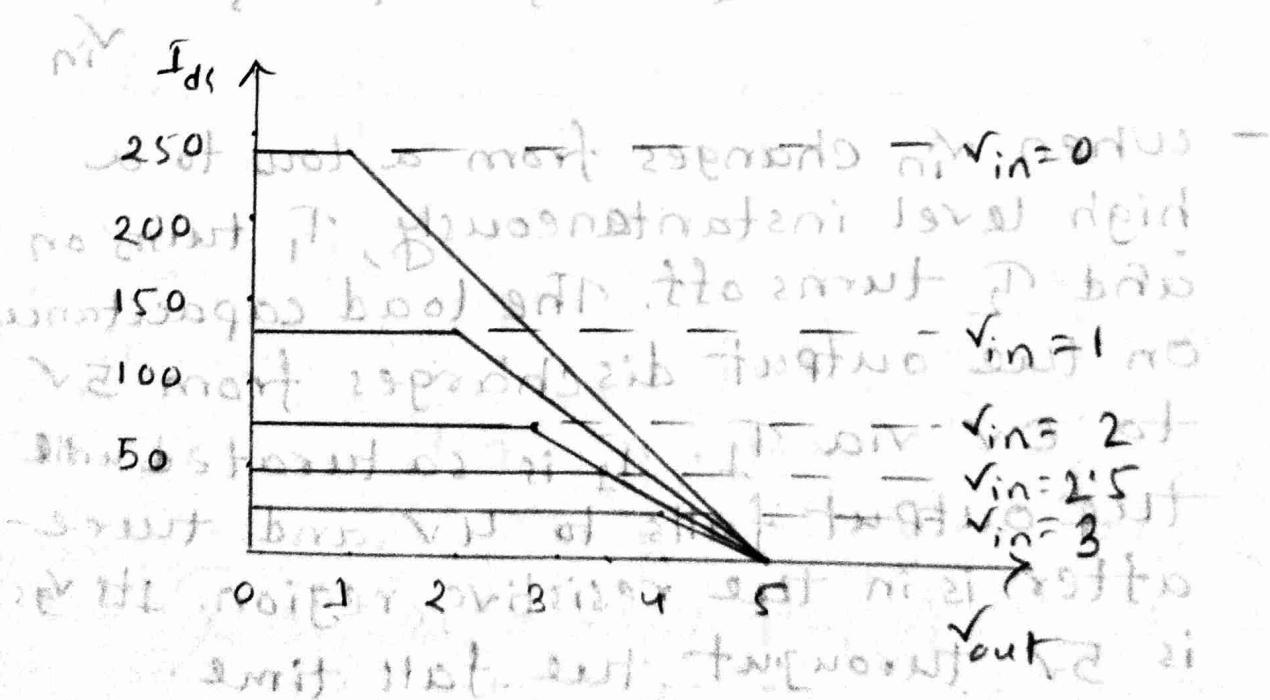
$$\frac{w_2}{L_L} = \gamma, \frac{e\mu n}{D} = 15 \mu A/V^2$$

Pinch off occurs when  $V_{SD} = V_{SG} - V_{TP} = V_{SG} - 1$

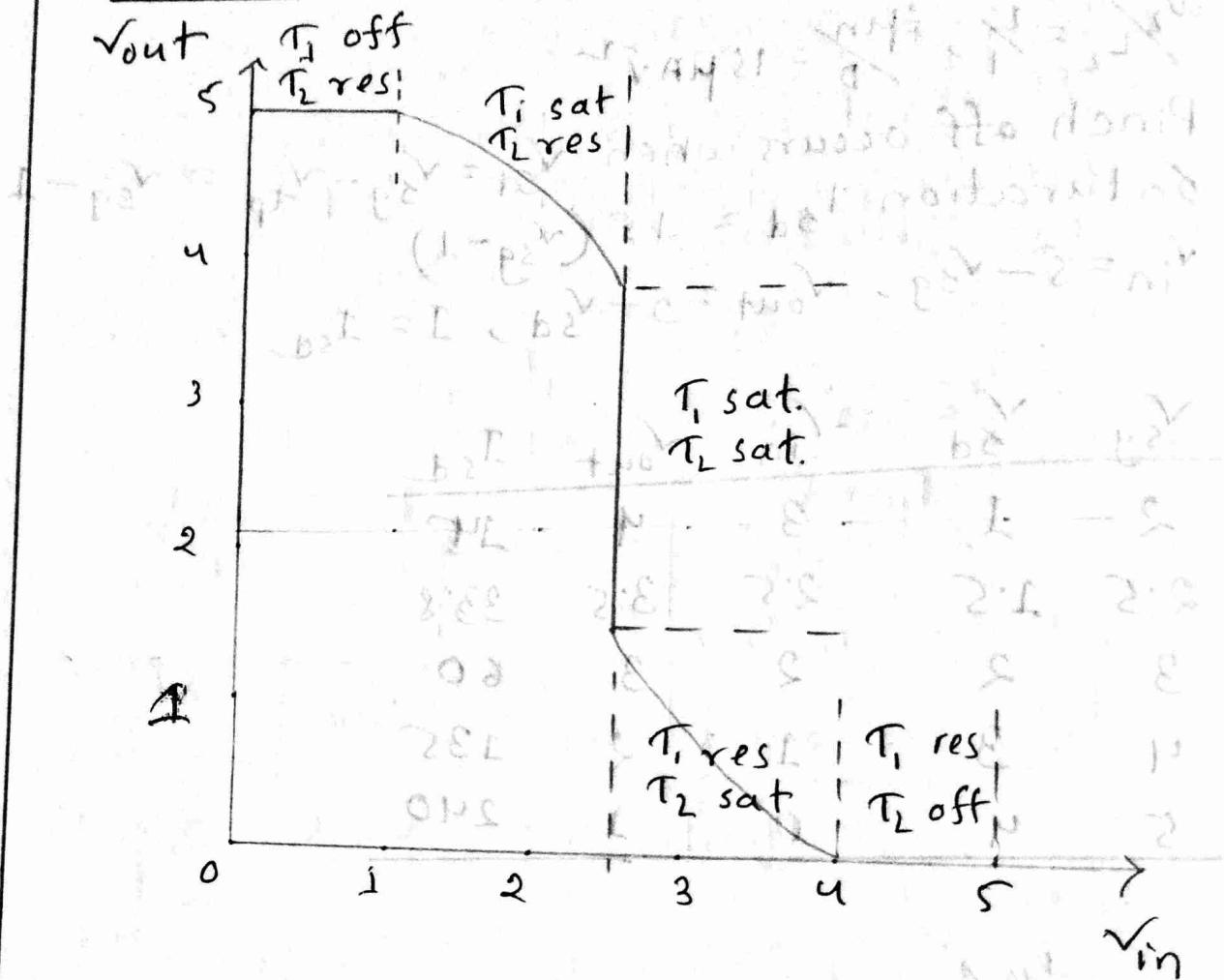
Saturation  $I_{SD} = 15(V_{SG} - 1)$

$$V_{in} = 5 - V_{SG}, V_{out} = 5 - V_{SD}, I = I_{SD}$$

$V_{SG}$	$V_{SD}$	$V_{in}$	$V_{out}$	$I_{SD}$
2	1	3	4	15
2.5	1.5	2.5	3.5	33.8
3	2	2	3	60
4	3	1.5	2	135
5	4	0	1	240



## \* Transfer Characteristics:



- When  $V_{in}$  changes from a low to a high level instantaneously,  $T_1$  turns on and  $T_2$  turns off. The load capacitance to ground via  $T_1$  discharges the output from  $5V$  to  $4V$ .  $T_1$  is saturated until after  $V_{in}$  is in the resistive region. Its  $V_{GS}$  is  $5V$  throughout the fall time.

- When  $v_{in}$  changes from a high to low instantaneously,  $T_1$  turns off and  $T_2$  turns on. The load capacitance on the output charges from 0V to 5V via  $T_2$ . The load capacitance on the output During the rise,  $T_2$  is saturated until the output reaches 1V and thereafter in the resistive mode.  $v_{gs}$  of  $T_2$  is 5V throughout the output rise.

- From the equations of saturated current

$$I_{gs} = \frac{EMn}{D} \cdot \frac{w_1}{L_1} (v_{gs} - v_{te})^{\gamma} \quad \approx T_1$$

$$= \frac{EMn}{D} \cdot \frac{w_1}{L_1} (5-1)^{\gamma}$$

$$= \frac{EMn}{D} \cdot \frac{w_1}{L_1} \quad \text{Using } v_{te} = 1V \quad (\text{A})$$

$$I_{sg} = \frac{EMp}{D} \cdot \frac{w_2}{L_2} \quad \approx T_2$$

$$\therefore I_{gs} = I_{sg}$$

$$\Rightarrow \frac{w_1/L_1}{w_2/L_2} = \frac{\mu_p}{\mu_n} = \frac{\mu_p}{2\mu_p}$$

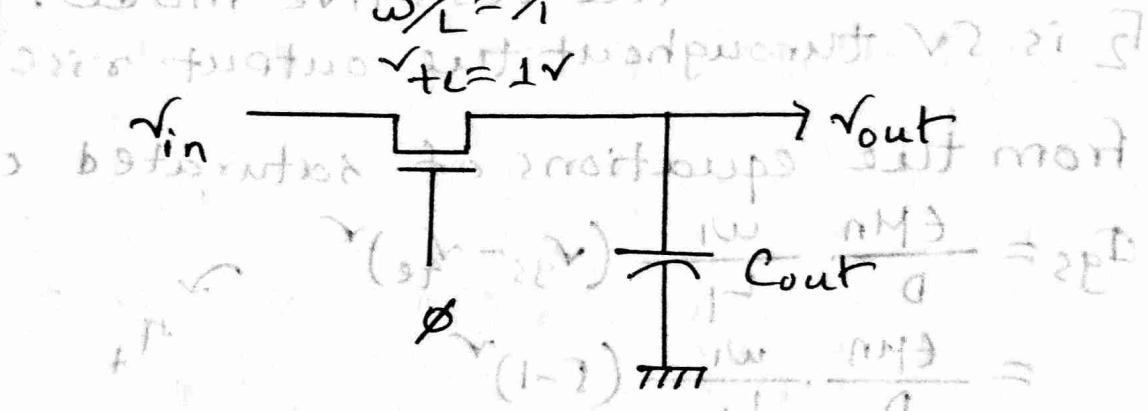
The mobility of holes is half of the electrons

$$\therefore \frac{w_1/L_1}{w_2/L_2} = 1/2$$

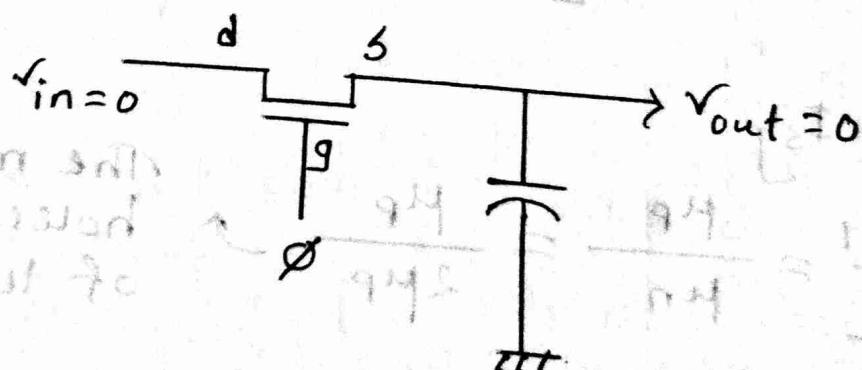
$$\omega_1/L_1 = \gamma_1 \quad \omega_2/L_2 = 2\gamma_1$$

## NMOS Pass Transistor:

↳ The device acts as a voltage controlled switch, allowing the device's input switch, allowing the device's input to be selectively transmitted to its output.

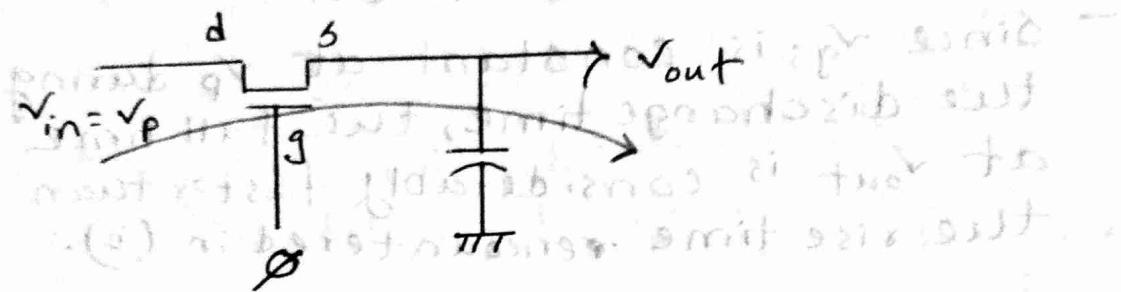


(a)  $V_{in} = 0V$ ,  $V_{out} = 0V$  initially



- No current flows through the device as  $V_{ds} = 0$ .

(b)  $v_{in} = v_p$  and initial  $v_{out} = 0$ :  
Initial output voltage is zero.

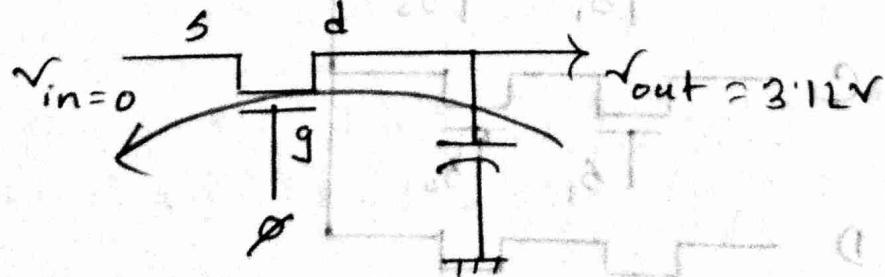


- Current flows from  $v_{in}$  to  $v_{out}$ , causing  $v_{out}$  to rise as  $C_{out}$  is charged. Initially  $v_{gs} = v_p$ , but as the output rises,  $v_{gs}$  drops and the rise at  $v_{out}$  is halted when  $v_{gs} - v_{te} = 0V$ .
- Because of body effect,  $v_{out}$  only rises to  $3.12V$ , if  $v_p = 5V$ .

(c)  $v_{in} = v_p$ ,  $v_{out} = v_p - v_{te}$ :

- No current flows as  $v_{gs} - v_{te} = 0$ .  $v_{out}$  remains at  $v_p - v_{te}$ .

(d)  $v_{in} = 0V$ , initial  $v_{out} = v_p - v_{te}$ :

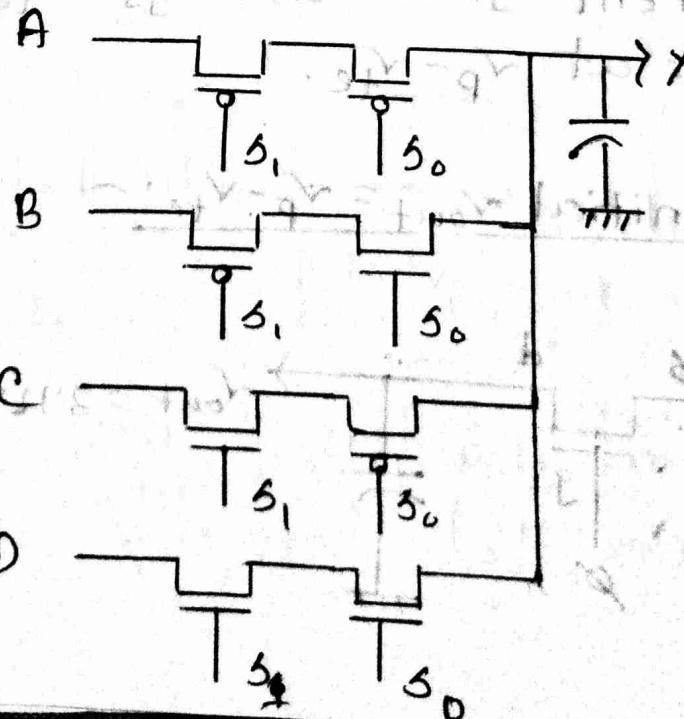


- Current flows from  $V_{out}$  to  $V_{in}$  causing  $V_{out}$  to discharge to 0V.
- Since  $V_{GS}$  is constant at  $V_p$  during the discharge time, the fall time at  $V_{out}$  is considerably faster than the rise time encountered in (b).

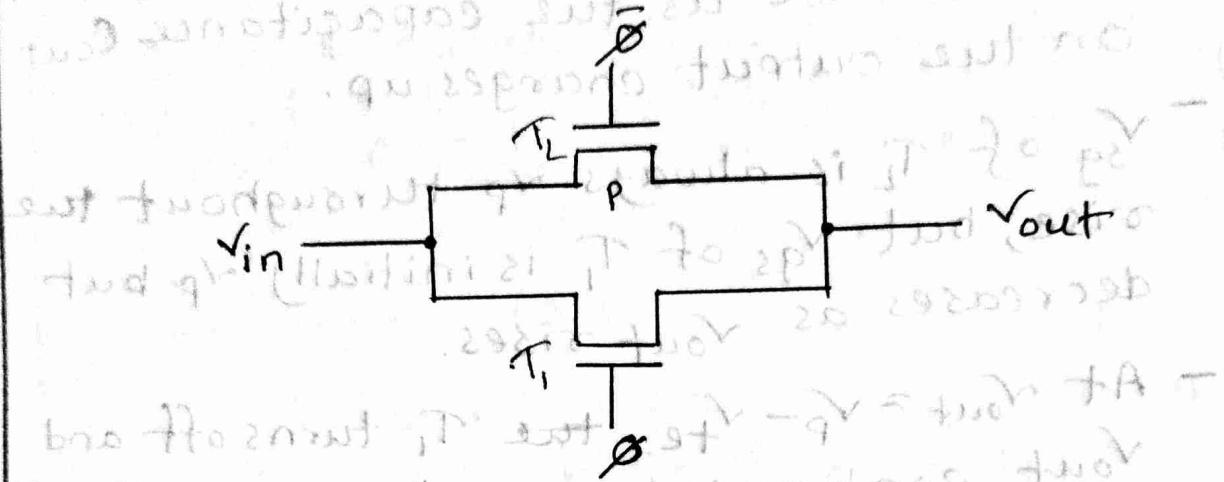
### Pass transistor 4-to-1 MUX:

$S_1, S_0$  Output

A	0	C
1	1	D



## Q1 CMOS Pass Gate



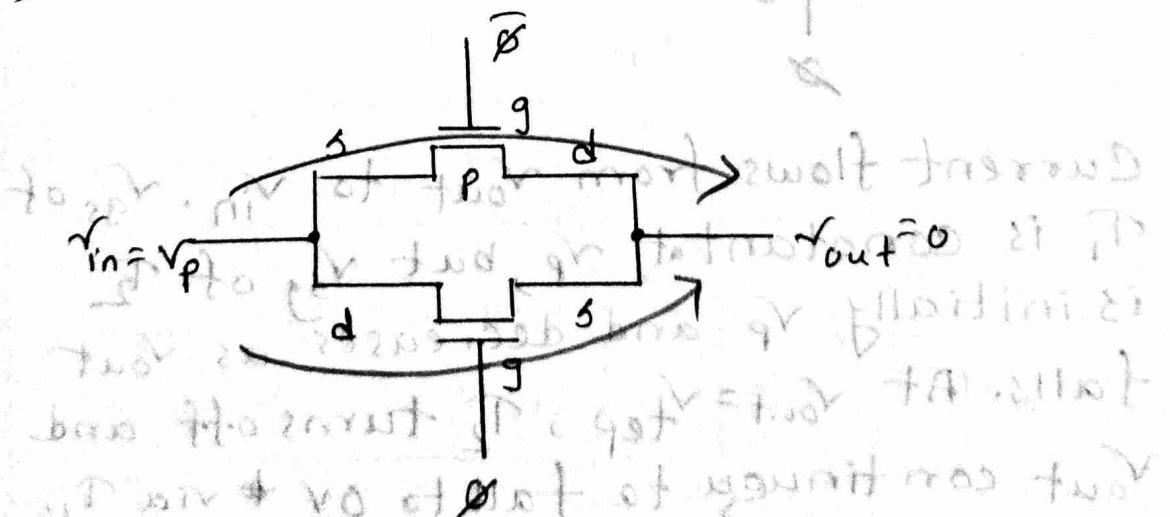
(a)  $V_{in} = 0V$ , initial  $V_{out} = 0V$ :

- No current flows.

(b)  $V_{in} = V_p$ , initial  $V_{out} = V_p$ :

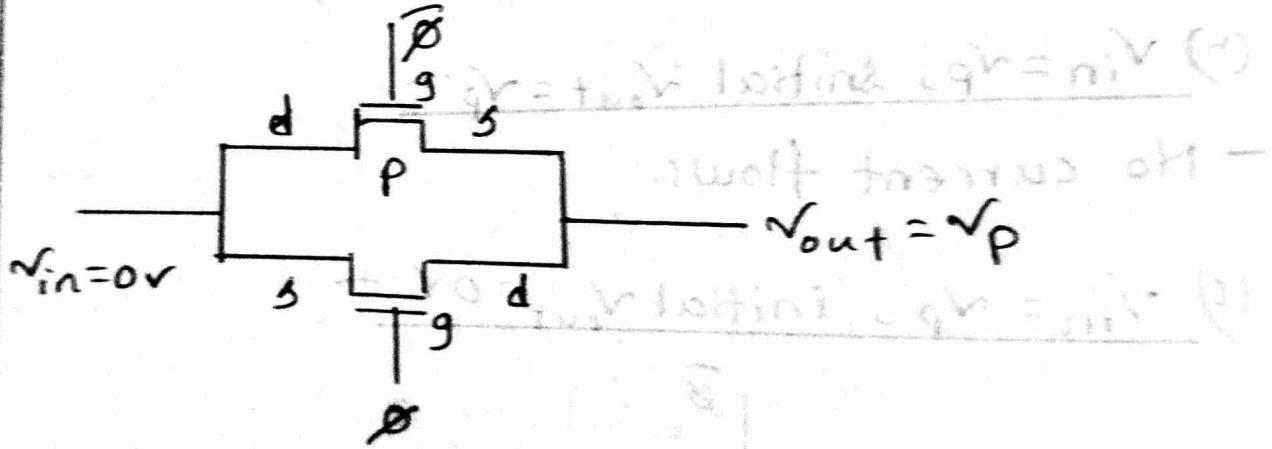
- No current flows.

(c)  $V_{in} = V_p$ , initial  $V_{out} = 0V$ :



- Current flows from  $v_{in}$  to  $v_{out}$  causing  $v_{out}$  to rise as the capacitance  $C_{out}$  on the output changes up.
- $v_{sg}$  of  $T_2$  is always  $\sqrt{p}$  throughout the rise, but  $v_{gs}$  of  $T_1$  is initially  $\sqrt{p}$  but decreases as  $v_{out}$  rises.
- At  $v_{out} = \sqrt{p} - v_{t_{ex}}$ ,  $T_1$  turns off and  $v_{out}$  continues to rise to  $\sqrt{p}$  via  $T_2$ .

(d)  $v_{in} = 0V$ , initial  $v_{out} = \sqrt{p}$ : C turns off

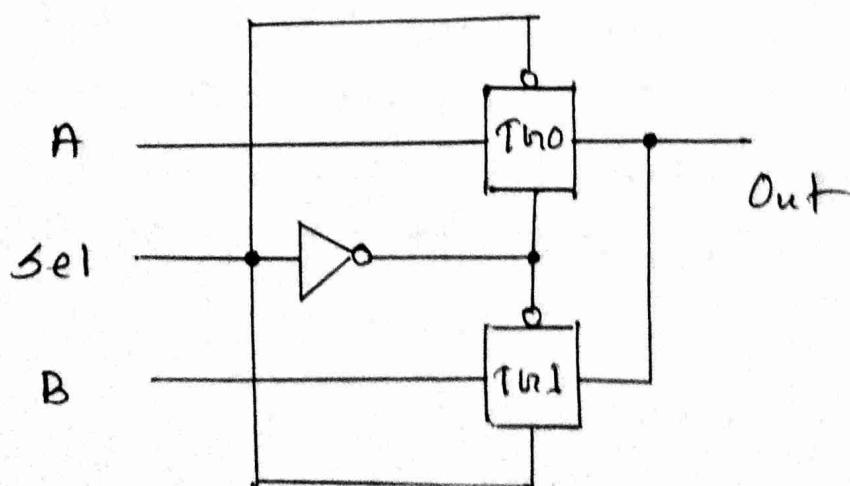
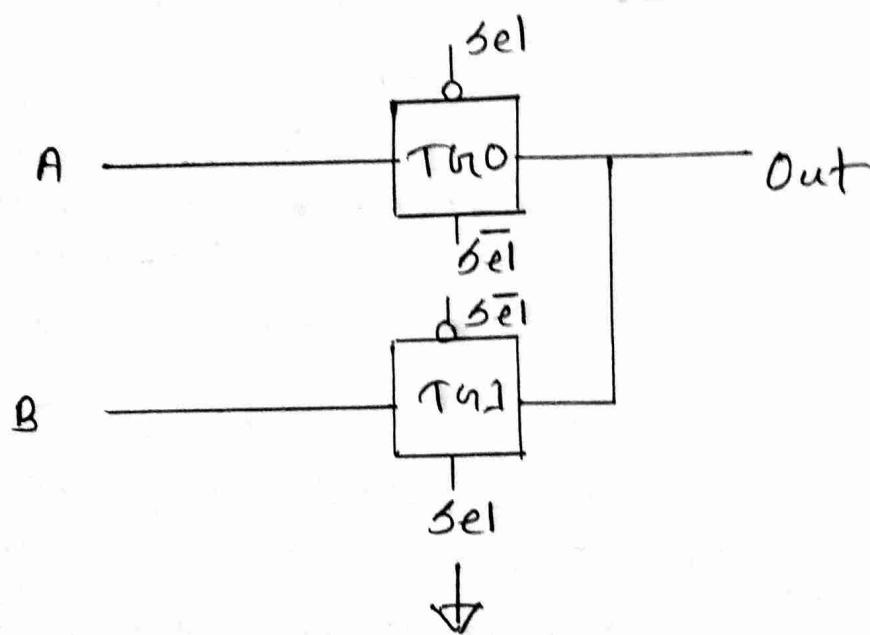


- Current flows from  $v_{out}$  to  $v_{in}$ .  $v_{gs}$  of  $T_1$  is constant at  $\sqrt{p}$ , but  $v_{sg}$  of  $T_2$  falls. At  $v_{out} = \sqrt{v_{t_{ex}}}$ ,  $T_2$  turns off and  $v_{out}$  continues to fall to  $0V$  via  $T_1$ .

\* CMOS Logic with Pass / Transmission Gate:

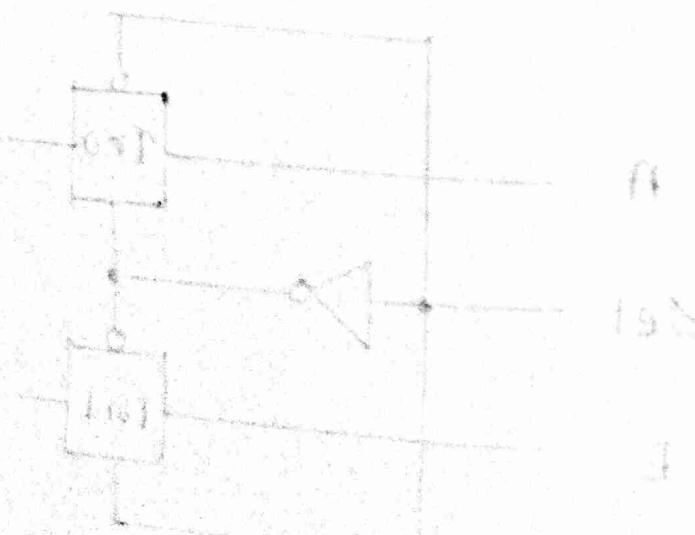
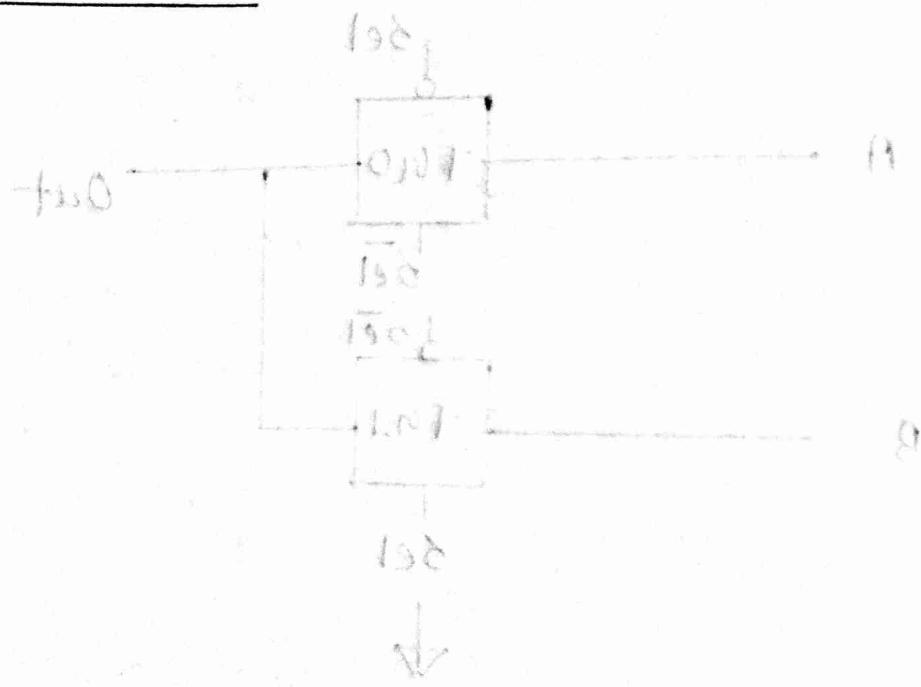
- 2-to-1 multiplexer with Tg

Sel	Output
0	A
1	B



- XOR gate with Th=

A	B	F
0	0	0
0	1	1
1	0	1
1	1	0



## Buffer Circuits

many **Lecture 5. pdf** + **Book**

- Some gate outputs in a design, for example clock signals, need to be connected to a large number of gates and thus drive a large capacitive load.

$$\text{edge time} \propto \frac{C_{\text{out}}}{w/L}$$

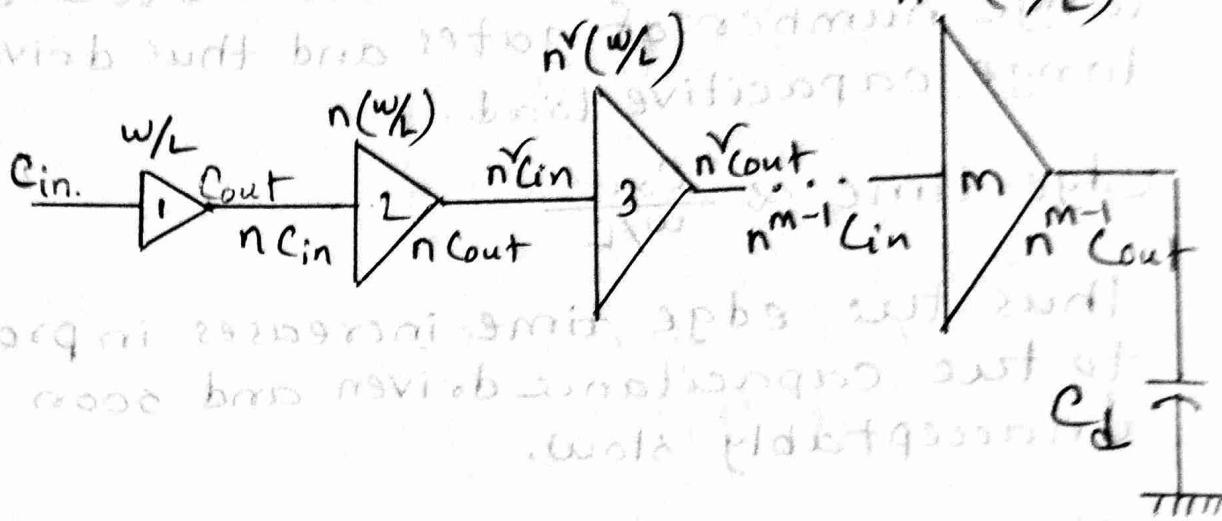
Thus the edge time increases in proportion to the capacitance driven and soon becomes unacceptably slow.

- This speed loss can be avoided by suitably increasing the width-to-length ratio of all transistors in the driving gate. This increases its current capability. Unfortunately this increase in the dimensions of the driver gate causes its input capacitance to rise. This in turn increases the loading of its preceding gate, causing an unacceptable loss of speed here.

now repeat for next question

for 3 marks

— For this reasons, a large capacitive load cannot be directly driven from a standard gate output. Instead, a buffer chain is used.



~~for other w/L =  $\frac{C_d}{C_{in}}$~~

$$\text{for other } \frac{C_d}{C_{in}} = n^m$$

$$\Rightarrow n^m = \frac{C_d}{C_{in}}$$

$$\Rightarrow m \ln n = \ln \frac{C_d}{C_{in}}$$

$$\Rightarrow m = \frac{\ln(C_d/C_{in})}{\ln n}$$

— If  $t_{min}$  is average delay through each inverter, then delay through each stage =  $n t_{min}$

- Total delay,  $T_{\text{tot}} = m n t_{\min}$

$$= \frac{n}{I_{\min}} t_{\min} \ln \frac{C_d}{C_{in}}$$

- Optimal stage ratio -

$$\frac{d}{dn} T_{\text{tot}} = 0$$

$$\Rightarrow \frac{d}{dn} \frac{n}{I_{\min}} t_{\min} \ln \frac{C_d}{C_{in}} = 0$$

$$\Rightarrow \underbrace{t_{\min} \ln \frac{C_d}{C_{in}}}_{\neq 0}, \frac{d}{dn} \frac{n}{I_{\min}} = 0$$

$$\downarrow \neq 0$$

$$\Rightarrow \frac{1 + I_{\min}}{(I_{\min})^2} = 0$$

$$\Rightarrow 1 + I_{\min} = 0$$

$$\Rightarrow I_{\min} = 1$$

$$\Rightarrow I_{\min} = I_n e$$

$$\therefore n = e$$

$\hookrightarrow$  Driver sites are exponentially tapered.

- Optimal delay,  $T_{\text{opt}} = e t_{\min} \ln \frac{C_d}{C_{in}}$

$$\begin{aligned} \frac{d}{dn} \frac{n}{I_{\min}} \\ = \frac{I_{\min} + n \cdot 1/n}{(I_{\min})^2} \\ = \frac{1 + I_{\min}}{(I_{\min})^2} \end{aligned}$$