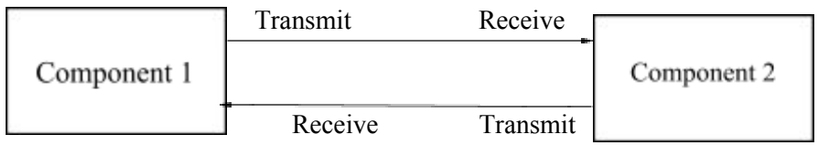
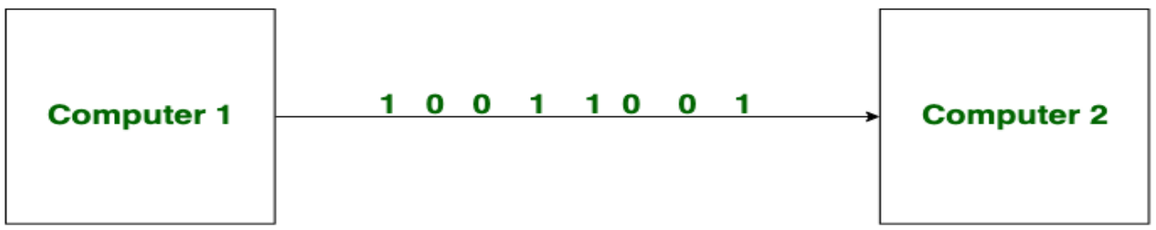
8251 USART (Programmable Communication Interface)

Communication: Communication means transmission of data.



Types of Transmission:

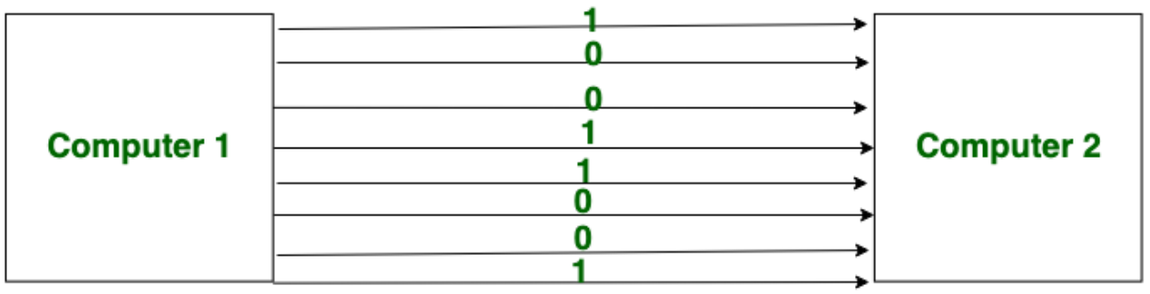
Serial Transmission of data:



Serial Transmission

- One bit at a time is sent.
- Single communication wire is used.
- Low cost.
- Suitable for long distance communication.
- Comparatively slower.
- A refence signal is used to check the received data is errorless or not.

Parallel Transmission of data:



Parallel Transmission

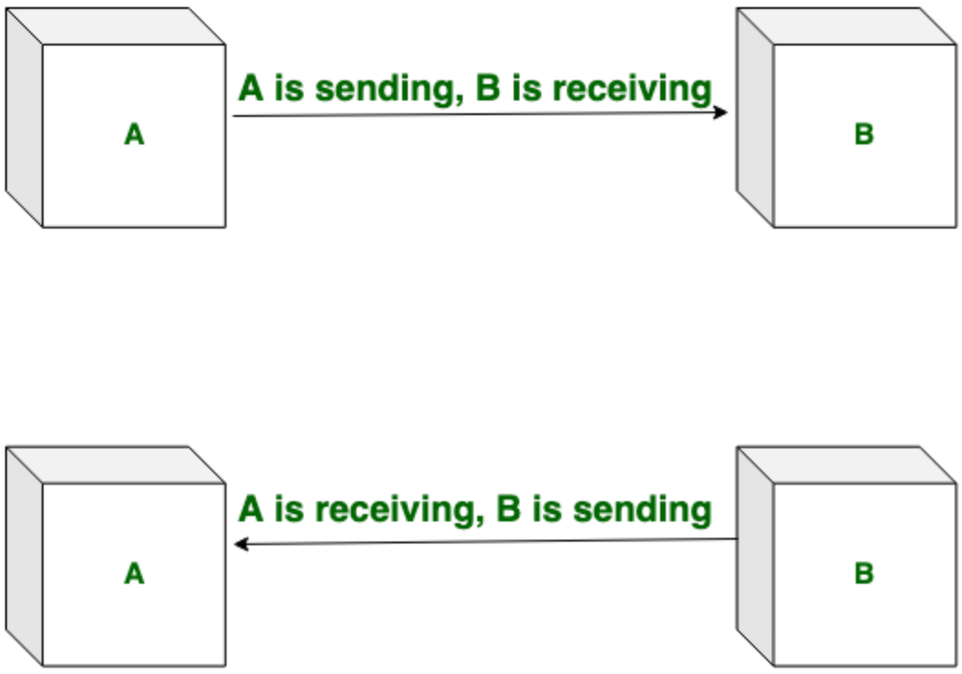
- All bits are transmitted simultaneously.
- Multiple communication channel is used.
- High cost.
- Suitable for short distance communication.
- A refence signal is used to check the received data is errorless or not.

Serial Data Transmission Modes:

Simplex:
In simplex mode, Sender can send the data but that sender can't receive the data. It is a unidirectional communication. Example of simplex mode are: Keyboard and monitor.

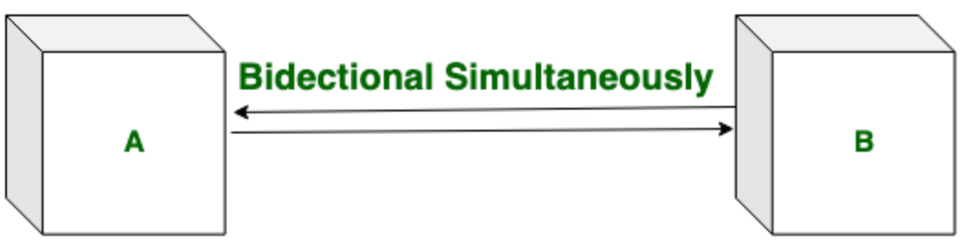
Simplex mode

Half-duplex:
In half duplex mode, Sender can send the data and also can receive the data but one at a time. It is two-way directional communication but one at a time. Example of half duplex mode is: Walkie-Talkies.



Half duplex mode

Fullduplex:
In full duplex mode, Sender can send the data and also can receive the data simultaneously. It is two-way directional communication simultaneously. Example of half duplex mode is: Telephone.



Full duplex mode

Serial Data Transmission Schemes:

- Serial communication requires co-ordination between sender and receiver.
- When to start the transmission and when to end it.
- When one particular bit or byte ends and another begins.
- When the receiver capacity has been exceeded.

For this, there is need a synchronization between sender and receiver.

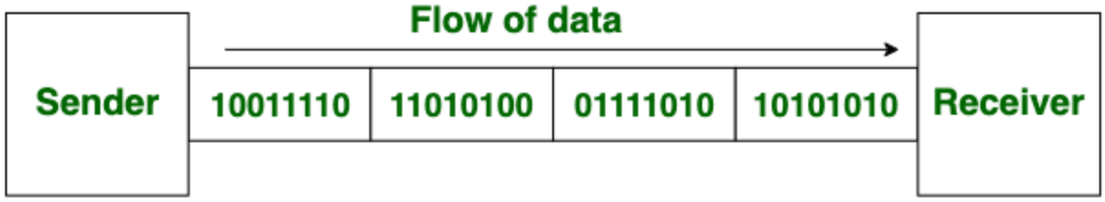
Synchronization: A protocol defines the specific methods of co-ordination or communication between sender and receiver is synchronization.

Types of serial data transmission schemes:

Synchronous Transmission:

- In Synchronous Transmission, data is sent in form of blocks or frames.

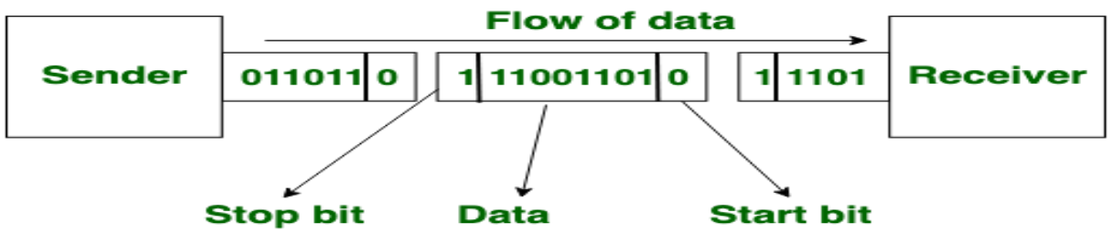
- This transmission is the full duplex type.
- Between sender and receiver the synchronization is compulsory.
- Synchronization is achieved by sending the sync bits.
- It is more efficient and more reliable than asynchronous transmission to transfer the large amount of data.
- Examples: Video conferencing. Most network protocols (such as Ethernet, SONET, Token Ring) use synchronous transmission.



Synchronous Transmission

Asynchronous Transmission:

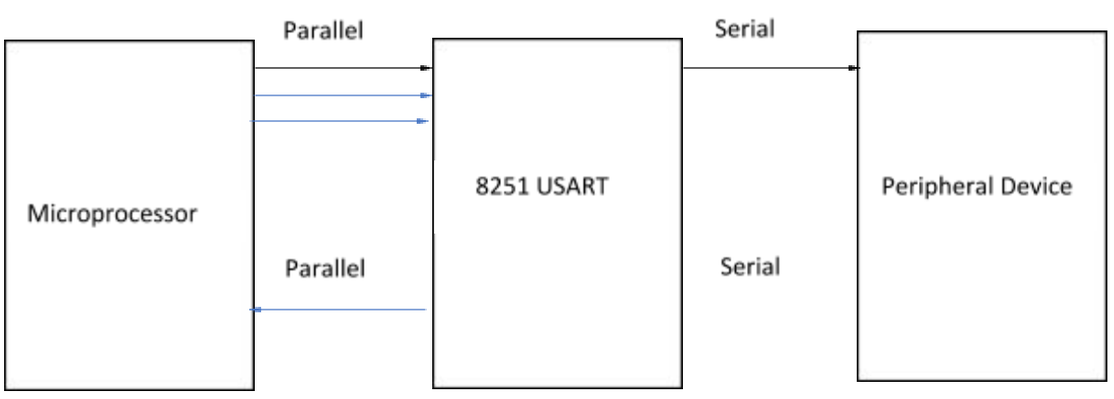
- In Asynchronous Transmission, data is sent in form of byte or character.
- This transmission is the half duplex type transmission.
- In this transmission one start bit and two stop bits are added with data.
- Start bit 0 and stop bits are 1.
- It does not require synchronization.
- Examples: Emails.



Asynchronous Transmission

Needed of 8251 USART:

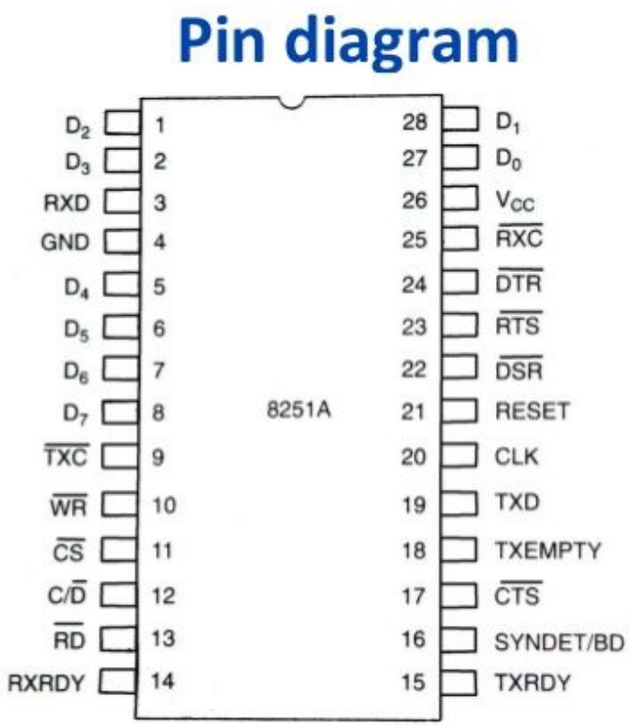
- When the microprocessor communicates with the peripheral devices then it sends the data into serial form.
- But the problem is that, it stores or computes the data into parallel form.
- In terms of transmitting, microprocessor needs to convert the parallel data into serial form and transmit it.
- In terms of receiving it receives the data into serial form and convert it into parallel form to store it.
- So, all the process indicates that microprocessor needs to perform the conversion operation all the time when it communicates with the peripheral devices.
- So, we need to use a device which will perform the conversion operation and provide an interface between microprocessor and peripheral devices.



8251 universal synchronous asynchronous receiver transmitter (USART) acts as a mediator between microprocessor and peripheral to transmit serial data into parallel form and vice versa.

1. It takes data serially from peripheral (outside devices) and converts into parallel data.
2. After converting the data into parallel form, it transmits it to the CPU.
3. Similarly, it receives parallel data from microprocessor and converts it into serial form.
4. After converting data into serial form, it transmits it to outside device (peripheral).

8251 USART Pin Diagram



D0 to D7 (l/O terminal)
This is bi-directional data bus which receive control words and transmits data from the CPU and sends status words and received data to CPU.

RESET (Input terminal)
A "High" on this input forces the 8251 into "reset status."

CLK (Input terminal)
CLK signal is used to generate internal device timing. CLK signal is independent of RXC or TXC. However, the frequency of CLK must be greater than 30 times the RXC and TXC at Synchronous mode and Asynchronous "x1" mode, and must be greater than 5 times at Asynchronous "x16" and "x64" mode.

WR (Write)(Input terminal)
This is the "active low" input terminal which receives a signal for writing transmit data and control words from the CPU into the 8251.

RD (Read)(Input terminal)
This is the "active low" input terminal which receives a signal for reading receive data and status words from the 8251.

C/D (Command/Data) (Input terminal)

This is an input terminal which receives a signal for selecting data or command words and status words when the 8251 is accessed by the CPU. If C/D = low, data will be accessed. If C/D = high, command word or status word will be accessed.

CS (Cheap Select) (Input terminal)
This is the "active low" input terminal which selects the 8251 at low level when the CPU accesses.

TXD (Transmit Data) (output terminal)
This is an output terminal for transmitting data from which serial-converted data is sent out.

TXRDY (Transmit Ready) (output terminal)
This is an output terminal which indicates that the 8251 is ready to accept a transmitted data character.

TXEMPTY (Transmit Empty) (Output terminal)
This is an output terminal which indicates that the 8251 has transmitted all the characters and had no data character.

Note: As the transmitter is disabled by setting CTS "High" or command, data written before disable will be sent out. Then TXD and TXEMPTY will be "High". Even if a data is written after disable, that data is not sent out and TXE will be "High". After the transmitter is enabled, it sent out. (Refer to Timing Chart of Transmitter Control and Flag Timing)

TXC (Transmitter Clock) (Input terminal)
This is a clock input signal which determines the transfer speed of transmitted data. In "synchronous mode," the baud rate will be the same as the frequency of TXC. In "asynchronous mode", it is possible to select the baud rate factor by mode instruction. It can be 1, 1/16 or 1/64 the TXC.

RXD (Receive Data) (input terminal)
This is a terminal which receives serial data.

RXRDY (Receiver Ready) (Output terminal)
This is a terminal which indicates that the 8251 contains a character that is ready to READ.

RXC (Receiver Clock) (Input terminal)
This is a clock input signal which determines the transfer speed of received data. In "synchronous mode," the baud rate is the same as the frequency of RXC. In "asynchronous mode," it is possible to select the baud rate factor by mode instruction. It can be 1, 1/16, 1/64 the RXC.

SYNDET/BD (Input or output terminal)
This is a terminal whose function changes according to mode. In "internal synchronous mode." this terminal is at high level, if sync characters are received and synchronized. If a status word is read, the terminal will be reset. In "external synchronous mode, "this is an input terminal. A "High" on this input forces the 8251 to start receiving data characters.

In "asynchronous mode," this is an output terminal which generates "high level" output upon the detection of a "break" character if receiver data contains a "low-level" space between the stop bits of two continuous characters. The terminal will be reset, if RXD is at high level. After Reset is active, the terminal will be output at low level.

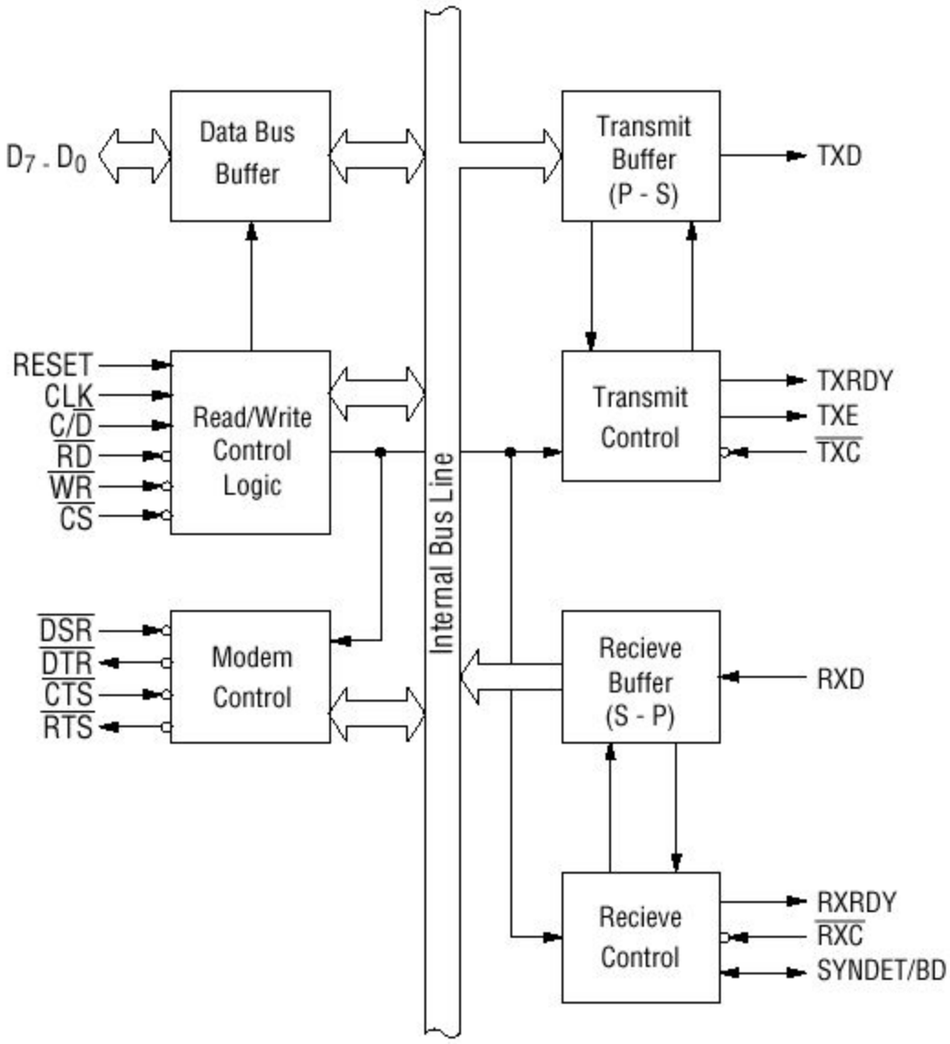
DSR (Data Set Ready) (Input terminal)
This is an input port for MODEM interface. Usually used to test modem conditions such as data set ready.

DTR (Data Transmit Ready) (Output terminal)
This is an output port for MODEM interface. It is possible to set the status of DTR by a command. Which is used for modem control.

CTS (Clear to Send Data) (Input terminal)
This is an input terminal for MODEM interface which is used for controlling a transmit circuit.

RTS (Request to Send Data) (Output terminal)
This is an output port for MODEM interface. It is possible to set the status of RTS by a command. Which is used for modem control.

Block diagram and functional description of 8251 USART:



Data Bus Buffer:

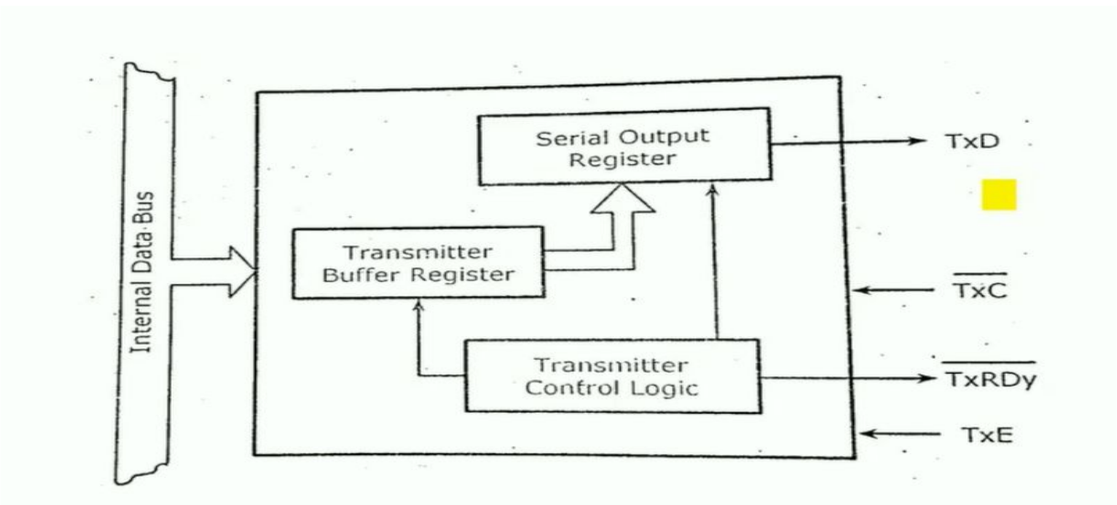
This bidirectional, 8-bit buffer used to interface the 8251A to the system data bus and also used to read or write status, command word or data from or to the 8251A. it contains 8-bit registers which is double buffered.

Read/Write control logic:

- The Read/Write Control logic interfaces the 8251A with microprocessor, determines the functions of the 8251A according to the control word written into its control register and monitors the data flow.
- This section has three registers and they are control register, status register and data buffer.
- C / $\overline{D}$ stands for Command/Data. When command is active high, then control register is selected for writing control word or reading status word.
- When Data is active low, data buffer is selected for read or write operation.
- When the reset is high, it forces 8251A into the idle mode.
- CLK provides clock input for 8251 to communicate with the microprocessor.

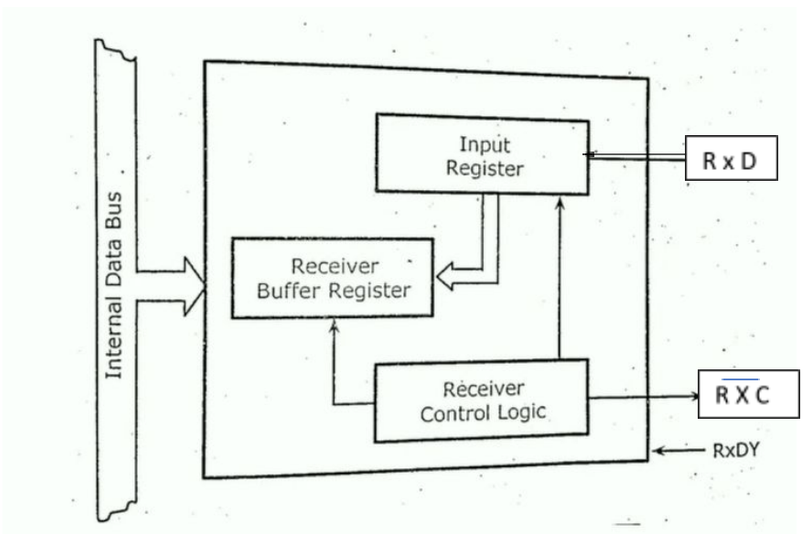
$\overline{CS}$	C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	Operation
1	X	X	X	Invalid
0	0	0	1	data CPU< ----- 8251
0	0	1	0	data CPU ----- > 8251
0	1	0	1	Status word CPU < ----------8251
0	1	1	0	Control word CPU---------- > 8251

Transmitter section:



- The transmitter section accepts parallel data from microprocessor and converts them into serial data.
- The transmitter section is double buffered, it has a buffer register to hold an 8-bit parallel data and another register called output register to convert the parallel data into serial bits.
- When output register is empty, the data is transferred from buffer to output register. Now the processor can again load another data in buffer register.
- If buffer register is empty, then T x RDY is goes to high.
  If output register is empty, then T x EMPTY goes to high.
- The clock signal controls the rate at which the bits are transmitted by the USART.

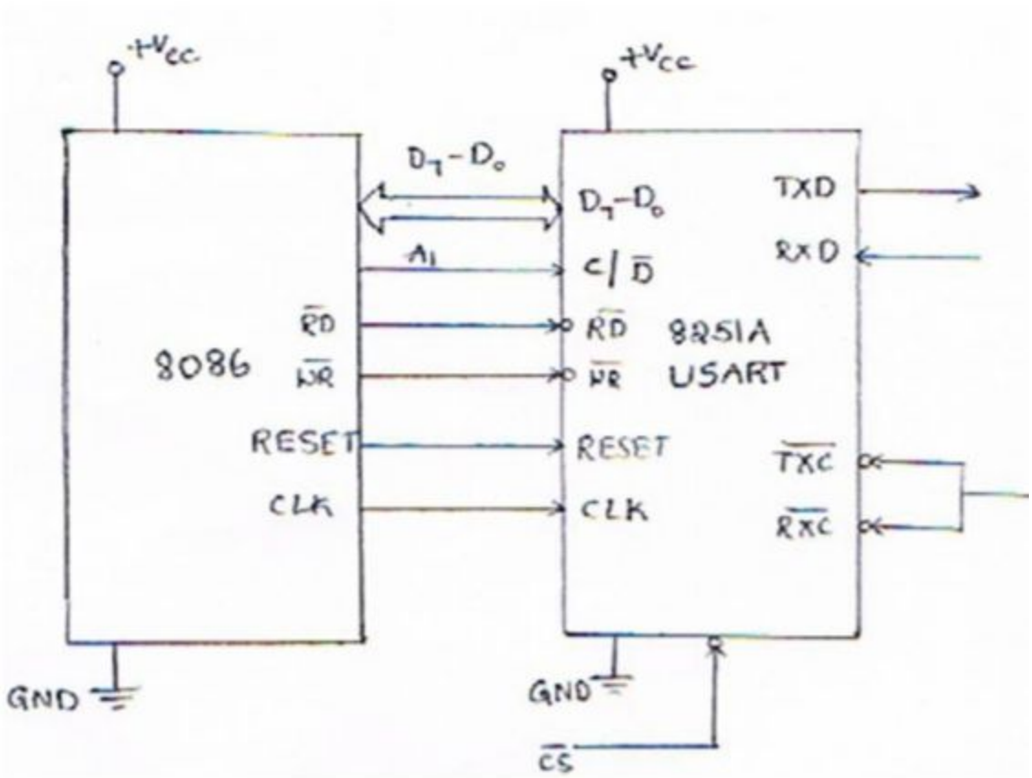
Receiver Section:



- The receiver section accepts serial data and converts them into parallel data.

- The receiver section is double buffered, it has an input register to receive serial data and convert to parallel, and a buffer register to hold the parallel data.
- When the input register loads a parallel data to buffer register, the R x RDY line goes high.
- The clock signal controls the rate at which bits are received by the USART.
- During asynchronous mode, the signal SYNDET/BRKDET will indicate the break in the data transmission. During synchronous mode, the signal SYNDET/BRKDET will indicate the reception of synchronous character.

Interfacing of 8251 USART with 8086 Microprocessor:



Mode Instruction Format of 8251 USART

Microprocessor gives control words to the 8251 through the control register. The control words are of two types:

1. **Mode Instruction**
2. **Command Word**
3. **Status Word**

Mode Instruction: Mode instruction is used to set the function of 8251. When 8251 is reset, then it will go to the idle state by clearing the functionality of each pin as same as initial state. After resetting the 8251, whatever is written in the control register it will be the mode instruction. Mode instruction includes:

- Synchronous / Asynchronous transmission of 8251
- Stop bit length (Asynchronous Mode)
- Character length
- Parity Bit
- Baud rate factor (Asynchronous Mode)

- Internal / External Synchronization (Synchronous Mode)
- No of Sync characters (Synchronous Mode)

Control Word or bit configuration for Mode Instruction in Asynchronous Mode:

D7	D6	D5	D4	D3	D2	D1	D0
S2	S1	EP	PEN	L2	L1	B2	B1

No of Stop Bits

S2	S1	No.
0	0	invalid
0	1	1 bit
1	0	1.5 bit
1	1	2 bits

Even Parity Generator

1	Even Parity
0	Odd Parity

Parity Enable

1	Enable
0	Disable

Character Length

L2	L1	No of bits
0	0	5
0	1	6
1	0	7
1	1	8

Baud Rate Factor

B2	B1	Mode
0	0	Synchronous Mode
0	1	‘1’ x of clock frequency (Asynchronous Mode)
1	0	‘16’ x of clock frequency (Asynchronous Mode)
1	1	‘64’ x clock frequency (Asynchronous Mode)

Control Word or bit configuration for Mode Instruction in Synchronous Mode:

D7	D6	D5	D4	D3	D2	D1	D0
SCS	ESD	EP	PEN	L2	L1	0	0

Single Character Sync

1	Single Character
0	Double Character

External Sync Detect

1	SYNDET is an output
0	SYNDET is an output

Even Parity Generator

1	Even Parity
0	Odd Parity

Parity Enable

1	Enable
0	Disable

Character Length

L2	L1	No of bits
0	0	5
0	1	6
1	0	7
1	1	8

Command Word Format of 8251 USART

Command is used for setting the operation of the 8251. Items to be set by command are as follows:

• Transmit Enable/Disable

• Receive Enable/Disable

• DTR, RTS Output of data.

• Resetting of error flag.

• Sending to break characters

• Internal resetting

• Hunt mode (synchronous mode)

D7	D6	D5	D4	D3	D2	D1	D0
EH	IR	RTS	ER	SBRK	R x EN	DTR	T x EN
Enter on Hunt Mode 1 - Start Searching for Sync Characters	**Internal Reset** 1 Reset of 8251	**Request to Send** 1 RTS active Low signal so, RTS=0 and active 0 RTS=1 and inactive	**Error Reset** 1 Reset of error flags	**Send Break Character** 1 It forces TxD to be low and break characters are sent 0 Normal Operation	**Receiver Enable** 1 Enable 0 Disable	**Data Transmit Ready** 1 DTR active Low signal so, DTR=0 and active 0 DTR=1 and inactive	**Transmit Enable** 1 Enable 0 Disable

Status Word Format of 8251 USART

D7	D6	D5	D4	D3	D2	D1	D0
DSR	SYNDET/BRKDET	FE	OE	PE	TxRMPTY	RxRDY	TxRDY

D0 (TxRDY): When TxRDY is high then, 8251 will be ready to accept transmitted data character. When D0 bit is 1, then TxRDY will active.

D1 (RxRDY): When RxRDY is high then, 8251 will be ready to receive serial data from I/O. When D1 bit is 1, RxRDY will active.

D2 (TxEMPTY): When all the characters are transmitted then TxEMPTY will go high. When, D2 bit is 1, TxEMPTY will active.

D3 PE (Parity Error): If parity error is detected then the PE will be high or 1.

D4 OE (Overrun Error): When the microprocessor does not read a character before the next character available. Then OE will be high or 1.

D5 FE (Framing Error): When a valid stop bit is not detected at the end of every character. Then FE will be high or 1.

D6 (SYNDET/BRKDET): In synchronous mode, when sync bit is detected then SYNDET will be high. In asynchronous mode, when stop bits are detected the BRKDET will be high.

D7 DSR (Data Set Ready): DSR is an active low signal, so if D7 is 1 then DSR=0 and it is active. If D7 is 0 then DSR=1 and it is inactive.