Heaven's Light Is Our Guide

RAJSHAHIUNIVERSITY OF ENGINEERING & TECHNOLOGY
DEPARTMENT OF COMPUTER SCIENCE &ENGINEERING
3rd Year Even Semester Examination 2019

COURSE NO: CSE 3203 COURSE TITLE: **Computer Architecture and Design**

FULL MARKS: 72 TIME: 3 HRS

N.B. (i) Answer any **SIX** questions taking any **THREE** from each section.
(ii) Figures in the right margin indicate full marks.
(iii) Use separate answer script for each section.

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SECTION : A

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			Marks
Q.1.	(a)	What is Von-Neumann architecture? Explain how instruction is executed in Von-Neumann architecture step by step.	3 2/3
4/5	(b)	How do hardware engineers design and implement a real life CPU? Explain with figure.	4 1
	(c)	Why do hardware engineers use Hardware Description Language (HDL) in their daily job? Implement a half subtractor in Verilog HDL along with a test bench.	5 1
Q.2.		Consider following binary numbers, A=11, B=10,C=111	
	(a)	Draw an unsigned subtractor which can perform SUB A, B (A-B) instruction.	3
	(b)	Draw an unsigned divider which can perform DIV A, B (A/B) instruction.	3
	(c)	Draw a booth multiplier which can perform MUL B,C (BxC) instruction.	6
Q.3.	(a)	Show the memory hierarchy with a suitable diagram.Explain the purposes of caches. What must be the minimum hit ratio that justifies the purposes of using caches?	4 3/4
8/12	(b)	How to take advantage of locality of caches by increasing the block size? Write the basic cache algorithm.	4 2/4
	(c)	Explain the working principle of direct mapped cache with suitable example.	4 3/4
Q.4.	(a)	Explain IEEE-754 single precision and double precision floating point representation system.	2 2/2
12/12	(b)	Explain the purpose of bias exponent. Write the steps of representing floating points.	4 4/4
	(c)	Represent -26.625_{10} using the IEEE 754 single precision floating point representation system.	6 6/6

SECTION : B

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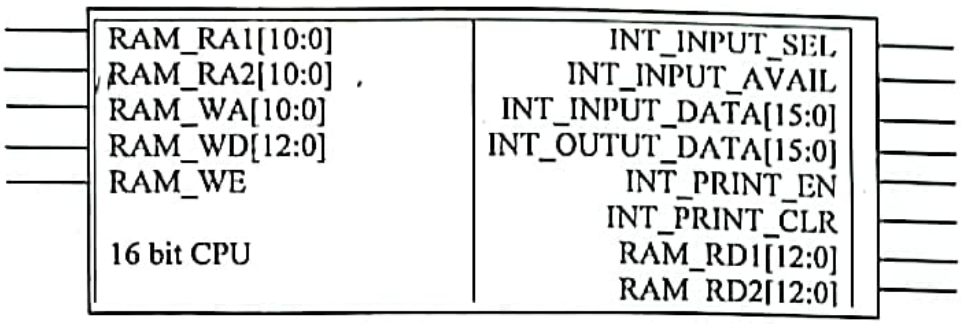
Q.5.	(a)	Explain the role of HDD, RAM, Cache memory and Register in memory hierarchy.	3
	(b)	Draw RAM based on the following configurations:	
		i) 4x4 RAM with one read and one write operations.	5
		ii) 2x4 RAM with two write operations. Same memory location cannot be written at the same time.	4
Q.6.	(a)	Derive the simplified logical expression of the 1-bit full adder circuit. Draw the diagram of combined 4 bit parallel adder and subtractor.	4 3/4
9/12	(b)	Show each step for calculating the product of the two numbers, 6_{10} and -4_{10} using Booth's algorithm.	4 4/4
	(c)	Design a 4 bit barrel shifter using 4 to 1 channel multiplexers and also explain the working principle.	4 2/4
Q.7.	(a)	What is interrupt? What are the differences between software interrupt and hardware interrupt?	2 1/2
	(b)	Write down software interrupt and hardware interrupt functions in assembly for output operation where software interrupt can accept multiple output values which can be sent to hardware interrupt to output values one at a time. Pseudocode is given bellow:	3 1/3
2/5			

```
Push all the output values as parameters to STACK
Push no. of parameters
CALL SOFTWARE_INT
#Inside SOFTWARE_INT
#All output values will be popped one at a time
#and will be sent to HARDWARE_INT
```

	(c)	Consider following CPU chip:	7



(i) Connect CPU chip with RAM chip, connect 16 switches, to input port and 8 LEDs to output port of CPU.

(ii) Write down assembly program so that AND operation can be performed between 1st half of 16 switches and second half of 16 switches and 8 LEDs can be used to provide output.

Q.8. (a) Define pipelining. Explain data hazard and control hazard with example. 4 2/4

(b) Find data hazard and control hazard from following code snippet: 4 1/2

```
XOR R1,R1
XOR R2,R2
ADD R1,5
CMP R1,R2
JL LABEL
```

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Use pipelining diagram to show how hazards will be avoided if stall strategy is used.

(c) Define parallel processing. Explain Flynn Taxonomy. 4 3/4

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