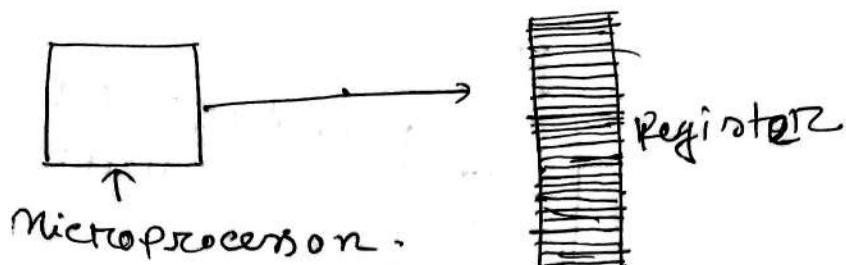


101

CSB - 310
BP

2A day

05-02-2018



→ Register microprocessor is smart embedded 2MIPS

Register → AX, BX, CX, DX.

16 bit



AX (16bit) { 8 bit high byte : AH
8 bit low byte : AL

1. Assembly Language programming & organization of IBM PC

→ Ytha Yee

→ Charles Marut

2. The intel microprocessor

→ Barry Brey

203

CSE - 3109

BP

2nd day

07.02.2018

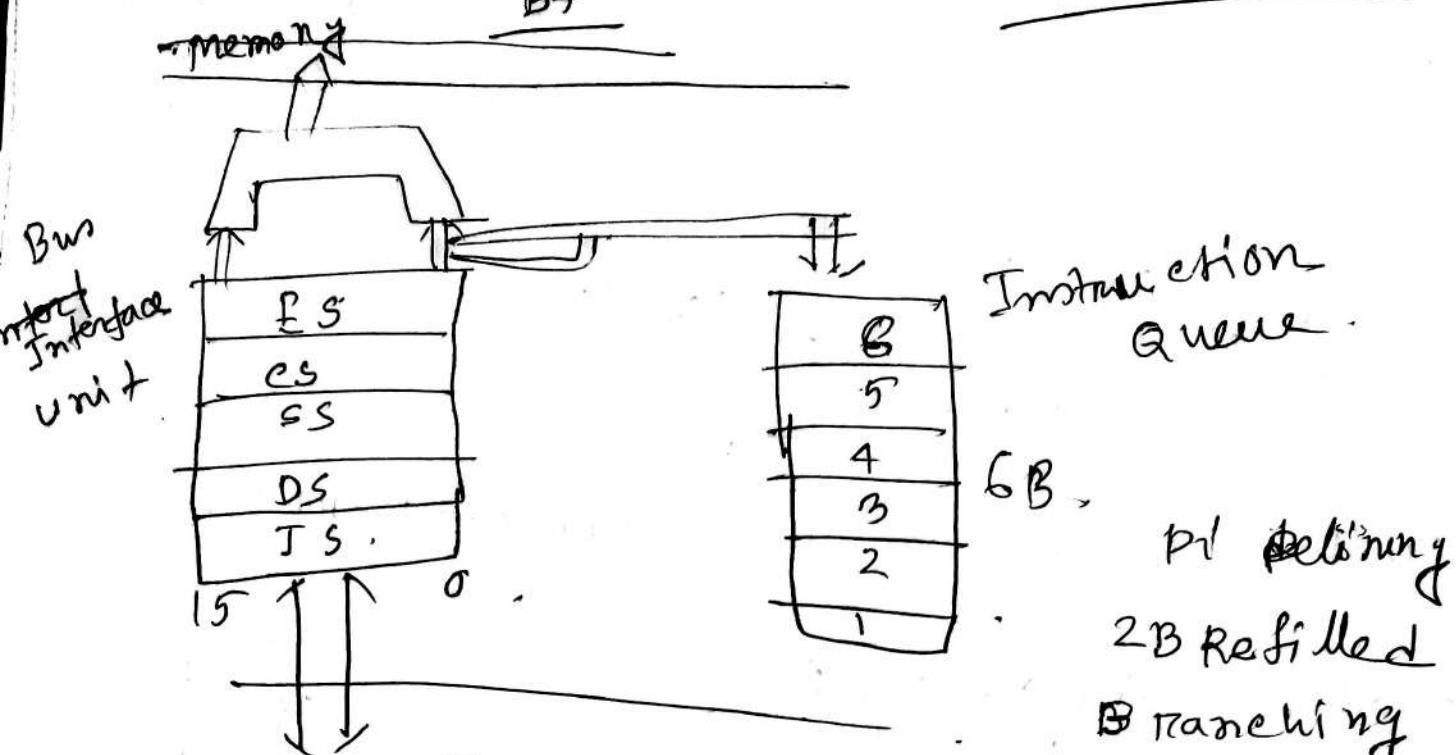


Fig-1

8086 → 16-bit Microprocessor

8088 → 8-Bit Version

Bus → It is generally used to transfer data from one to another

Address bus
Data bus
Control bus

→ 3 Types of Buses

Different microprocessor's bus size vary like

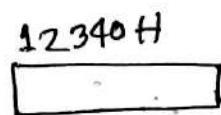
For figure-1

Address bus → 20 bit
Data bus → 16 bit

→ A For Address \rightarrow 20 bit we can use memory ~~20~~₂ 20.

ES → Extra Segment }
CS → code " } 4 type of Segment
SS → Stack "
DS → Data "

B ES, CS, SS, DS → One type of register.

 \Rightarrow code segment + first byte of address

12340H \rightarrow 1234H = (segment address)

Segment : offset .

1234H = 0000H

\rightarrow Segment \times 10 + offset . (Logical \rightarrow physical conversion)

Instruction pointer (IP)

IP \rightarrow 16 bit .

\rightarrow code segment \times IP (16 bit data insert + 97) .

Instruction Queue (6 byte)

\rightarrow Address of instruction point the first IQ to me ,

Q1 Why microprocessor doesn't delay ?

Pi Pending \rightarrow get ready data for next stage.

ZB Refilled \rightarrow get refill the after execution of 2 Byte from the queue.

Branching Problem \rightarrow

```
if (    ) {  
    10.  
    2.  
}  
  
→ 6B memory ( 2100 )
```

```
10.  
1.  
else {  
    1.  
    2.  
}  
10.  
}  
  
→ 6B memory ( 2100 )
```

\Rightarrow If condition run normal or else condition - Guard
Then we need to clear if condition data (6 byte)
and reload 6 byte data for else condition.
This is called branching problem.

A Typical Microprocessor's Assembly Language code

- MODEL SMALL
- STACK 100H
- CODE

MAIN PROC .

MAIN ENDP,

END MAIN;

→ code segment.

mainfunction define
me.

→ Here, we write code.

→ /Code model

→ If we insert a decimal value 1101.

Binary value

1101 B.

Hexadecimal value

1ABC H

MOV Destⁿ, Source

ADD Destⁿ, Source

8086 Emulator /]
MASM

→ Here one must be variable and one register
if $\text{MOV Dest}^n = \text{Varz}$, then $\text{Source} = \text{register}$

MOV AX, 2

MOV A, AX

$A = 2$

$A = A + 4 ;$

If we want to operation through register;

MOV Ax, 4.

ADD A, Ax n.

Here will be stored in A.] A=variable

101

CPU-3109
BP

2D day
10.02.2018

DB → B

DW → 2B .

DD → 2W

DQ → 4W

DT → 10B

Var1 DB 20H

Var1 DB ? [→ (For blank variable)]

+ Var1 DB 10H, 20H, 30H
T ↓ ↓ ↑
101H (address) 101H 102H 103H
{ (address) }

SUB D,S .

ADD D,S

70-
78161-

MOV D,S .

XCHG D,S

INC D

DEC D

Interrupt

INT 21h

↳ Microprocessor → interrupt आवृत्ति
Microprocessor → interrupt आवृत्ति

② INT 21h (console input / output &
terminal input / output)

* AH ← 1. (with command AH ← 1 user will give
21h fn call 20 जारी single
character input लिया & AL Q अंगठी)

* AH ← 1. Single character input to AL.

* AH ← 2.

↳ Single character output from DL & copy to AL.

* AH ← 9.

↳ String output from DX

DX should contain the offset of string
to be printed.

write a program Input a character and output the character

• MODEL SMALL

• STACK 100H

① ← • CODE .

MAIN PROC

→ (code)



MAIN

~~MAIN END~~ MOV AX, @DATA
~~END MAIN~~ MOV DS, AX.

LEA DX, MSG.

MOV AH, 9

INT 21h

MOV AH, 1

~~INT~~ INT 21h.

MOV DL, AL

MOV AH, 2

INT 21h.

→ ~~MOV~~ INT 21h AH, uCH
MAIN END P

END MAIN

LEA → Load Effective Address.

• DATA MSG DB 'please enter a char\$'

→ Program Segment Prefix 256 B. [It is a one kind of memory]

DS, ES ↑
MOV DS, @DATA

(10)

101

CSB & 21/09
BP 5in

21
12.02.2018

4 bit → 4004 (1971) → 6808 → 6808

8 bit → 8008, 8080, 8085 → 286

16 bit → 8086, 8088, 80186

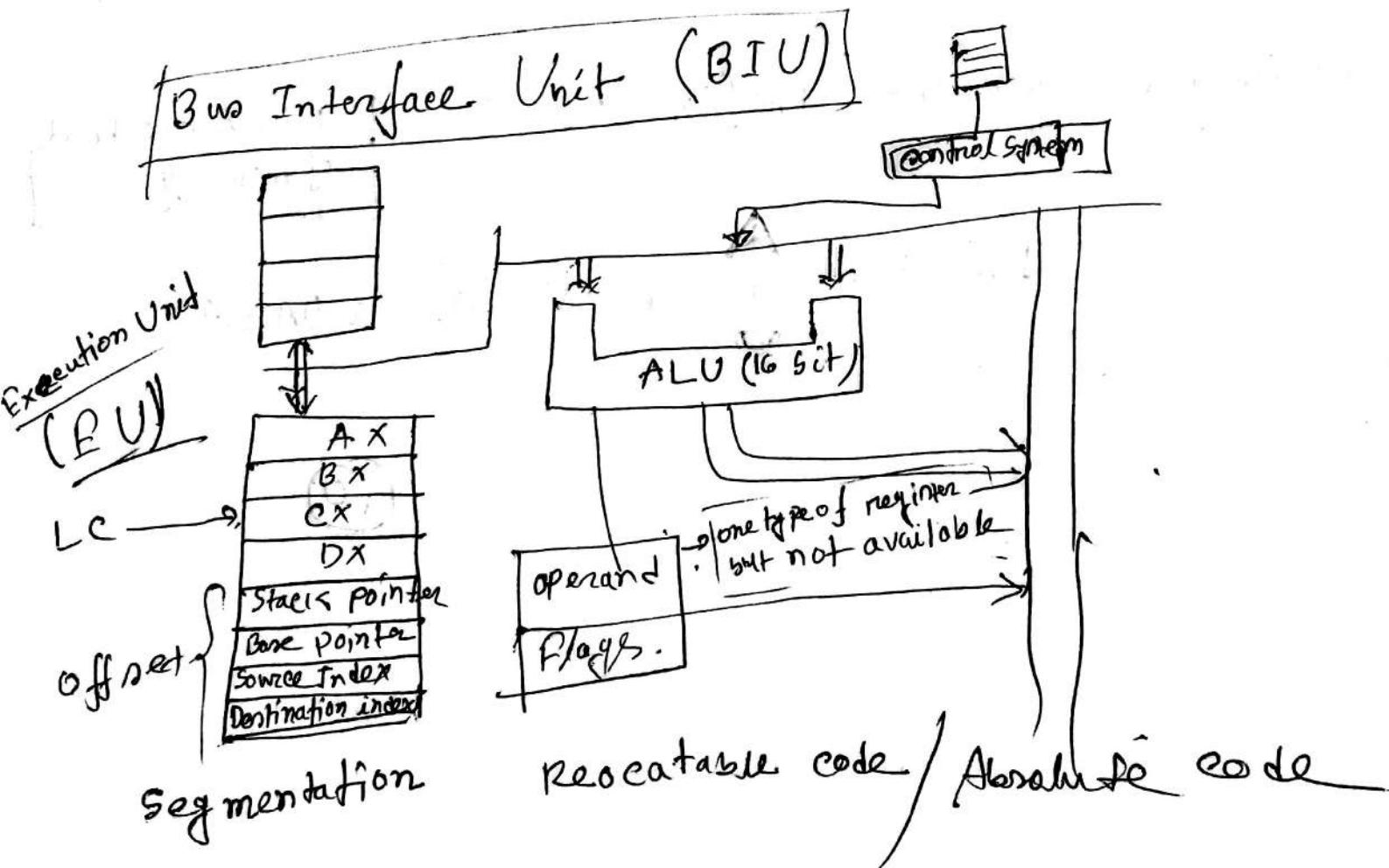
32 bit → 80386, 486

64 bit → Pentium, PT → TV,
Core 2 Duo, Dual core

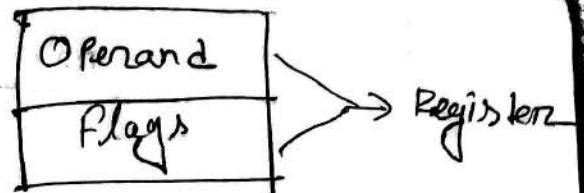
Xeon, Core i3 - i7 → Intel

Power PC, G3, G4, G5

x86 → 8086 architecture based microprocessors
Motorola ←



ADD Ax, Bx
Opcde Operand



Stack Segment : Stack pointer / Base pointer.

Extra Segment (ES) : Destination Index (DI).

Data Segment (DS) : Source Index (SI)

Assignment : Relocatable Code

Absolute machine Code

Assembler

203

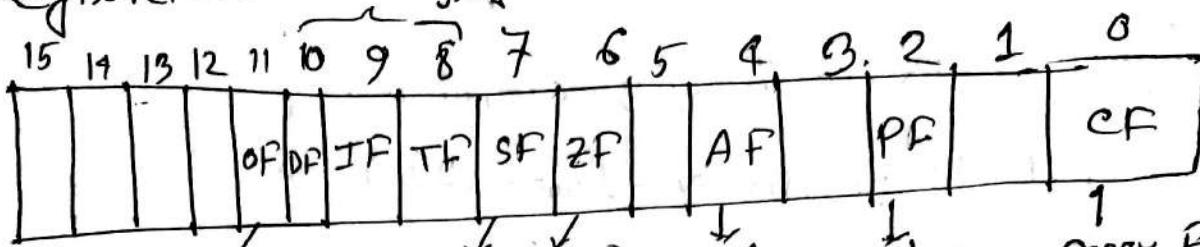
CSB - 3109
BP Siz

3rd day

19.02.2018

Flag

Registers .



CP → gf carry out from msb or borrow into msb

PF → Even no. of 1 in low byte.

AF → gf carry out from 3rd bit or
borrow into 3rd bit.

ZF → gf zero result.

SF → gf sign bit 1.

8-10 → Control Flag.

0-7 & 11-15 → Status Flag.

* CF is part of msb while ZF is not but AF is part of
Auxiliary 3rd bit like ZF is part of basic
difference.

$$AX = \frac{F}{1\ 1\ 1\ 1\ 1} \quad \frac{F}{1\ 1\ 1\ 1\ 1} \quad \frac{F}{1\ 1\ 1\ 1\ 1}$$

$$BX = \frac{F}{1\ 1\ 1\ 1\ 1} \quad \frac{E}{1\ 1\ 1\ 1\ 0} \quad \frac{F}{1\ 1\ 1\ 1\ 1} \quad \frac{E}{1\ 1\ 1\ 1\ 1} \quad \frac{0}{1\ 1\ 1\ 1\ 1}$$

$$(1 \overbrace{1\ 1\ 1\ 1\ 1}^F \overbrace{1\ 1\ 1}^E 0) \quad \overbrace{1\ 1\ 1\ 1}^F \quad \overbrace{1\ 1\ 0}^D$$

MOV AX, FFEE

MOV BX, PEFF

ADD AX, BX.

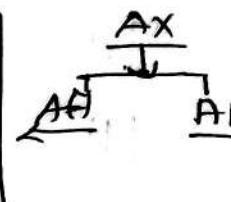
CF = 1

PF = 0

AF = 1

ZF = 0

SF = 1



CT-1 : Chapter - 3, 4, 5

BLSI
APCS

101

CSE -3109

BP Sir

30 day

17.02.2018

Jump

Instructions:

(a)

J A → CF = 0, ZF = 0

J B → CF = 0

J AE → CF = 1

J BE → CF = 1, ZF = 1

JMP destination
Label

unsigned
representation

conditional
jump instruction

CMP D, 5

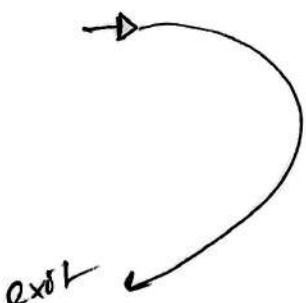
SUB AX, 10

JA mypos

→ same → CMP AX, 10

JA --

JMP destination Label
↳ jump to this label



exit

→ need not to be in same
segment.

If we want to print character from A to Z.

• CODE

MOV DL, ~~65~~ 65

AH, 2 PRINT :

MOV AH, 2

INT 21h

ADD DL, 1 → CMP DL, 75

JMP PRINT JA exit

Exit : → MOV AH, 4CH
INT 21h

MAIN ENDP

END MAIN

• Compare Two character

MOV AH, 1

INT 21h

AL ← C1.

MOV BL, AL

INT 21h .

AL, ← C2

MOV AH, 2

CMP ~~DL~~ AL, BL

JA printit

MOV DL, BL

JMP PRINT:

printit :

MOV DL, AL

~~INT 21h~~

PRINT :

INT 21h .

Unsigned

$$\begin{array}{r}
 11 \rightarrow 3 \\
 01 \rightarrow 1 \\
 \hline
 100 \rightarrow 4
 \end{array}
 \quad \left. \begin{array}{l} \\ \\ \end{array} \right\} \text{memory 6 words}$$

Signed

$$\begin{array}{r}
 11 \rightarrow -1 \\
 01 \rightarrow 1 \\
 \hline
 00 \rightarrow 0
 \end{array}
 \quad \left. \begin{array}{l} \\ \\ \end{array} \right\} \text{memory 6 words}$$

✓ Unsigned overflow $\leftarrow \boxed{\text{CF} = 1}$ $\text{CF} = \text{carry flag}$

✓ Signed overflow

$7FFF \rightarrow 0111\ 1111\ 1111\ 1111$ $7FFF \rightarrow 0111\ 1111\ 1111\ 1111$
--

Signed

$$\begin{array}{r}
 0111 \rightarrow 7 \\
 0111 \rightarrow 7 \\
 \hline
 1010 \rightarrow 14
 \end{array}$$

Signed overflow

Signed bit

range, $-8 \rightarrow 7$.

✓ $\boxed{\text{OF} = 1}$ \rightarrow when signed overflow occurs
✓ $\boxed{\text{OF} = 0}$ \rightarrow when signed overflow ! occurs (not occur)

✓ $\text{msb_in} \neq \text{msb_out} \rightarrow \boxed{\text{OF} = 1}$
 $\text{msb_in} = \text{msb_out} \rightarrow \boxed{\text{OF} = 0}$

JA Divides JG₂ / JNL₂ }
 JGE / JNL }
 JL / JNGE }
 JLE / JNA } Signed jump

ASCIIf

JC CF = 1.
 ↓ jump if carry.

If CF = 1 or not
 then we can check it by
 JC

AX = 7FFF

BX = 8000

CMP AX, BX

JA label-big

If AX is bigger

JG₂ label-big

If signed

ASCIIf → 27

Extended ASCIIf → '28

101

CSE - 3109

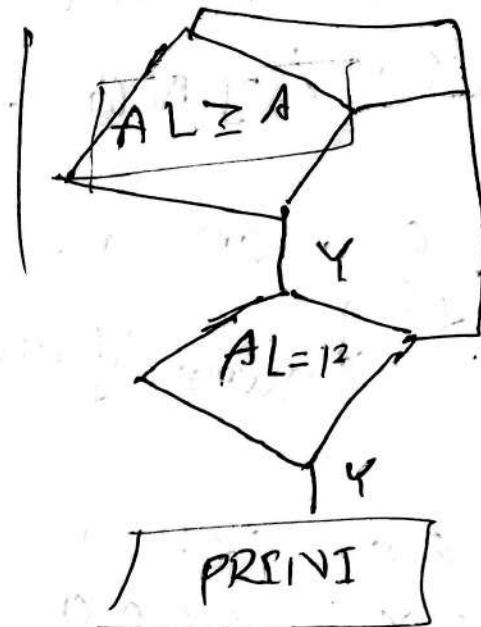
BP Sir

40 day

25.02.2018

• CODE .

```
MOV AX, @ DATA  
MOV DS, AX  
try again:  
MOV AH, 1  
INT 21h ; Scan  
CMP AL, 'A'  
JGE chkr-2.  
JMP try-again
```



Chkr-2:

CMP AL, 'P'

JLE CPRINT .

JMP try again

CPRINT:

MOV AH, 2

MOV DL, AL / '1'

INT 21h

SUB BL, 'A'

MOV AL, BL

INT 21h .

LOOP

Label:

Lo

Loop Label;

→ MOV CX, 10

AL, '0'
TOP : -
MOV AL, 2.
INT 21 h
INC AL
~~JMP TOP~~
CMP AL, 9
JGE out
JMP TOP.

(Chapter 12 → The End)

8086 → Architecture → BIU, PU → already
PIN DIAGRAM → must read.

101

CSP-3109

BP

5 A day

27.02.2020

{ AND
 OR
 XOR
 SHL
 SHR

destination, source.

destination, source

destination, source

destination - CL

destination - CL

}

mask

Filter

NOT

destination

~~OR~~

1101 → AL

OR AL, 02h

~~0000 1101~~
~~0000 0010~~
 2
 mask

✓

XOR

$$\begin{array}{r}
 1 \quad 0 \\
 1 \quad 0 \\
 \hline
 0 \quad 0
 \end{array}$$

MOV AL, 02h

XOR AL, AL

NAND

$$'a' \rightarrow \begin{array}{l} 0100 \quad 0001 \\ 0010 \quad 0000 \end{array} \rightarrow 41h$$

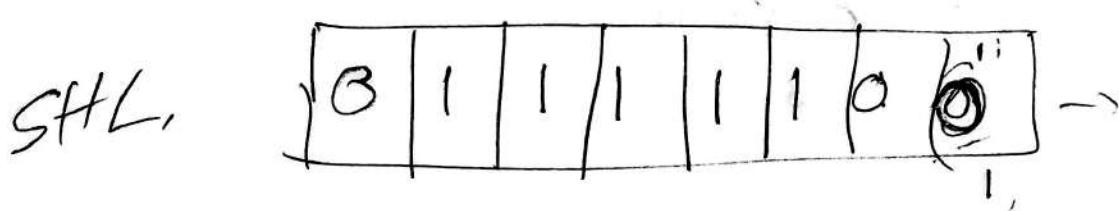
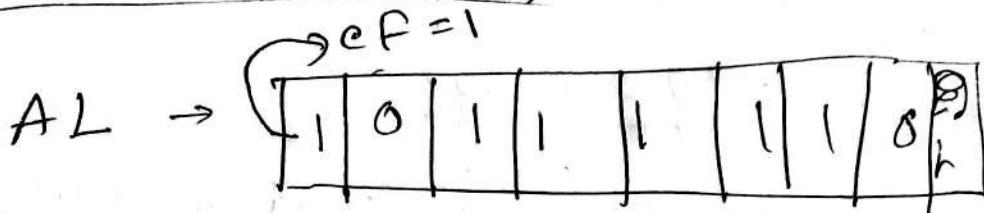
$$'A' \rightarrow 0110 \quad 0001 \rightarrow 61h$$

• OR : AL, 20h

- (i) No carry bit
- (ii) No overflow

} masking ~~masking~~ Advantages

✓ SHL (Shift Left)



JC \rightarrow Jump in carry \rightarrow 9. 2nd (25) 0200
କାର୍ଯ୍ୟ କରିବାରେ CF କି ଲାଗୁ।

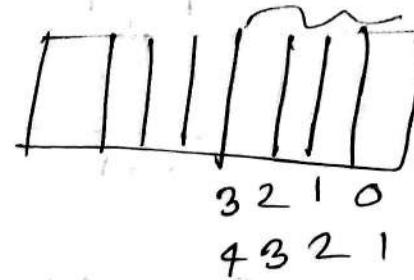
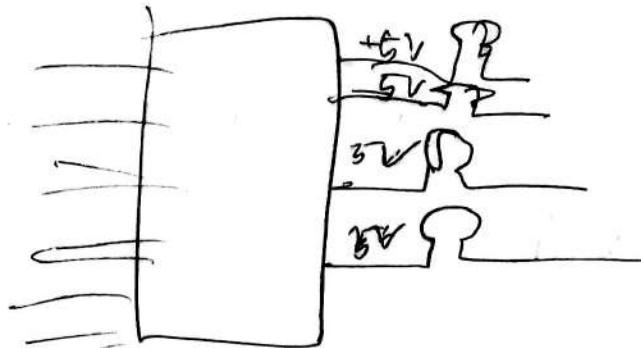
Not 1's complement

ODD even

$$\begin{array}{r} 0 \quad 11111 \quad 00 \\ \rightarrow 1 \quad 00000 \quad 11 \end{array}$$

AND, 1)

$$\begin{array}{r} 3 \quad 0000 \quad 00 \\ 00 \end{array}$$



`Mov AL, ORH`

Assignment: → Can we run/execute a 64 bit software / program in a 32 bit CPU? Why?

Ans: ~~not~~ • 64 GB (6 گیگابائیٹز,

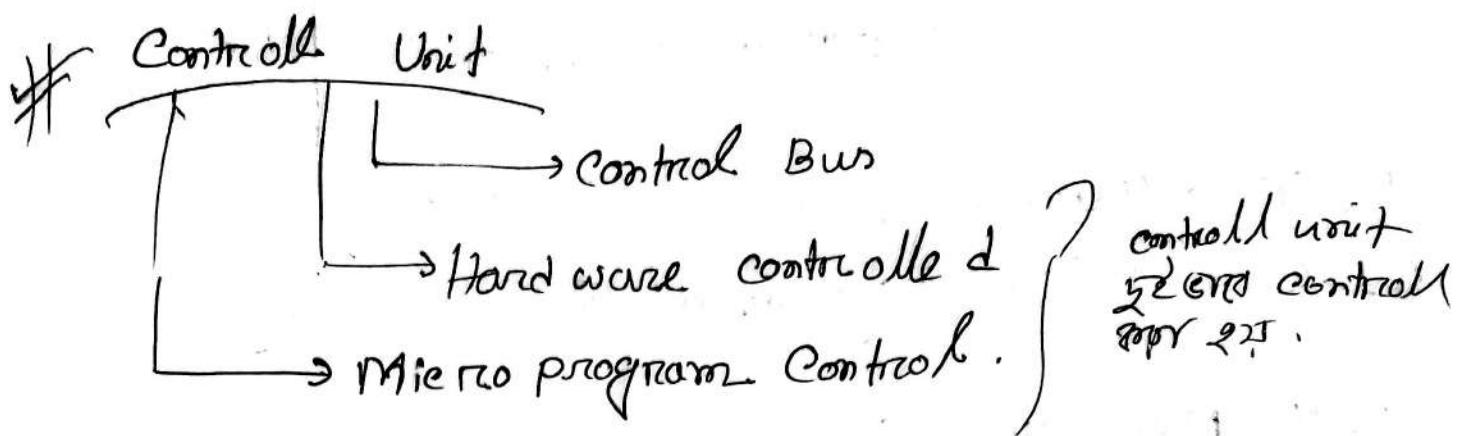
203

CSE - 3109

5 day

BP Sir

03.03.2018



RISC Architecture

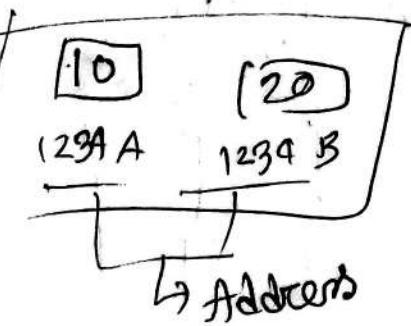
RISC & CISC Architecture

{ RISC: Reduced Instruction Set Computer .
CISC: Complex Instruction Set Computer .
Microprocessor design concept → SET }

ISA : Instruction Set Architecture → Microprocessor
(Q3) Vital .

MOV AX, Var1
Registers

→ memory → single cycle



LOAD AX, [1234 A]
LOAD BX, [1234 B]
ADD AX, BX
STORE [1234]

RISC

12

→ multiple cycle

ADDITION $[1234A], [1234B]$

→ CISC (complex)

1. step 1
2. step 2
3. common
4. step 3
5. step 4
6. step 5

RISC → Hardware use করা হচ্ছে

CISC → Microprogram করা হচ্ছে

MULTIPLICATION

IF : Instruction Fetch

ID : Instruction Decode

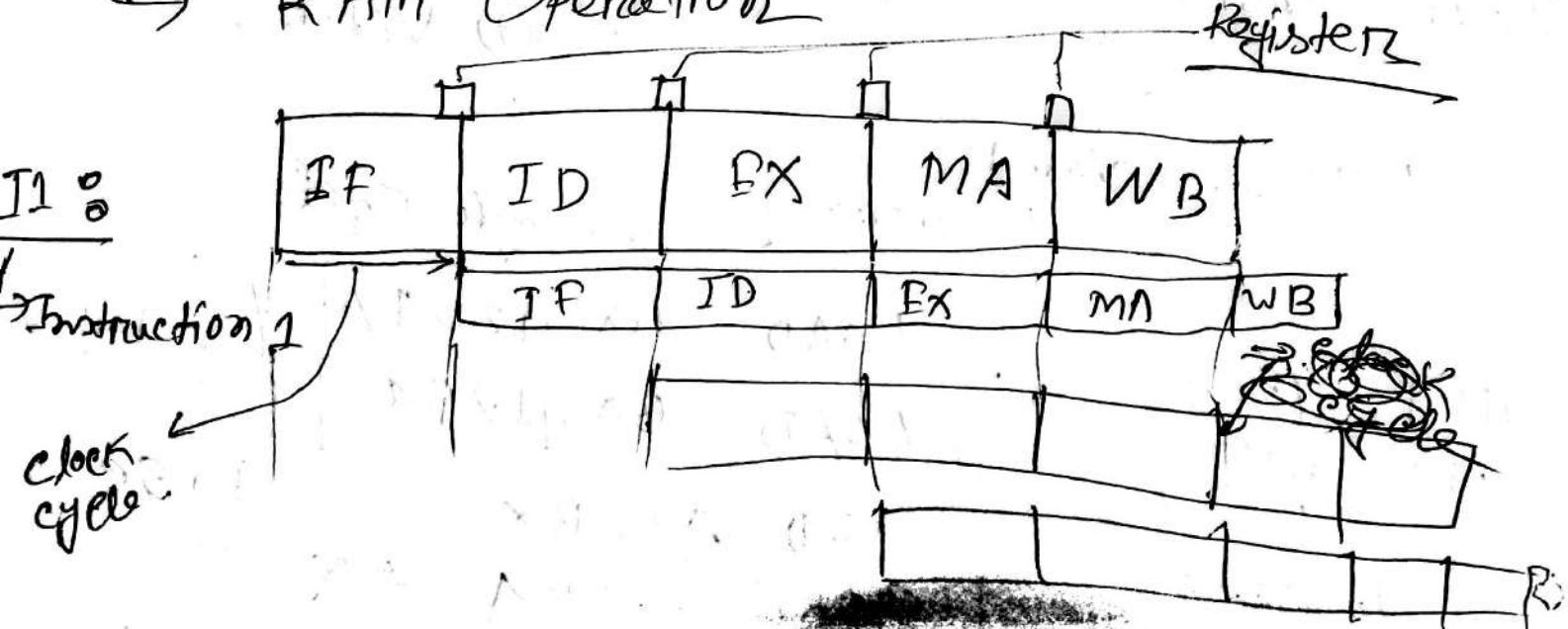
BX : Execute or Execute

MA : Memory Access

WB : Write Back

Pipelining

→ RAM Operation



→ Program Execution Operations
→ Program Execution Operations → Program Execution Operations

LOAD Ax, m

STORE Σ M, AX.

ADD $A \times, BX$

CSC-G Functions

उत्तराधिकारी & code द्वारा
Variation लकी

Rise - simple circuit
for parallel operation

Power Consumption

RISC Power consumption over one Single cycle

GTSE

~~CISC~~: power consumption এবং কোর্স instruction design
CISC: power consumption এবং কোর্স instruction design
complex / multiple cycle প্রক্রিয়ান এবং Gr.

RAM →
memory operation



Which is better?

$$\text{Time} = I \times CPT$$

clock period time (S)
clk period/cycle
cycle/instruction.

No. of instruction/program

$$I \rightarrow 32 \text{ h}$$

0011 0001
0000 0001

$$AL \rightarrow ①$$

0000 0001

0000 0010

161

CSE - 3109

BP Size

5 days

02.03.2018

CT-1 → FLAG Register changing

ROR → Rotated Right



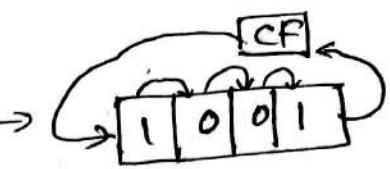
CF

ROR AX, CL

ROL → Rotated Left

RCR →

Right



RCL →

Left

same last data
at first entry

then CF Go to
value first. So
MPA 1

Binary bit String & Input

DX ← 10111100

Register - 16 bit, so can store
2¹⁶ 16 bit input in it

→ Data Input Loop & Flag ZF.

XOR DL, DL

MOV AH, 1

INT 21h

AND AL, 01h

SHL DL, 1

OR DL, AL

AL Go to 2⁸ Character
2⁸ bits = 8 bit & 1 bit = 8 bits

AL = 00000001

31h

0011 0001
0000 0001

AND

0000 0001 → 01h

DX ← 1011

$$\begin{array}{r}
 \text{DL} \quad 0000\ 0000 \\
 \text{AL} \quad 0000\ 0001 \\
 \text{OR} \quad \hline
 0000\ 0001
 \end{array}$$

Hexadecimal Input

~~MOV CL, 4~~
~~XOR DL, D2~~
~~MOV AH, 1~~
~~INT 21h~~

~~AND AL, 0Fh~~
~~SHL DL, CL~~

~~OR DL, AL~~

Start repeat
 0-9 ടു അവലെ
 ഒരു തന്നെ

$$\begin{array}{r}
 \text{9192} \\
 9 \rightarrow \text{Input} \\
 \text{AL} = 0011\ 1001 \\
 \text{AND} \quad \hline
 0000\ 1001
 \end{array}$$

$$\begin{array}{r}
 \text{DL} 0000\ 0000 \\
 \text{OR AL} 0000\ 1001 \\
 \hline
 \text{DL} 0000\ 1001
 \end{array}$$

DL - ~~ഒരു~~ bit
 Shift ~~കുറച്ച് എല്ലാ~~
 next Hex input ~~ഒരു~~
 പൂരിച്ചു

~~MOV AH, 1~~
~~INT 21h~~
~~SUB AL, 37h~~
~~SHL DL, CL~~
~~OR DL, AL~~

OABACh

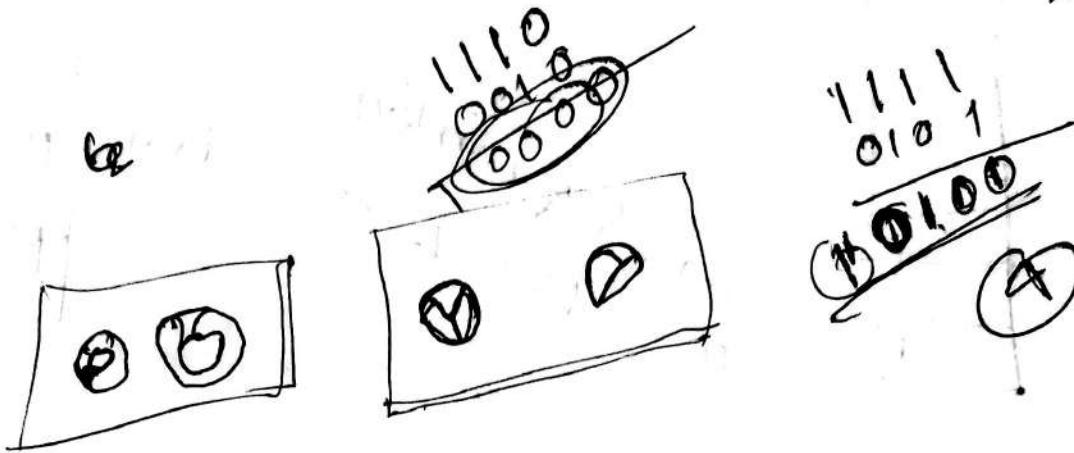
A = ~~65d~~ = 41h

$$\begin{array}{r}
 41\ 1\ h \\
 0100\ 0001 \\
 \text{SUB} \rightarrow 0011\ 0111 \rightarrow 37h \\
 \hline
 0000\ 1010
 \end{array}$$

Here, $A = 65$ $d = 41h$
 $A = 10$ and 22 then 55 $d = 37h$,
Subtract ~~and~~ ~~20~~,

$$\begin{array}{r} B \quad 41h \\ - 37h \\ \hline \text{Sub} \quad 10d \end{array}$$

100
~~00~~



31

$$DL = 10, 10$$

 $XOR DL, DL$

~~10~~
~~10~~

$$\begin{array}{r} DL = 00 \\ - 00 \\ \hline 00 \end{array}$$

00

00

00

00

203

CSE-3109
BP Sim

7c day

25.03.2018

Stack operation



→ stack pointer
16 bit operation

}
PUSH source
PUSHF → Flag
 register -
 POP destination
 POP F

- Stack operation 16 bit operation.
- Register & memory operation push data to stack & data.
- PUSHF - अनु रूप वर्ग में flag को stack पर push कर.

MAIN PROC

MAIN ENDP

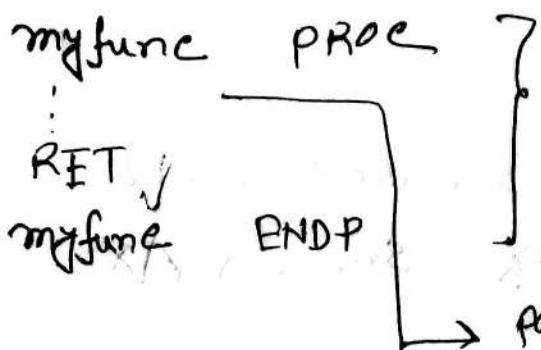
} user define function जे body.

name PROC

RET

name ENDP

} user define function



User define function . " "
parameters passing ?

In Assembly

CALL myfunc

→ In C programming

```
f(int a, int b){  
    printf ("%d %d", a, b);  
}
```

```
main(){  
    int a, b;  
    f(a, b);  
}
```

জন্ম ফর একে পারমিটে কল-জোড় বল দেখি CALL ফর উচিত,

```
main PROC  
    POPF,  
    PUSHF  
    CALL myfunc
```

} import CALL ফর দেখি mainfn
১০ data change হবে কে অবস্থা
CALL কে ওপর PUSHF & main
Proc কে মণ্ডি POPF কে জোড় ,

inc

MULTIPLICATION

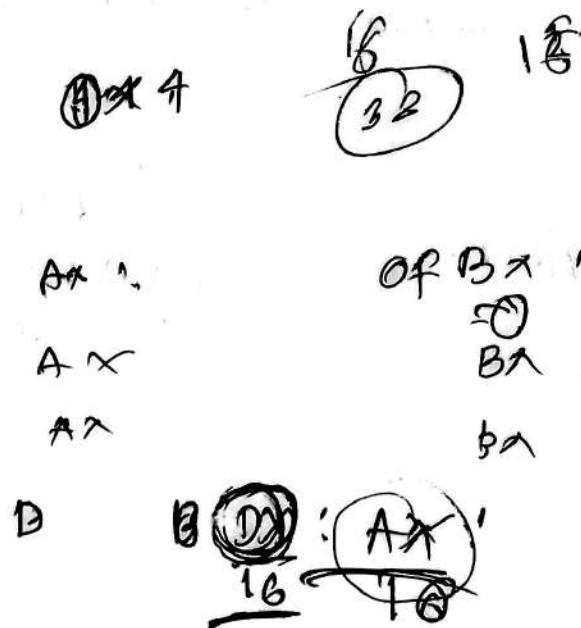
MUL Source $\xrightarrow{\text{Reg}}$ $AX = \text{Source} \times AL$
 IMUL Source $\xrightarrow{\text{Reg}}$ $DX:AX = \text{Source} \times AX$

\hookrightarrow Signed operation

ব্যবহার 32 bit হয়ে তবে $DX:AX$ এর সময় প্রাপ্ত 16 bit DX গুরুত্বের
 মধ্যে 16 bit, AX ও 16 bit।

$$\left\{ \begin{array}{l} 2^{16}-1 = 65535 \rightarrow AX \\ \text{By source} = 2 \times AX \\ DX:AX \end{array} \right\}$$

কোরি check করার টা overflow flag (OF) check করার $[DX:AX]$
 ফ. 32 bit হবলে কোরি!



203

CSB - 3109
BP size

8 day

02.04.2018

Q.T #2 solve

$$\begin{aligned}
 & \checkmark 100000 \times 5\% \times C_g \times t_g + 100000 \times \frac{5\%}{100} \times (100-20\%) \times C_c \times \\
 & 100000 \times \frac{80}{100} \times 8 \times 100 \times 10^{-9} + 100000 \times \frac{20}{100} \times 6 \times 1000 \\
 & = 64 \times 10^3 \\
 & = 64 \text{ ms}
 \end{aligned}$$

Decimal Input

0 - 9

$$\begin{aligned}
 & 134 \\
 & 0 \times 10 + 1 = 1 \\
 & 1 \times 10 + 3 = 13 \\
 & 13 \times 10 + 4 = 134
 \end{aligned}$$

AX, BX, DX

→ Input
 → Input for AL Go & gave 2B,
 → AX Q input consider 00000000 Add 7080
 → AND $\overline{AX}, 000fh$ → Input:
 → XOR BX, BX → AH, 2
 → INT 21h
 Mov DX, AX ; [1 (input)]

Mov Ax, 10

MUL BX ; [Result in AX]

ADD AX, DX [Result in AX]

MOV BX, AX [First step result'in]

JMP Input BX

Stack

ADD ~~AX, DR~~

Mov -Dx,Ax -

push Ax

10)

CSR-3109
BP size

8 day

03.04.2018

DIV Divisor

IDIV Divisor

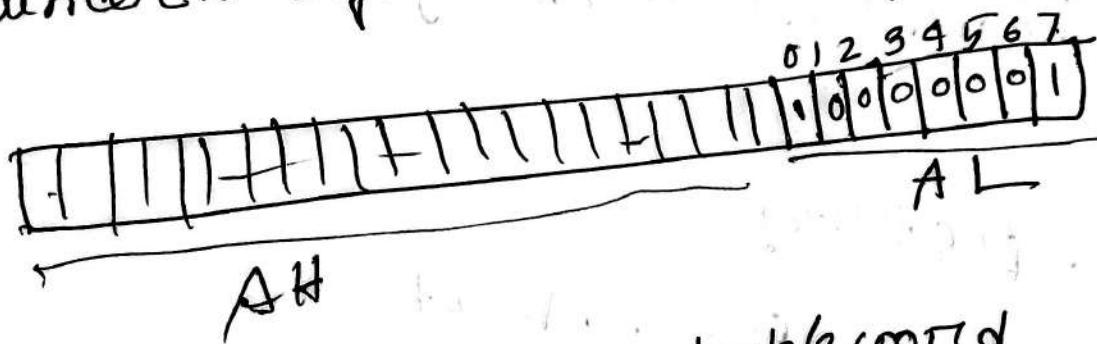
divisor) AX (AL

AH

divisor) DX : AX (AX

DX

Remainder's sign = dividend's sign.



CWD \rightarrow word - double word
CBW \rightarrow Byte-word

MOV AL, -5

CBW

MOV BL, 2

IDIV BL

ADDRESSING MODE

Register indirect

high Level Language

```

int * p;
p = &a;
int [10];
printf("%d", *p);
("%d", p),
a[2]
    
```

→ Register contains the address of some memory.

MOV AX, [Register]

General use DS

DS
DI → 16 bit

DS: SI

BS: DI

My array DW

10, 20, 30, 40,
A, B, C, D.

→ When we need to print one value then we move it into DL and print it.

MOV AH, 2

INT 21h

LDA SI, myarray

PRINT ~~MOV AH, 2~~

MOV DL, [SI]

INT 21h

10, 20, 30, 40

DS: DI

POINT ~~DS: DI~~

ADD SI, 2

Loop print:

Based / Indexed

~~Address~~ Addressing mode

[offset + displacement]

offset [displacement]

✓ ~~MUL~~ mov AX, 0
mov DL, Myarray [AX]

ADD AX, 2

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BP size

9/10/2018

07.09.2018

- Based Add. mode
- Indexed Add. mode
- Based Indexed Add. mode

✓ Register + Displacement

Base/I

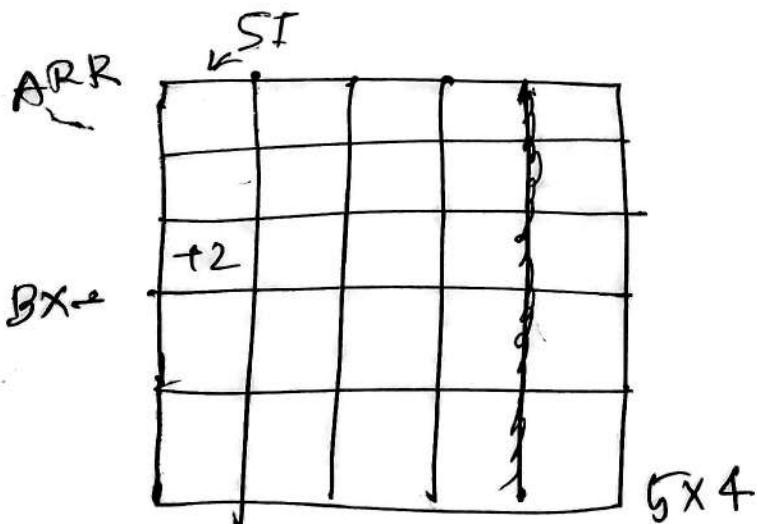
Register ৰে প্ৰথম Base add & তলে I এৰে দিবলি কৈ টাৰ্পে

Go Add.

↓ DW

✓ ARR [R] [c]

✓ 2 dimensional অৱৰ্গ এৰে কৈ টাৰ্পে Base d
Indexed Add. mode উল দিবলি,



ARR content +2 কৈ দিবলি (Suppose) Array কৈ data input

দিবলি :

~ BX কৈ Row কৈ দিবলি & SI কৈ Column কৈ দিবলি

```

    MOV CX, 3
    XOR SI, SI
    MOV BX, 16
    ADD ARR [BX] [SI], CX
    ADD SI, 2

```

→ DW → word type array
 ARR [R] [C]

0	2	4	6
8	10	12	14
BX → 16			

LABEL

{ Just like C program's Structure }
 ↪ not totally }

STUDENT LABEL WORD

```

ROLL 15300
MARKS DB 30
MOV AX, STUDENT

```

} 16 bit [1 + 1 byte = 2 bytes]
 = 16 bit
 AX → 16 bit → word type
 Student → word type

→ A H → A L .

```

MOV AX, ST
MOV BH, ROLL

```

এখন কোরা declare করি
 আরেকবার GOTO করলে
 এই কোরটি নামসহ, নাইট নাফ

PTR

→ byte pointer
 ↪ keyword

```

MOV BYTE PTR [BX], 10
WORD

```

16 bit 8 bit
 MOV AX, BL
 LS0, RS2 operation G
 SHIFT 20 bit not same

MOV [SI], 2
 PTR → just like type casting in C

MSG DB 'RUET'

LBA SI, MSG

→ SIG ring odd
for assign error

mov word PTR [BX], 10
↳ word type

20)

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BP SRC

9e day

16.09.2018

XLAT

→ Translate Great INT.

BX ← table index

[BX table के value एवं Convert हो]

AL ← Byte value to be converted,

XLAT [BX & AL का value Gya base के अनुकूल]

CODE

B	C	D	B	F	A	...
---	---	---	---	---	---	-----

[code = Array]

LEA BX, CODE

MOV AL, 01h

XLAT

65h	66h	68h	...
Y	Z	A	B C D E F ...



MSG

D	C	F
---	---	---

LEA BX, CODE

LEA ~~SI~~, SI, MSG

MOV AL, [SI]

XLAT

MOV DL, AL

MOV AH, 2

INT 21h

~~TNS~~ SI

→ BAD

INVEST.

Duplicate করাবলৈ

CODE DB 65

DUP (' ',), Y2AB -

String

✓ movSB /W

value moves that movSB
movSB → four byte
mowsW → four word

DS : DI



Destination Array

DS : SI



Source Array

S [R | V | E | T]

→ Source Array

ST ← Source

D [| |]

→ Destination Array

DI ← Des

GT

✓ mov Ax @ DATA

MOV BS, AX

CLD

LEA

SI, S

LEA

DI, D

movSB

~~movSB~~

MOV SB

MOVSB

SB/W

~~STOSB / W~~
for string type

LODS B/W → AV/Ax DS : SI

STOSB/W → ES:DI ALIAX

→ Microprocessor (256 memory 256)

DF → Direction Flag

$D\beta \rightarrow 0$ $S/I / D/I \propto$
Value ~~too~~ \propto $\frac{1}{D}$

$DF \leftarrow 1$ $S1 / DI \text{ Go Value}$

Digitized by srujanika@gmail.com

$$DF \Leftarrow 0$$

→ CLD encro

$$D_F \leftarrow 1$$

↳ STD মেঘালয়ি

10)

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B.P.SIR

90 doff
17/09/2018

- ✓ REPB
- ✓ REPB2

String operation

- ✓ SCASB / W
- ✓ CMPSB / W

A	B	C	D
---	---	---	---

SCASB → String \Rightarrow check কোনো কোনো পার্টিকুলর চরার প্রেসে কোনো পার্টিকুলর চর আছে ?

AL / AX
 \hookrightarrow C

✓ CMPSB → Compare করা, SCASB কোনো কোনো এই কোনো operation করে পারে, CMPSB কোনো কোনো array কে operation করে,

DS: SI



CT-3 (10A)

Q: Stack কি মডেলের string দাখিল ?

REPE → (Repeat while equal)
REPNE → (Repeat while not zero).

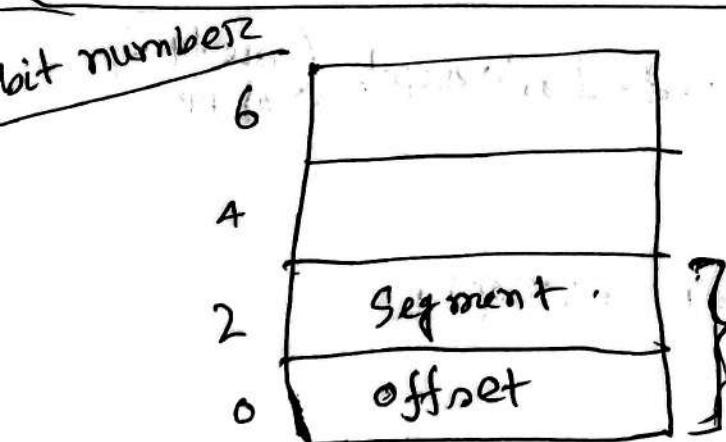
CX, 4 → controls copying until counter

- ✓ before we use MOVS.B many times but it is not needed
while we use REPE, it's work like multiple
~~REP~~ MOVS.B command. REPE will control with
CX.

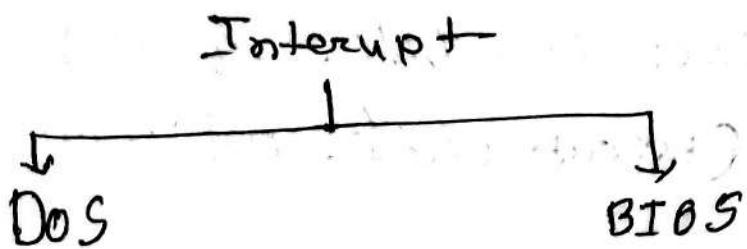
Interrupt

- Software INT.
- Hardware INT
 - ↳ NMI Int.
- Exception .(processor exception)

Interrupt Vector Table



$$2^8 \times 4B \rightarrow 1KB$$



→ ~~After~~ प्रूप्ति, Int 21h ट्रेकल अ वीटोर टॉबल 6 ~21
 ① इन्टरफ़ेस लेनल अ अड्रेस 0000. (2nd अड्रेस) बिट्स
 कैरेक्टर फंक्शन ए अक्टुल्य पॉइंट अप अ अ
 फंक्शन (ए अ रन डॉक्टर)

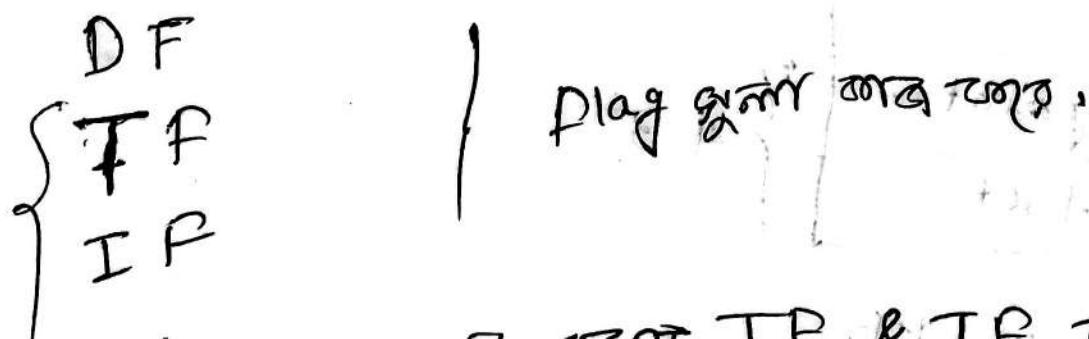
Processor's Interrupt Process

INT R → Interrupt request. (microprocessor pin)

INT A → (Interrupt Acknowledge) [INT R
 execute 2nd प्रूप्ति अ INT A अ सिग्नल फॉर
 अप्पे INT A execute 2nd]

✓ INT A अ 2nd अ नंबर ऑर (2nd अ नंबर) अ
 अप्पे & क्रेमल ऑपरेशन अप्पी

NMI → Non maskable Input Interrupt (one type
 of pin)



Interrupt process अ शायद TP & IP टो डिरो
 अप्पे अप्पी

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BP

10th day

23,09,2018

Timing of 8086

for read / write
cycle

Max mode }
Min mode }

Gr. 52 mode of 8086

Co-processor ~~Max~~ → (multiprocessing)

8086 के गोले Co-processor = 8087

8087 → Math Co-processor

→ Block Diagram

Latch

Trans receiver

Clock generator

+ Memory

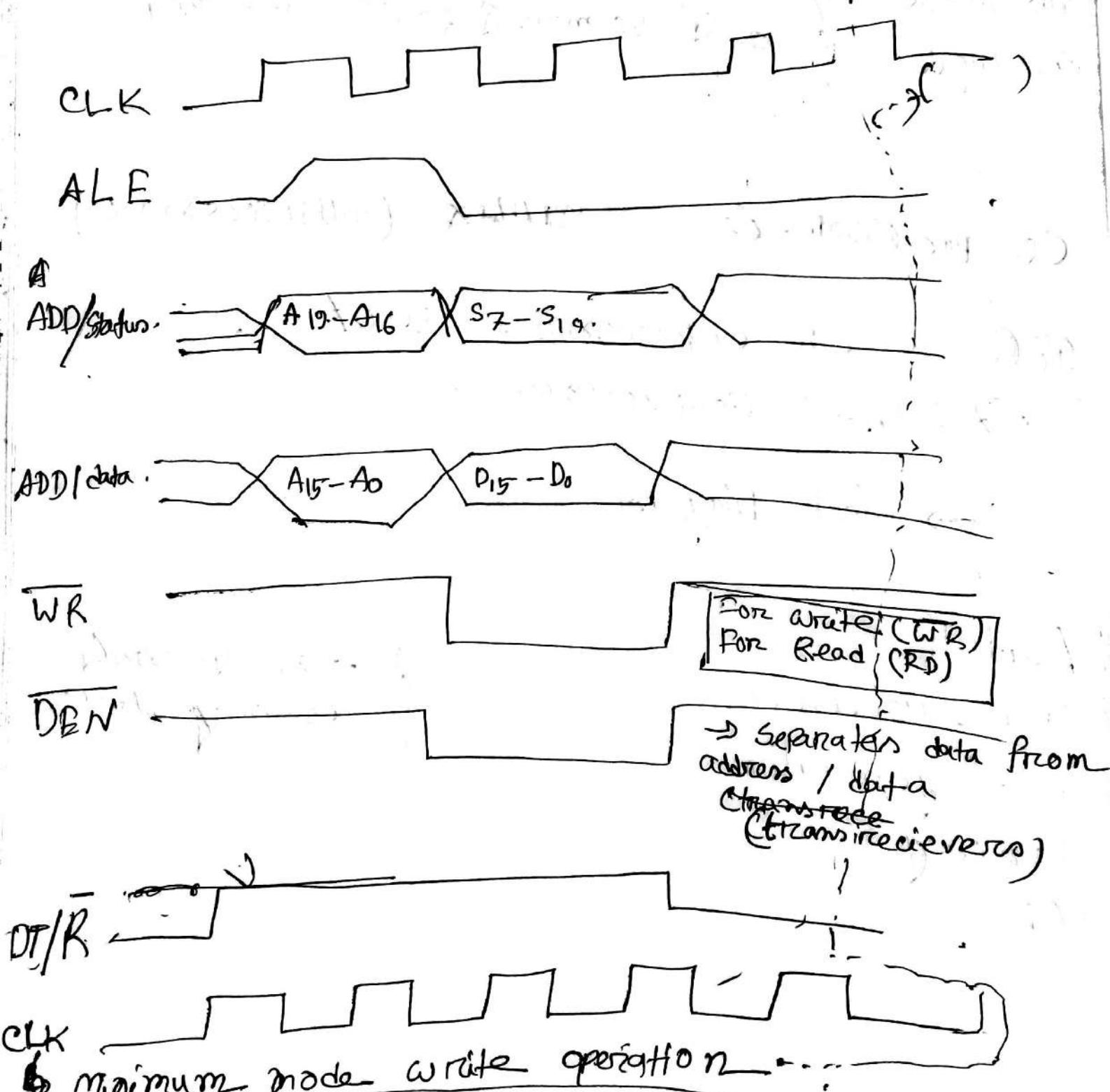
I/O

} 8086 के लाई
necessary blocks.

3. S. Latch
transreceivers
clock generator
Microprocessor - କେବଳ ତାର ଏଣ୍ଡି ଏବଂ ଅଭାବନୀୟ

Q) Microprocessor G 1
Why these 3 are necessary in microprocessor?

✓ Submission date : 12.B day



- ✓ At Maximum mode GR operation Home work
 - ✓ Write to GR same as WR
 - ✓ Read GR same as all name but RD
 - ✓ Min. mode \rightarrow microprocessor will work
 - ✓ Max mode \rightarrow memory chip GR memory per work
- \Rightarrow DMA operation
- DMA = Direct Memory Access.
- \rightarrow SRAM
- \rightarrow DRAM
- } Internet

101

CS P-3109
BP

10D day

24.04.2018

- ✓ Introduction to Assembly language
- ✓ logic and Arithmetic operation
- ✓ flag and flow control
- ✓ Array
- ✓ string manipulation
- ... Introduction to diff - ty pe of microprocessor
- ... organization of 8086 microprocessors
- ✓ component of micro computer
- ✓ I/O device
- ✓ peripheral interfacing . (I/O)
- ✓ DMA controller (chip). (8237)
- ✓ interrupt controller
- ✓ Interrupt structure
- ✓ Interrupt related PIN
- ✓ co-processor
- ✓ RISE & CISe
- ✓ Direct Video RAM Accessing
- ✓ memory And IO