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Darlington pairs or connection:

A very popular connection of two bipolar junction transistors for operation as one "super beta" transistor is the Darlington connection. It is used in digital system. The main feature of the Darlington connection is that the composite transistor acts as a single unit with a current gain that is the product of the current gains of the individual transistors.

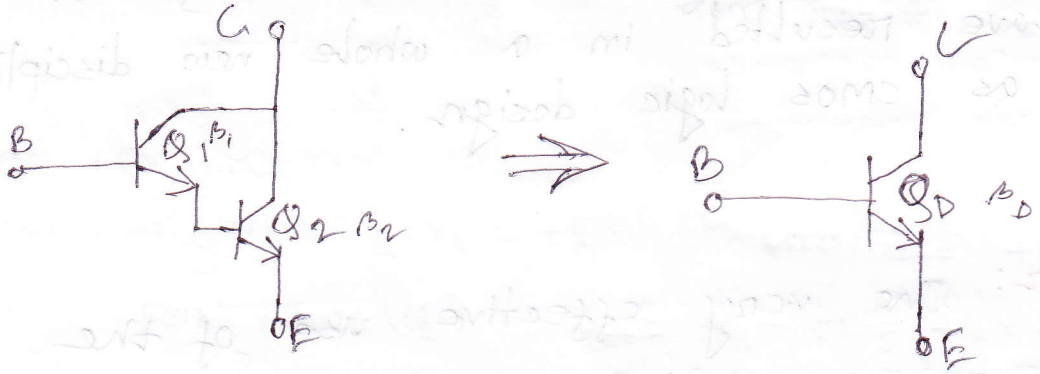


Fig: Darlington connection

If the connection is made using two seperate transistors having current gains of β_1 and β_2, the Darlington connection provides a current gain of

$$\beta_D = \beta_1 \beta_2$$

If two transistors are matched so that $\beta_1 = \beta_2 = \beta$,

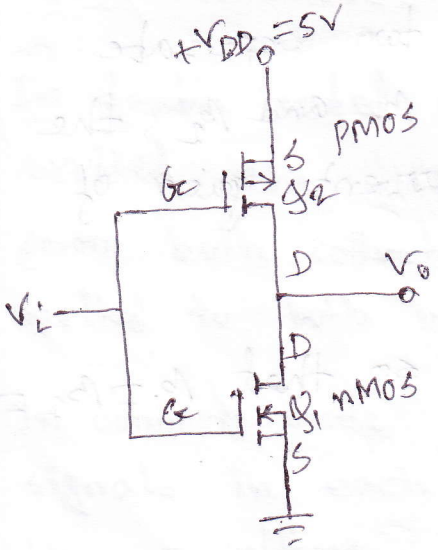
then $\beta_D = \beta \cdot \beta = \beta^2$

i.e., a Darlington connection provides a transistor having a large current gain, typically a few thousand.

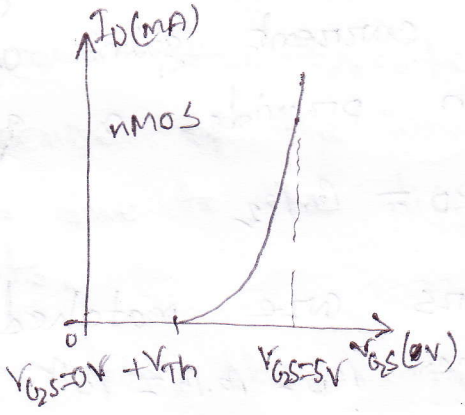
CMOS: A very effective logic circuit can be established by constructing a p-channel and n-channel MOSFET on the same substrate. The induced p-channel on the left and the induced n-channel on the right for the p and n-channel devices respectively. The configuration is referred to as a complementary MOSFET (CMOS).

The relatively high input impedance, fast switching speeds and lower operating power levels of the CMOS configuration have resulted in a whole new discipline referred to as CMOS logic design.

CMOS inverter: One very effective use of the complementary MOSFET is as an inverter. An inverter is a logic circuit that inverts the applied signal.



CMOS inverter circuit



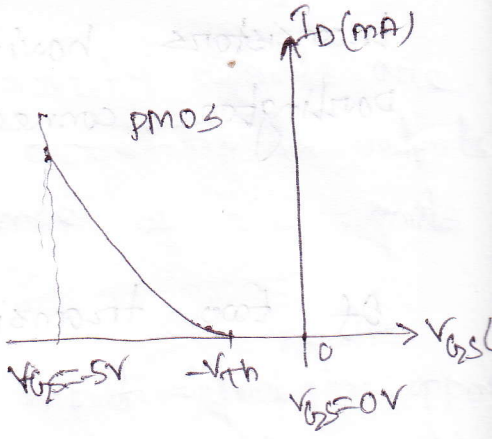


Fig: characteristic off & on condition

At 0V input,

when 0V is applied to the CMOS circuit as input, it provides 0V to both NMOS and PMOS gates.

For NMOS (Q_1): $V_{GS} = V_i - 0V = 0 - 0 = 0V$

For PMOS (Q_2): $V_{GS} = V_i - (+V_{DD}) = 0 - 5V = -5V$

Input of 0V to an NMOS Q_1 leaves the device "off". But gate to source voltage of PMOS Q_2 being -5V (gate at 0V is 5V less than source at +5V), resulting in that device turning on. The output V_o is then +5V.

At +5V input,

when $V_i = +5V$, it provides +5V to both gates.

For NMOS (Q_1): $V_{GS} = V_i - 0V = +5V - 0V = +5V$

For PMOS (Q_2): $V_{GS} = V_i - (+5V) = +5V - 5V = 0V$

The inputs result in transistor Q_1 being turned on and transistor Q_2 remaining off. the output then near 0V through conducting transistor Q_2.

Operation of CMOS circuit →

V_i(V)	Q_1	Q_2	V_o(V)
0V	off	on	+5V
+5V	on	off	0V

Differential Amplifier Circuit:

A very popular connection used in IC units that has two inputs and two separate outputs and the emitter is common to both transistor. Such connection of logic circuit is called the differential amplifier circuit.

A number of input signal combinations are possible in the differential amplifier circuit;

1. Single-ended operation.
2. Double-ended operation.
3. Common-mode operation.

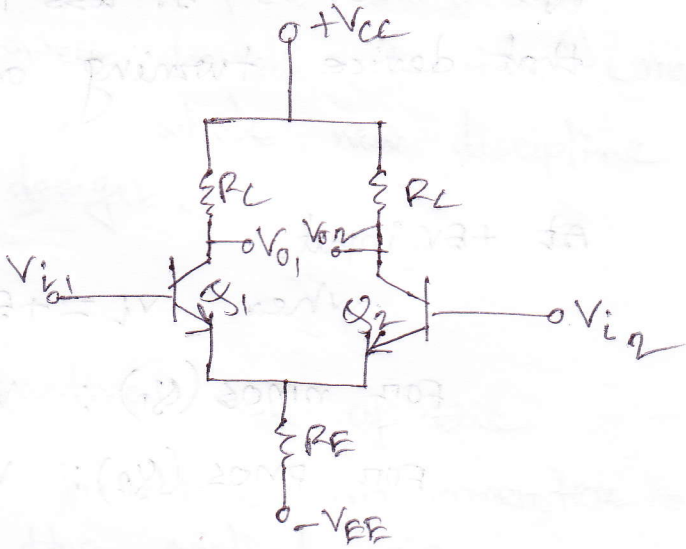


Fig: Differential Amplifier circuit

In single-ended operation, a single input is applied to either input with other input connected to ground, resulting in output from both collectors.

In double ended operation, two opposite-polarity signals are applied. The difference of the inputs resulting in outputs from both collectors due to the difference of the signals applied to both inputs.

In common-mode operation, the common input signal results in opposite signals in each collector, these signals canceling, so that the resulting output signal is zero.

The main feature of the differential amplifier is the very large gain when opposite signals are applied to the input. So, double-ended operation is the most preferable