Programmable Logic Array (PLA)

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PLA

- A Programmable Logic Device (PLD) is an electronic component used to build reconfigurable digital circuits. Unlike a logic gate, which has a fixed function, a PLD has an undefined function at the time of manufacture. Before the PLD can be used in a circuit it must be programmed, that is, reconfigured.

- A Programmable Logic Array (PLA) is a kind of programmable logic device used to implement **Combinational** logic circuits.

- PLA is a circuit that allows implementing Boolean functions in sum-of-product form.

PLA…

- Both AND and OR arrays are programmable.

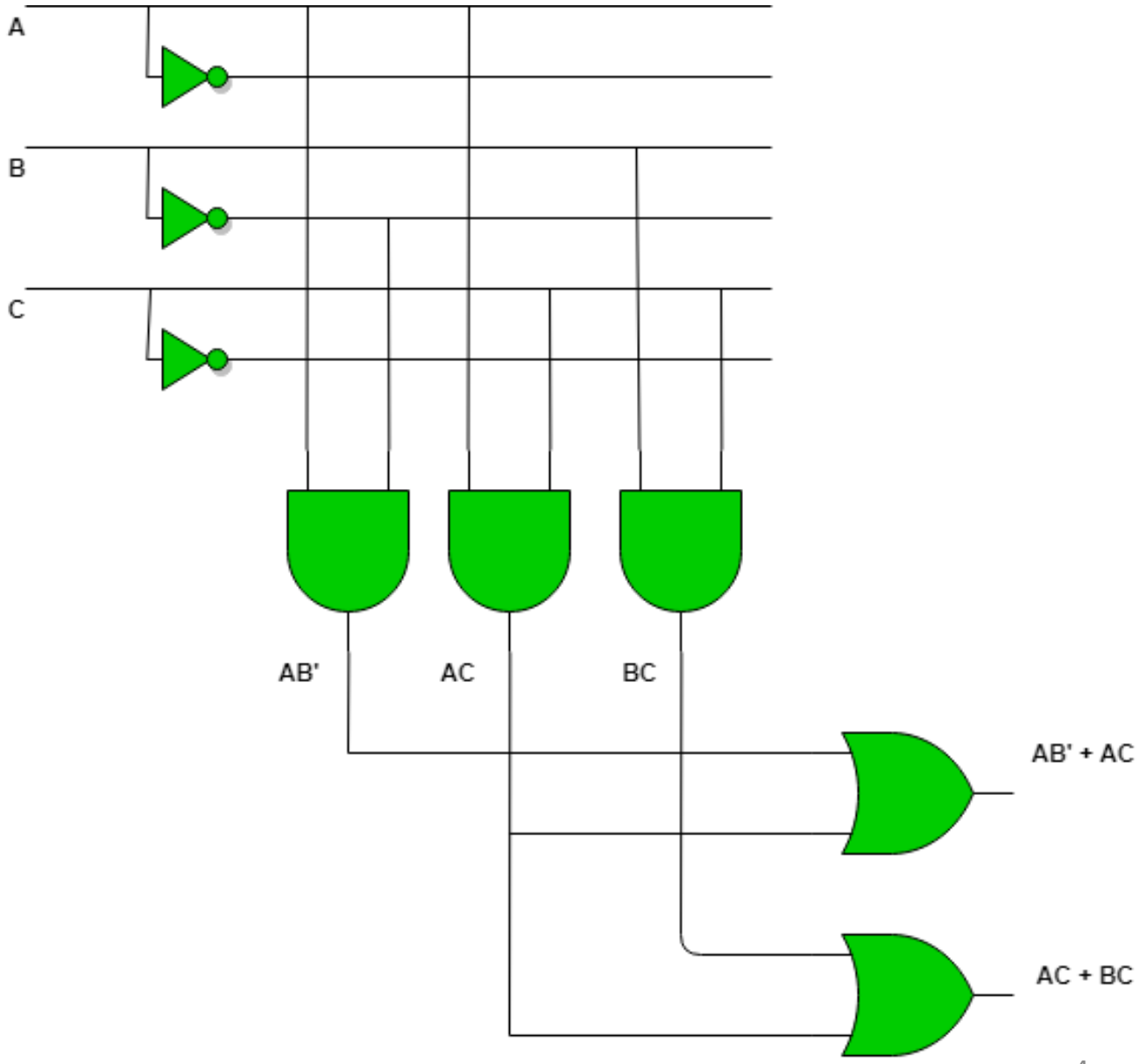
- The number of AND functions in the AND array is independent of the number of inputs.

- Similarly, the number of OR functions in the OR array is independent of both the number of inputs and number of AND functions in the AND array.

PLA…

F1 = AB’ + AC

F2 = BC + AC



PLA…

: 5 × 8 × 4 PLA shown symbolically and programmed for:

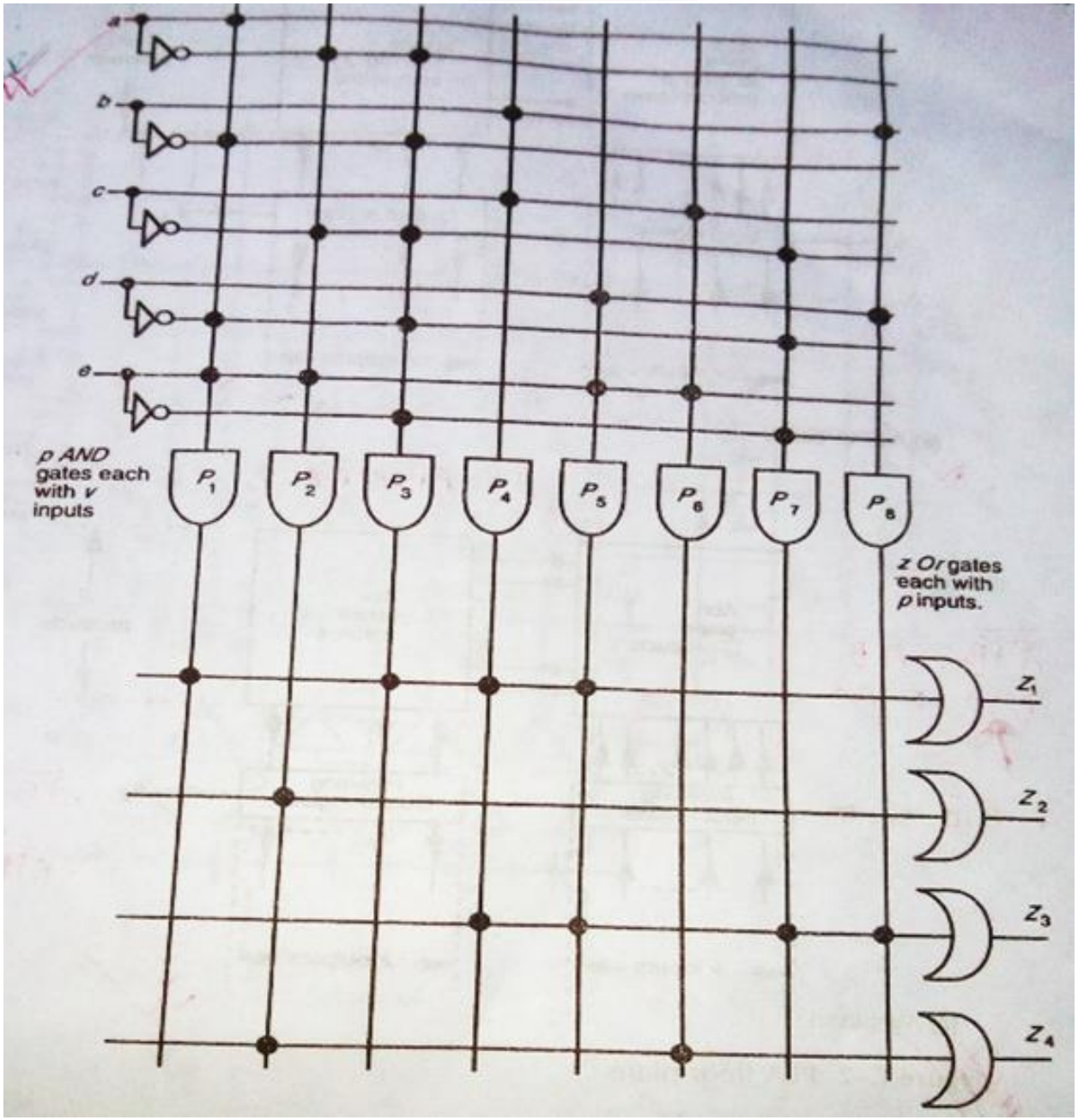
$Z_1 = p_1 + p_3 + p_4 + p_5 \therefore Z_1 = a\bar{b}\bar{d}\bar{e} + \bar{a}\bar{b}\bar{c}\bar{d}\bar{e} + bc + de$

$Z_2 = p_2 \qquad \therefore Z_2 = \bar{a}\bar{c}e$

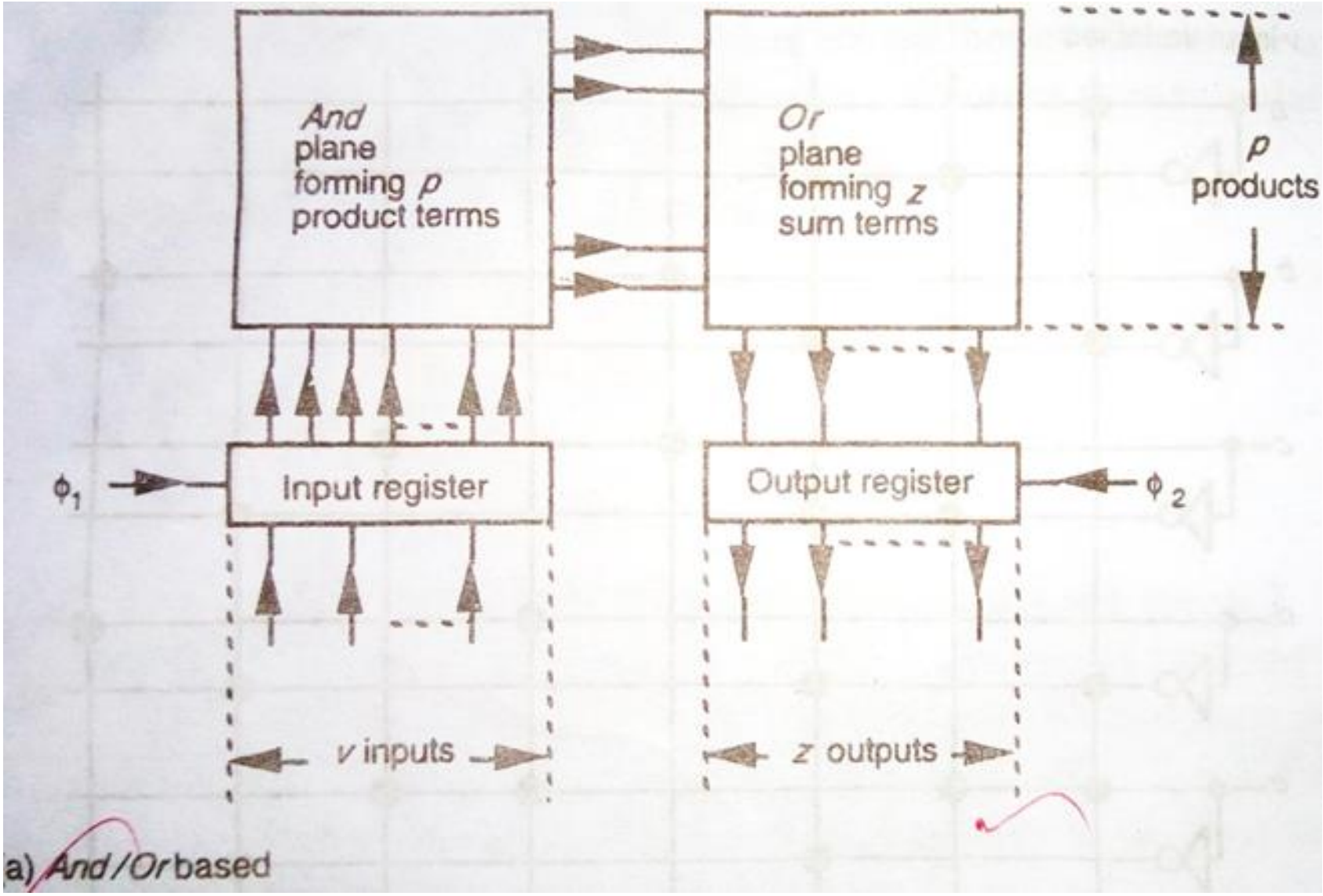
$Z_3 = p_4 + p_5 + p_7 + p_8 \therefore Z_3 = bc + de + \bar{c}\bar{d}\bar{e} + bd$

$Z_4 = p_2 + p_6 \qquad \therefore Z_4 = \bar{a}\bar{c}e + ce$

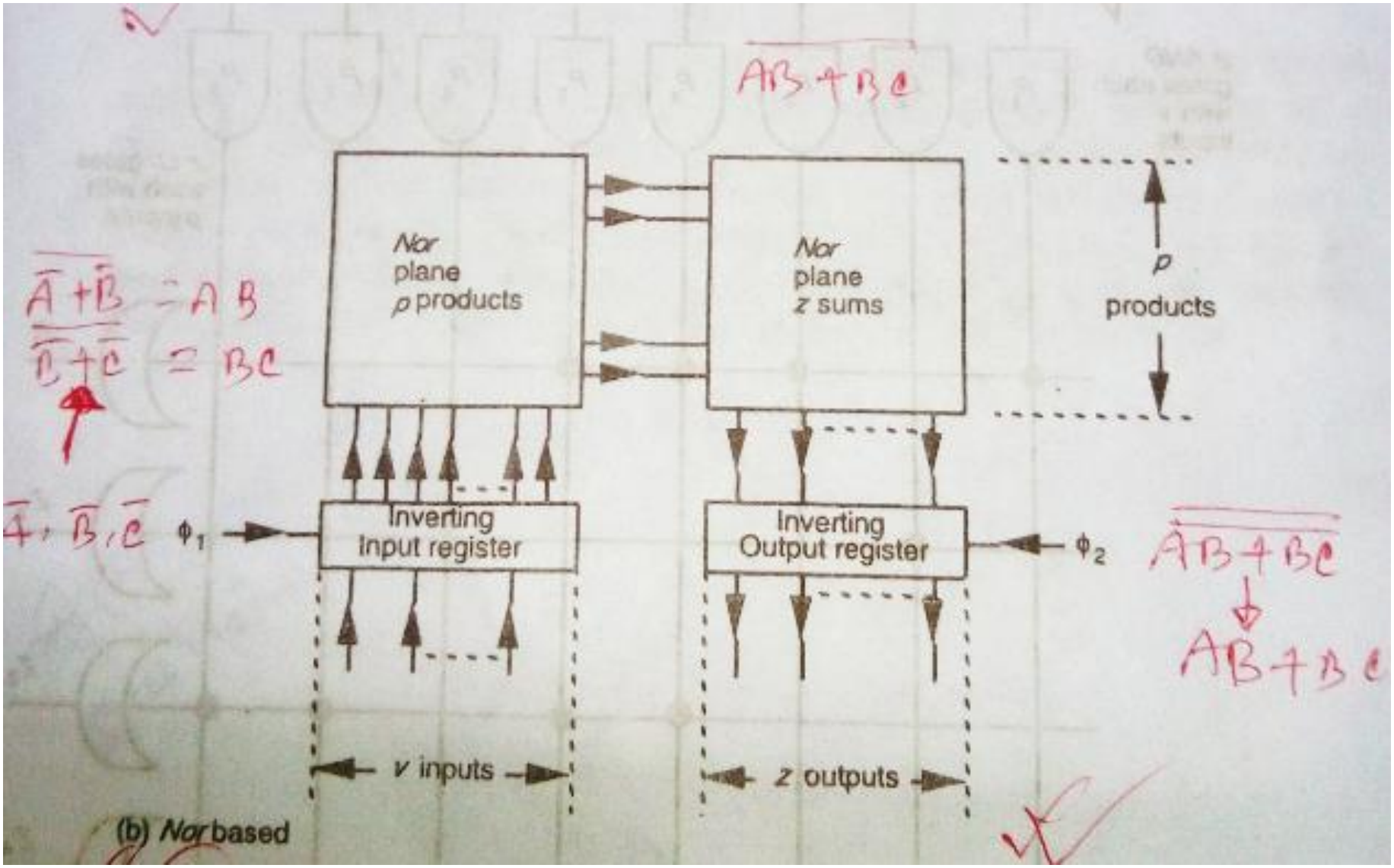
PLA…


a
b
c
d
e
p AND gates each with v inputs
P1
P2
P3
P4
P5
P6
P7
P8
z Or gates each with p inputs.
Z1
Z2
Z3
Z4

PLA Floorplan



PLA Floorplan…



PLA

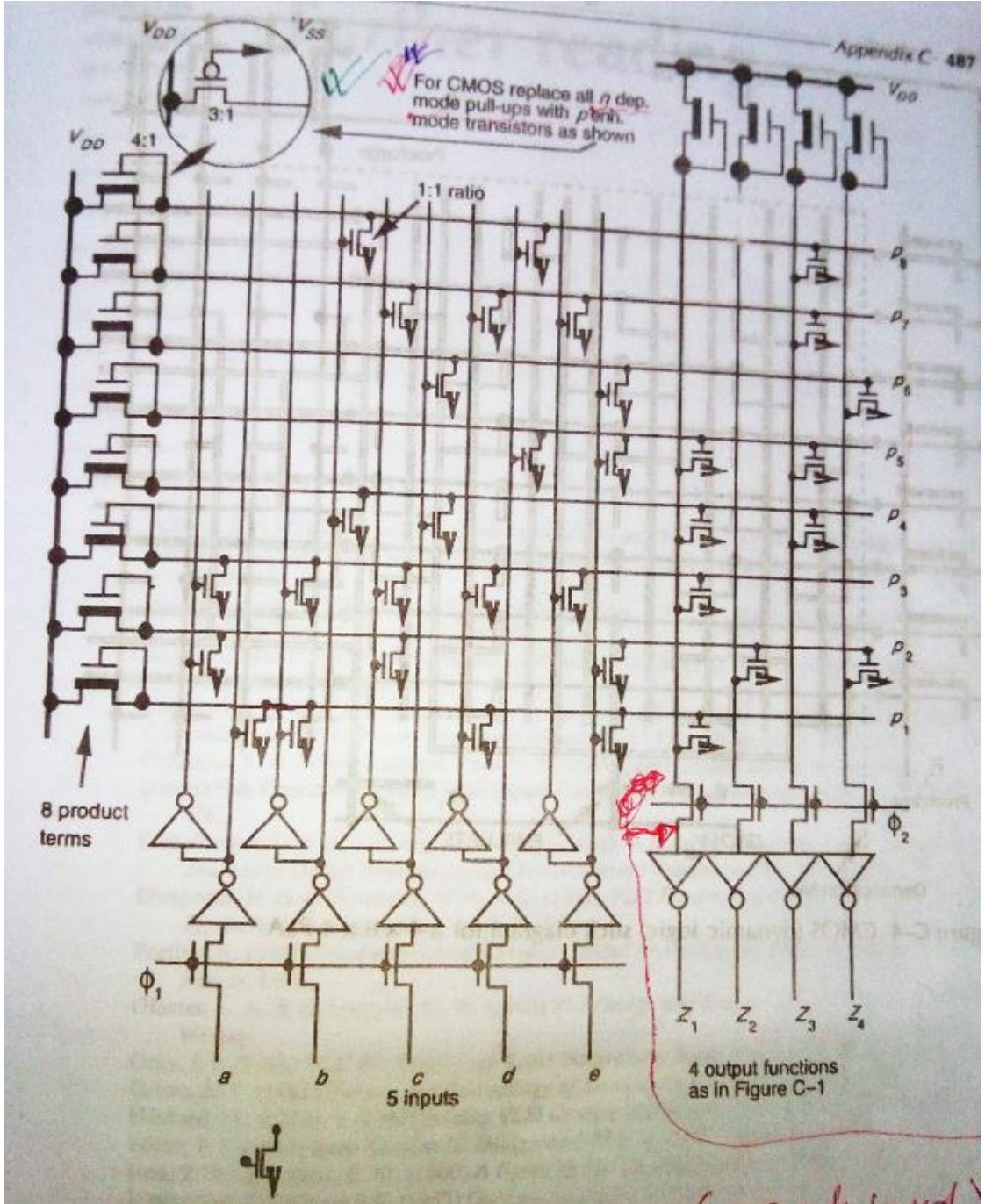
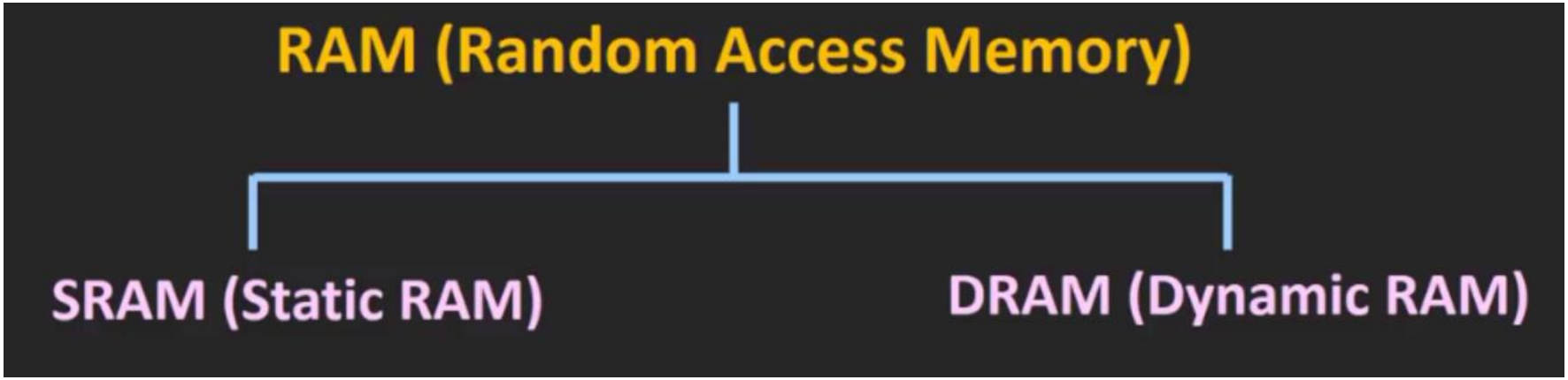


Figure C–3 PLA arrangement for multiple output function (NOR gate based)

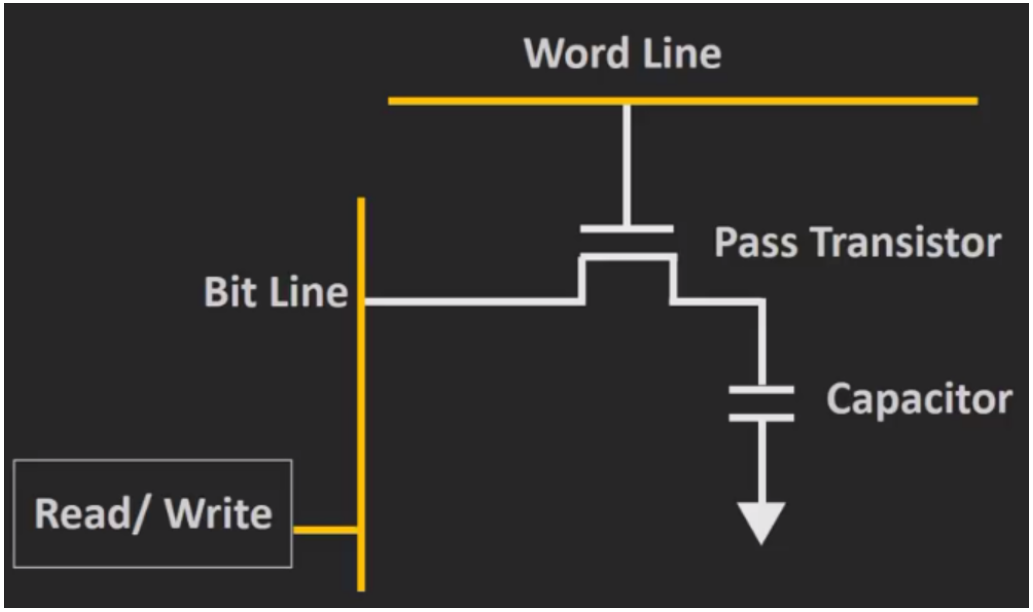
RAM



One Bit DRAM Cell

Internal Structure

- Consists of one transistor and one capacitor.
- Memory bit is stored as charge across the capacitor.
- Charged capacitor indicates logic 1 and no charge indicate logic 0.
- The capacitor is accessed through the pass transistor.
- When the pass transistor is ON, the capacitor can be read or written.



One Bit DRAM Cell…

Internal Structure…

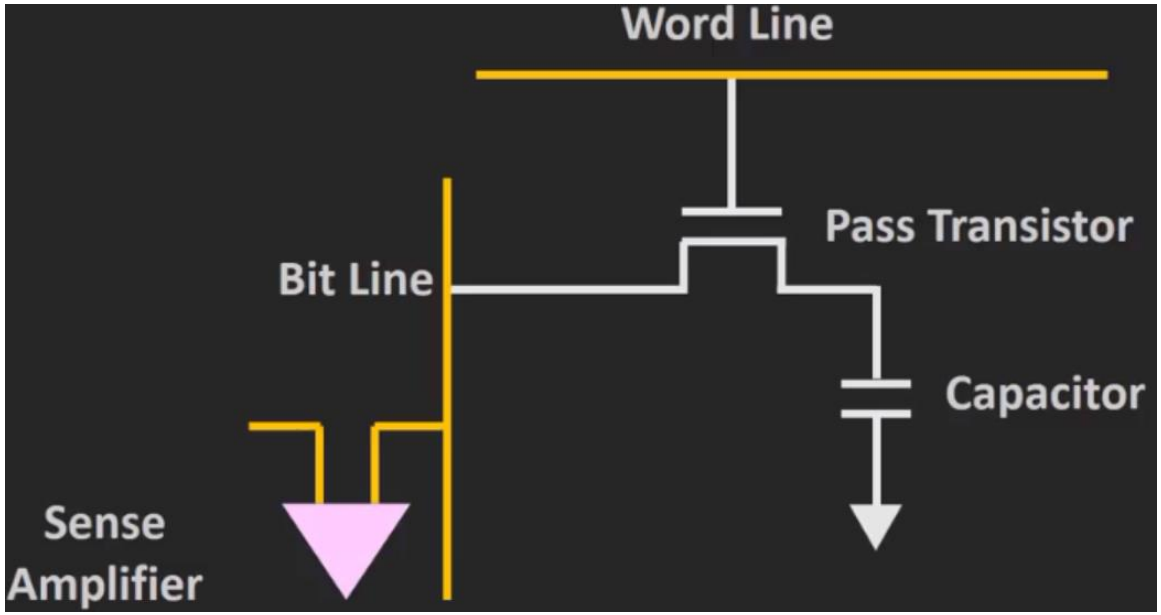
- When the transistor is OFF, the charge across the capacitor should remain as it is. So in ideal case the capacitor should not lose its charge. But in the actual case, there will be some leakage current and because of that the capacitor will lose it's charge gradually. For this reason, the dynamic cell requires the periodic **refresh cycles**. That's why it is called Dynamic RAM.

*https://downloads.reactivemicro.com/Electronics/DRAM/DRAM%20Refresh.pdf

One Bit DRAM Cell…

Read Operation

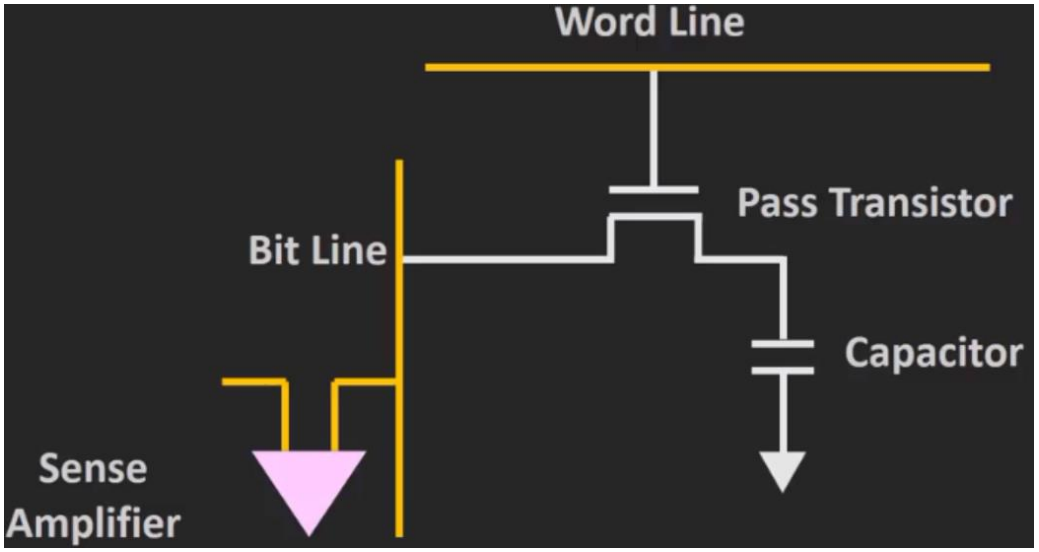
- First, the pass transistor should be turned ON. This can be done by applying voltage across the Word Line (WL).
- When voltage is applied on the WL, charge across the capacitor will be available at Bit Line (BL).
- Then using the Sense Amplifier, the voltage available at BL is read.



One Bit DRAM Cell…

Read Operation…

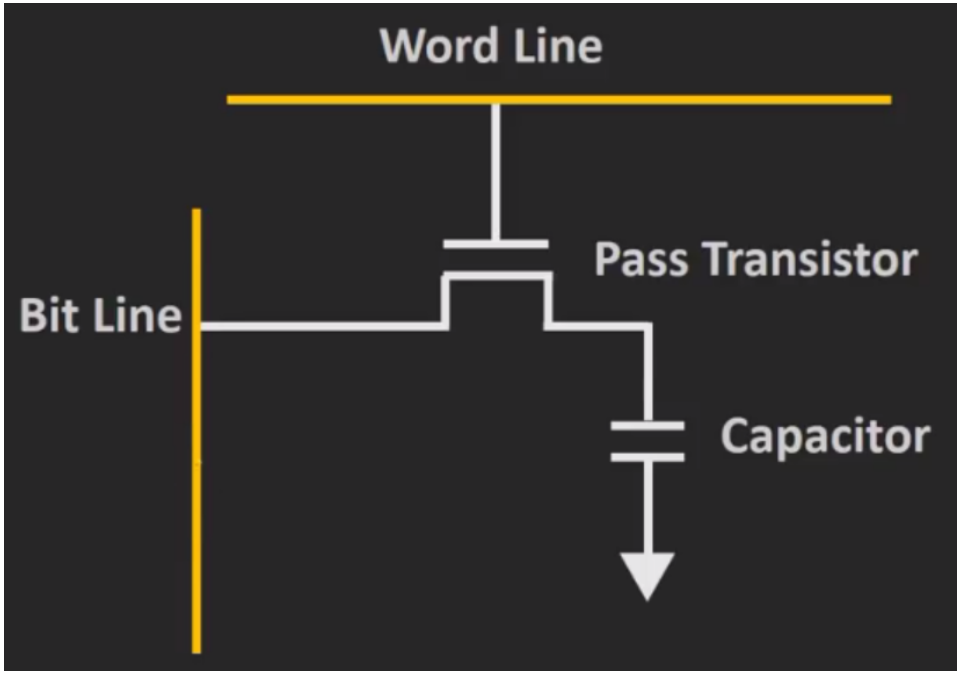
- **Increasing Read Speed:** Let, initially WL is ON, BL=0, Capacitor charge is 2V (logic 1). Then BL will receive 2V from 0V via Pass Transistor and read operation is done. But if BL is pre-charged such as 1V initially then it will receive voltage from 1V to 2V via pass transistor and read operation is done. This is faster than when BL=0 initially. That's way, pre-charging can increase read speed.



One Bit DRAM Cell…

Write Operation

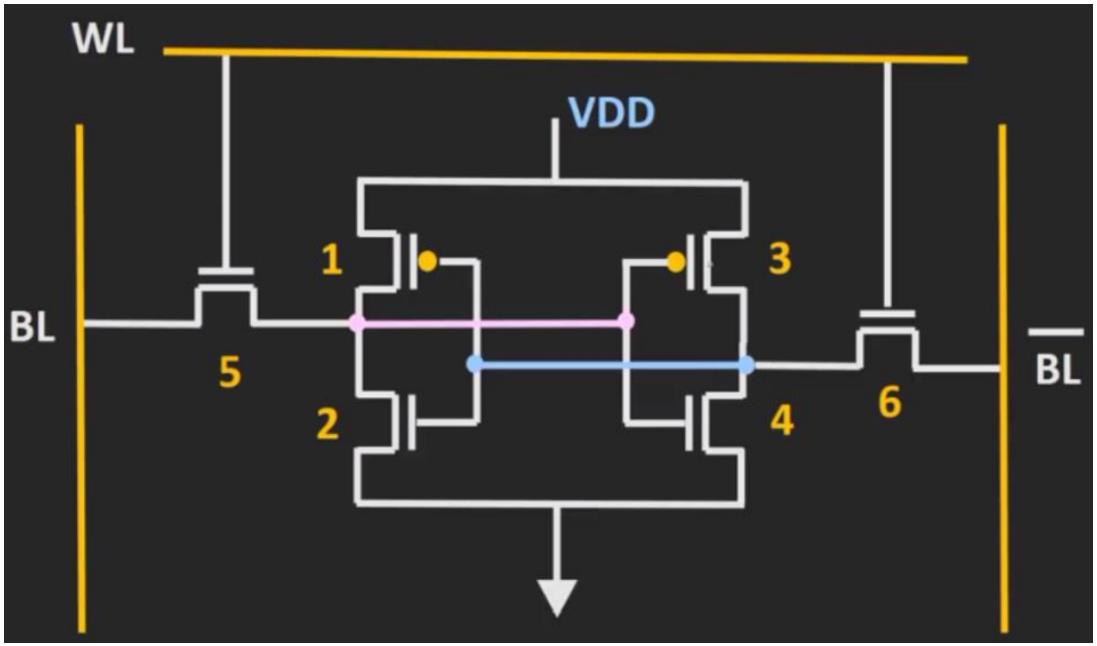
- During the read operation the BL is pre-charged to some finite value.
- Then the WL is set to High and the pass transistor is turned ON.
- Thus the voltage on BL will be moved to the capacitor through the pass transistor. That's way, Write Operation is performed.



SRAM Cell (6 Transistor)

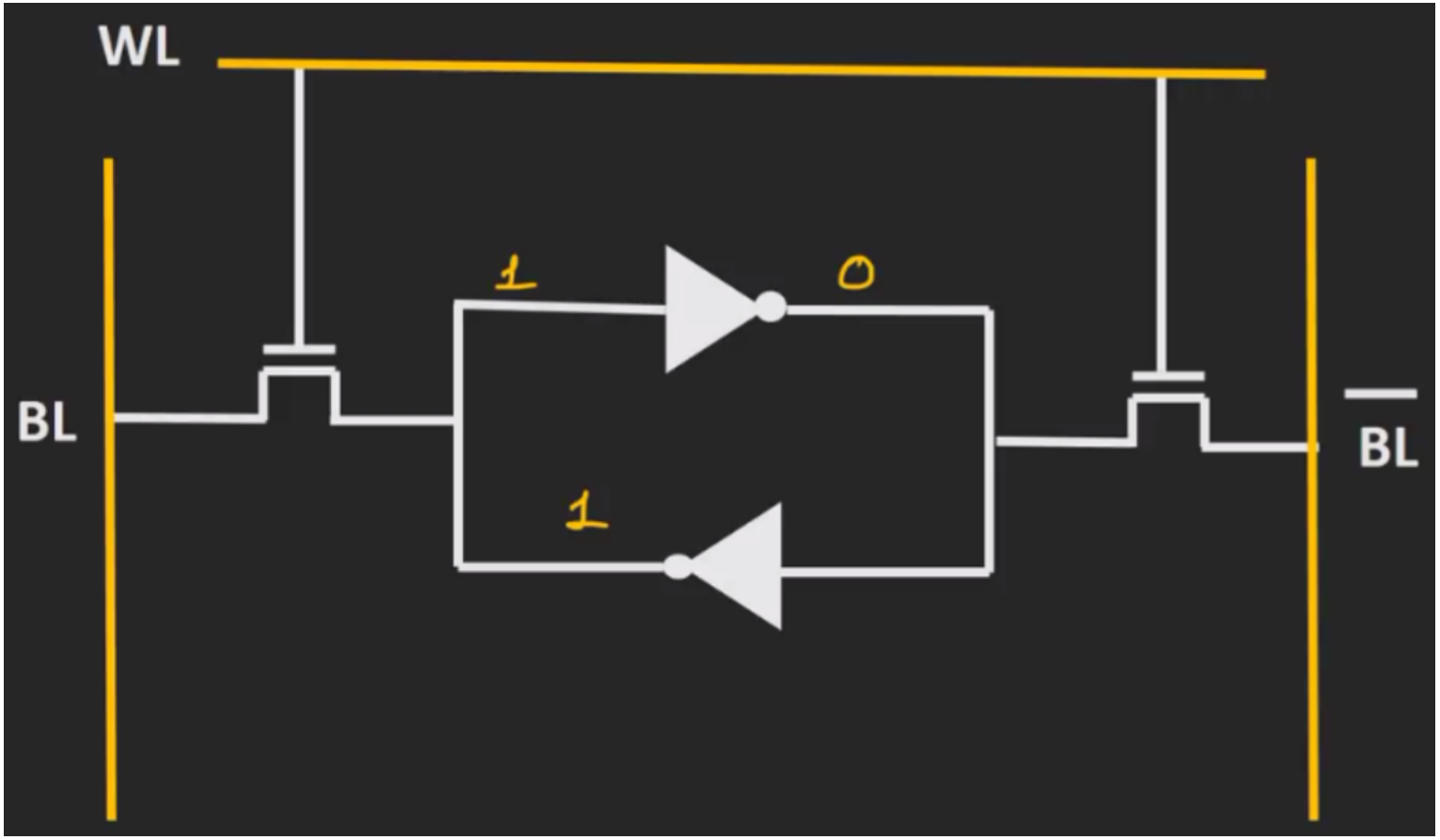
Internal Structure

- Consists of 6 transistors (T).
- Out of the 6T, two transistors are the pass transistors(5 & 6) which will give access to the BL.
- Remaining 4T are cross-coupled inverters. Transistor 1 and 2 form the 1st CMOS inverter; Transistor 3 and 4 form the 2nd CMOS inverter.



SRAM Cell (6 Transistor)…

Internal Structure (Simplified form)



SRAM Cell (6 Transistor)…

Internal Structure

- In case of SRAM Cell, the memory bit is stored between the two cross coupled inverters.

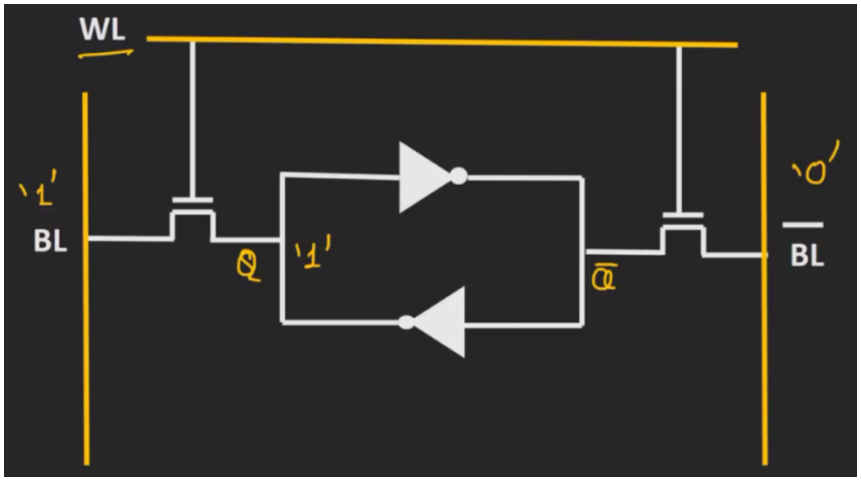
- Lets, if we have latched logical 1 then at the output of the 1st inverter will be logical 0. Again the output of the 2nd inverter will be logic 1.

- So, as far as the power is supplied to the SRAM, the logic 1 will be get circulated between the two inverters. Thus we do not require any kind of refresh cycles during the SRAM operation. That's why, called static RAM.

SRAM Cell (6 Transistor)…

Read Operation

- First of all, the two pass transistors are turned on applying High Voltage to the WL.
- When pass transistors are turned ON, whatever voltage at point Q will be available at BL and voltage at Q’ will be available at BL’.
- Then using the sense amplifier, we can sense the voltage difference between BL and BL’ and can read that voltage of SRAM Cell.



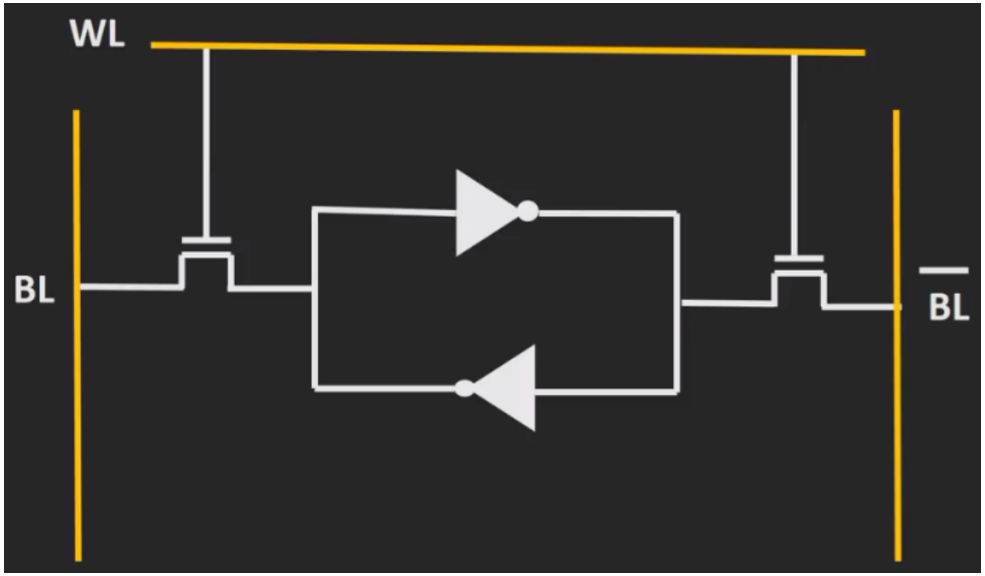
SRAM Cell (6 Transistor)…

Write Operation

- Whatever voltage is required to be written on the inverter pair, is to be applied on the BL.

- Lets, initially BL= logic 1, inverter pair contains logic 0, BL'= logic 0.

- When WL will be high, then inverter pair will be written by logic 1.



SRAM Vs DRAM

	SRAM (Static RAM)	DRAM (Dynamic RAM)
Usage	Cache Memory	Main Memory
Speed	Very Fast	Fast
Cost	Costly	Cheaper than SRAM
Density	Low	High

References

[1] https://www.youtube.com/watch?v=r787m_IaR1I&t=9s
[2] http://www.iosrjournals.org/iosr-jvlsi/papers/vol8-issue1/Version-1/E0801014346.pdf

Thanks