8254

Programmable Timer 8254

Internal structure

8254

D0
D1
D2
D3
D4
D5
D6
D7
$\overline{RD}$
WR
A0
A1
$\overline{CS}$
VCC
GND

CLK1
OUT 1
GATE 1

CLK1
OUT 1
GATE 1

CLK2
OUT 2
GATE 2

$D_0 - D_7$ — Date Bus Transfer

$\overline{RD}$
WR
A0
A1
$\overline{CS}$
— Read/Write Logic

Internal Bus

Control Word Register

Cnter 0 — CLK 0, OUT 0, GATE 0

Cnter 1 — CLK 1, OUT 1, GATE 1

Cnter 2 — CLK 2, OUT 2, GATE 2
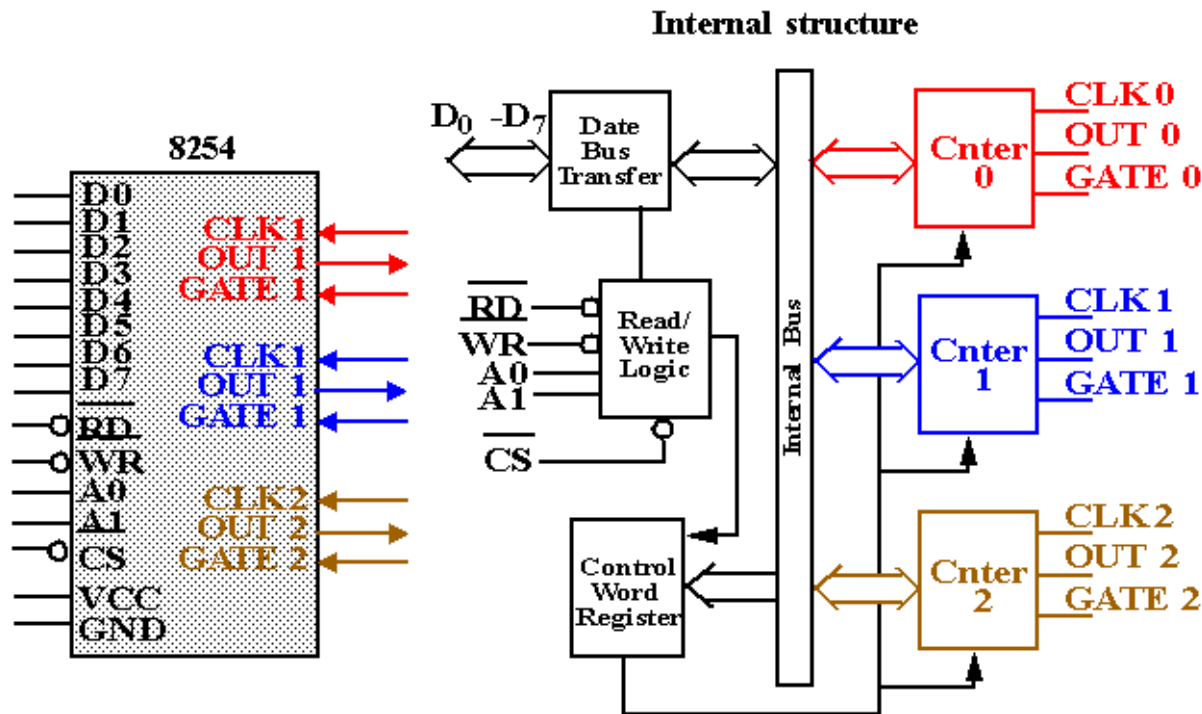
A_1	A_0	Function
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control Word

Timer and Counter (8254 IC)

Pin Diagram

Figure 5-1. 8253 Pin and Function Diagram
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Timer and Counter (8254 IC)
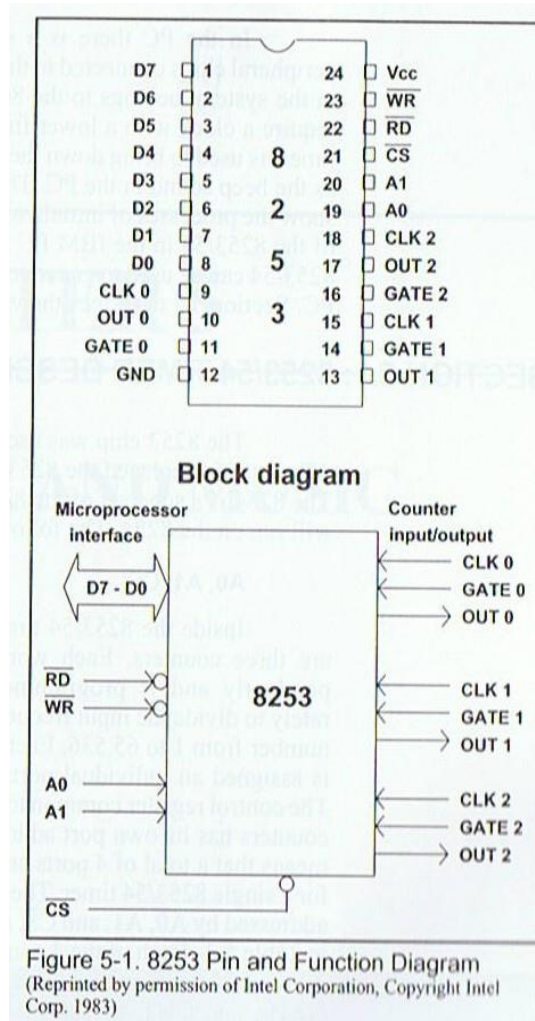
Counter Selection

THE CONTROL WORD REGISTER AND COUNTERS ARE SELECTED ACCORDING TO THE SIGNALS ON LINE A0 and A1 AS SHOWN BELOW
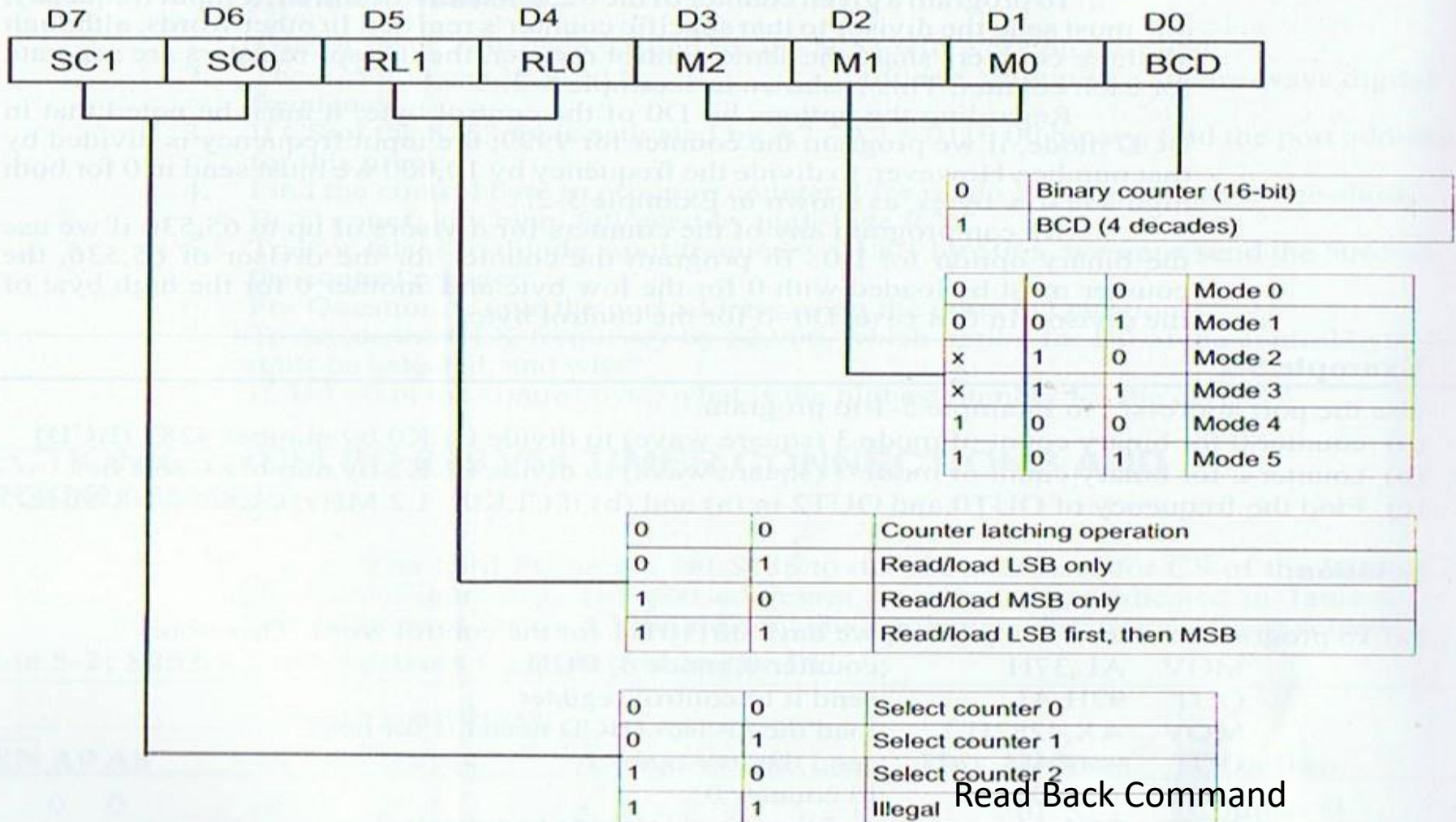
A1	A0	Selection
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control Register

Timer and Counter (8254 IC)

8254 Programming

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD

0	Binary counter (16-bit)
1	BCD (4 decades)

0	0	0	Mode 0
0	0	1	Mode 1
×	1	0	Mode 2
×	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

0	0	Counter latching operation
0	1	Read/load LSB only
1	0	Read/load MSB only
1	1	Read/load LSB first, then MSB

0	0	Select counter 0
0	1	Select counter 1
1	0	Select counter 2
1	1	Illegal

Read Back Command

Timer and Counter (8254 IC)

Figure 5-2. 8253/54 Control Word Format
(Reprinted by permission of Intel Corporation. Copyright Intel Corp. 1983)

Mode of Operation

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

Timer and Counter (8254 IC)

8253 / 8254 Timer

- Each of the three counter has 3 pins associated
  - CLK: input clock frequency

    8253: 0 ~ 2 MHz,   8254: 0 ~ 8 MHz

  - OUT: can be square wave, or one shot

  - GATE: Enable (high) or disable (low) the counter

- Data Pins: (D0 ~ D7)

  - Allow the CPU to access various registers inside the 8253/54 for both read and write operations. RD and WR are connected to IOR and IOW of control bus.

8253 / 8254 Timer

- Each of the three counters must be programmed separately

- Control byte must be first written into the control register. The 8253/54 must be initialized before use

- The programmer can not only write the value of the divisor into the 8253/54, but read the content of the counter at any given time as well

- All counters are down counters.

8253 / 8254 Timer

- To program a given counter to divide the CLK input frequency, one must send the divisor to that specific counter's register.

- Although all three counters share the same control register, the divisor registers are separate for each counter

- Example: given the port addresses for 8254:
  Counter 0: 80H   Counter 1: 81H

  Counter 2: 82H   Control Reg: 83H

Timer and Counter (8254 IC)

8254 Programming

- Each counter may be programmed with a count of 1 to FFFFH.

- Each counter has a program control word used to select the way the counter operates.

  - If two bytes are programmed, then the first byte (LSB) stops the count, and the second byte (MSB) starts the counter with the new count.

8254 Read Back Command

❑ 8254 Read Back Command

1	1	$\overline{COUNT}$	$\overline{STATUS}$	CNT2	CNT1	CNT0	0

❑ 8254 status word format

| OUTPUT	NULL COUNT	RW1	RW0	M2	M1	M0	BCD

8254 Modes

- **Mode 0: An events counter enabled with G.**
  - The output becomes a logic 0 when the control word is written and remains there until N plus the number of programmed counts.
  - Gate signal has to be high to initialize the count.
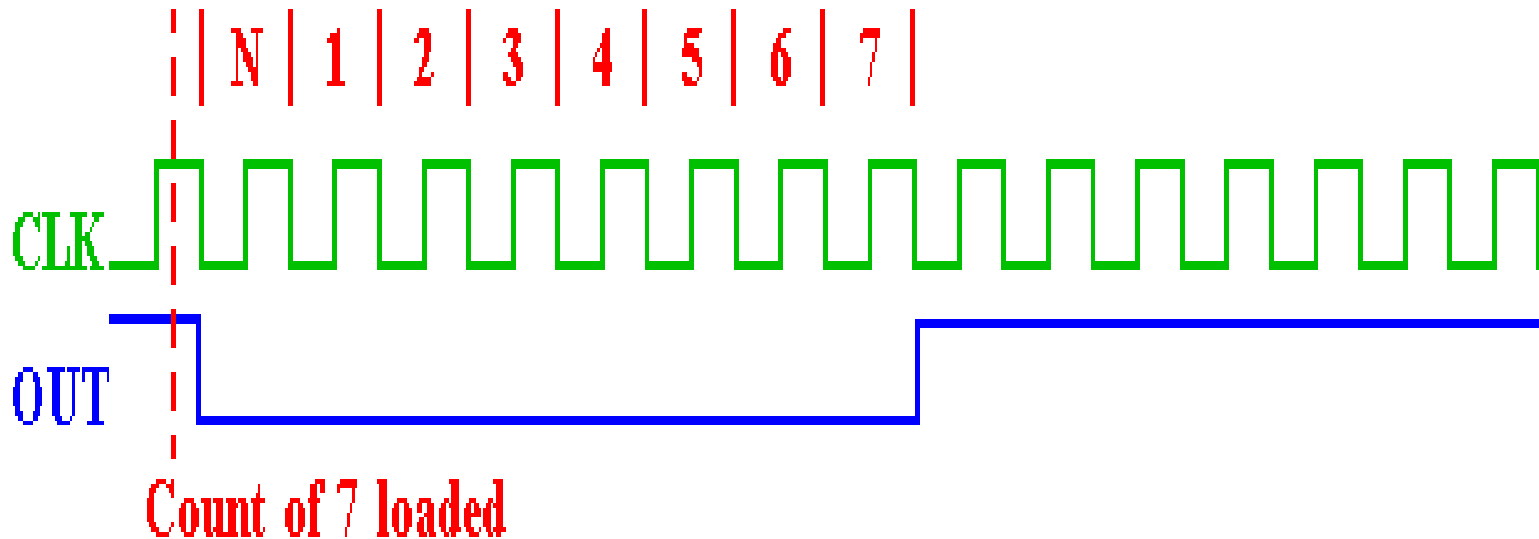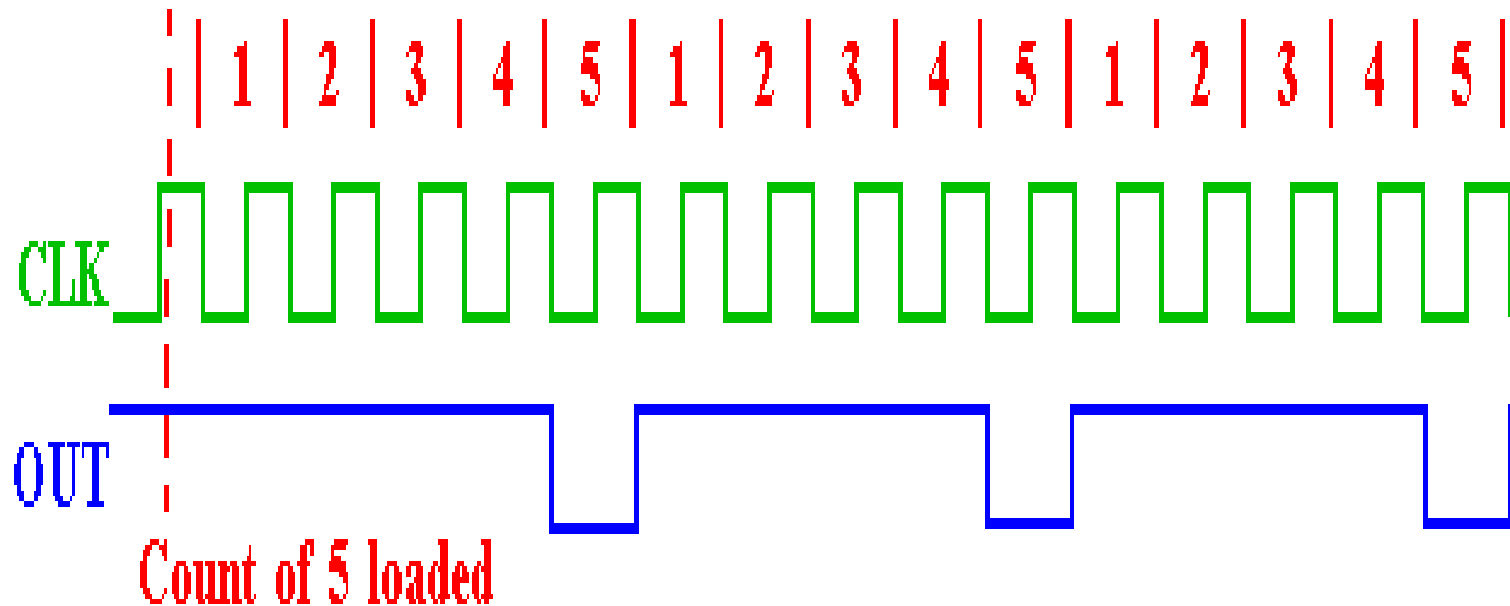
8254 Modes

Mode 1: One-shot mode.

- The G input triggers the counter to output a 0 pulse for `count' clocks.

- Counter reloaded if G is pulsed again.
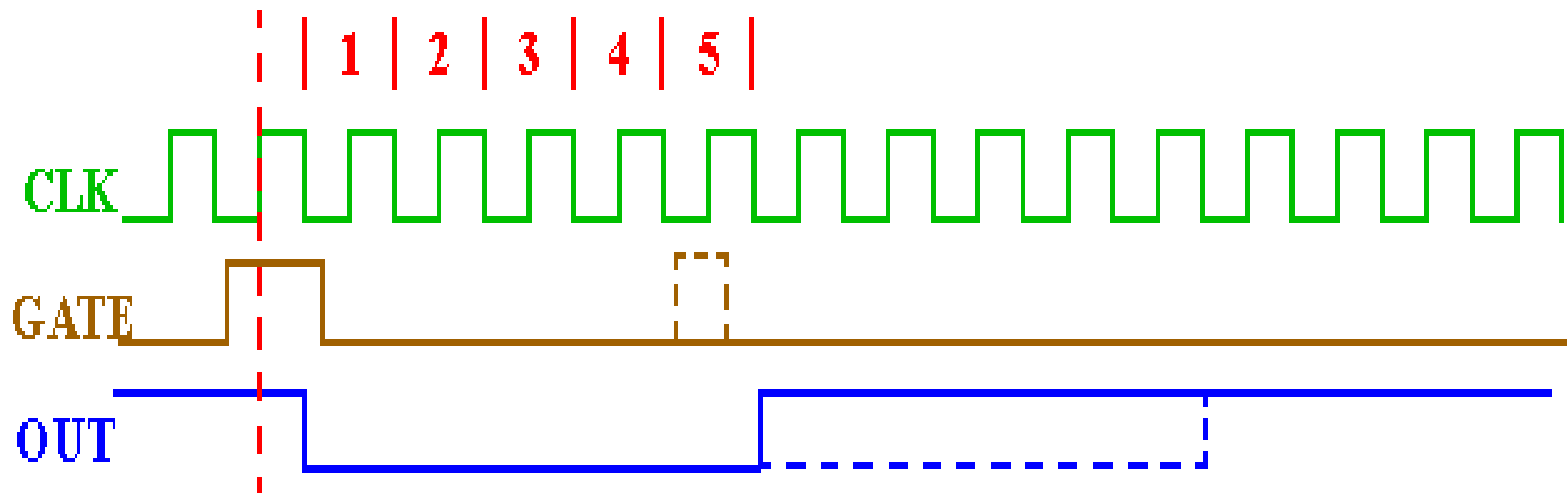
Trigger with count of 5

8254 Modes

- **Mode 2:Rate Generator**: Counter generates a series of pulses 1 clock pulse wide.
  - The seperation between pulses is determined by the count.
  - The cycle is repeated until reprogrammed or G pin set to 0. Reloaded


Count of 5 loaded

8254 Modes

– **Mode 3: Square Wave Generator:** Generates a continuous square-wave with G set to 1.
  - If count is even, 50% duty cycle otherwise OUT is high 1 cycle longer.

Timer and Counter (8254 IC)
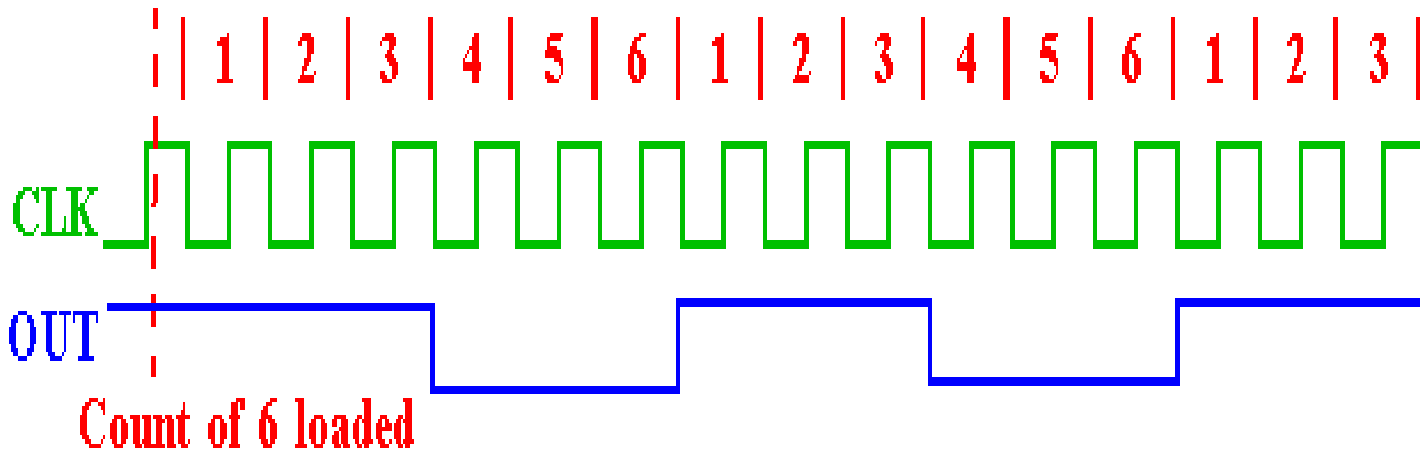
8254 Modes

- **Mode 4: Software triggered one-shot** (G must be 1). In this mode OUT is initially high; it goes low for one clock period at the end of the count. The count must be RELOADED - (*UNLIKE MODE 2)* for subsequent outputs.

Trigger with count of 8
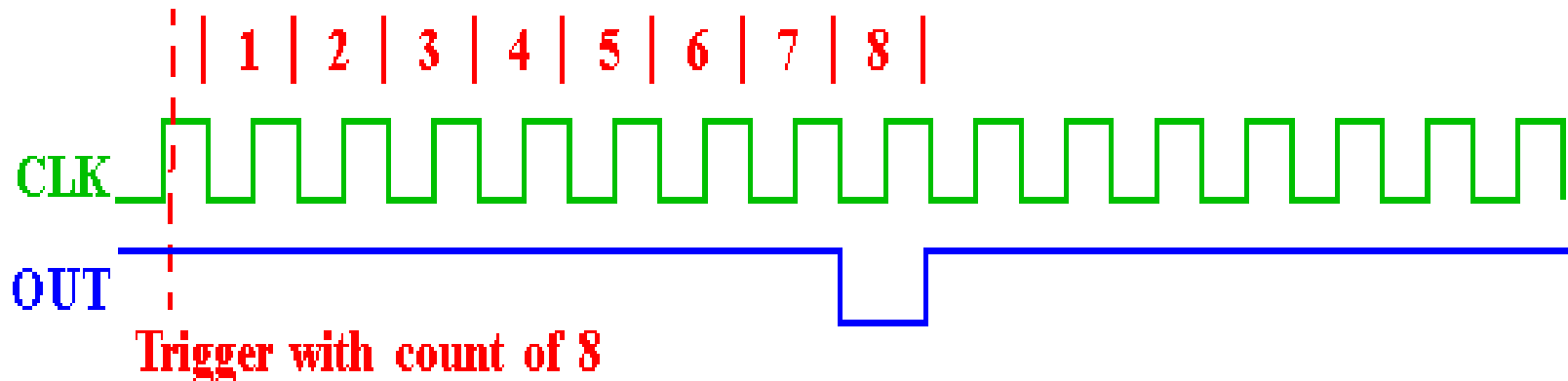
Mode 5

- This mode is similar to MODE 4 except that it is triggered by the rising pulse at the gate. Initially, the OUT is low and when the GATE pulse is triggered from low to high , the count begins. At the end of the count the OUT goes low for one clock period.