The Fabrication Process of CMOS Transistor

There was an era, where computers were such mammoth in size that to install them, easily a room space was required. But today they are so evolved that we can even carry them as notebooks easily. The innovation that made this possible was the concept of Integrated Circuits. In **Integrated Circuits**, a large number of active and **passive elements** along with their interconnections are developed over a small silicon wafer typically of 50 by 50 mils in cross section. The basic processes followed for production of such circuits include epitaxial growth, masked impurity diffusion, oxide growth, and oxide etching, using photolithography for making pattern.

The components over the wafer include resistors, transistors, diodes, capacitors etc… The most complicated element to manufacture over IC's is transistors. **Transistors are of various types** such as CMOS, BJT, FET. We choose the type of transistor technology to be implemented over an IC based on requirements. In this article let us get familiarized with the concept of **CMOS fabrication** (or) fabrication of transistors as CMOS.

CMOS Fabrication

For less power dissipation requirement **CMOS technology** is used for implementing transistors. If we require a faster circuit then transistors are implemented over **IC using BJT**. Fabrication of **CMOS transistors** as IC's can be done in three different methods.

The N-well / P-well technology, where n-type diffusion is done over a p-type substrate or p-type diffusion is done over n-type substrate respectively.

The **Twin well technology**, where **NMOS and PMOS transistor** are developed over the wafer by simultaneous diffusion over an epitaxial growth base, rather than a substrate.

The silicon On Insulator process, where rather than using silicon as the substrate an insulator material is used to improve speed and latch-up susceptibility.

N- well/ P- well Technology

CMOS can be obtained by integrating both **NMOS and PMOS transistors** over the same silicon wafer. In N–well technology an n-type well is diffused on a p-type substrate whereas in P- well it is vice- verse.

CMOS Fabrication Steps

The **CMOS fabrication process flow** is conducted using twenty basic fabrication steps while manufactured using N- well/P-well technology.

Making of CMOS using N well

Step 1: First we choose a substrate as a base for fabrication. For N- well, a P-type silicon substrate is selected.

Substrate

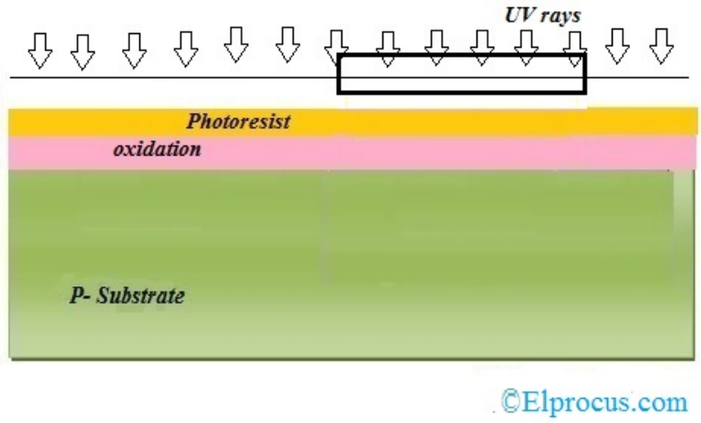
Step 2 – Oxidation: The selective diffusion of n-type impurities is accomplished using SiO2 as a barrier which protects portions of the wafer against contamination of the substrate. SiO_2 is laid out by oxidation process done exposing the substrate to high-quality oxygen and hydrogen in an oxidation chamber at approximately 1000^0c

Oxidation

Step 3 – Growing of Photoresist: At this stage to permit the selective etching, the SiO2 layer is subjected to the photolithography process. In this process, the wafer is coated with a uniform film of a photosensitive emulsion.

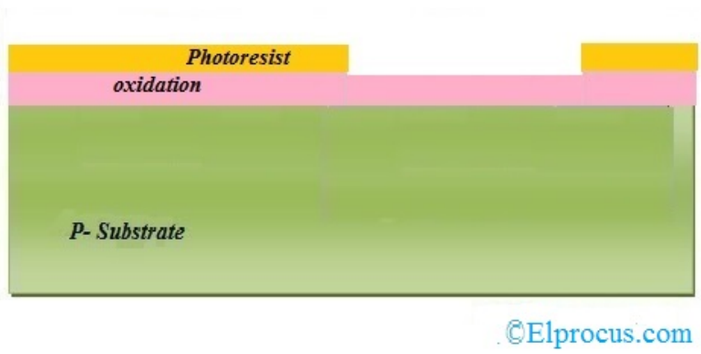
Growing of Photoresist

Step 4 – Masking: This step is the continuation of the photolithography process. In this step, a desired pattern of openness is made using a stencil. This stencil is used as a mask over the photoresist. The substrate is now exposed to **UV rays** the photoresist present under the exposed regions of mask gets polymerized.



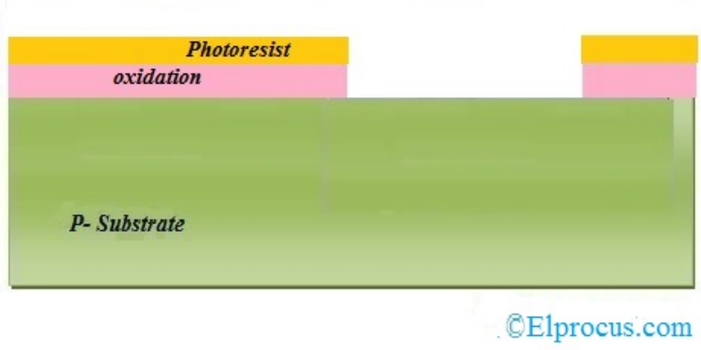
Masking of Photoresist

Step 5 – Removal of Unexposed Photoresist: The mask is removed and the unexposed region of photoresist is dissolved by developing wafer using a chemical such as Trichloroethylene.



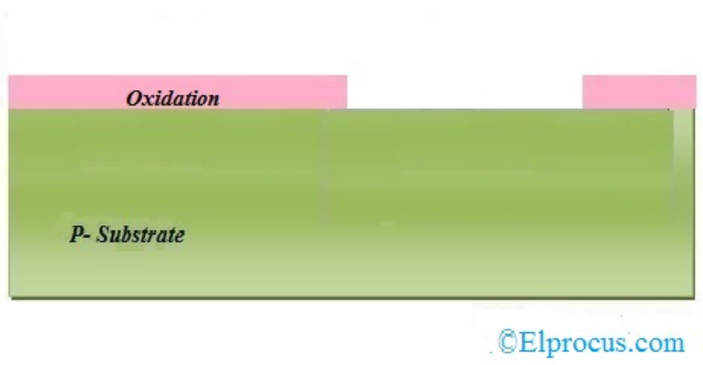
Removal of Photoresist

Step 6 – Etching: The wafer is immersed in an etching solution of hydrofluoric acid, which removes the oxide from the areas through which dopants are to be diffused.



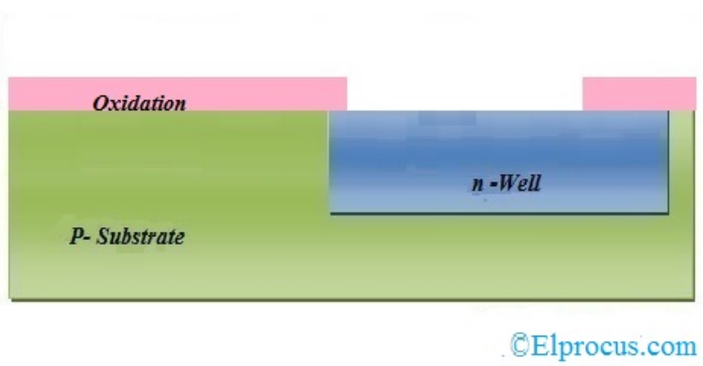
Etching of SiO2

Step 7 – Removal of Whole Photoresist Layer: During the **etching process**, those portions of SiO2 which are protected by the photoresist layer are not affected. The photoresist mask is now stripped off with a chemical solvent (hot H2SO4).



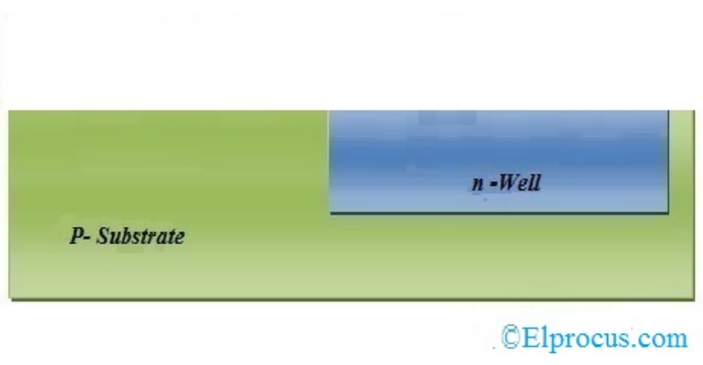
Removal of Photoresist Layer

Step 8 – Formation of N-well: The n-type impurities are diffused into the p-type substrate through the exposed region thus forming an N- well.



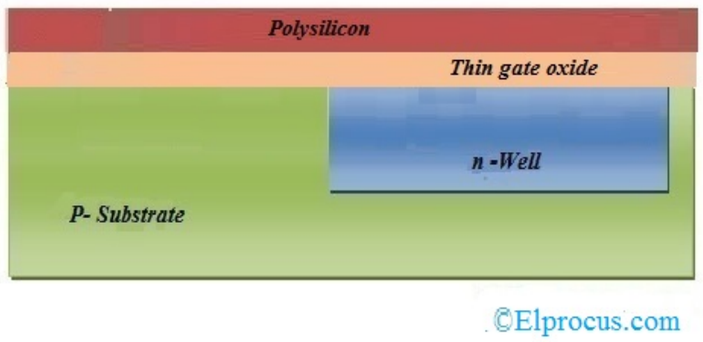
Formation of N-well

Step 9 – Removal of SiO2: The layer of SiO2 is now removed by using hydrofluoric acid.



Removal of SiO2

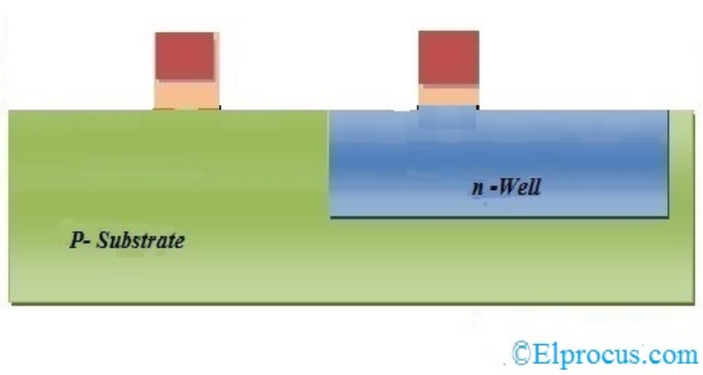
Step 10 – Deposition of Polysilicon: The misalignment of the gate of a **CMOS transistor** would lead to the unwanted capacitance which could harm circuit. So to prevent this “Self-aligned gate process” is preferred where gate regions are formed before the formation of source and drain using ion implantation.



Deposition of Polysilicon

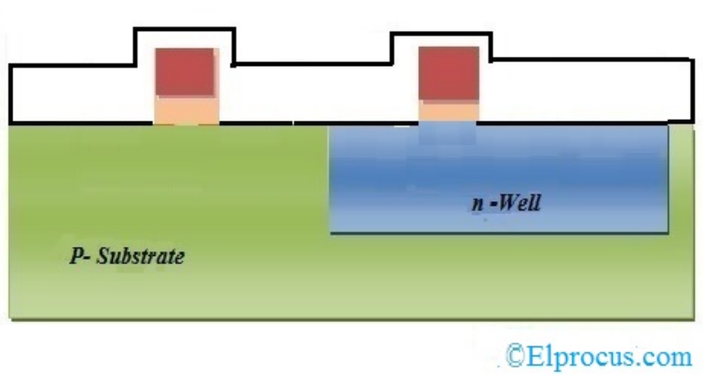
Polysilicon is used for formation of the gate because it can withstand the high temperature greater than 8000^0c when a wafer is subjected to annealing methods for formation of source and drain. Polysilicon is deposited by using **Chemical Deposition Process** over a thin layer of gate oxide. This thin gate oxide under the Polysilicon layer prevents further doping under the gate region.

Step 11 – Formation of Gate Region: Except the two regions required for formation of the gate for **NMOS and PMOS transistors** the remaining portion of Polysilicon is stripped off.



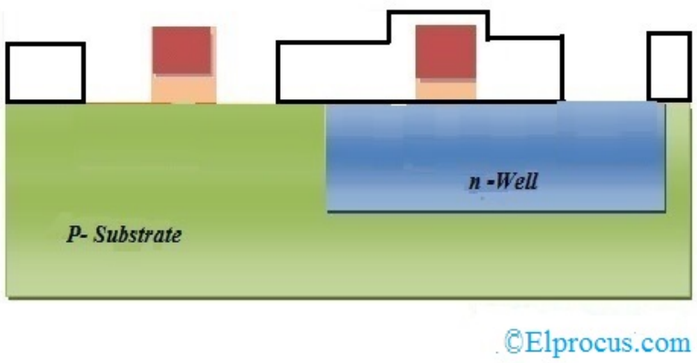
Formation of Gate Region

Step 12 – Oxidation Process: An oxidation layer is deposited over the wafer which acts as a shield for further **diffusion and metallization processes**.



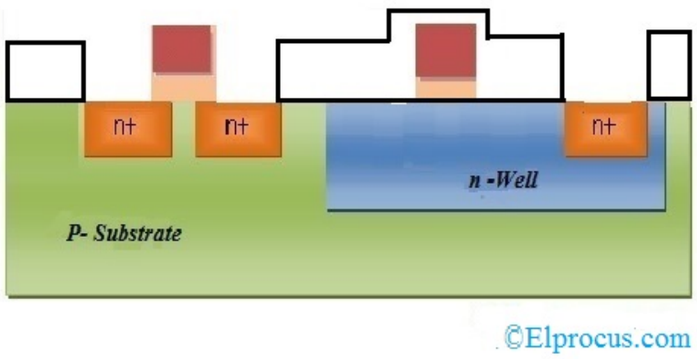
Oxidation Process

Step 13 – Masking and Diffusion: For making regions for diffusion of n-type impurities using masking process small gaps are made.



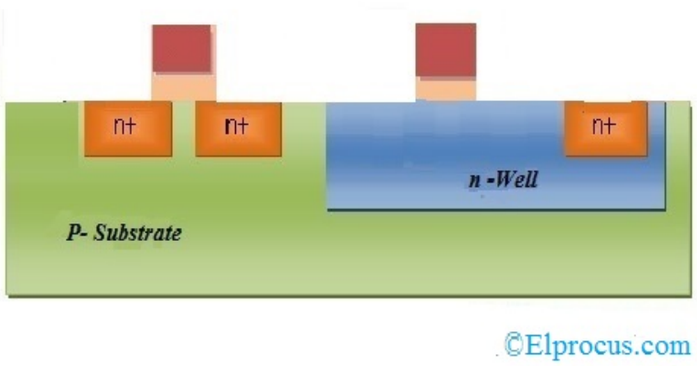
Masking

Using diffusion process three n+ regions are developed for the formation of terminals of NMOS.



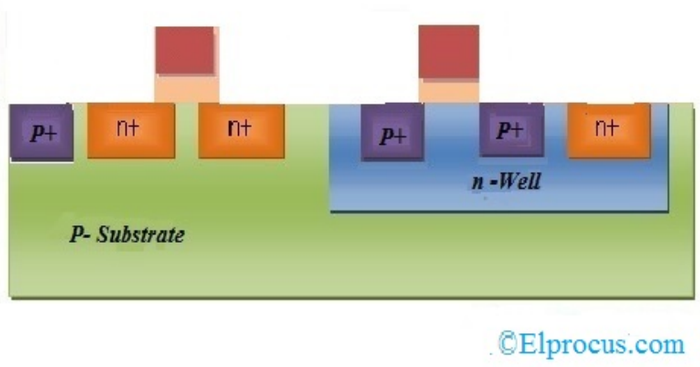
N-diffusion

Step 14 – Removal of Oxide: The oxide layer is stripped off.



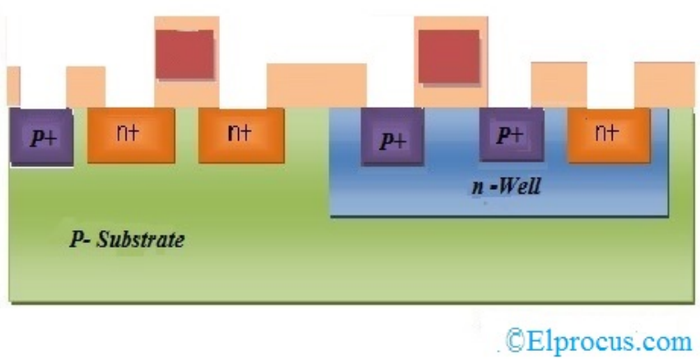
Removal of Oxide

Step 15 – P-type Diffusion: Similar to the n-type diffusion for forming the terminals of PMOS p-type diffusion are carried out.



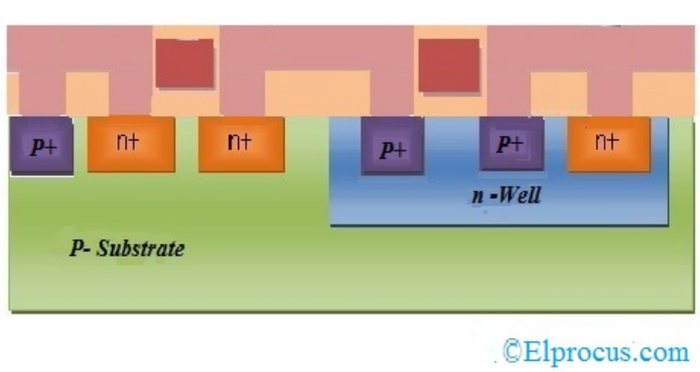
P-Type Diffusion

Step 16 – Laying of Thick Field oxide: Before forming the metal terminals a thick field oxide is laid out to form a protective layer for the regions of the wafer where no terminals are required.



Thick Field oxide Layer

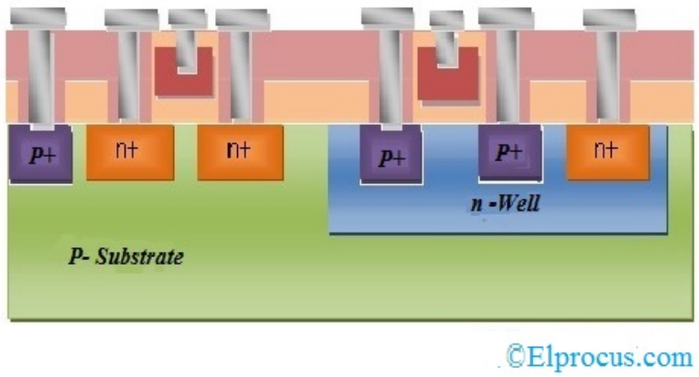
Step 17 – Metallization: This step is used for the formation of metal terminals which can provide interconnections. Aluminum is spread on the whole wafer.



Metallization

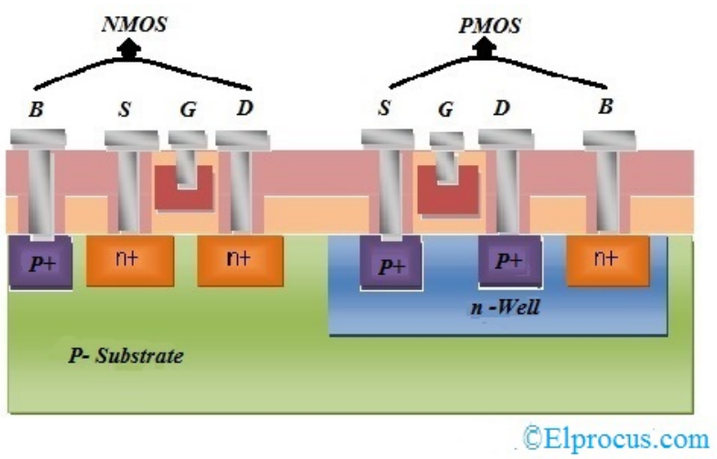
Step 18 – Removal of Excess Metal: The excess metal is removed from the wafer.

Step 19 – Formation of Terminals: In the gaps formed after removal of excess metal terminals are formed for the interconnections.



Formation of Terminals

Step 20 – Assigning the Terminal Names: Names are assigned to the terminals of **NMOS and PMOS transistors**.



Assigning Terminal names

Making of CMOS using P well Technology

The p-well process is similar to N well process except that here n-type substrate is used and p-type diffusions are carried out. For simplicity usually, N well process is preferred.

Twin Tube Fabrication of CMOS

Using Twin-tube process one can control the gain of P and N-type devices. Various steps involved in the **fabrication of CMOS using Twin-tube method** are as follows

- A lightly doped n or p-type substrate is taken and the epitaxial layer is used. Epitaxial layer protects the latch-up problem in the chip.
- The high purity silicon layers with measured thickness and exact dopant concentration are grown.
- Formation of tubes for P and N well.
- Thin oxide construction for protection from contamination during diffusion processes.
- Source and drain are formed using ion implantation methods.
- Cuts are made for making portions for metal contacts.
- Metallization is done for drawing metal contacts

CMOS IC Layout