Muthu Adithya Ramnarayanan

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Education

Georgia Institute of Technology — Atlanta, GA
MS. Electrical and Computer Engineering — *Aug. 2024 – Dec 2026*

University of Wisconsin - Madison — Madison, WI
BS. Computer Engineering — *Aug. 2021 – May 2024*

Technical Skills

Languages: SystemVerilog, Embedded C, C/C++, CUDA, Python, Java, Bazel
Tools: UVM, FreeRTOS, git, gdb, bash, Cadence Virtuoso, Synopsys ICC, Questa, Quartus, Xilinx
Coursework: Generative and Geometric Deep Learning, Computer Architecture, VLSI, Digital Circuits and Components, Digital System Design and Synthesis, Embedded Systems and Microprocessors, Algorithms, Parallel Programming, Operating Systems, Matrix Methods in Machine Learning, Artificial Neural Networks

Experience

RISC-V Cores Intern — Jan. 2025 – Aug 2025
Tenstorrent — *Austin, TX*

- Brought up ascalon single-core design on an emulation platform, optimizing for hardware resource utilization
- Built working custom Linux kernel with OpenSBI and UART polling for embedded systems
- Optimized DOOM game graphics rendering in C++ using frame buffers and memory-efficient data structures
- Wrote C++/SystemVerilog testbenches for customer memory subsystem validation

Researcher — Sept. 2024 – Jan 2025
Georgia Institute of Technology — *Atlanta, GA*

- Implemented and enhanced GNNBuilder, a high level framework to convert Graph Neural Networks to FPGA designs for improved inference performance
- Worked with Xilinx Vitis HLS to synthesize, profile and debug high level designs for deadlocks, logical errors and caching errors
- Experimented with pipelining, caching and Out-of-order execution for current SOTA GNNs

Software Engineer — Sept. 2024 – Jan 2025
Elvo AI — *San Francisco, CA*

- Architected and delivered Elvo AI's AWS tech stack, including authentication and auto-scaling
- Developed the first frontend in Next.js, then transitioned to a mobile-first approach with Expo
- Implemented scalable databases to support rapid growth and high availability
- Designed ML pipelines and automated agentic workflows to optimize operational efficiency by 30%

Undergraduate Student Researcher — Mar. 2023 – May 2024
University of Wisconsin - Madison — *Madison, WI*

- Built a 10MHz (±25Hz) digital modulator/demodulator as a part of an IARPA project
- Designed and implemented pipelined versions of hardware ASK, BPSK and MFSK modulation for RF antennas
- Enhanced FPGA designs for improved clock stability and developed more accurate digital PWM designs

Projects

Embedded ML Inference System | *Embedded C, Device Drivers, RISC-V, ML* — May 2024 – Aug 2024

- Designed a custom RISC-V CPU using SystemVerilog featuring specialized ML instruction sets, enhancing inference performance
- Implemented and Profiled open-source RISC-V C compiler with new instruction sets for improved efficiency
- Developed robust driver software for seamless integration of camera input and peripheral devices
- Achieved 30% reduction in inference time for imagenet model with a similar base RISC-V CPU