Amplifier Circuit Design in LTSpice® and DesignSpark PCB®

Level 3 Electronics and Communication

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Abstract

A TI LM386 audio amplifier circuit was designed to drive an 8 Ω speaker, with a maximum gain of 35 dB and maximum bass boost of 6 dB without clipping a 65 dBSPL input. First the schematic was simulated in LTSpice® to ensure the design met the specification. Secondly a layout was formulated using DesignSpark PCB®.

1 Schematic design

Figure 1 provides an overview of the system the amplifier circuit was designed for.

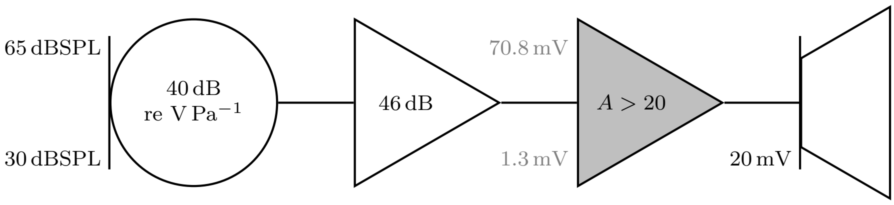

Figure 1: System block diagram, indicating minimum and maximum inputs to the system and amplifier circuit A.

The LM386 datasheet described how to implement much of the circuit in Figure 2 [1].

Contrary to the datasheet, the schematic included no Boucherot cells as the load had no inductive component. The DC decoupling capacitors were chosen to be suitably large to avoid significantly filtering frequencies above 20 Hz. C2 was originally 2200 µF, but had to be reduced due to PCB size constraints. The schematic also includes two supply bypass capacitors to filter noise on the 12 V line.

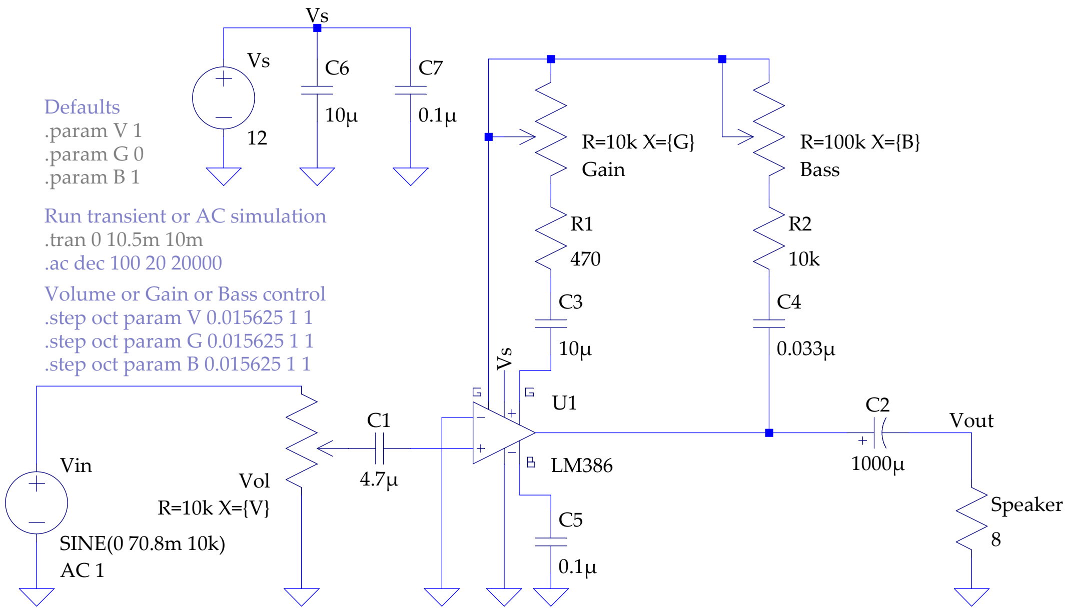

Figure 2: Audio amplifier LTSpice® schematic.

A potentiometer provided volume control without distorting the gain response by attenuating the amplifier input. This can be seen in Figure 3.

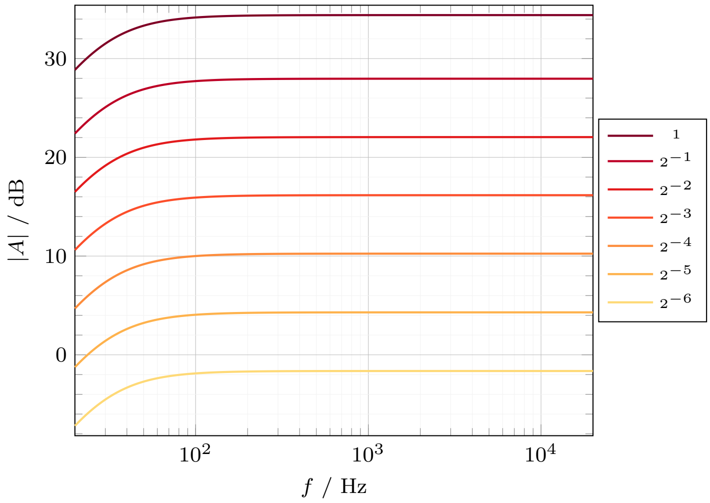

Figure 3: Bode plot of amplifier gain as volume potentiometer varies logarithmically. Set with maximum gain and minimum bass boost.

In simulation, bypassing pins 1 and 8 with a purely capacitive load resulted in clipping for the 70.8 mV input. The 46 dB maximum gain was limited to 35 dB by placing R1 in series with POT2. Varying POT2 varied the gain loop resistance from 470 Ω to 10 470 Ω, decreasing the gain as indicated in Figure 4. At 35 dB, the output was undistorted, as evidenced by Figure 5.

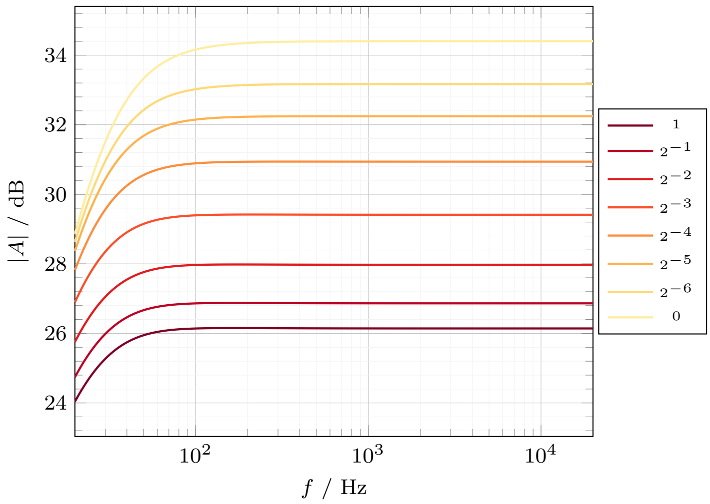

Figure 4: Bode plot of amplifier gain as gain potentiometer varies logarithmically. Set with maximum volume and minimum bass boost.

The datasheet describes how a 10 kΩ resistor is required to boost bass by 6 dB. In simulation, increasing the series resistance reduced this effect. A 100 kΩ potentiometer was sufficient to effectively open circuit the bass boost branch. Figure 6 illustrates the 0 dB to 6 dB boost at 80 Hz.

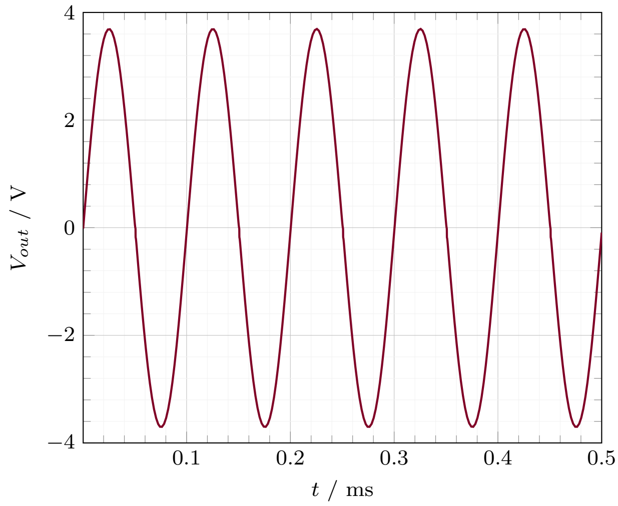

Figure 5: Maximum output voltage across speaker in response to the maximum input voltage—65 dBSPL, 10 kHz.

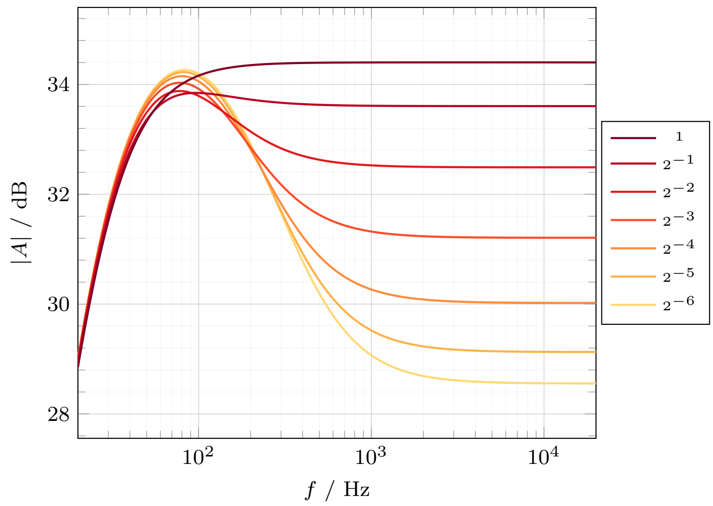

Figure 6: Bode plot of amplifier gain as bass boost potentiometer varies logarithmically. Set with maximum volume and gain.

2 PCB design

Table 1 lists the components used to implement the schematic. A large package was used for the input decoupling capacitor to mitigate the capacitance change in X7R capacitors subjected to DC biases. A C0G capacitor was used for the bass boost capacitor, as simulations showed the voltage across this component varied wildly and C0G capacitors have no DC response.

Table 1: Bill of materials.

Ref	Description	Package	Manufacturer number	RS number
C1	4.7 µF, 25 V, X7R cap	1210	KEMET C1210C475K3RACTU	691-1256
C2	1000 µF, 25 V, Al cap	FK–H	Panasonic EEVF1KE102Q	708-3434
C3	10 µF, 10 V, X7R cap	0805	KEMET C0805C106K8RACTU	802-9854
C4	0.033 µF, 25 V, C0G cap	0805	KEMET C0805C333J3GACTU	(*Farnell*)
C5,7	0.1 µF, 25 V, X7R cap	0603	KEMET C0603C104J3RACTU	801-5237
C6	10 µF, 25 V, X7R cap	1206	KEMET C1206C104K3RACTU	802-9977
JACK1	3.5 mm, stereo jack	thru	Swithcraft 35RAPC2BV4	(*Farnell*)
POT1,2	10 kΩ, logarithmic pot	thru	Bourns 91A1A-B28-D15L	522-5153
POT3	100 kΩ, logarithmic pot	thru	Bourns 91A1A-B28-D20L	522-5175
R1	470 Ω, 50 V, resistor	0603	Panasonic ERJPA3F4700V	826-6966
R2	10 kΩ, 50 V, resistor	0603	Panasonic ERJPA3F1002V	826-6704
U1	LM386 audio amplifier	SOIC	TI LM386M-1/NOPB	536-1366

Custom PCB symbols were created for the Panasonic FK-series size-H package [2]; the stereo jack [3] and the potentiometers [4].

To ensure all traces were sufficiently wide, the maximum current through each branch was simulated. The trace widths are listed in Table 2. 10 mil was the nominal width, whilst 15 mil was for the supply, ground and output traces to minimise voltage drop. These can be seen in Figure 7.

Table 2: Trace width calculations due to maximum current with 25 V supply, 1 oz/ft^2 trace, 10 °C temperature rise at 25 °C.

Branch	$f_{I_{\max}}$ / Hz	I_{max} / mA	Width / mil
Vs	85	470	4.2
Vin	33	0	0.0
C1	24	0	0.0
C2	85	500	4.6
C3	20000	110	0.5
C4	20000	170	1.0
C5	20000	0	0.0
C6	20000	0	0.0
C7	20000	0	0.0
U1.1	20000	65	0.3

The larger bypass capacitor C6 was placed as close to the supply as possible, whilst bypass capacitors C5 and C7 were placed close to the LM386. The input, output and LM386 were each given their own ground to limit interference. The input and output return paths follow the outward path on the other side of the board and the gain and bass boost loops were also minimised.

The board was optimised for size and number of vias: measuring 2060 by 1280 mil, with 0 vias.

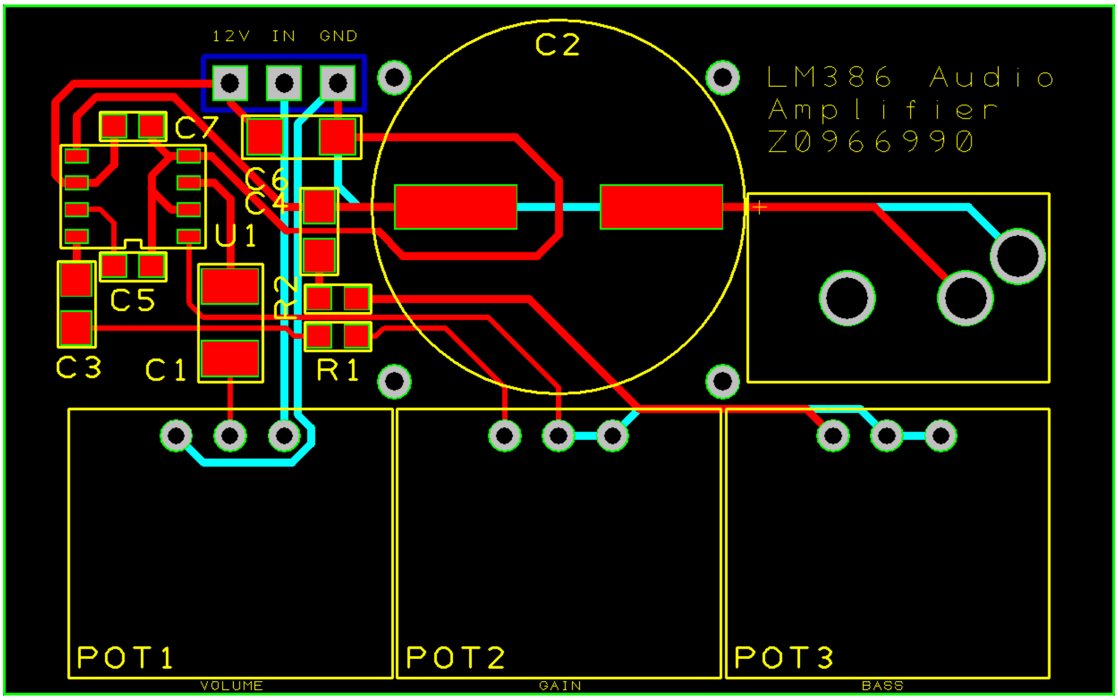

Figure 7: Audio amplifier DesignSpark PCB® layout.

References

[1] SNAS545C, Rev. C, Texus Instruments, 2017.

[2] DME0000COL92, Rev. A, Panasonic, 2017.

[3] 35RAPC$_{V4}$, Rev. G, Switchcraft, 2015.

[4] 9XAXA, Rev. 05/13, Bourns, 2013.