Ryan Dang

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EDUCATION

Brown University, *B.S. Computer Engineering, GPA 4.0* Expected Graduation May 2027

- Relevant Courses: Digital Design, Computer Systems, Dynamics and Vibrations, Calculus II & III, Object Oriented Design, Data Structures and Algorithms, Electricity and Magnetism, Linear Algebra, Circuits, Embedded Systems

EXPERIENCE

IEEE Solid-State Circuits Society Chipathon June 2025 - Present

Digital Building Block Designer Remote

- Designing 4-input MUX, 3-input AND, and 4-input OR standard cells for the **GF180MCU** open-source PDK, contributing to digital design automation using **LLM-driven** RTL-to-GDSII workflows

Wright State University Research Experience for Undergraduates (REU) June 2025 - August 2025

Hardware Security Research Intern Dayton, OH

- Implemented a Ring Oscillator Network (RON) on a **Basys 3** FPGA in **Vivado** for hardware Trojan detection using side-channel analysis and measuring frequencies to detect localized power anomalies
- Applied machine learning (SVM and Random Forest) with **scikit-learn** and **pandas** to detect hardware Trojans, improving prior results (97.4% → 98.8% accuracy, 7.1% → 0% FPR) and an F1 score of 0.986 for Trojan-free detection

Brown University Engineering Department January 2025 - May 2025

Dynamics and Vibrations Teaching Assistant Providence, RI

- Led office hours for **20+** students to clarify concepts in kinematics, force balance, and harmonic motion

AA Technology May 2024 - July 2024

PCB Manufacturing Engineer Intern Ronkonkoma, NY

- Increased conformal coating throughput by **1.5x** by optimizing motion paths and programming for a robotic arm
- Achieved a **5%** reduction in lead time by interpreting PCB schematics, developing a bill of materials in **Excel,** and cross-referencing customer part specifications with datasheets to ensure accuracy with design requirements

PROJECTS

UDP Packet Processor Present

- Developing a packet processor on an FPGA, enabling line-rate parsing, checksum verification, and header extraction

FPGA Pong Game December 2024 - January 2025

- Implemented Pong on a **Basys 3** FPGA, using **Verilog** to create modular components for paddle control, ball movement, VGA display synchronization, game state tracking, and **UART** TX/RX for serial communication

Tetris and Custom Controller January 2024 - February 2024

- Developed a Tetris clone from scratch in **Java** with custom game logic, collision detection, scoreboard, and a physical controller using a custom PCB (**Altium**) and 3D-printed housing (**Fusion 360**)

ACTIVITIES

Engineering Department Undergraduate Group Providence, RI

Events Coordinator October 2024 - Present

- Increased Engineering Week engagement by **30%** through interactive events, such as trivia night and Lego challenges

Brown Formula Racing Providence, RI

Electrical Engineer January 2024 - Present

- Reduced wiring complexity and volume by **10%** by redesigning the power distribution system via a custom PCB
- Placed **top 20** in the US, assembled a custom wiring harness for the car using DTM and ring connectors

SKILLS

Technical: FPGA, PCB Design, x86, I2C, SPI, UART, UDP
Languages/Tools: Verilog, C/C++, Python, Java, Vivado, Lattice Diamond, Altium, LTSpice, Linux, Docker, Git
Instruments: Oscilloscope, Signal Analyzer, Waveform Generator, Multimeter
Interests: Brown Men's Volleyball, Piano, Guitar, Biking