Curriculum Vitaé

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Education:

Center for Advanced Computer Studies, University of Louisiana, Louisiana
1986: Ph.D. in Computer Science

R.E.C. Rourkela, Sambalpur University, INDIA
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B.I.T. Sindri, Ranchi University, INDIA
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Experience:

The Pennsylvania State University (1997–present), Pennsylvania
Professor, Department of Computer Science and Engineering

The Pennsylvania State University (1992–1997), Pennsylvania
Associate Professor, Department of ECE and Computer Science and Engineering

The Pennsylvania State University (1986–1992), Pennsylvania
Assistant Professor, Department of Electrical and Computer Engineering

University of Louisiana (1983–1986), Louisiana
Research/Teaching Assistant, The Center for Advanced Computer Studies

Indian Institute of Technology (1981–1983), Kharagpur, India
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Research Interests:

Parallel & distributed computer architectures; network of workstations (NOWs)/clusters; communication networks & communication mechanisms; resource management (scheduling); multi-core/SoC architectures; QoS support in clusters and Internet; performance evaluation; fault-tolerant computing; mobile computing; multimedia systems.

Journal Papers

1. Das, C. R. and L. N. Bhuyan, "Bandwidth Availability of Multiple-Bus Multiprocessors," *IEEE Transactions on Computers*, Special Issue on Parallel Processing, pp. 918-926, October 1985.
2. Das, C. R., L. N. Bhuyan, and V. V. S. Sarma, "Effect of Maintenance on the Dependability and Performance of Multiprocessor Systems," *IEEE Transactions on Reliability*, Special Issue on Fault Tolerant Computing, pp. 208-215, June 1987.
3. Das, C. R. and L. N. Bhuyan, "Reliability and Fault-Tolerance Issues of Multiprocessor and Multicomputer Systems," (Invited Paper) in Sadhana, *Journal of Indian Academy of Sciences*, pp. 129-154, October 1987.
4. Das, C. R. and L. N. Bhuyan, "Dependability Evaluation of Interconnection Networks," *Information Sciences: An International Journal*, 43(1/2):107-138, October 1987.
5. Kim, J., C. R. Das, W. Lin, and T.-Y. Feng, "Reliability Evaluation of Hypercube Multicomputers," *IEEE Transactions on Reliability*, Special Issue on Reliability of Parallel and Distributed Computing Networks, pp. 121-129, April 1989.
6. Lin, W., T. L. Sheu, C. R. Das, T.-Y. Feng, and C. L. Wu, "A Conflict-Free Routing Scheme on Multistage Interconnection Networks," *IEEE Transactions on Computers*, 38(8):1086-1097, August 1989.
7. Das, C. R., J. T. Kreulen, M. J. Thazhuthaveetil, and L. N. Bhuyan, "Dependability Modeling for Multiprocessors," *IEEE Computer*, 23(10):7-19, October 1990.
8. Kim, J., C. R. Das, and W. Lin, "A Top-Down Processor Allocation Scheme for Hypercube Computers," *IEEE Transactions on Parallel and Distributed Systems*, 2(1):20-30, January 1991.
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10. Das, C. R. and J. Kim, "A Unified Task-Based Dependability Model for Hypercube Computers," *IEEE Transactions on Parallel and Distributed Systems*, 3(3):312-324, May 1992.
11. Das, C. R., P. Mohapatra, L. Tien, and L. N. Bhuyan, "An Availability Model for MIN-Based Multiprocessors," *IEEE Transactions on Parallel and Distributed Systems*, pp. 1118-1129, October 1993.
12. Mohapatra, P., C. R. Das, and T.-Y. Feng, "Performance Analysis of Cluster-Based Multiprocessors," *IEEE Transactions on Computers*, 43(1):109-114, January 1994.
13. Yang, M. K. and C. R. Das, "A Parallel Branch-and-Bound Algorithm On a Class of Multiprocessors," *IEEE Transactions on Parallel and Distributed Systems*, 5(1):74-86, January 1994.
14. Kim, J. and C. R. Das, "Hypercube Communication Delay with Wormhole Routing," *IEEE Transactions on Computers*, 43(7):806-814, July 1994.
15. Yousif, M. S., C. R. Das, and M. J. Thazhuthaveetil, "A Cache Coherence Protocol for MIN-based Multiprocessors," *Journal of Supercomputing*, 8:163-185, August 1994.
16. Yu, C. S. and C. R. Das, "Disjoint Task Allocation Algorithms for MIN Machines with Minimal Conflicts," *IEEE Transactions on Parallel and Distributed Systems*, 6(4):373-387, April 1995.
17. Mohapatra, P., C. Yu, and C. R. Das, "A Lazy Scheduling Scheme for Hypercube Computers," *Journal of Parallel and Distributed Computing*, 27(1):26-37, May 1995.
18. Mohapatra, P. and C. R. Das, "On Dependability Evaluation of Mesh Connected Systems," *IEEE Transactions on Computers*, 44(9):1073-1084, September 1995.

19. Sheu, T.-L., W. Lin, and C. R. Das, "Distributed Fault Diagnosis in Multistage Network-Based Multiprocessors," *IEEE Transactions on Computers*, 44(9):1085-1095, September 1995.
20. Agarwala, A. and C. R. Das, "Experimenting with A Shared Virtual Memory Environment for Hypercubes," *Journal of Parallel and Distributed Computing*, 29:228-235, September 1995.
21. Merchawi, N. S., S. R. T Kumara, and C. R. Das, "A Probabilistic Model for the Fault Tolerance of Multilayer Perceptions," *IEEE Transactions on Neural Networks*, 7(1):201-205, January 1996.
22. Mohapatra, P. and C. R. Das, "Performance Analysis of Finite-Buffered Asynchronous Multistage Interconnection Networks," *IEEE Transactions on Parallel and Distributed Systems*, 7(1):18-25, January 1996.
23. Mohapatra, P., C. Yu, and C. R. Das, "Allocation and Mapping Based Reliability Analysis of Multistage Interconnection Networks," *IEEE Transactions on Computers*, 45(5):600-606, May 1996.
24. Boura, Y. and C. R. Das, "Performance Analysis of Buffering Schemes in Wormhole Routers," *IEEE Transactions on Computers*, 46(6):687-694, June 1997.
25. Yoo, B. S. and C. R. Das, "A Fast and Efficient Processor Management Techniques for K-ary n-cubes," *Journal of Parallel and Distributed Computing*, 55(2):192-214, December 1998.
26. Vaidya, A., C. R. Das, and A. Sivasubramaniam, "A Testbed for Evaluation of Fault-Tolerant Routing in Multiprocessor Interconnection Networks," *IEEE Transactions on Parallel and Distributed Systems*, Special Issue on Fault-tolerant Routing, 10(10):1052-1066, October 1999.
27. Nagar, S., A. Banerjee, A. Sivasubramaniam, and C. R. Das, "Scheduling Alternatives to Coscheduling on a Network of Workstations," *Journal of Parallel and Distributed Computing*, Special Issue on Software support for Distributed Computers, 59(2):302-327, November 1999.
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29. Vaidya, A., C. R. Das, and A. Sivasubramaniam, "Impact of Virtual Channel and Adaptive Routing on Application Performance," *IEEE Transactions on Parallel and Distributed Systems*, 12(2):223-237, February 2001.
30. Yoo, B. S. and C. R. Das, "A Good Processor Management Scheme = Fast Allocation + Efficient Scheduling," to appear in *Journal of Parallel and Distributed Computing*
31. Yoo. B. S. and C. R. Das, "A Fast and Efficient Allocation Scheme for Mesh-Connected Multicomputers," *IEEE Transactions on Computers*, 51(1):46-60, January 2002.
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33. Lim, S., G. Cao, and C. R. Das, "A Unified Bandwidth Reservation and Admission Control Mechanism for QoS Provisioning in Cellular Networks", *Wireless Communications and Mobile Computing (WCMC) Journal (special issue on Performance Evaluation of Wireless Networks)*, Vol. 4, No. 1, pp. 3-18, Feb 2004.
34. Cao, G., L. Yin, and C. R. Das, "A Cooperative Cache Based Data Access Framework for Ad Hoc Networks", *IEEE Computer*, pp. 32-39, Feb. 2004.
35. Zhu, H., G. Cao, G. Kesidis, and C. R. Das, "An Adaptive Power-Conserving Service Discipline for Bluetooth", *Computer Communication*, Vol. 27 (9), pp. 828-839, Sept. 2004.

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4. Sheu, T. L., W. Lin, and C. R. Das, "An Efficient Parallel Algorithm of Conjugate Gradient Method," *International Conference on Supercomputing*, pp. 488-496, May 1987.
5. Lin, W., M. J. Thazhuthaveetil, and C. R. Das, "A Parallel Matrix Inversion Algorithm with Dynamic Communication Structures," *International Conference on Supercomputing*, pp. 460-466, May 1988.
6. Macaluso, J., C. R. Das, and W. Lin, "A Reliability Predictor for MIN-Connected Multiprocessor Systems," *International Conference on Parallel Processing*, pp. 392-399, August 1988.
7. Lin, W., T.-L. Sheu, C. R. Das, C.-L. Wu, and T.-Y. Feng, "Fast Data Selection and Broadcast On the Butterfly Network," *International Workshop on Future Trends of Distributed Computing Systems in the 90's*, pp. 65-72, September 1988.
8. Lin, W., T.-L. Sheu, and C. R. Das, "A Quadtree Communication Structure for Fast Data Searching and Distribution," *COMPSAC*, pp. 316-323, October 1988.
9. Sheu, T. L., W. Lin, and C. R. Das, "A Parallel Eigen Value Algorithm with Dynamic Communication Structure," *International Computer Symposium*, pp. 117-122, December 1988.

10. Das, C. R. and J. Kim, "An Analytical Model for Computing Hypercube Availability," *International Symposium on Fault-Tolerant Computing Systems*, pp. 530-537, June 1989.
11. Sheu, T. L., W. Lin, C. R. Das, and M. J. Irwin, "Distributed Fault Diagnosis in the Butterfly Parallel Processor," *International Conference on Parallel Processing*, I, pp. 172-175, August 1989.
12. Kim, J., C. R. Das, and W. Lin, "A Processor Allocation Scheme for Hypercube Computers," *International Conference on Parallel Processing*, (II), pp. 231-238. (Daniel L. Slotnick Award for the Most Original Paper), August 1989.
13. Das, C. R., L. Tien, and L. N. Bhuyan, "Availability Evaluation of MIN-Connected Multiprocessors Using Decomposition Technique," *International Symposium on Fault-Tolerant Computing Systems*, pp. 176-183, June 1990.
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15. Algudady, M. S., C. R. Das, and M. J. Thazhuthaveetil, "A Write Invalidate Cache Coherence Protocol for MIN-Based Multiprocessors," *ISMM International Conference on Parallel and Distributed Computing and Systems*, pp. 77-81, October 1990.
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17. Kim, J. and C. R. Das, "Modeling Wormhole Routing in a Hypercube," *International Conference on Distributed Computing Systems*, pp. 386-393, May 1991. (Outstanding Paper Award).
18. Yang, M. K. and C. R. Das, "A Parallel Branch-and-Bound Algorithm for MIN-Based Multiprocessors," (poster paper) *ACM SIGMETRICS Conference on Measurements and Modeling of Computer Systems*, pp. 222-233, May 1991.
19. Kim, J. and C. R. Das, "On Subcube Dependability in a Hypercube," *ACM SIGMETRICS Conference on Measurements and Modeling of Computer Systems*, pp. 111-119, May 1991.
20. Algudady, M. S., C. R. Das, and M. J. Thazhuthaveetil, "Cache-Based Checkpointing Scheme for MIN-Based Multiprocessors," *International Conference on Parallel Processing*, pp. 497-500, August 1991.
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22. Yu, C. S. and C. R. Das, "Multitasking in Multistage Interconnection Network Machines," *International Conference on Distributed Computing Systems*, pp. 30-37, June 1992.
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25. Orzechowski, N. S., S. R. T. Kumara, and C. R. Das, "Performance of Multilayer Neural Networks in Binary-to-Binary Mappings Under Weight Errors," *the IEEE International Conference on Neural Networks*, III, pp. 1684-1689, April 1993.
26. Orzechowski, N. S., S. R. T. Kumara, and C. R. Das, "Performance Analysis of Neural Networks," *ORSA/TIMS Annual Meeting*, May 1993.

27. Mohapatra, P., C. S. Yu, and C. R. Das, "A Lazy Scheduling Scheme for Improving Hypercube Performance," *International Conference on Parallel Processing*, I, pp. 110-117, August 1993.
28. Mohapatra, P. and C. R. Das, "A Queueing Model for Finite-Buffer MINs," *International Conference on Parallel Processing*, I, pp. 210-213, August 1993.
29. Algudady, M. S., C. R. Das, and M. J. Thazhuthaveetil, "A Hierarchical Cache-Coherence Protocol with Limited Inclusion," *International Conference on Parallel Processing*, I, pp.254-257, August 1993.
30. Boura, Y. and C. R. Das, "A Class of Partially Adaptive Routing Algorithms for n-dimensional Meshes," *International Conference on Parallel Processing*, III, pp. 175-182, August 1993.
31. Mohapatra, P., S. Wong, and C. R. Das, "Analytical Modeling of Combining in Multistage Interconnection Networks," *Modeling Techniques and Tools for Computer Performance Evaluation*, (poster paper), May 1994.
32. Boura, Y. M. and C. R. Das. "Efficient Fully Adaptive Wormhole Routing in n-Dimensional Meshes," *International Conference on Distributed Computing Systems*, pp. 589-596, June 1994.
33. Mohapatra, P., S. Wong, and C. R. Das, "Performance Analysis of Combining Multistage Interconnection Networks," *International Conference on Parallel Processing*, I, pp. 13-16, August 1994.
34. Agarwala, A. and C. R. Das, "A Shared Memory Environment for Hypercubes," *International Conference on Parallel Processing*, I, pp. 200-207, August 1994.
35. Yu, C. and C. R. Das, "Limit Allocation: An Efficient Processor Management Scheme for Hypercubes," *International Conference on Parallel Processing*, II, pp. 143-150, August 1994.
36. Yousif, M. S. and C. R. Das, "A Switch Cache Design for MIN-Based Shared-Memory Multiprocessors," *Conpar94 International Conference on Parallel Processing*, Springer-Verlag LNCS 854, pp. 426-437, September 1994.
37. Boura, Y. M., C. R. Das, and T. M. Jacob, "A Performance Model for Adaptive Routing in Hypercubes," *First International Workshop on Parallel Processing*, pp. 11-16, December 1994.
38. Boura, Y. M. and C. R. Das, "Modeling Virtual Channel Flow Control in Hypercubes," *IEEE Symposium on High Performance Computer Architecture*(HPCA-1), pp. 166-175, January 1995.
39. Boura, Y. M. and C. R. Das, "Fault-Tolerant Routing in Mesh Networks," *International Conference on Parallel Processing*, I, pp. 106-109, August 1995.
40. Yoo, B. S., C. R. Das, and C. Yu, "Processor Management Techniques for Mesh Connected Multiprocessors," *International Conference on Parallel Processing*, II, pp. 105-112, August 1995.
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47. Seed, D., A. Sivasubramaniam, and C. R. Das, "Communication in Parallel Applications: Characterization and Sensitivity Analysis," *International Conference on Parallel Processing*, pp. 446-453, August 1997.
48. Yoo, B. S., C. R. Das, and J. Kim, "A Performance Modeling Technique for Mesh-Connected Systems," *International Conference on Parallel and Distributed Systems*, pp. 408-413, *Seoul, Korea*, December 1997.
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52. Vaidya, A., A. Sivasubramaniam, and C. R. Das, "LAPSES: A Recipe for High Performance Adaptive Router Design," *IEEE Symposium on High Performance Computer Architecture*(HPCA-5), pp. 236-243, Orlando, January 1999.
53. Nagar, S., A. Banerjee, A. Sivasubramaniam, and C. R. Das, "A Closer Look at Co-Scheduling Approaches for a Network of Workstations," Eleventh ACM Symposium on Parallel Algorithms and Architectures (SPAA), pp. 96-105, St. Malo, France, June 1999.
54. Yang, M. K. and C. R. Das, "A Parallel Optimal Branch-and-Bound Algorithm for MIN-Based Multiprocessors," International Conference on Parallel Processing. pp. 112-119. Aizu-Wakamatsu City, Japan, September 1999.
55. Kasbekar, M., S. Yajnik, R. Klemm, Y. Huang, and C. R. Das, "Issues in the Design of a Reflective Library for Checkpointing for C++ Objects," Symposium on Reliable Distributed Systems (SRDS), pp. 224-233, Lausanne, Switzerland, October 1999.
56. Kasbekar, M., C. Narayanan, and C. R. Das, "Selective Checkpointing and Rollbacks in Multithreaded Object-Oriented Environments," 1999 Pacific Rim International Symposium on Dependable Computing (PRDC), pp. 121-128, Hong Kong, December 1999.
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58. Kim, S. and C. R. Das, "A Reliable Statistical Admission Control Policy for Interactive Video-On-Demand Servers with Interval caching," *International Conference on Parallel Processing*, pp. 135-142, August 2000.
59. Kim, S., C. R. Das, and A. Sivasubramaniam, "Performance Analysis of A Buffer Management Technique for Interactive Video-on-Demand" International Conference on Multimedia Modeling (MMM'2000), Japan, November 2000.
60. Kasbekar, M. and C. R. Das, "Selective Checkpointing and Rollbacks in Multithreaded Distributed Systems," International Conference on Distributed Computing Systems (ICDCS), pp. 39-46, Arizona, April 2001.
61. Yum, K. H., E. J. Kim, and C. R. Das, "QoS Provisioning in Clusters: An Investigation of Router and NIC Design," Proc. *International Symposium on Computer Architecture*(ISCA), pp. 120-129, Sweden, June 2001.

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75. Kim, E. J., K. H. Yum, N. Kim, C. R. Das, M. Yousif and J. Duato, “Performance Enhancement Techniques for InfiniBandTM Architecture,” Proc. of *the 9th International Symposium on High-Performance Computer Architecture(HPCA-9)*, pp. 256-264, February 2003.

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87. Lim, S., W. Lee, G. Cao, C. R. Das, "Performance Comparison of Cache Invalidation Strategies for Internet-based Mobile Ad Hoc Networks," Proc. of the IEEE International Conference on Mobile Ad-hoc and Sensor Systems (MASS), Fort Lauderdale, Florida, Oct 2004.
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98. Richardson, T. D., C. Nicopoulosr, D. Park, N. Vijayakrishnan, Y. Xie, and C. R. Das, "A Hybrid SoC Interconnect with Dynamic TDMA-Based Transaction-Less Buses and On-Chip Networks," Proc. of the *Proceedings of the VLSI Design* , 2006.
99. Kim, J., D. Park, C. A. Nicopoulos, N. Vijaykrishnan, and C. R. Das, "Performance Enhancement through Early Release and Buffer Optimization in Network-on-Chip Router Architectures," in the special workshop on *Future Interconnects and Networks on Chip, at Design Automation and Test in Europe* (DATE 06).
100. Park, D., C. A. Nicopoulos, J. Kim, N. Vijaykrishnan, Chita R. Das, "Exploring Fault-Tolerant Network-on-Chip Architectures", in *the Proceedings of Dependable Systems and Networks (DSN06)*, pp. 93-102, Philadelphia, 2006
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108. Reetuparna Das, Asit K. Mishra, Chrysostomos Nicopoulos, Dongkook Park, N. Vijaykrishnan, Ravishankar Iyer, Chita R. Das, "Performance and Power Optimization through Data Compression in Network-on-Chip Architectures", *International Symposium on High Performance Computer Architecture*, Salt Lake City, Utah (HPCA, 2008).
109. Dongkook Park, Soumya Eachempati,Reetuparna Das, Asit K. Mishra, N. Vijaykrishnan, Yuan Xie , Chita R. Das, "MIRA : A Multilayered Interconnect Router Architecture", *35th International Symposium on Computer Architecture (ISCA, 2008).*
110. Patankar. P, Nam. G, Kesidis. G, Das. C,"Exploring Anti-Spam Models in Large Scale VoIP Sytems",*International Conference on Distributed Computing Systems, ICDCS 2008.*

Books or Parts of Books

Das, C. R., L. N. Bhuyan, and V. V. S. Sarma, "Effect of Maintenance on the Dependability and Performance of Multiprocessor Systems," *IEEE Tutorial on Advances in Distributed System Reliability*, pp. 59-66, 1990.

Macaluso, J., C. R. Das, and W. Lin, "A Reliability Predictor for MIN-Connected Multiprocessor Systems," *IEEE Tutorial on Advances in Distributed System Reliability*, pp. 260-273, 1990.

Kim, J., C. R. Das, and W. Lin, "A Top-Down Processor Allocation Scheme for Hypercube Computers," *Interconnection Networks for High Performance parallel Computers*, pp. 620-630, Edited by I. D. Scherson and A. S. Youssef, IEEE Computer Society Press.

Yousif, M. S., M. J. Thazhuthaveetil, and C. R. Das, "Cache Coherence in Multiprocessors: A Survey," *Advances in Computers*, 40:127-179, Academic Press, August 1995.

Kim, J. and C. R. Das, "Modeling Wormhole Routing In a Hypercube," *IEEE Tutorial on Multiprocessor Performance measurement and Evaluation*, pp. 383-390, 1995.

Das, C. R. and P. Mohapatra, "Dependability Modeling of Parallel and Distributed Computers," In Chapter 7, *Parallel Computing: Paradigms and Applications*, edited by A. Y. Zomaya, International Thomson Computer Press, 1996.

Lim, Sun-Ho, C. Yu, and C. R. Das, "Randomized Overhearing to Improve Routing and Energy Performance in Mobile Ad Hoc Networks," In *Performance Analysis of Mobile and Ad Hoc Networks*, Chapter 6, pp. 115-134, Nova Science Publishers Inc., Nov 2006.

Yu, C., and C. R. Das, "Performance Analysis of Mobile and Ad Hoc Networks," Edited Book, Nova Science Publishers, Inc., 2006.

Student Supervision:

Ph.D. Students : 28 (21 completed)

J. Kim (Professor, POSTECH, Korea), M. S. Yousif (Intel), M. K. Yang (Associate Professor, University of Ulsan, Korea), P. Mohapatra (Professor, UC, Davis), N. Marchaoui (Associate professor, McGill Univ.), C. Yu (Associate Professor, Cleveland State Univ.), Y. Boura (Pyramid Co.), B. S. Yoo (LL Nat'l Lab), A. Vaidya (Intel), S. Kim (Assistant Professor, San Jose State Univ.), M. Kasbekar (Akamai), K. H. Yum (Assistant Professor, UTexas, San Antonio), N. Sarhan (Assistant Professor, Wayne State Univ.), E. J. Kim (Assistant Professor, Texas A&M Univ.), X. Deng (Assistant Professor, St. Cloud State Univ.), S. Lim (Assistant Professor, South Dakota State Univ.), S. Yi (ETRI, Korea), G. S. Choi (Samsung, Korea), J. H. Kim (Samsung, Korea), J. M. Kim (Assistant Professor, G. Tech, Savannah), D. Ersoz (Cisco).

M.S. Students : 50+
B.S. (Honors Students): 15+

Courses Taught:
Logical Design of Digital Systems, Fault-Tolerant Systems, Performance Evaluation, Computer Architecture, Data Communication Networks, Multiprocessor Architecture, Parallel I/O, Internet QoS.

Research Grants:
Dependability and Performance Models for Parallel Computers. National Science Foundation, Research Initiation, PI, 1988-89, $59,400.

An Educational Supplement Proposal for Developing a System Modeling Package for Undergraduate Education. Supplemental support to Research Initiation, National Science Foundation, PI, 1989-90, $20,000.

Evaluation of Parallel Architecture for BM/C^3 Applications (with T.-Y. Feng, W. Lin, M. J. Thazhuthaveetil). Rome Air Development Center, Co-PI, 1988-89, $500,000.

Evaluation Technique for Hypercube and MIN-Based Architectures. National Science Foundation, (with T.-Y.Feng), Co-PI, 1991-94, $253,777.

Low Cost Adaptive Routing Algorithms for n-Dimensional Meshes. National Science Foundation, PI, 1994-1996, $116,969.

Parallelization of Fire Growth Codes. NASA/STIR, (with A. Kulkarni), Co-PI, 1995-1996, $6,000.

A Proposal for the Revision of the Logic Design of Digital Systems Course. College of Engineering, PI, 1995-1996, $8,500.

Application-Driven Network Performance Evaluation. National Science Foundation, PI, 1996-1999, $224,496.

Developing and Evaluating Low-cost Communication for a Network of Workstations. IBM/SUR Equipment, (with A. Sivasubramaniam), PI, 1996-1997, $193,240.

CISE Research Instrumentation for Developing a NOW Platform for Parallel Processing. National Science Foundation, (with A. Sivasubramaniam), PI, 1997-1998, $110,550.

Application-Driven Network Performance Evaluation. REU Supplement, National Science Foundation, PI, 1997-1998, $10,000.

A Low-Cost High Performance Computing Platform. CISE Research Instrumentation. National Science Foundation, (with A. Sivasubramaniam), PI, 1999-2001, $79,973.

An Integrated Approach for Quality of Service in Cluster Networks. National Science Foundation, (with A. Sivasubramaniam), PI, 1999-2002, $380,365.

Performance Modeling of Unisys Computer Systems. PI, Unisys Corporation, 1999-2003, $140,000.

MediaWorm: A Single-Chip Router Architecture. Pennsylvania/Pittsburgh Digital Greenhouse Consortium, (with M. J. Irwin, V. Narayanan), PI, 2000-2001, $298,481.

Scalable and Efficient Scheduling Techniques for Clusters. National Science Foundation, PI, 2001-2004, $254,883.

QoS Provisioning in InfiniBand Architecture (IBA) for System Area Networks. National Science Foundation, PI, 2002-2005, $331,964.

I^3C: An Infrastructure for Innovation in Information Computing. Research Infrastructure Grant, National Science Foundation, (with R. Acharya, C. L. Giles, M. J. Irwin, and P. E. Plassmann), PI, 2002-2008, $2,561,036 (includes $765,307 University matching).

Exploring Network-on-Chip (NoC) Architecture Design Space. National Science Foundation, PI, 2004-2007, $190,000.

Exploring Cluster-Based Data Center Design Space for High Performance and Dependability. National Science Foundation, PI, 2005-2008, $346,529.

Purposeful Node Mobility for Mission-Oriented Sensor Networks. National Science Foundation, (with G. Cao, T. Laporta, and G. Kesidis), 2005-2008, $450,000.

Protecting TCP Congestion Control: Tools for Design, Analysis, and Emulation. National Science Foundation, Co-PI, (with G. Kesidis), 2005-2008, $350,000, total grant with Purdue University $675,000.

Impact of User-Level Communication on Data Center Performance. Intel Research, PI, 2005-2008, $195,000.

Performance and Energy-Efficient Network-on-Chip (NoC) Architectures. Intel Research, PI, 2006-2009, $150,000.

Randomized Session-Memory Purging in Internet Routers. Cisco, (with G. Kesidis), Co-PI, 2007-2009, $98,540.

HoDoo: Holistic Design of On-chip Interconnects. National Science Foundation, (with V. Narayanan and Yuan Xie), PI, 2007-2010, $630, 894.

Collaborative Data Access in Wireless P2P Networks, National Science Foundation, (with G. Cao), Co-PI, 2007-2010, $600,000.

Honors and Awards:

Fellow of IEEE, 2000

Daniel L. Slotnick Award for the Best Original Paper.
A Processor Allocation Scheme for Hypercube Computers, *International Conference on Parallel Processing,* Aug. 1989.

IEEE Computer Society Outstanding Paper Award.
Modeling Wormhole Routing in a Hypercube, *International Conference on Distributed Computing Systems,* May 1991.

Best Paper Award.
Selective Checkpointing and Rollbacks in Multi-threaded Object-oriented Environment, *Pacific-Rim Dependable Computing (PRDC) Symposium,* December 1999.

IEEE Computer Society Appreciation Award.
For effectively running HPCA-12 as the Program Chair, February 2006.

Teaching Award.
Department of Computer Science and Engineering, 2001.

University Administrative Activities:

Chair, College of Engineering Chair Professor Evaluation Committee, 2004-2006
Chair, Search Committee for Deaprtment Head, Computer Science and Engineering
Chair, Department Promotion and Tenure Committee
Chair, Department Faculty Search Committee
Chair, Department Graduate Committee
Chair, Deaprtment Award Committee
Member, College of Engineering Graduate Council
Member, University Graduate Council
Memember, Department Promotion and Tenure Committee, Faculty Search Committee, Graduate Committee, Personnel Committee, Undergraduate Committee, and Award Committee

Professionaa Activities:

Editorial and Technical Committee Activities:
Associate Editor, *IEEE Transactions on Computers*, 2001-2004
Associate Editor, *IEEE Transactions on Parallel and Distributed Systems*, 1994-1997
Chair, IEEE Technical Committee on Distributed Processing (TCDP), 2002-2005.
IEEE (CS) Fellow Selection Committee, 2002-2005.
Editor-in-Chief Search Committee member, IEEE Transactions on Dependable and Secure Computing, 2003.
Chair, IEEE TPDS EIC evaluation Committee, 2002-2003.
Member, Advisory Board, *IEEE Technical Committee on Computer Architecture (TCCA)*, 1995-1998

Program Committee Activities:
General Co-Chair, *International Conference on Parallel Processing*, 1996
General Chair, *Euro-Par Workshop on Routing and Communication in Networks*, Passau, 1997
Program Chair, *6th International Conference on Advanced Computing* , India, 1998
Workshop Chair *International Conference on Parallel Processing*, 1998
Program Chair, *7th International Conference on Advanced Computing* , India, 1999
General Chair, *International Conference on Information Technology,*, India, December 2001
Program Chair, Twelfth International Conference on High Performance Computer Architecture (HPCA-12), 2006.
Program Vice-Chair, (Cyber-infrastructure for Distributed Computing), 28th Int. Conf. on Distributed Compuitng Systems, (ICDCS-2008), China
Program Committee Member, *IEEE Symposium on High Performance Computer Architecture*, 1996-
Program Committee Member, *ACM SIGMETRICS Conference on Measurements and Modeling of Computer Systems*, 1996
Program Committee Member, *International Conference on Distributed Computing Systems*, 1991-
Program Committee Member, *International Conference on Parallel Processing*, 1990-
Program Committee Member, *HiPC*, 1999-
Program Committee Member,, *IPDPS*, 1995-
Program Committee Member, *MASCOT*, 1996
Program Committee Member, *Workshop on Fault-Tolerant Parallel and Distributed Systems*, 1992
Program Committee Member, *Int. Workshop on Depandable Systems*, In Conjuction with IPDPS, 2000-
Program Committee Member, *Pacific Rim Int. Symposium on Depandable Computing* (PRDC), 2001, 2003

Program Committee Member, *Int. Conference on Advanced Computing (ADCOM)* , India, 1998, 2003
Program Committee Member, *Int. Conference on Advanced Computing*, December 2001, 2002
Program Committee Member, *International Conference on Advanced Computing*, December 2001
India, December 2001
Session Chair, ICPP, ICDCS, FTCS, PRDC, HPCA
Lecturer, ACM, 1993-94
Member, ACM
Referee, *IEEE Transactions on Computers*, *IEEE Transactions on Parallel and Distributed Systems*, *IEEE Computer*, *IEEE Transactions on Reliability*, *Journal of Parallel and Distributed Computing*, *Journal of Supercomputing*, *International Conference on Parallel Processing*, *International Symposium on Fault-Tolerant Computing Systems*, *International Symposium on Computer Architecture*, *International Conference on Distributed Computing Systems*, *International Symposium on High Performance Computer Architecture*, *Pacific Rim Int. Symposium on Depandable Computing*, *ACM SIGMETRICS Conference on Measurements and Modeling of Computer Systems*
Referee, *Army Research Office*
Referee, *NSF*

Research Summary

The main area of my research is on Parallel and Distributed Computer architectures, and can be can be categorized into the following themes: *Evaluation of Multiprocessor Architectures*, *Design and Analysis of Routers and Network Architectures*, *Resource Management in Multiprocessors*, and *Cluster Systems*. During my tenure at Penn State, I have supervised 21 Ph.D. students, more than 50 M.S. students and about 12 B.S. Honors students in these areas. My research results have appeared in top quality international journals (such as IEEE TPDS, IEEE TC, JPDC) and highly selective conference proceedings (such as ISCA, HPCA, MICRO, SIGMETRICS, ICDCS, ICPP, IPDPS, ICS, ISPLED, and SPAA), and the research has been supported by various funding agencies. In the last five years, I have been a PI/Co-PI of reserch grants totaling to more than $5.8M. Here is a briefly description of my contributions in each of these areas (with pointers to selected publications) followed by an outline of my current research work.

Evaluation of Multiprocessor Architectures

Performance and dependability (reliability/availability) evaluation of multiprocessor architectures is essential to assess whether a design meets the high-level requirements, to identify design bottlenecks, to select an optimal architecture for specific requirements, and to design better systems in the future. However, evaluation of such architectures becomes extremely complex when the underlying communication network is included in the model. Therefore, most prior research refrained from including the network architecture in evaluating multiprocessor systems.

The uniqueness of my evaluation work is the inclusion of the underlying interconnection network in developing performance, dependability, and performance-related dependability (performability) models for various parallel machines. We have developed elegant performance and dependability models for various architectures such as bus-based systems [1], hypercubes ([10], [14], [24], [44], [53]), MIN-based systems ([11], [22], [47]), mesh-connected systems [18], k-ary-n-cubes [77], and clusters [12]. Specifically, the analytical model for the hypercube network with wormhole switching mechanism [51] was the first accurate technique that captured the chained blocking possible in wormhole switching. This work received the IEEE Computer Society Outstanding Paper Award at the International Conference on Distributed Computing Systems (ICDCS), 1991.

Design and Analysis of Routers and Network Architectures

A high-throughput, low-latency communication network is essential to building a scalable, high performance multiprocessor. The network topology, switching mechanism, message routing algorithm, and application workload together determine performance of a network. While my research over the years has looked into various aspects of designing high performance networks, I have specifically worked on developing efficient routing algorithms for direct networks, evaluation of networks with realistic workloads, and designing faster routers/switches. We have developed partially and fully adaptive routing algorithms for hypercubes and meshes that require minimal number of virtual channels (VCs) to provide deadlock freedom (no VC for partially adaptive routing in n-dimensional meshes [64] and 2 virtual channels for fully adaptive routing algorithm [66]). In addition, we have developed an analytical model to capture virtual channel flow control and routing adaptivity in hypercubes ([72]). Extension of these algorithms to handle link and node faults in a network has also been proposed [73].

While the research on network design and analysis is quite rich, very little work was done in evaluating networks with realistic workloads. The three communication attributes that are required for any network performance study are the message inter-arrival time distribution with the corresponding generation rate, the spatial distribution of messages or the traffic pattern, and the message size (volume). Typical synthetic environments have assumed that the temporal distribution is exponential, the spatial distribution is uniform or a few localized communication patterns, and the message size is a fixed number of bytes. While evaluations with such synthetic workloads have been accused of providing inaccurate performance estimates, performance evaluation with realistic workloads is quite complex and challenging. In this regard, we

have initiated research on *workload characterization* of parallel applications and *application-driven performance evaluation* [78]. Using the temporal, spatial and volume attributes of communications, we have analyzed the communication properties of shared memory and distributed memory applications. It has been shown that it is possible to quantify the temporal and spatial behavior of parallel applications using known mathematical distributions, which in turn can be used in application-driven performance evaluation. The impact of performance enhancement features such as virtual channel flow control and routing adaptivity with realistic workloads has been analyzed ([29], [79]).

Design of fast routers is essential not only to build scalable interconnects, but also to enhance the performance of the entire system. We have developed a pipelined router architecture, called LAPSES (look-ahead routing, intelligent path selection, and economic storage) that uses a minimal size routing table in supporting any routing algorithm in a regular network [86].

Resource Management in Multiprocessors

Prudent management of system resources is essential to maximize the system throughput and utilization, while minimizing the average response time in a multi-user environment. Resource management in multiprocessors is a well researched area. It consists of two steps; processor allocation and job scheduling. Processor allocation is concerned with allocating the parallel processes of a job to processors, while scheduling decides the next job/process for execution. Both these techniques complement each other in maximizing the delivered performance of a multiprocessor. Primarily contiguous allocation of processors to processes of a parallel job has been used to minimize the communication overhead, and thus improve the performance of closely-coupled multiprocessors. Since dynamic allocation is an NP-complete problem, a plethora of allocation algorithms for different multiprocessors have been proposed with varying degree of allocation ability and complexity.

We have proposed efficient processor allocation algorithms for hypercubes ([8], [46], [69]), MINs ([16]), and k-ary n-cubes/meshes ([25], [74], [80]). In particular, the *free list* policy [46], proposed for the hypercube multiprocessors, received the Daniel Slotnick Award for the best original paper at the 1989 International Conference on Parallel Processing (ICPP). An elegant scheduling algorithm, called *lazy scheduling* was proposed ([17]) to boost the hypercube performance further.

Cluster systems

Cluster systems, also known as network of workstations/PCs (NOW), are becoming a predominant and cost-effective style for designing scalable, high performance computers. These systems are gaining acceptance not just in scientific applications but also in emerging commercial applications such as database servers and web servers. The tremendous surge in dynamic web contents, multimedia objects, e-commerce, and other web-enabled applications requires providing high performance and quality-of-service (QoS) support in clusters.

My research on cluster systems has focused on three issues: design of high performance cluster interconnects, QoS provisioning in cluster interconnects, and scheduling techniques for clusters. In the area of high performance cluster interconnects, we have looked into the design of routers and network interfaces (NIs). We have set up a NOW laboratory to conduct various types of theoretical and experimental research. In particular, we are exploring the feasibility of providing QoS support in commercially successful wormhole-switched routers. We have proposed a new wormhole router, called MediaWorm, that can support integrated traffic in clusters ([32], [91]). Recently, we have proposed modifications to the industry standard virtual interface architecture (VIA) to efficiently support real-time traffic in the NI [95]. A number of interesting research issues involving hardware and software mechanisms to provide QoS support in routers, and modifications to user-level communication mechanisms for QoS provisioning are currently being investigated ([98], [100]).

Unlike tightly-coupled multiprocessors, coscheduling of parallel processes in a loosely-coupled cluster is much more challenging because of the individual node autonomy, and relatively high communication

overhead. Therefore, a few other scheduling alternatives such as dynamic coscheduling (DCS) and implicit coscheduling (ICS, SB) have been proposed in the literature. These schemes use the locally available message arrival information to schedule communicating processes of a job simultaneously. Using the user-level communication strategies such as U-Net, Fast Message, and VIA, they are shown to be quite efficient. We have proposed a design spectrum for implementing nine different coscheduling algorithms and in particular have proposed an efficient scheme, called *periodic boost* that is shown to be more efficient on Solaris platforms ([27], [87]). All these algorithms have been implemented on an UltraSPARC workstation cluster, connected by Myrinet. This experimental testbed can be used for studying many scheduling alternatives. Any off-the-shelf MPI applications can run on this platform.

Since the implementation of any prior coscheduling algorithm needs substantial effort, we have developed a generic framework for implementing any coscheduling algorithm on a Linux cluster [116]. In addition, we have proposed a new coscheduling, called Coordinated Coscheduling (CC), which has the potential to outperform all prior techniques [115]. This framework and the CC scheme has been implemented on a Myrinet connected 16-node Linux cluster on top of VIA and GM. Also, we have shown that it is possible to gain significant performance benefits by employing coscheduling algorithms on commercial platforms, which currently use various forms of batch scheduling. We are now porting the framework and the CC scheme to large Linux platforms to test with various scientific workloads. This experimental research is conducted in collaboration with the Lawrence Livermore National laboratory (LLNL) and Penn State's main computing center.

Current Research

My current work on cluster systems emphasizes on practical scheduling algorithms, QoS support in the cluster interconnects and NICs, and design of energy-efficient interconnects. For the scheduling work, we want to develop practical coscheduling algorithms that can provide better performance than the batch scheduling. The QoS support research is conducted in collaboration with Intel and other members of the InfiniBand Trade Association (IBTA). Our simple congestion control technique ([105], [109]) is currently being examined by several IBTA members for inclusion in the IBA specification. Clusters are now used for designing data centers that include web servers, application servers and database servers. We are now examining the impact of user-level communication and coscheduling algorithms on the performance of cluster-based data centers. In addition, energy consumption in clusters has become a serious concern due to their high power budgets. Also, the critical nature of many Internet-based services demand high server availability. Therefore, design of high performance, energy-efficient, and dependable clusters has become a pressing issue from socio-economic and environmental standpoints. In collaboration with our VLSI group, I have started design and analysis of energy-efficient cluster interconnects [114]. In particular, we have proposed a dynamic link shut down scheme, called DLS, to conserve energy. Compared to the prior dynamic voltage scaling (DVS) technique that incurs significant performance penalty, the DLS scheme can provide a better tradeoff between performance and power. We are also investigating the dependability implications of energy-efficient designs. Furthermore, I am expanding my research to network-on-chip (NoC) architectures to design SoC systems. Due to my inherent interest, I will attempt to develop performance and dependability models for such systems considering various practical limitations, and will conduct workload characterization of scientific and commercial applications for clusters.

The QoS ideas in the router have many similarities to the QoS concept in the Internet. I am currently supervising two Ph.D. students on Internet QoS. We are developing a control theoretic approach to analyze and design various Active Queue management (AQM) schemes for Internet congestion control ([106], [107], [118], 119]). We have designed an AQM scheme, which can detect non-responsive TCP and UDP flows, and thus, can be used to dynamically quarantine such flows [120]. Also, I am currently expanding my research to wireless/mobile/ad hoc systems. A Ph.D. student is examining the advantage of using caching for combining ad hoc networks with the wired Internet for universal information accessibility ([112,117]).

Multicore/SoC Archietectures

Design and Analysis of data Centers