Curriculum Vitaé

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Education:

1986	Ph.D. in Computer Science, Center for Advanced Computer Studies, University of Louisiana, Louisiana
1981	M.S. in Electrical Engineering, R.E.C. Rourkela, Sambalpur University, India
1976	B.S. in Electronics and Communication, B.I.T. Sindri, Ranchi University, India

Experience:

July 1st, 2016 -	Interim Head, Department of Computer Science and Engineering, The Pennsylvania State University, Pennsylvania
2009 -	Distinguished Professor, Department of Computer Science and Engineering, The Pennsylvania State University, Pennsylvania
2008 - 2010	Program Director, Computer Architecture Program, CISE/CCF Division, National Science Foundation, Virginia
1997 -	Professor, Department of Computer Science and Engineering, The Pennsylvania State University, Pennsylvania
1992 - 1997	Associate Professor, Department of ECE and Computer Science and Engineering, The Pennsylvania State University, Pennsylvania
1986 - 1992	Assistant Professor, Department of Electrical and Computer Engineering The Pennsylvania State University, Pennsylvania

Research Interests:

Parallel & Distributed Computer Architectures; Multi-core/SoC Architectures; GPGPU systems; Heterogeneous Architectures; Communication Networks & Communication Mechanisms; Cloud Systems; Performance Evaluation; Fault-tolerant Computing; Mobile Platforms.

Journal Papers

1. Das, C. R. and L. N. Bhuyan, "Bandwidth Availability of Multiple-Bus Multiprocessors," *IEEE Transactions on Computers*, Special Issue on Parallel Processing, pp. 918-926, October 1985.
2. Das, C. R., L. N. Bhuyan, and V. V. S. Sarma, "Effect of Maintenance on the Dependability and Performance of Multiprocessor Systems," *IEEE Transactions on Reliability*, Special Issue on Fault Tolerant Computing, pp. 208-215, June 1987.
3. Das, C. R. and L. N. Bhuyan, "Reliability and Fault-Tolerance Issues of Multiprocessor and Multicomputer Systems," (Invited Paper) in Sadhana, *Journal of Indian Academy of Sciences*, pp. 129-154, October 1987.
4. Das, C. R. and L. N. Bhuyan, "Dependability Evaluation of Interconnection Networks," *Information Sciences: An International Journal*, 43(1/2):107-138, October 1987.
5. Kim, J., C. R. Das, W. Lin, and T.-Y. Feng, "Reliability Evaluation of Hypercube Multicomputers," *IEEE Transactions on Reliability*, Special Issue on Reliability of Parallel and Distributed Computing Networks, pp. 121-129, April 1989.
6. Lin, W., T. L. Sheu, C. R. Das, T.-Y. Feng, and C. L. Wu, "A Conflict-Free Routing Scheme on Multistage Interconnection Networks," *IEEE Transactions on Computers*, 38(8):1086-1097, August 1989.
7. Das, C. R., J. T. Kreulen, M. J. Thazhuthaveetil, and L. N. Bhuyan, "Dependability Modeling for Multiprocessors," *IEEE Computer*, 23(10):7-19, October 1990.
8. Kim, J., C. R. Das, and W. Lin, "A Top-Down Processor Allocation Scheme for Hypercube Computers," *IEEE Transactions on Parallel and Distributed Systems*, 2(1):20-30, January 1991.
9. Algudady, M .S., C. R. Das, and M. J. Thazhuthaveetil, "A Write Invalidate Cache Coherence Protocol for MIN-Based Multiprocessors," *International Journal of Mini and Microcomputers*, 14(1):39-44, March 1992.
10. Das, C. R. and J. Kim, "A Unified Task-Based Dependability Model for Hypercube Computers," *IEEE Transactions on Parallel and Distributed Systems*, 3(3):312-324, May 1992.
11. Das, C. R., P. Mohapatra, L. Tien, and L. N. Bhuyan, "An Availability Model for MIN-Based Multiprocessors," *IEEE Transactions on Parallel and Distributed Systems*, pp. 1118-1129, October 1993.
12. Mohapatra, P., C. R. Das, and T.-Y. Feng, "Performance Analysis of Cluster-Based Multiprocessors," *IEEE Transactions on Computers*, 43(1):109-114, January 1994.
13. Yang, M. K. and C. R. Das, "A Parallel Branch-and-Bound Algorithm On a Class of Multiprocessors," *IEEE Transactions on Parallel and Distributed Systems*, 5(1):74-86, January 1994.
14. Kim, J. and C. R. Das, "Hypercube Communication Delay with Wormhole Routing," *IEEE Transactions on Computers*, 43(7):806-814, July 1994.
15. Yousif, M. S., C. R. Das, and M. J. Thazhuthaveetil, "A Cache Coherence Protocol for MIN-based Multiprocessors," *Journal of Supercomputing*, 8:163-185, August 1994.
16. Yu, C. S. and C. R. Das, "Disjoint Task Allocation Algorithms for MIN Machines with Minimal Conflicts," *IEEE Transactions on Parallel and Distributed Systems*, 6(4):373-387, April 1995.
17. Mohapatra, P., C. Yu, and C. R. Das, "A Lazy Scheduling Scheme for Hypercube Computers," *Journal of Parallel and Distributed Computing*, 27(1):26-37, May 1995.
18. Mohapatra, P. and C. R. Das, "On Dependability Evaluation of Mesh Connected Systems," *IEEE Transactions on Computers*, 44(9):1073-1084, September 1995.

19. Sheu, T.-L., W. Lin, and C. R. Das, "Distributed Fault Diagnosis in Multistage Network-Based Multiprocessors," *IEEE Transactions on Computers*, 44(9):1085-1095, September 1995.
20. Agarwala, A. and C. R. Das, "Experimenting with A Shared Virtual Memory Environment for Hypercubes," *Journal of Parallel and Distributed Computing*, 29:228-235, September 1995.
21. Merchawi, N. S., S. R. T Kumara, and C. R. Das, "A Probabilistic Model for the Fault Tolerance of Multilayer Perceptions," *IEEE Transactions on Neural Networks*, 7(1):201-205, January 1996.
22. Mohapatra, P. and C. R. Das, "Performance Analysis of Finite-Buffered Asynchronous Multistage Interconnection Networks," *IEEE Transactions on Parallel and Distributed Systems*, 7(1):18-25, January 1996.
23. Mohapatra, P., C. Yu, and C. R. Das, "Allocation and Mapping Based Reliability Analysis of Multistage Interconnection Networks," *IEEE Transactions on Computers*, 45(5):600-606, May 1996.
24. Boura, Y. and C. R. Das, "Performance Analysis of Buffering Schemes in Wormhole Routers," *IEEE Transactions on Computers*, 46(6):687-694, June 1997.
25. Yoo, B. S. and C. R. Das, "A Fast and Efficient Processor Management Techniques for K-ary n-cubes," *Journal of Parallel and Distributed Computing*, 55(2):192-214, December 1998.
26. Vaidya, A., C. R. Das, and A. Sivasubramaniam, "A Testbed for Evaluation of Fault-Tolerant Routing in Multiprocessor Interconnection Networks," *IEEE Transactions on Parallel and Distributed Systems*, Special Issue on Fault-tolerant Routing, 10(10):1052-1066, October 1999.
27. Nagar, S., A. Banerjee, A. Sivasubramaniam, and C. R. Das, "Scheduling Alternatives to Coscheduling on a Network of Workstations," *Journal of Parallel and Distributed Computing*, Special Issue on Software support for Distributed Computers, 59(2):302-327, November 1999.
28. Kasbekar, M., C. Narayan, and C. R. Das, "Selective Checkpointing and Rollback in Multi-threaded Object-oriented Environment," *IEEE Transactions on Reliability*, selected as one of the four best papers from the 1999 Pacific-Rim Dependable Computing Symposium, 48(4):325-337, December 1999.
29. Vaidya, A., C. R. Das, and A. Sivasubramaniam, "Impact of Virtual Channel and Adaptive Routing on Application Performance," *IEEE Transactions on Parallel and Distributed Systems*, 12(2):223-237, February 2001.
30. Yoo. B. S. and C. R. Das, "A Fast and Efficient Allocation Scheme for Mesh-Connected Multicomputers," *IEEE Transactions on Computers*, 51(1):46-60, January 2002.
31. Yum, K. H., E. J. Kim, A. S. Vaidya, and C. R. Das, "MediaWorm: A QoS Capable Router Architecture for Clusters," *IEEE Transactions on Parallel and Distributed Systems*, Vol. 13, No. 12, pp. 1261-1274, December 2002.
32. Lim, S., G. Cao, and C. R. Das, "A Unified Bandwidth Reservation and Admission Control Mechanism for QoS Provisioning in Cellular Networks", *Wireless Communications and Mobile Computing (WCMC) Journal (special issue on Performance Evaluation of Wireless Networks)*, Vol. 4, No. 1, pp. 3-18, Feb 2004.
33. Cao, G., L. Yin, and C. R. Das, "A Cooperative Cache Based Data Access Framework for Ad Hoc Networks", *IEEE Computer*, pp. 32-39, Feb. 2004.
34. Zhu, H., G. Cao, G. Kesidis, and C. R. Das, "An Adaptive Power-Conserving Service Discipline for Bluetooth", *Computer Communication*, Vol. 27 (9), pp. 828-839, Sept. 2004.
35. Sarahan, N and C. R. Das, "Caching and Scheduling in NAD-Based Multimedia Servers", *IEEE Transactions on Parallel and Distributed Systems*, Vol. 15, No. 10, PP. 921-933, Oct. 2004.

36. Lim, S., W. Lee, G. Cao, and C. R. Das, "A Novel Caching Scheme for Improving Internet-based Mobile Ad Hoc Networks Performance, " Ad Hoc Networks Journal, Elsevier Science, Vol. 4(2), pp. 225-239, March 2006.
37. Kim, E. J., K. H. Yum, G. M. Link, N. Vijayakrishnan, M. Kandemir, M. J. Irwin, and C. R. Das, "Energy Optimization Techniques in Cluster Interconnects," *IEEE Transactions on Computers, Special issue on Low-Power Design*, 2005.
38. Kim, E. J., K. H. Yum, C. R. Das, M. Yousif, and J. Duato, "Exploring IBA Design Space for Improved Performance," *IEEE Transactions on Parallel and Distributed Systems*, Vol. 18 (4), pp. 498-510, April 2007.
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41. Kim, Suneuy and C. R. Das, "An analytical model for interval caching in interactive video servers," to appear in *Journal of Network and Computer Applications (JNCA)*, (Elsevier publisher).
42. Deng, X., S. Yi, G. Kesidis, and C. R. Das, "A Control Theoretic Analysis of Active Queue Management Schemes," to appear in *IEEE Transactions on Networking*.
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46. Lim, S., C. Yu, and C. R. Das, " RandomCast: An Energy Efficient Communication Scheme for Mobile Ad Hoc Networks", *IEEE Transactions on Mobile Computing*, 2009.
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48. Gunwoo Nam, Pushkar Patankar, George Kesidis, Chita R. Das, Cetin Seren, "Mass Purging of Stale TCP Flows in Per-Flow Monitoring Systems", ICCCN 2009.
49. Zhao, J., G. Cao, and C. R. Das, "Cooperative Caching in Wireless P2P Networks: Design, Implementation, and Evaluation", *IEEE Transactions on Parallel and Distributed Systems (TPDS)*, pp. 229-241, Feb. 2010.
50. Nicopoulos, C. A., S. Srinivasan, A. Yanamandra, D. Park, N. Vijaykrishnan, C.R. Das, and M.J. Irwin, "On the Effects of Process Variation in Network-on-Chip Architectures", *IEEE Transactions on Dependable and Secure Computing (TDSC)*, pp. 240-254, July 2010.
51. Lim, S., C. Yu, and C. R. Das, "A Realistic Mobility Model for Wireless Networks of Scale-Free Node Connectivity", *International Journal of Mobile Communication*, 8(3):351-369, May 2010.
52. Choi, G. S.and C. R. Das, "A Superscalar Software Architecture Model for Multi-Core Processors (MCPs)", *Journal of Systems and Software*, 83(10):1823-1837, Oct. 2010.

53. Yum, K. H., Y. Jin, E. J. Kim, and C. R. Das,“ Integration of Admission, Congestion, and Peak Power Control in QoS-aware Clusters”, *Journal of Parallel and Distributed Computing*, 70(11):1087-1099, Nov. 2010.
54. Mishra, A. K., J. L. Hellerstein, W. Cirne, and C. R. Das, “ Towards Characterizing Cloud Backend Workloads: Insights from Google Compute Clusters”, *Proceedings of the International Conference on Measurement and Modeling of Computer Systems* (SIGMETRICS 2010). pp. 34-41, June 2010.
55. Mishra, A. K., A. Yanamandra, R. Das, S. Eachempati, R. Iyer, N. Vijaykrishnan, and C. R. Das, “RAFT: A router architecture with frequency tuning for on-chip networks”, Journal of Parallel and Distributed Computing, 2011 (JPDC).
56. Das, R., O. Mutlu, T. Moscibroda, and C. R. Das, “Aergia: A Network-on-Chip Exploiting Packet Latency Slack”, *Top Picks, IEEE Micro*, 2011.
57. Lim, S., C. Yu, C. R. Das, “Cache Invalidation Strategies for Internet-based Vehicular Ad Hoc Networks”, *Computer Communications*, February 2012.
58. Surender, S. C., R. Narayan, C. R. Das, “Cross-layer Resource Allocation in UWB Noise OFDM based Ad Hoc Surveillance Networks”, *EURASIP Journal on Wireless Communication and Networking*, January 2013.

Refereed Conference Papers

1. Das, C. R. and L. N. Bhuyan, “Computation Availability of Multiple-Bus Multiprocessors ,” *International Conference on Parallel Processing*, pp. 807-813, August 1985.
2. Das, C. R. and L. N. Bhuyan, “Reliability Simulation of Multiprocessor Systems,” *International Conference on Parallel Processing*, pp. 591-598, August 1985.
3. Bhuyan, L. N. and C. R. Das, “Dependability Evaluation of Multicomputer Networks,” *International Conference on Parallel Processing*, pp. 576-583, August 1986.
4. Sheu, T. L., W. Lin, and C. R. Das, “An Efficient Parallel Algorithm of Conjugate Gradient Method,” *International Conference on Supercomputing*, pp. 488-496, May 1987.
5. Lin, W., M. J. Thazhuthaveetil, and C. R. Das, “A Parallel Matrix Inversion Algorithm with Dynamic Communication Structures,” *International Conference on Supercomputing*, pp. 460-466, May 1988.
6. Macaluso, J., C. R. Das, and W. Lin, “A Reliability Predictor for MIN-Connected Multiprocessor Systems,” *International Conference on Parallel Processing*, pp. 392-399, August 1988.
7. Lin, W., T.-L. Sheu, C. R. Das, C.-L. Wu, and T.-Y. Feng, “Fast Data Selection and Broadcast On the Butterfly Network,” *International Workshop on Future Trends of Distributed Computing Systems in the 90’s*, pp. 65-72, September 1988.
8. Lin, W., T.-L. Sheu, and C. R. Das, “A Quadtree Communication Structure for Fast Data Searching and Distribution,” *COMPSAC*, pp. 316-323, October 1988.
9. Sheu, T. L., W. Lin, and C. R. Das, “A Parallel Eigen Value Algorithm with Dynamic Communication Structure,” *International Computer Symposium*, pp. 117-122, December 1988.
10. Das, C. R. and J. Kim, “An Analytical Model for Computing Hypercube Availability,” *International Symposium on Fault-Tolerant Computing Systems*, pp. 530-537, June 1989.
11. Sheu, T. L., W. Lin, C. R. Das, and M. J. Irwin, “Distributed Fault Diagnosis in the Butterfly Parallel Processor,” *International Conference on Parallel Processing*, I, pp. 172-175, August 1989.

12. Kim, J., C. R. Das, and W. Lin, "A Processor Allocation Scheme for Hypercube Computers," *International Conference on Parallel Processing*, (II), pp. 231-238. (Daniel L. Slotnick Award for the Most Original Paper), August 1989.
13. Das, C. R., L. Tien, and L. N. Bhuyan, "Availability Evaluation of MIN-Connected Multiprocessors Using Decomposition Technique," *International Symposium on Fault-Tolerant Computing Systems*, pp. 176-183, June 1990.
14. Algudady, M. S., C. R. Das, and W. Lin, "A Fault-Tolerant Task Mapping Algorithms for MIN-Based Multiprocessors," *International Conference on Parallel Processing*, I, pp. 445-448, August 1990.
15. Algudady, M. S., C. R. Das, and M. J. Thazhuthaveetil, "A Write Invalidate Cache Coherence Protocol for MIN-Based Multiprocessors," *ISMM International Conference on Parallel and Distributed Computing and Systems*, pp. 77-81, October 1990.
16. Das. C. R., M. S. Algudady, and M. J. Thazhuthaveetil, "A Write-Update Cache Coherence Protocol for MIN-Based Multiprocessor Systems with Accessibility-Based Split Caches," *Supercomputing '90*, pp. 544-553, November 1990.
17. Kim, J. and C. R. Das, "Modeling Wormhole Routing in a Hypercube," *International Conference on Distributed Computing Systems*, pp. 386-393, May 1991. (Outstanding Paper Award).
18. Yang, M. K. and C. R. Das, "A Parallel Branch-and-Bound Algorithm for MIN-Based Multiprocessors," (poster paper) *ACM SIGMETRICS Conference on Measurements and Modeling of Computer Systems*, pp. 222-233, May 1991.
19. Kim, J. and C. R. Das, "On Subcube Dependability in a Hypercube," *ACM SIGMETRICS Conference on Measurements and Modeling of Computer Systems*, pp. 111-119, May 1991.
20. Algudady, M. S., C. R. Das, and M. J. Thazhuthaveetil, "Cache-Based Checkpointing Scheme for MIN-Based Multiprocessors," *International Conference on Parallel Processing*, pp. 497-500, August 1991.
21. Yang, M. K. and C. R. Das, "Analytical Modeling of a Parallel Branch-and-Bound Algorithm on MIN-Based Multiprocessors," *International Parallel Processing Symposium*, March 1992.
22. Yu, C. S. and C. R. Das, "Multitasking in Multistage Interconnection Network Machines," *International Conference on Distributed Computing Systems*, pp. 30-37, June 1992.
23. Das, C. R., P. Mohapatra, and C. S. Yu, "Allocation-Based Subcube Dependability for MIN-Based Multiprocessors," *Workshop on Fault-Tolerant Parallel and Distributed Systems*, pp. 124-131, July 1992.
24. Kim, J., K. G. Shin, and C. R. Das, "Performability Evaluation of Gracefully Degradable Hypercube Multicomputers," *Workshop on Fault-Tolerant Parallel and Distributed Systems*, pp. 140-147, July 1992.
25. Orzechowski, N. S., S. R. T. Kumara, and C. R. Das, "Performance of Multilayer Neural Networks in Binary-to-Binary Mappings Under Weight Errors," *The IEEE International Conference on Neural Networks*, III, pp. 1684-1689, April 1993.
26. Orzechowski, N. S., S. R. T. Kumara, and C. R. Das, "Performance Analysis of Neural Networks," *ORSA/TIMS Annual Meeting*, May 1993.
27. Mohapatra, P., C. S. Yu, and C. R. Das, "A Lazy Scheduling Scheme for Improving Hypercube Performance," *International Conference on Parallel Processing*, I, pp. 110-117, August 1993.
28. Mohapatra, P. and C. R. Das, "A Queueing Model for Finite-Buffer MINs," *International Conference on Parallel Processing*, I, pp. 210-213, August 1993.

29. Algudady, M. S., C. R. Das, and M. J. Thazhuthaveetil, "A Hierarchical Cache-Coherence Protocol with Limited Inclusion," *International Conference on Parallel Processing*, I, pp.254-257, August 1993.
30. Boura, Y. and C. R. Das, "A Class of Partially Adaptive Routing Algorithms for n-dimensional Meshes," *International Conference on Parallel Processing*, III, pp. 175-182, August 1993.
31. Mohapatra, P., S. Wong, and C. R. Das, "Analytical Modeling of Combining in Multistage Interconnection Networks," *Modeling Techniques and Tools for Computer Performance Evaluation*, (poster paper), May 1994.
32. Boura, Y. M. and C. R. Das. "Efficient Fully Adaptive Wormhole Routing in n-Dimensional Meshes," *International Conference on Distributed Computing Systems*, pp. 589-596, June 1994.
33. Mohapatra, P., S. Wong, and C. R. Das, "Performance Analysis of Combining Multistage Interconnection Networks," *International Conference on Parallel Processing*, I, pp. 13-16, August 1994.
34. Agarwala, A. and C. R. Das, "A Shared Memory Environment for Hypercubes," *International Conference on Parallel Processing*, I, pp. 200-207, August 1994.
35. Yu, C. and C. R. Das, "Limit Allocation: An Efficient Processor Management Scheme for Hypercubes," *International Conference on Parallel Processing*, II, pp. 143-150, August 1994.
36. Yousif, M. S. and C. R. Das, "A Switch Cache Design for MIN-Based Shared-Memory Multiprocessors," *Conpar 94 International Conference on Parallel Processing*, Springer-Verlag LNCS 854, pp. 426-437, September 1994.
37. Boura, Y. M., C. R. Das, and T. M. Jacob, "A Performance Model for Adaptive Routing in Hypercubes," *First International Workshop on Parallel Processing*, pp. 11-16, December 1994.
38. Boura, Y. M. and C. R. Das, "Modeling Virtual Channel Flow Control in Hypercubes," *IEEE Symposium on High Performance Computer Architecture* (HPCA-1), pp. 166-175, January 1995.
39. Boura, Y. M. and C. R. Das, "Fault-Tolerant Routing in Mesh Networks," *International Conference on Parallel Processing*, I, pp. 106-109, August 1995.
40. Yoo, B. S., C. R. Das, and C. Yu, "Processor Management Techniques for Mesh Connected Multiprocessors," *International Conference on Parallel Processing*, II, pp. 105-112, August 1995.
41. Vaidya, A. S, B. S. Yoo, and C. R. Das, "On the Dependability Modeling of Parallel Computers," In *Fault-Tolerant Systems and Software (Proceedings of the First Conference on Fault-Tolerant Systems*, Madras, India*)*, edited by R. Mittal, C. R. Muthukrishnan, V. P. Bhatkar, pp. 82-91, December 1995.
42. Rahman, S. and C. R. Das, "Parallel Simulation of Mesh Routing Algorithms," *International Conference on Distributed Computing Systems*, pp. 158-165, May 1996.
43. Vaidya, A. S., B. S. Yoo, C. R. Das, and J. Kim, "A Task-Based Dependability Model for k-ary n-cubes," *International Conference on Parallel Processing*, Vol. I, pp. 9-16, August 1996.
44. Chodnekar, S., V. Srinivasan, A. Vaidya, A. Sivasubramaniam, and C. R. Das, "Towards a Communication Characterization Methodology for Parallel Applications," *IEEE Symposium on High Performance Computer Architecture* (HPCA-3), pp. 310-319, February 1997.
45. Vaidya, A., A. Sivasubramaniam, and C. R. Das, "Performance Benefits of Virtual Channels and Adaptive Routing: An Application-Driven Study," *International Conference on Supercomputing*, pp. 140-147, July 1997.
46. Yoo, B. S. and C. R. Das, "A Good Processor Management Scheme = Fast Allocation + Efficient Scheduling," *International Conference on Parallel Processing*, pp. 280-287, August 1997.

47. Seed, D., A. Sivasubramaniam, and C. R. Das, "Communication in Parallel Applications: Characterization and Sensitivity Analysis," *International Conference on Parallel Processing*, pp. 446-453, August 1997.

48. Yoo, B. S., C. R. Das, and J. Kim, "A Performance Modeling Technique for Mesh-Connected Systems," *International Conference on Parallel and Distributed Systems*, pp. 408-413, *Seoul, Korea*, December 1997.

49. Kim, S., A. Sivasubramaniam, and C. R. Das, "Analyzing Cache Performance Multimedia Servers," *Workshop on Architectural and Operating System Support for Multimedia Applications*, pp. 38-47, Minneapolis, August 1998.

50. Agnihotri, P, V. Agrawala, K. Morooney, and C. R. Das, "The Penn State Computing Condominium Scheduling System," *ACM/IEEE conference on Supercomputing* (SC), October 1998.

51. Kasbekar, M., C. Narayan, and C. R. Das, "Using Reflection for Checkpointing Objected Oriented Programs," *OOPSLA*, pp. 71-75, Vancouver, Canada, October 1998.

52. Vaidya, A., A. Sivasubramaniam, and C. R. Das, "LAPSES: A Recipe for High Performance Adaptive Router Design," *IEEE Symposium on High Performance Computer Architecture* (HPCA-5), pp. 236-243, Orlando, January 1999.

53. Nagar, S., A. Banerjee, A. Sivasubramaniam, and C. R. Das, "A Closer Look at Co-Scheduling Approaches for a Network of Workstations," Eleventh ACM Symposium on Parallel Algorithms and Architectures (SPAA), pp. 96-105, St. Malo, France, June 1999.

54. Yang, M. K. and C. R. Das, "A Parallel Optimal Branch-and-Bound Algorithm for MIN-Based Multiprocessors," International Conference on Parallel Processing. pp. 112-119. Aizu-Wakamatsu City, Japan, September 1999.

55. Kasbekar, M., S. Yajnik, R. Klemm, Y. Huang, and C. R. Das, "Issues in the Design of a Reflective Library for Checkpointing for C++ Objects," Symposium on Reliable Distributed Systems (SRDS), pp. 224-233, Lausanne, Switzerland, October 1999.

56. Kasbekar, M., C. Narayanan, and C. R. Das, "Selective Checkpointing and Rollbacks in Multithreaded Object-Oriented Environments," 1999 Pacific Rim International Symposium on Dependable Computing (PRDC), pp. 121-128, Hong Kong, December 1999.

57. Yum, K. H., A. Vaidya, C. R. Das, and A. Sivasubramaniam, "Investigating QoS Support for Traffic Mixes with the MediaWorm Router," *IEEE Symposium on High Performance Computer Architecture* (HPCA-6), pp. 97-106, France, January 2000.

58. Kim, S. and C. R. Das, "A Reliable Statistical Admission Control Policy for Interactive Video-On-Demand Servers with Interval caching," *International Conference on Parallel Processing*, pp. 135-142, August 2000.

59. Kim, S., C. R. Das, and A. Sivasubramaniam, "Performance Analysis of A Buffer Management Technique for Interactive Video-on-Demand," Proc. of the *International Conference on Multimedia Modeling*, (MMM'2000), Japan, November 2000.

60. Kasbekar, M. and C. R. Das, "Selective Checkpointing and Rollbacks in Multithreaded Distributed Systems," Proc. of the *International Conference on Distributed Computing Systems* (ICDCS), pp. 39-46, Arizona, April 2001.

61. Yum, K. H., E. J. Kim, and C. R. Das, "QoS Provisioning in Clusters: An Investigation of Router and NIC Design," Proc. *International Symposium on Computer Architecture* (ISCA), pp. 120-129, Sweden, June 2001.

62. Sarahan, N. and C. R. Das, "Adaptive Block Rearrangement Policies for Video-On-Demand Servers," Proc. *International Conference on Parallel Processing*, pp. 452-459, Spain, September 2001.

63. Lim, S., G. Cao, and C. R. Das, "A Differential Bandwidth Reservation Algorithm for Multimedia Wireless Networks," Proc. of the Mobile Computing Workshop, *International Conference on Parallel Processing*, pp. 447-452, Spain, September 2001.

64. Kim, E. J., K. H. Yum, and C. R. Das, "An Analytical Model for a QoS Capable Cluster Interconnect," Proc. *Inter. Conf. on Measurement, Modeling and Evaluation of Computer and Communication Systems* (MMB), pp. 9-24, Germany, September 2001.

65. Cao, G. and C. R. Das, "On the Effectiveness of a Counter-Based Cache Invalidation Scheme and its Resiliency to Failures in Mobile Environments," Proc. of the *20th IEEE Symposium on Reliable Distributed Systems (SRDS)*, October 2001.

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Student Supervision:

Ph.D. Students : 38 (31 completed)

J. Kim (POSTECH, Korea), M. S. Yousif (IBM), M. K. Yang (University of Ulsan, Korea), P. Mohapatra (UC, Davis), N. Marchaoui (IBM), C. Yu (Cleveland State Univ.), Y. Boura (Pyramid Co.), B. S. Yoo (LL Nat'l Lab), A. Vaidya (NVIDIA), S. Kim (San Jose State Univ.), M. Kasbekar (Akamai), K. H. Yum (UTexas, San Antonio), N. Sarhan (Wayne State Univ.), E. J. Kim (Texas A&M Univ.), X. Deng (CDC), S. Lim (Texas Tech, Lubbock), S. Yi (ETRI, Korea), G. S. Choi (Yeungnam University, Korea), J. H. Kim (Samsung, Korea), J. M. Kim (Georgia Tech), D. Ersoz (Cisco), D. Park (Intel), P. Patnaker (Cisco), R. Das (Univ. of Michigan), A. K. Mishra (Intel), S. Surender (Cisco), S. Lim (Oak Ridge Natl. Lab), B. Sharma (Microsoft), A. Jog (College of William & Mary), O. Kayiran (AMD Research), N. Chidambaram (Apple)

M.S. Students : 55+

B.S. (Honors Students): 15+

Courses Taught:

Logical Design of Digital Systems, Fault-Tolerant Systems, Performance Evaluation, Computer Architecture, Data Communication Networks, Multiprocessor Architecture, Network-on-Chip (NoC) architectures, Parallel I/O, Internet QoS.

Research Grants:

Dependability and Performance Models for Parallel Computers. National Science Foundation, Research Initiation, PI, 1988-89, $59,400.

An Educational Supplement Proposal for Developing a System Modeling Package for Undergraduate Education. Supplemental support to Research Initiation, National Science Foundation, PI, 1989-90, $20,000.

Evaluation of Parallel Architecture for BM/C^3 Applications (with T.-Y. Feng, W. Lin, M. J. Thazhuthaveetil). Rome Air Development Center, Co-PI, 1988-89, $500,000.

Evaluation Technique for Hypercube and MIN-Based Architectures. National Science Foundation, (with T.-Y.Feng), Co-PI, 1991-94, $253,777.

Low Cost Adaptive Routing Algorithms for n-Dimensional Meshes. National Science Foundation, PI, 1994-1996, $116,969.

Parallelization of Fire Growth Codes. NASA/STIR, (with A. Kulkarni), Co-PI, 1995-1996, $6,000.

A Proposal for the Revision of the Logic Design of Digital Systems Course. College of Engineering, PI, 1995-1996, $8,500.

Application-Driven Network Performance Evaluation. National Science Foundation, PI, 1996-1999, $224,496.

Developing and Evaluating Low-cost Communication for a Network of Workstations. IBM/SUR Equipment, (with A. Sivasubramaniam), PI, 1996-1997, $193,240.

CISE Research Instrumentation for Developing a NOW Platform for Parallel Processing. National Science Foundation, (with A. Sivasubramaniam), PI, 1997-1998, $110,550.

Application-Driven Network Performance Evaluation. REU Supplement, National Science Foundation, PI, 1997-1998, $10,000.

A Low-Cost High Performance Computing Platform. CISE Research Instrumentation. National Science Foundation, (with A. Sivasubramaniam), PI, 1999-2001, $79,973.

An Integrated Approach for Quality of Service in Cluster Networks. National Science Foundation, (with A. Sivasubramaniam), PI, 1999-2002, $380,365.

Performance Modeling of Unisys Computer Systems. PI, Unisys Corporation, 1999-2003, $140,000.

MediaWorm: A Single-Chip Router Architecture. Pennsylvania/Pittsburgh Digital Greenhouse Consortium, (with M. J. Irwin, V. Narayanan), PI, 2000-2001, $298,481.

Scalable and Efficient Scheduling Techniques for Clusters. National Science Foundation, PI, 2001-2004, $254,883.

QoS Provisioning in InfiniBand Architecture (IBA) for System Area Networks. National Science Foundation, PI, 2002-2005, $331,964.

I^3C: An Infrastructure for Innovation in Information Computing. Research Infrastructure Grant, National Science Foundation, (with R. Acharya, C. L. Giles, M. J. Irwin, and P. Raghavan), PI, 2002-2008, $2,561,036 (includes $765,307 University matching).

Exploring Network-on-Chip (NoC) Architecture Design Space. National Science Foundation, PI, 2004-2008, $190,000.

Exploring Cluster-Based Data Center Design Space for High Performance and Dependability. National Science Foundation, PI, 2005-2008, $346,529.

Purposeful Node Mobility for Mission-Oriented Sensor Networks. National Science Foundation, (with G. Cao, T. Laporta, and G. Kesidis), 2005-2008, $450,000.

Protecting TCP Congestion Control: Tools for Design, Analysis, and Emulation. National Science Foundation, Co-PI, (with G. Kesidis), 2005-2008, $350,000, total grant with Purdue University $675,000.

Impact of User-Level Communication on Data Center Performance. Intel Research, PI, 2005-2008, $195,000.

Performance and Energy-Efficient Network-on-Chip (NoC) Architectures. Intel Research, PI, 2006-2009, $150,000.

Randomized Session-Memory Purging in Internet Routers. Cisco, (with G. Kesidis), Co-PI, 2007-2009, $98,540.

HoDoo: Holistic Design of On-chip Interconnects. National Science Foundation, (with V. Narayanan and Yuan Xie), PI, 2007-2010, $630,894.

Collaborative Data Access in Wireless P2P Networks. National Science Foundation, (with G. Cao), Co-PI, 2007-2010, $600,000.

Investigating Resource Contracts with Statistical Guarantees for Google Data Centers. Google Research, PI, 2010-2011, $65,000.

Exploring Design of On-Chip Interconnects for SoC/CMP Architectures. Intel Research, PI, 2010-2011, $75,000.

Data Center on a Chip: Design Space Exploration. Intel Research, PI, 2010-2011, $50,000.

Harnessing Cross-Layer Heterogeneity for future CMPs. National Science Foundation - EAGER, (with A. Sivasubramaniam, V. Narayanan, Y. Xie and M. Kandemir), PI, 2011-2012, $300,000.

Exploring Managed Soft Computing for Data Intensive Applications. National Science Foundation - EAGER, (with A. Sivasubramaniam and M. Kandemir), PI, 2011-2012, $300,000.

Architecting the Next Generation Memory Hierarchy - A Holistic Approach. National Science Foundation - (with M. Kandemir, A. Sivasubramaniam, O. Mutlu, and Y. Xie), PI, 2012-2016, $1,700,000.

INSpiRE: Infrastructure for heterogeNeous System ResEarch. National Science Foundation - (with M. Kandemir, A. Sivasubramaniam, V. Narayanan and D. Kiefer), PI, 2012-2015, $550,000.

Breaking the Physical Divide Between Computation and NAND-Flash Storage. National Science Foundation - (with M. Kandemir and A. Sivasubramaniam), Co-PI, 2013-2016, $800,000.

Visual Cortex on Silicon. National Science Foundation Expeditions - (with Vijaykrishnan Narayanan, John Carroll, Mary Beth Rosson, C. Giles), Co-PI, 2013-2018, $4,913,456.

PROM in Clouds: Exploiting Scheduling for Performance Optimization in Clouds. National Science Foundation, PI, 2013-2018, $495,197.

Extracting Scalable Parallelism by Relaxing the Contracts across the System Stack. National Science Foundation - (with M. Kandemir and A. Sivasubramaniam), Co-PI, 2013-2016, $850,000.

Enabling GPUs as First Class Computing Engines. National Science Foundation - (with M. Kandemir), Co-PI, 2014-2017, $484,068.

Virtualizing Coordinated Resource Management of Flows on Handhelds with VIADUCT. National Science Foundation - (with A. Sivasubramaniam and M. Kandemir), Co-PI, 2015-2018, $499,998.

A Fresh Look at Near Data Computing: Coordinated Data and Computation Government. National Science Foundation - (with M. Kandemir and A. Sivasubramaniam), Co-PI, 2016-2019, $875,000.

GEMDROID: A Comprehensive Platform for Studying Architectural Issues for Next Generation Mobile Systems. National Science Foundation - (with A. Sivasubramaniam and M. Kandemir), PI, 2016-2019, $1,000,000.

Honors and Awards:

Fellow of IEEE

ISCA Hall of Fame

HPCA Hall of Fame

Daniel L. Slotnick Award for the Best Original Paper: A Processor Allocation Scheme for Hypercube Computers, *International Conference on Parallel Processing,* Aug. 1989.

IEEE Computer Society Outstanding Paper Award: Modeling Wormhole Routing in a Hypercube, *International Conference on Distributed Computing Systems,* May 1991.

Best Paper Award: Selective Checkpointing and Rollbacks in Multi-threaded Object-oriented Environment, *Pacific-Rim Dependable Computing (PRDC) Symposium* December 1999.

Teaching Award: Department of Computer Science and Engineering, 2001.

Nominated for Best paper Award: Performance Comparison of Cache Invalidation strategies for Internet-based Mobile Ad Hoc networks. *International Conference on Mobile Ad-hoc and Sensor Systems* (MASS), Oct. 2004.

Nominated for Best paper Award: Coscheduling in Clusters: Is it a Viable Alternative?, *Super Computing, (SC),* Nov. 2004.

IEEE Computer Society Voluntary Service Award: for HPCA 2006, Program Chair, Austin, Texas, 2006.

Outstanding Achievement Award: IEEE Technical Committee on Distributed Systems (TCDP).

Distinguished Service Award: IEEE Computer Society for Chairing the Fellow Selection Committee.

IEEE Computer Society Outstanding Service Award: for HPCA-2010, General Co-Chair, Bangalore, India, 2010.

IEEE MICRO Top Picks: Aergia: Exploiting Packet Latency Slack in On-Chip Networks, *Special Issue: IEEE Micro's Top Picks from 2010 Computer Architecture Conferences*, Jan/Feb 2011.

Department/College Committee Activities:

Chair, College of Engineering Chair Professor Evaluation Committee, 2004-2006
Chair, Search Committee for Department Head, Computer Science and Engineering
Chair, Department Promotion and Tenure Committee
Chair, Department Faculty Search Committee
Chair, Department Graduate Committee
Chair, Department Award Committee
Member, College of Engineering Graduate Council
Member, University Graduate Council
Member, Department Promotion and Tenure Committee, Faculty Search Committee, Graduate Committee,
Member, Personnel Committee, Undergraduate Committee, Teaching Load Committee, IT Committee, EECS Strategic Committee
Member, College AD-14 Administrative Review Committee
Member, Non-tenure Track (NTT) Committee
Member, EECS Director Search Committee and Award Committee.

Selected Professional Society Activities:

Editorial and Technical Committee Activities:

Associate Editor, *IEEE Transactions on Parallel and Distributed Systems*, 1994-1997
Member, Advisory Board, *IEEE Technical Committee on Computer Architecture (TCCA)*, 1995-1998
Associate Editor, *IEEE Transactions on Computers*, 2001-2004
Chair, *IEEE Technical Committee on Distributed Processing (TCDP)*, 2002-2004.
Fellow Selection Committee, *IEEE (CS) Fellow Selection Committee*, 2002-2005.
Chair, *IEEE TPDS Editor-In-Chief evaluation Committee*, 2002-2003.
Editor-in-Chief Search Committee member, *IEEE Transactions on Dependable and Secure Computing*, 2003.
Editor-in-Chief Search Committee member, *IEEE Transactions on Computers*, 2004.
Chair, Editor-in-Chief Search Committee, *IEEE Transactions on Parallel and Distributed Systems*, 2006.
Chair, *IEEE Computer Society Conference Publications Operations Committee (CPOC)*, 2007-2009.
Vice-Chair, *IEEE Computer Society Fellow Selection Committee*, 2007-2008.
Chair, *IEEE Computer Society Fellow Selection Committee*, 2008-2009.
Member, Advisory Board, *Indian Institute of Technology, Bhubaneswar*, 2009-present
Member, Advisory Board, *IEEE Technical Committee on Computer Architecture (TCCA)*, 2010-present
Member, Advisory Board, *SoA University, Bhubaneswar*, 2014-present
Steering Committee, *International Conference on Information Technology (ICIT), India*

Selected Program Committee Activities:

Program Committee Member of various international Conferences such as ISCA, HPCA, MICRO, SIGMETRICS, ICDCS, IPDPS, PACT, ICAC, ICPP, ICS, FTCS, DSN, ANCS, PRDC, MASCOT, ADCOM, EEHiPC and HiPC.
General Co-Chair, *International Conference on Parallel Processing*, 1996
General Chair, *Euro-Par Workshop on Routing and Communication in Networks*, 1997

Program Chair, *6th International Conference on Advanced Computing* , 1998
Workshop Chair, *International Conference on Parallel Processing* (ICPP), 1998
Program Chair, *7th International Conference on Advanced Computing* , 1999
General Chair, *International Conference on Information Technology*, India, December 2001
Program Chair, *IEEE Symposium on High Performance Computer Architecture* (HPCA-2006).
Program Vice-Chair, *28th International Conference on Distributed Computing Systems*, (ICDCS-2008)
Steering Committee Member, *Workshop on Advancing Computer Architecture Research* (ACAR-1), 2010
Steering Committee Member, *Workshop on Advancing Computer Architecture Research* (ACAR-2), 2010
General Co-Chair, *IEEE Symposium on High Performance Computer Architecture* (HPCA), 2010
Steering Committee Member, *IEEE Symposium on High Performance Computer Architecture* (HPCA), 2010
Steering Committee Member, *IEEE Symposium on High Performance Computer Architecture* (HPCA), 2011
Steering Committee Member, *International Symposium on Computer Architecture* (ISCA), 2011
Program Co-Chair, *Sixth International Symposium on Network on Chip* (NOCS-2012), Denmark
General Co-Chair, *Seventh International Symposium on Network on Chip* (NOCS-2013), Arizona
Steering Committee Member, *International Symposium on Network on Chip* (NOCS 2013- Present)
Program Co-Chair, *Eleventh Symposium on Architectures for Networking and Communications Systems* (ANCS-2015), California

Government Administrative Activities:
Program Director, Computer Architecture Program, *National Science Foundation*, CISE/CCF Division, 2008-2010