



TLV170x 2.2-V to 36-V, microPower Comparator

1 Features

- Supply Range:
+2.2 V to +36 V or ± 1.1 V to ± 18 V
- Low Quiescent Current:
55 μ A per Comparator
- Input Common-Mode Range Includes Both Rails
- Low Propagation Delay: 560 ns
- Low Input Offset Voltage: 300 μ V
- Open Collector Outputs:
 - Up to 36 V Above Negative Supply Regardless of Supply Voltage
- Industrial Temperature Range:
–40°C to +125°C
- Small Packages:
 - Single: SC70-5, SOT-23-5, SOT553-5
 - Dual: VSSOP-8, X2QFN-8
 - Quad: TSSOP-14

2 Applications

- Overvoltage and Undervoltage Detectors
- Window Comparators
- Overcurrent Detectors
- Zero-Crossing Detectors
- System Monitoring for:
 - Power Supplies
 - White Goods
 - Industrial Sensors
 - Automotive
 - Medical

3 Description

The TLV170x family of devices offers a wide supply range, rail-to-rail inputs, low quiescent current, and low propagation delay. All these features come in industry-standard, extremely-small packages, making these devices the best general-purpose comparators available.

The open collector output offers the advantage of allowing the output to be pulled to any voltage rail up to +36 V above the negative power supply, regardless of the TLV170x supply voltage.

These devices are available in single (TLV1701), dual (TLV1702), and quad (TLV1704) channel versions. Low input offset voltage, low input bias currents, low supply current, and open-collector configuration make the TLV170x family flexible enough to handle almost any application, from simple voltage detection to driving a single relay.

All devices are specified for operation across the expanded industrial temperature range of –40°C to +125°C.

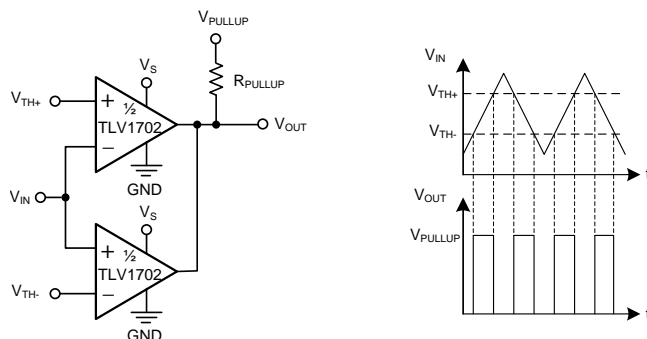
Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV1701	SOT553 (5)	1.20 mm x 1.60 mm
	SC-70 (5)	1.25 mm x 2.00 mm
	SOT-23 (5)	1.60 mm x 2.90 mm
TLV1702	X2QFN (8)	1.50 mm x 1.50 mm
	VSSOP (8) ⁽²⁾	3.00 mm x 3.00 mm
TLV1704	TSSOP (14)	4.40 mm x 5.00 mm

(1) For all available packages, see the package option addendum at the end of the datasheet.

(2) The VSSOP package is the same as the MSOP package.

TLV1702 as a Window Comparator



Stable Propagation Delay vs Temperature

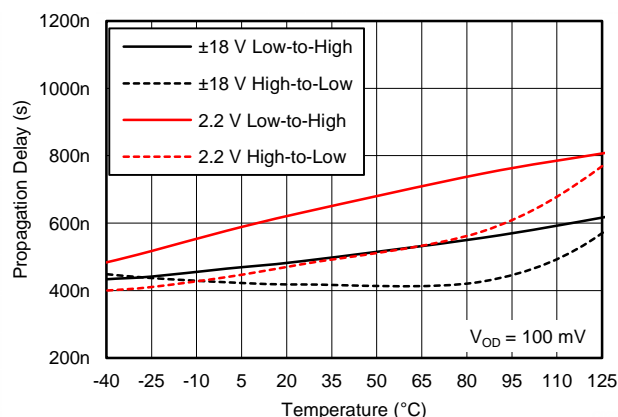


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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (December 2014) to Revision D	Page
• Changed document status to Production Data from Mixed Status	1
• Changed status of TLV1702 RUG package to Production Data	1
Changes from Revision B (October 2014) to Revision C	Page
• Changed TLV1701 DCK package from preview to production data	1
• Changed Handling Ratings table to ESD Ratings table, and moved storage temperature to Absolute Maximum Ratings table	6
Changes from Revision A (September 2014) to Revision B	Page
• Changed footnote 2 in Device Information table: added TLV1701 to list of available devices	1
• Added TLV1701 to list of production data packages in footnote for the <i>Pin Configuration and Functions</i> section	5
• Added TLV1701 row to $V_{(ESD)}$ parameter in Handling Ratings table	6

Changes from Original (December 2013) to Revision A
Page

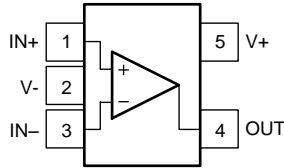
• Changed document format to latest data sheet standards; added new sections and moved existing sections	1
• Changed TLV1704 PW (TSSOP-14) package from preview to production data	1
• Added sub-bullet to the Open Collector Outputs feature	1
• Added second paragraph to the Description section.....	1
• Deleted package information from Description section; redundant information	1
• Changed Related Products table to Device Comparison table, moved from page 1, and added TLV370x family	4
• Added TLV1701, TLV1702 RUG, and TLV704 package drawings	5
• Added thermal information for TLV1702 RUG, TLV1704 PW, and all TLV1701 packages	6
• Moved switching characteristics parameters from Electrical Characteristics table to new Switching Characteristics table ..	7
• Changed all typical values in Switching Characteristics table.....	7
• Changed title for Figure 1	8
• Changed Figure 8	8
• Changed Figure 9	8
• Changed Figure 10	8
• Changed Figure 11	8
• Changed Figure 12	8
• Changed Figure 13	9
• Changed Figure 14	9
• Changed Application Information and moved section	13
• Deleted <i>Application Examples</i> section	13

5 Device Comparison

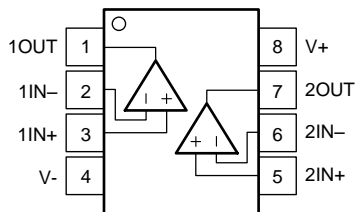
DEVICE	FEATURES
TLV3201	40-ns, 40- μ A, push-pull comparator
TLV3202	
TLV3501	4.5-ns, rail-to-rail, push-pull, high-speed comparator
TLV3502	
TLV3401	Nanopower open-drain output comparator
TLV3402	
TLV3404	
TLV3701	Nanopower push-pull output comparator
TLV3702	
TLV3704	
REF3325	3.9- μ A, SC70-3 voltage reference
REF3330	
REF3333	

6 Pin Configuration and Functions

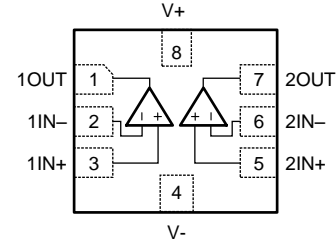
TLV1701
DBV (SOT-23-5), DCK (SC70-5), DRL (SOT553-5) Packages
Top View



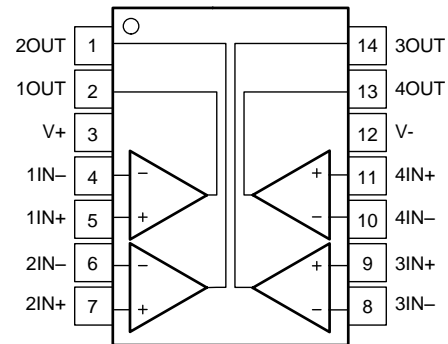
TLV1702
DGK (VSSOP-8) Package
Top View



TLV1702
RUG (X2QFN-8) Package
Top View



TLV1704
PW (TSSOP-14) Package
Top View



Pin Functions

NAME	PIN NO.			I/O	DESCRIPTION
	TLV1701 DBV, DCK, DRL	TLV1702 DGK, RUG	TLV1704 PW		
IN+	1	—	—	I	Noninverting input
1IN+	—	3	5	I	Noninverting input, channel 1
2IN+	—	5	7	I	Noninverting input, channel 2
3IN+	—	—	9	I	Noninverting input, channel 3
4IN+	—	—	11	I	Noninverting input, channel 4
IN-	3	—	—	I	Inverting input
1IN-	—	2	4	I	Inverting input, channel 1
2IN-	—	6	6	I	Inverting input, channel 2
3IN-	—	—	8	I	Inverting input, channel 3
4IN-	—	—	10	I	Inverting input, channel 4
OUT	4	—	—	O	Output
1OUT	—	1	2	O	Output, channel 1
2OUT	—	7	1	O	Output, channel 2
3OUT	—	—	14	O	Output, channel 3
4OUT	—	—	13	O	Output, channel 4
V+	5	8	3	—	Positive (highest) power supply
V-	2	4	12	—	Negative (lowest) power supply

7 Specifications

7.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage			+40 (±20)	V
Signal input pins	Voltage ⁽²⁾	(V _{S-}) – 0.5	(V _{S+}) + 0.5	V
	Current ⁽²⁾		±10	mA
Output short-circuit ⁽³⁾		Continuous		mA
Operating temperature range		–55	+150	°C
Junction temperature, T _J			150	°C
Storage temperature, T _{stg}		–65	+150	°C

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
- (3) Short-circuit to ground; one comparator per package.

7.2 ESD Ratings

			VALUE	UNIT
TLV1701 and TLV1702				
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1500	
TLV1704				
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage V _S = (V _{S+}) – (V _{S-})	2.2 (±1.1)		36 (±18)	V
Specified temperature	–40		125	°C

7.4 Thermal Information: TLV1701

THERMAL METRIC ⁽¹⁾		TLV1701			UNIT
		DRL (SOT553)	DCK (SC70)	DBV (SOT23)	
		5 PINS	5 PINS	5 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	271.5	283.6	233.1	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	115.6	94.1	156.4	°C/W
R _{θJB}	Junction-to-board thermal resistance	89.7	61.3	60.6	°C/W
ψ _{JT}	Junction-to-top characterization parameter	17.6	1.9	35.7	°C/W
ψ _{JB}	Junction-to-board characterization parameter	89.2	60.5	59.7	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Thermal Information: TLV1702 and TLV1704

THERMAL METRIC ⁽¹⁾		TLV1702		TLV1704	UNIT
		RUG (QFN)	DGK (VSSOP)	PW (TSSOP)	
		8 PINS	8 PINS	14 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	205.6	199	128.1	°C/W
θ_{JCTop}	Junction-to-case (top) thermal resistance	77.1	89.5	56.5	°C/W
θ_{JB}	Junction-to-board thermal resistance	107.0	120.4	69.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.0	22.0	9.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	107.0	118.7	69.3	°C/W
θ_{JCbott}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

7.6 Electrical Characteristics

at $T_A = +25^\circ\text{C}$, $V_S = +2.2\text{ V}$ to $+36\text{ V}$, $C_L = 15\text{ pF}$, $R_{PULLUP} = 5.1\text{ k}\Omega$, $V_{CM} = V_S / 2$, and $V_S = V_{PULLUP}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V _{OS}	Input offset voltage	T _A = 25°C, V _S = 2.2 V		±0.5	±3.5	mV
		T _A = 25°C, V _S = 36 V		±0.3	±2.5	mV
		T _A = −40°C to +125°C			±5.5	mV
dV _{OS} /dT	Input offset voltage drift	T _A = −40°C to +125°C		±4	±20	μV/°C
PSRR	Power-supply rejection ratio			15	100	μV/V
		T _A = −40°C to +125°C		20		μV/V
INPUT VOLTAGE RANGE						
V _{CM}	Common-mode voltage range	T _A = −40°C to +125°C		(V−)	(V+)	V
INPUT BIAS CURRENT						
I _B	Input bias current			5	15	nA
		T _A = −40°C to +125°C			20	nA
I _{OS}	Input offset current			0.5		nA
C _{LOAD}	Capacitive load drive		See Typical Characteristics			
OUTPUT						
V _O	Voltage output swing from rail	I _O ≤ 4 mA, input overdrive = 100 mV, V _S = 36 V			900	mV
		I _O = 0 mA, input overdrive = 100 mV, V _S = 36 V			600	mV
I _{SC}	Short circuit sink current			20		mA
	Output leakage current	V _{IN+} > V _{IN−}		70		nA
POWER SUPPLY						
V _S	Specified voltage range		2.2		36	V
I _Q	Quiescent current (per channel)	I _O = 0 A		55	75	μA
		I _O = 0 A, T _A = −40°C to +125°C			100	μA

7.7 Switching Characteristics

at $T_A = +25^\circ\text{C}$, $V_S = +2.2\text{ V}$ to $+36\text{ V}$, $C_L = 15\text{ pF}$, $R_{PULLUP} = 5.1\text{ k}\Omega$, $V_{CM} = V_S / 2$, and $V_S = V_{PULLUP}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pHL}	Propagation delay time, high-to-low	Input overdrive = 100 mV		460	ns
t_{pLH}	Propagation delay time, low-to-high	Input overdrive = 100 mV		560	ns
t_R	Rise time	Input overdrive = 100 mV		365	ns
t_F	Fall time	Input overdrive = 100 mV		240	ns

7.8 Typical Characteristics

at $T_A = +25^\circ\text{C}$, $V_S = +5\text{ V}$, $R_{\text{PULLUP}} = 5.1\text{ k}\Omega$, and input overdrive = 100 mV (unless otherwise noted)

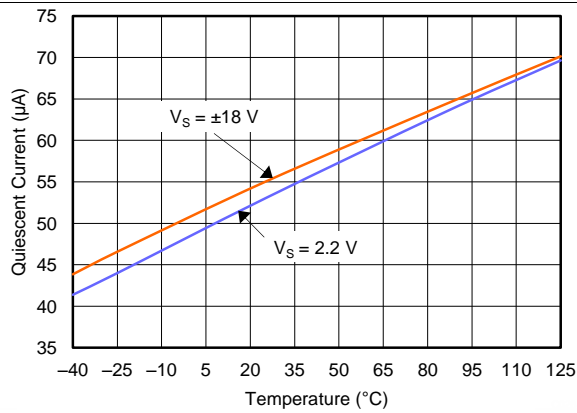


Figure 1. Quiescent Current vs Temperature

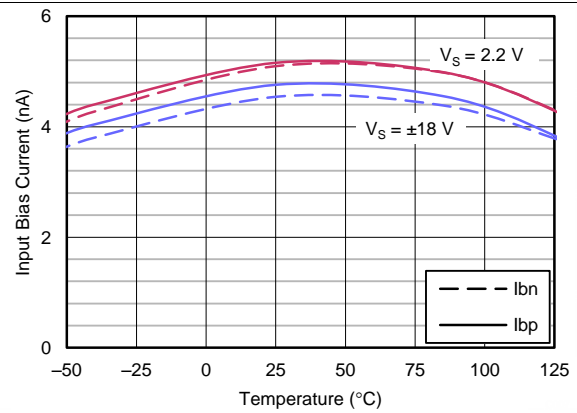


Figure 2. Input Bias Current vs Temperature

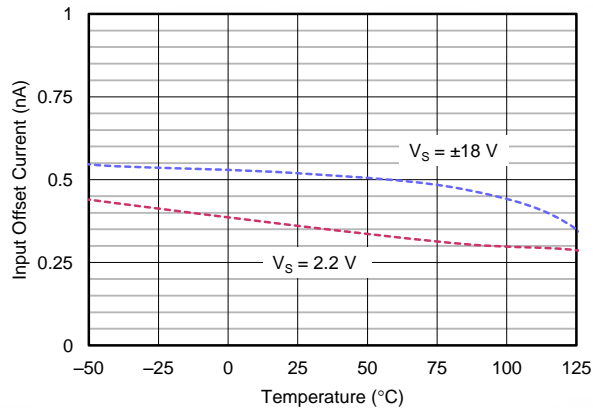


Figure 3. Input Offset Current vs Temperature

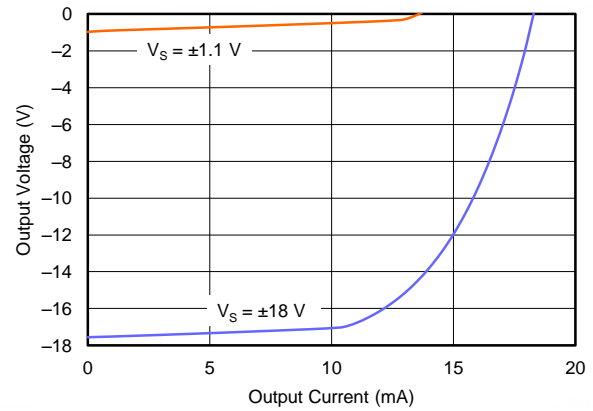


Figure 4. Output Voltage vs Output Current

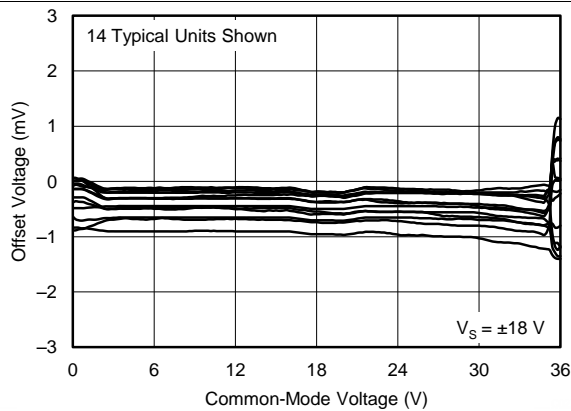


Figure 5. Offset Voltage vs Common-Mode Voltage

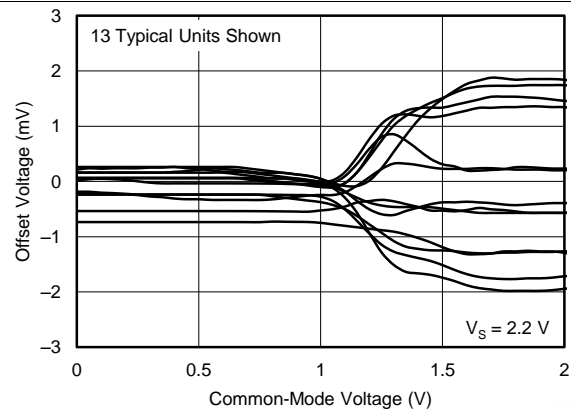


Figure 6. Offset Voltage vs Common-Mode Voltage

Typical Characteristics (continued)

at $T_A = +25^\circ\text{C}$, $V_S = +5\text{ V}$, $R_{\text{PULLUP}} = 5.1\text{ k}\Omega$, and input overdrive = 100 mV (unless otherwise noted)

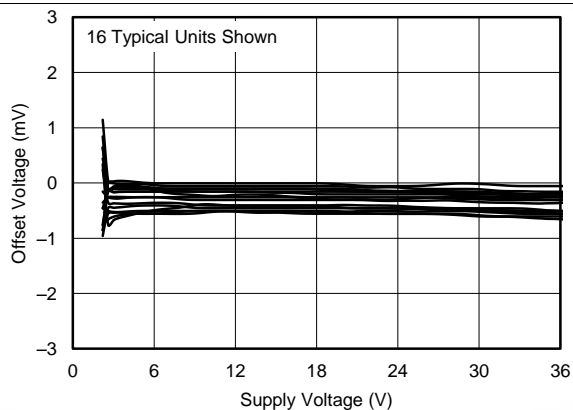


Figure 7. Offset Voltage vs Supply Voltage

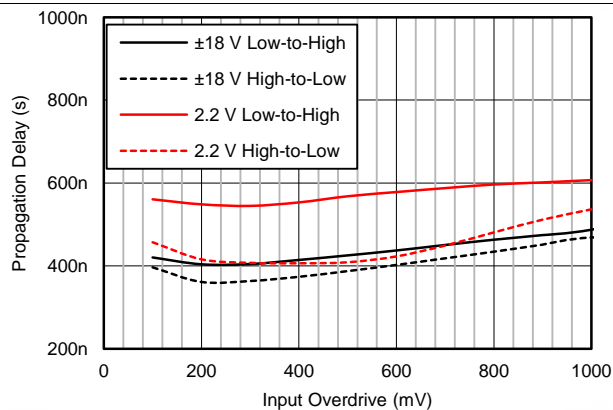


Figure 8. Propagation Delay vs Input Overdrive

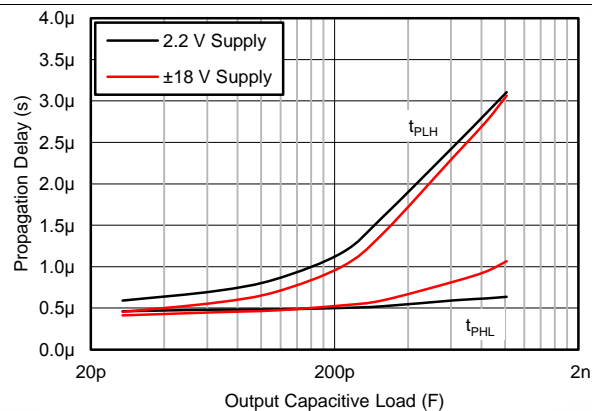


Figure 9. Propagation Delay vs Capacitive Load

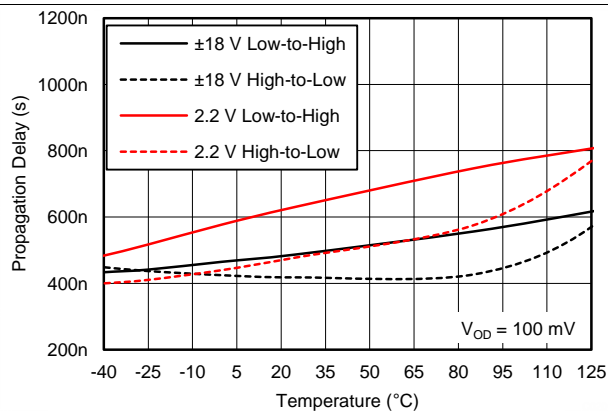


Figure 10. Propagation Delay vs Temperature

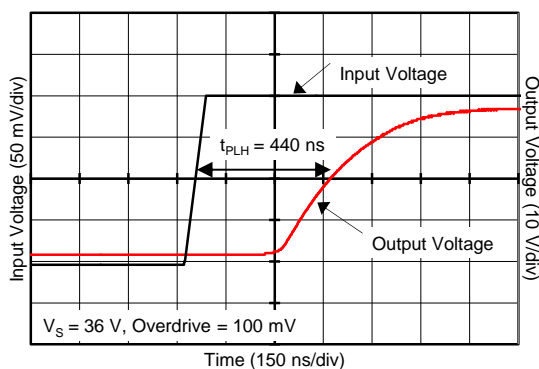


Figure 11. Propagation Delay (T_{pLH})

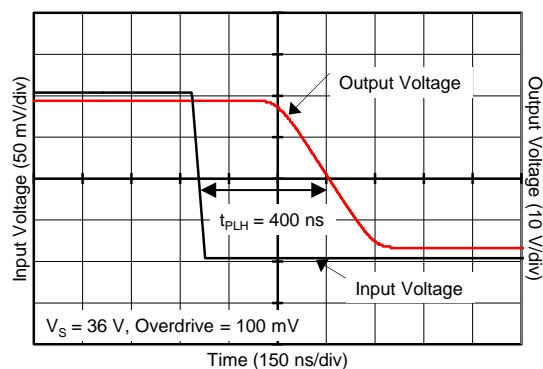


Figure 12. Propagation Delay (T_{pHL})

Typical Characteristics (continued)

at $T_A = +25^\circ\text{C}$, $V_S = +5\text{ V}$, $R_{\text{PULLUP}} = 5.1\text{ k}\Omega$, and input overdrive = 100 mV (unless otherwise noted)

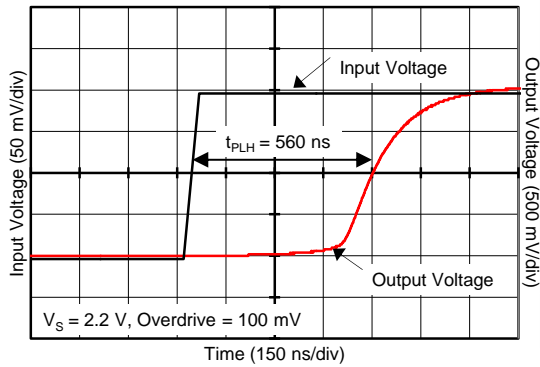


Figure 13. Propagation Delay (T_{pLH})

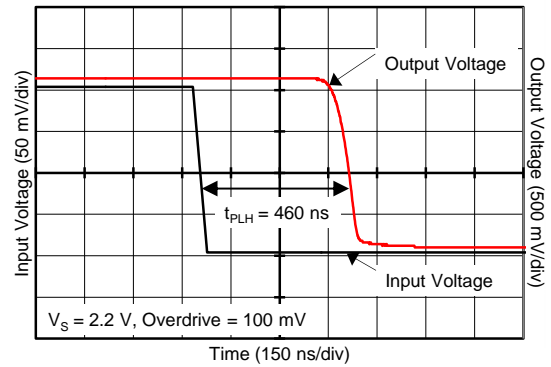


Figure 14. Propagation Delay (T_{pHL})

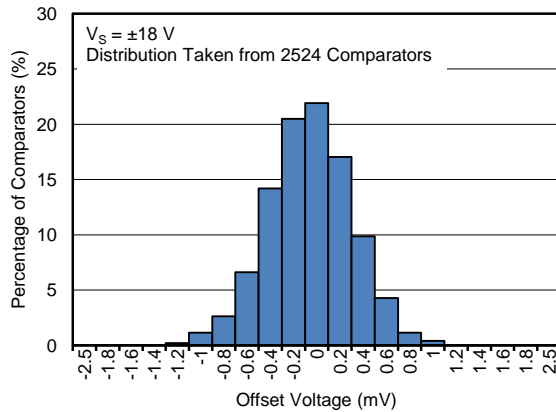


Figure 15. Offset Voltage Production Distribution

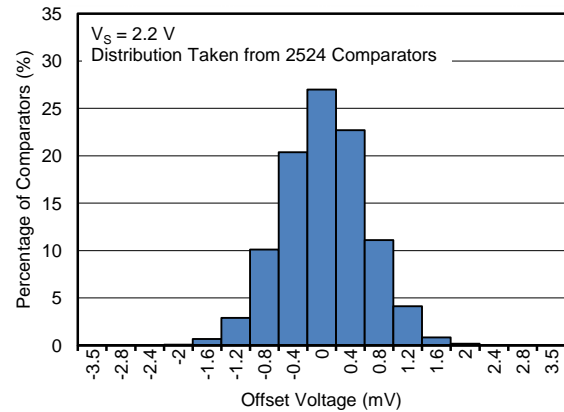


Figure 16. Offset Voltage Production Distribution

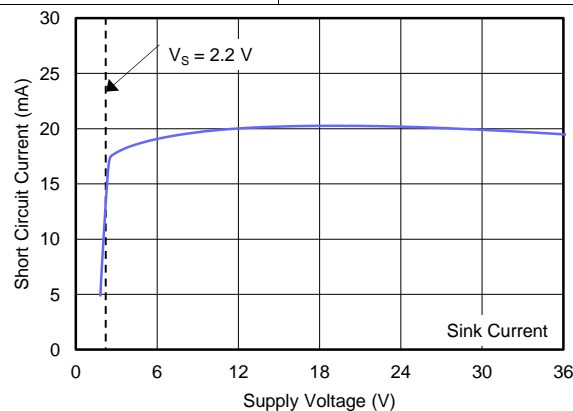


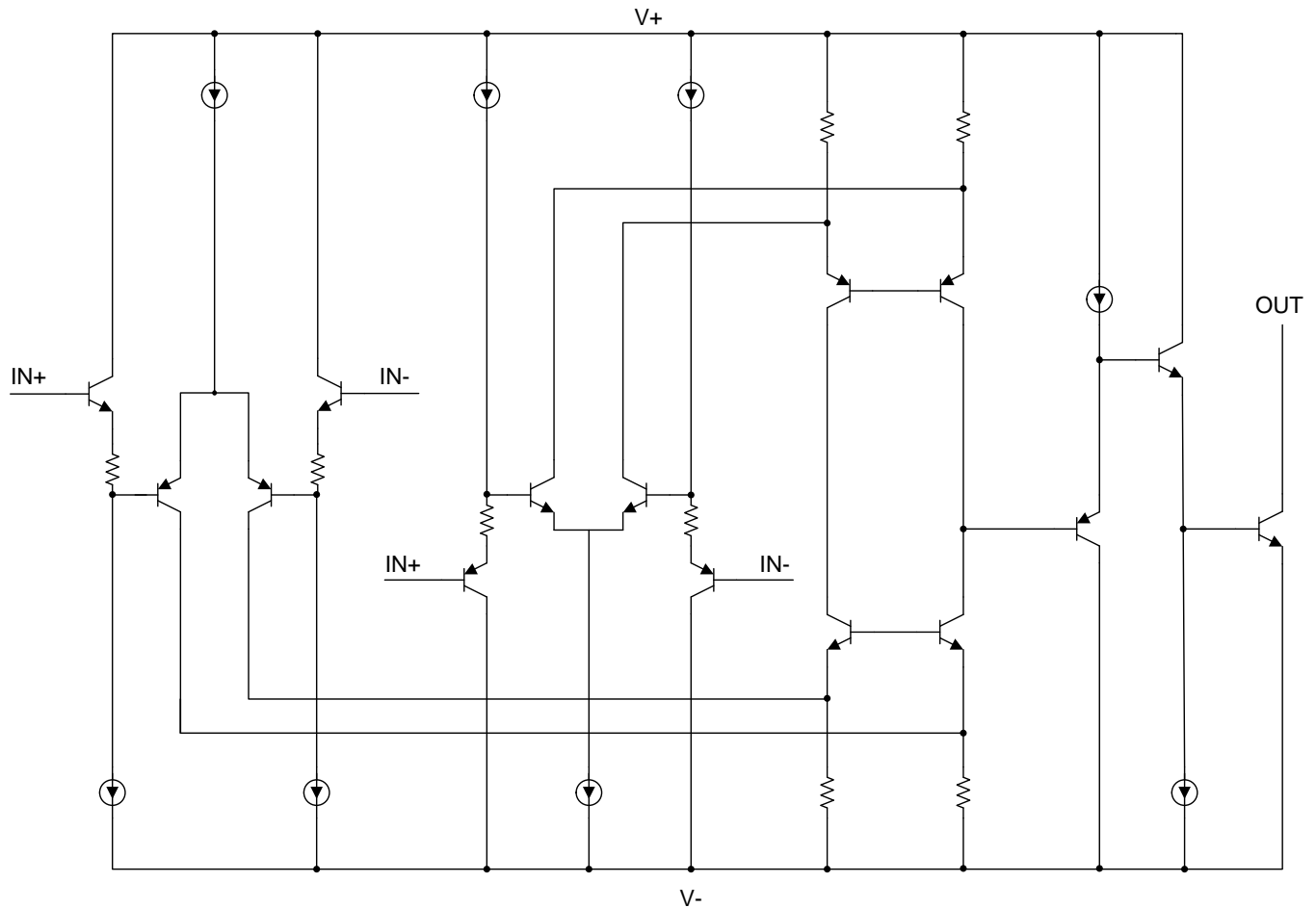
Figure 17. Short-Circuit Current vs Supply Voltage

8 Detailed Description

8.1 Overview

The TLV170x comparators features rail-to-rail input and output on supply voltages as high as 36 V. The rail-to-rail input stage enables detection of signals close to the supply and ground. The open collector configuration allows the device to be used in wired-OR configurations, such as a window comparator. A low supply current of 55 μ A per channel with small, space-saving packages, makes these comparators versatile for use in a wide range of applications, from portable to industrial.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Comparator Inputs

The TLV170x are rail-to-rail input comparators, with an input common-mode range that includes the supply rails. The TLV170x is designed to prevent phase inversion when the input pins exceed the supply voltage. Figure 18 shows the TLV170x response when input voltages exceed the supply, resulting in no phase inversion.

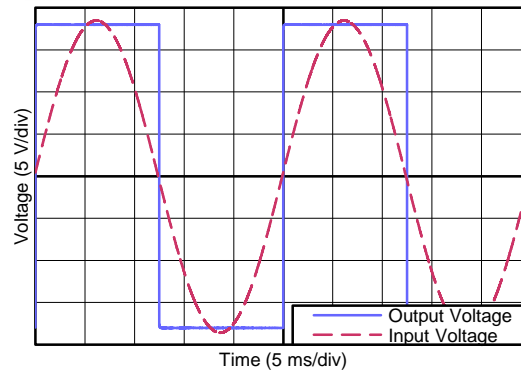


Figure 18. No Phase Inversion: Comparator Response to Input Voltage (Propagation Delay Included)

8.4 Device Functional Modes

8.4.1 Setting Reference Voltage

Using a stable reference is important when setting the transition point for the TLV170x. The REF3333, as shown in Figure 19, provides a 3.3-V reference voltage with low drift and only 3.9 μ A of quiescent current.

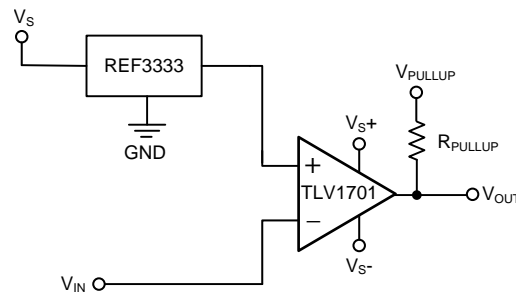


Figure 19. Reference Voltage for the TLV170x

9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TLV170x can be used in a wide variety of applications, such as zero crossing detectors, window comparators, over and undervoltage detectors, and high-side voltage sense circuits.

9.2 Typical Application

Comparators are used to differentiate between two different signal levels. For example, a comparator differentiates between an overtemperature and normal-temperature condition. However, noise or signal variation at the comparison threshold causes multiple transitions. This application example sets upper and lower hysteresis thresholds to eliminate the multiple transitions caused by noise.

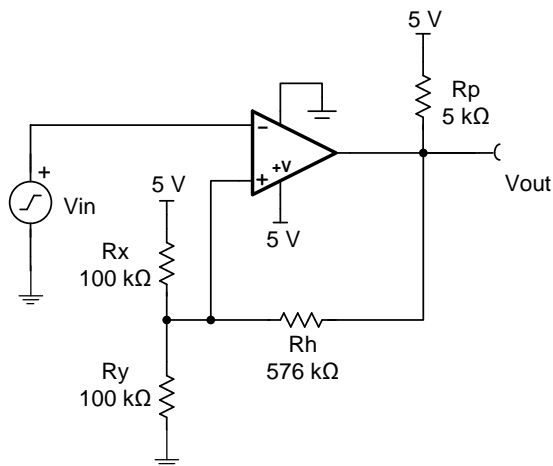


Figure 20. Comparator Schematic with Hysteresis

9.2.1 Design Requirements

The design requirements are as follows:

- Supply voltage: 5 V
- Input: 0 V to 5 V
- Lower threshold (VL) = 2.3 V \pm 0.1 V
- Upper threshold (VH) = 2.7 V \pm 0.1 V
- VH – VL = 2.4 V \pm 0.1 V
- Low power consumption

Typical Application (continued)

9.2.2 Detailed Design Procedure

Make a small change to the comparator circuit to add hysteresis. Hysteresis uses two different threshold voltages to avoid the multiple transitions introduced in the previous circuit. The input signal must exceed the upper threshold (VH) to transition low, or below the lower threshold (VL) to transition high.

Figure 20 illustrates hysteresis on a comparator. Resistor Rh sets the hysteresis level. An open-collector output stage requires a pullup resistor (Rp). The pullup resistor creates a voltage divider at the comparator output that introduces an error when the output is at logic high. This error can be minimized if $R_h > 100R_p$.

When the output is at a logic high (5 V), Rh is in parallel with Rx (ignoring Rp). This configuration drives more current into Ry, and raises the threshold voltage (VH) to 2.7 V. The input signal must drive above $V_H = 2.7$ V to cause the output to transition to logic low (0 V).

When the output is at logic low (0 V), Rh is in parallel with Ry. This configuration reduces the current into Ry, and reduces the threshold voltage to 2.3 V. The input signal must drive below $V_L = 2.3$ V to cause the output to transition to logic high (5 V).

For more details on this design and other alternative devices that can be used in place of the TLV1702, refer to Precision Design [TIPD144](#), *Comparator with Hysteresis Reference Design*.

9.2.3 Application Curve

Figure 21 shows the upper and lower thresholds for hysteresis. The upper threshold is 2.76 V and the lower threshold is 2.34 V, both of which are close to the design target.

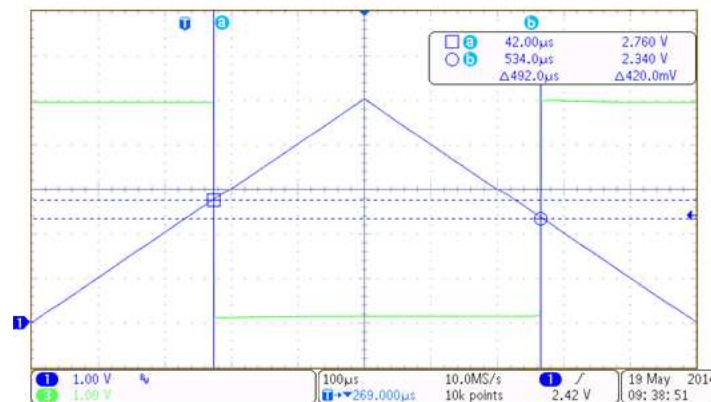


Figure 21. TLV1701 Upper and Lower Threshold with Hysteresis

10 Power Supply Recommendations

The TLV170x is specified for operation from 2.2 V to 36 V (± 1.1 to ± 18 V); many specifications apply from -40°C to $+125^{\circ}\text{C}$. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the [Typical Characteristics](#) section.

CAUTION

Supply voltages larger than 40 V can permanently damage the device; see the [Absolute Maximum Ratings](#).

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement; see the [Layout Guidelines](#) section.

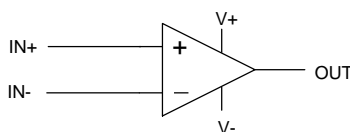
11 Layout

11.1 Layout Guidelines

Comparators are very sensitive to input noise. For best results, maintain the following layout guidelines:

- Use a printed circuit board (PCB) with a good, unbroken low-inductance ground plane. Proper grounding (use of ground plane) helps maintain specified performance of the TLV170x.
- To minimize supply noise, place a decoupling capacitor (0.1- μ F ceramic, surface-mount capacitor) as close as possible to V_S as shown in Figure 22.
- On the inputs and the output, keep lead lengths as short as possible to avoid unwanted parasitic feedback around the comparator. Keep inputs away from the output.
- Solder the device directly to the PCB rather than using a socket.
- For slow-moving input signals, take care to prevent parasitic feedback. A small capacitor (1000 pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes some degradation to propagation delay when the impedance is low. Run the topside ground plane between the output and inputs.
- Run the ground pin ground trace under the device up to the bypass capacitor, shielding the inputs from the outputs.

11.2 Layout Example



(Schematic Representation)

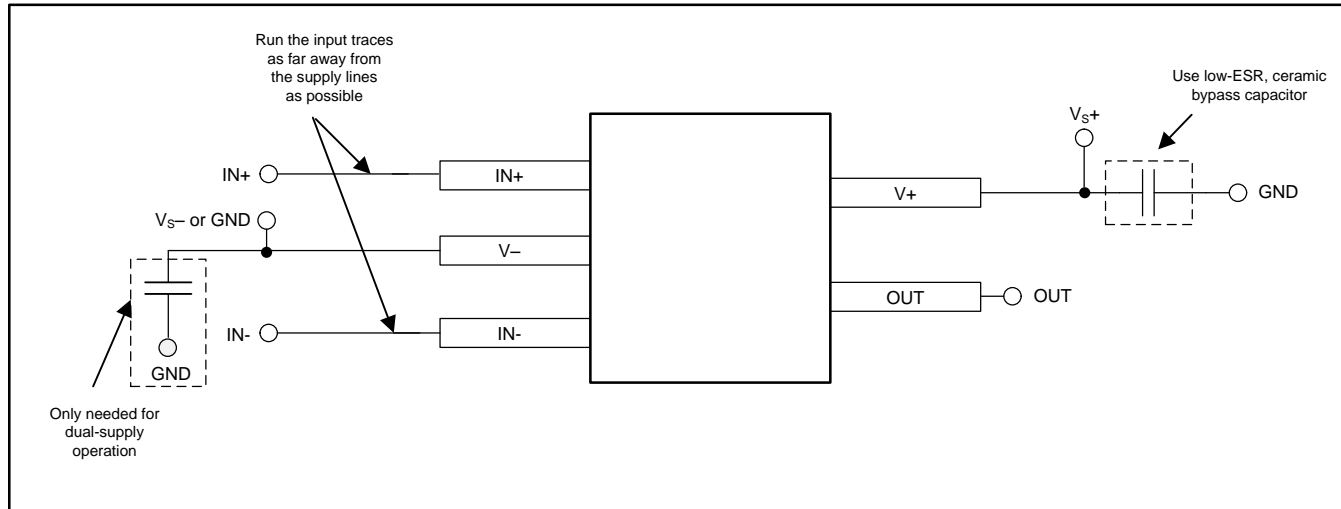


Figure 22. Comparator Board Layout

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

[TIDU020](#) — *Precision Design, Comparator with Hysteresis Reference Design.*

[SBOS392](#) — REF3333 Data Sheet

12.2 Related Links

[Table 1](#) lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TLV1701	Click here	Click here	Click here	Click here	Click here
TLV1702	Click here	Click here	Click here	Click here	Click here
TLV1704	Click here	Click here	Click here	Click here	Click here

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

[SLYZ022](#) — *TI Glossary.*

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV1701AIDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZAYF	Samples
TLV1701AIDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZAYF	Samples
TLV1701AIDCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SIR	Samples
TLV1701AIDCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SIR	Samples
TLV1701AIDRLR	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIS	Samples
TLV1701AIDRLT	ACTIVE	SOT	DRL	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIS	Samples
TLV1702AIDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1702	Samples
TLV1702AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1702	Samples
TLV1702AIRUGR	PREVIEW	X2QFN	RUG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	FC	
TLV1704AIPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL1704	Samples
TLV1704AIPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL1704	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV1701AIDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV1701AIDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV1701AIDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV1701AIDCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV1701AIDRLR	SOT	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
TLV1701AIDRLT	SOT	DRL	5	250	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
TLV1702AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV1704AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

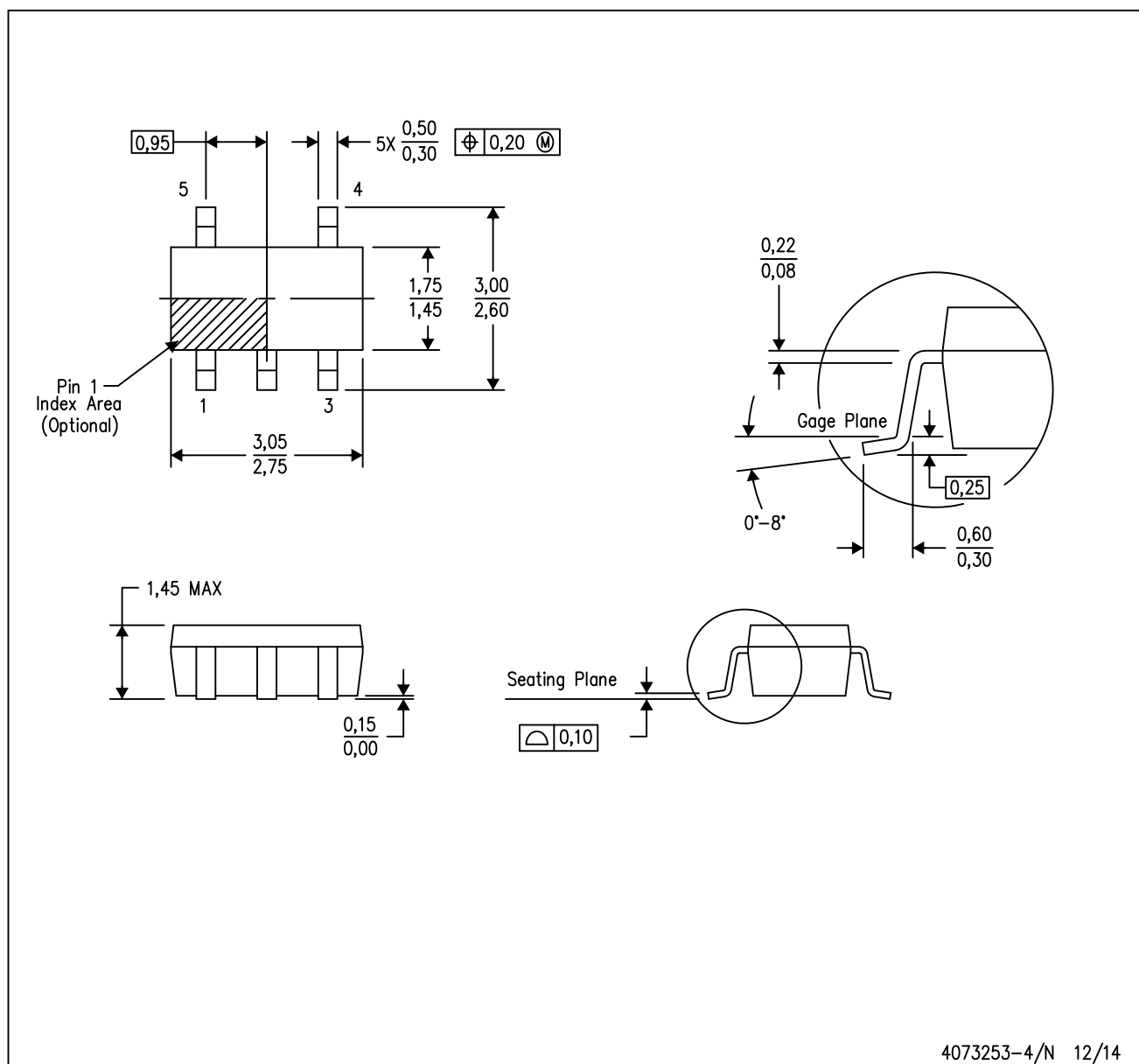


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV1701AIDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV1701AIDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV1701AIDCKR	SC70	DCK	5	3000	190.0	190.0	30.0
TLV1701AIDCKT	SC70	DCK	5	250	190.0	190.0	30.0
TLV1701AIDRLR	SOT	DRL	5	4000	202.0	201.0	28.0
TLV1701AIDRLT	SOT	DRL	5	250	202.0	201.0	28.0
TLV1702AIDGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
TLV1704AIPWR	TSSOP	PW	14	2000	367.0	367.0	35.0

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



4093553-3/G 01/2007

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

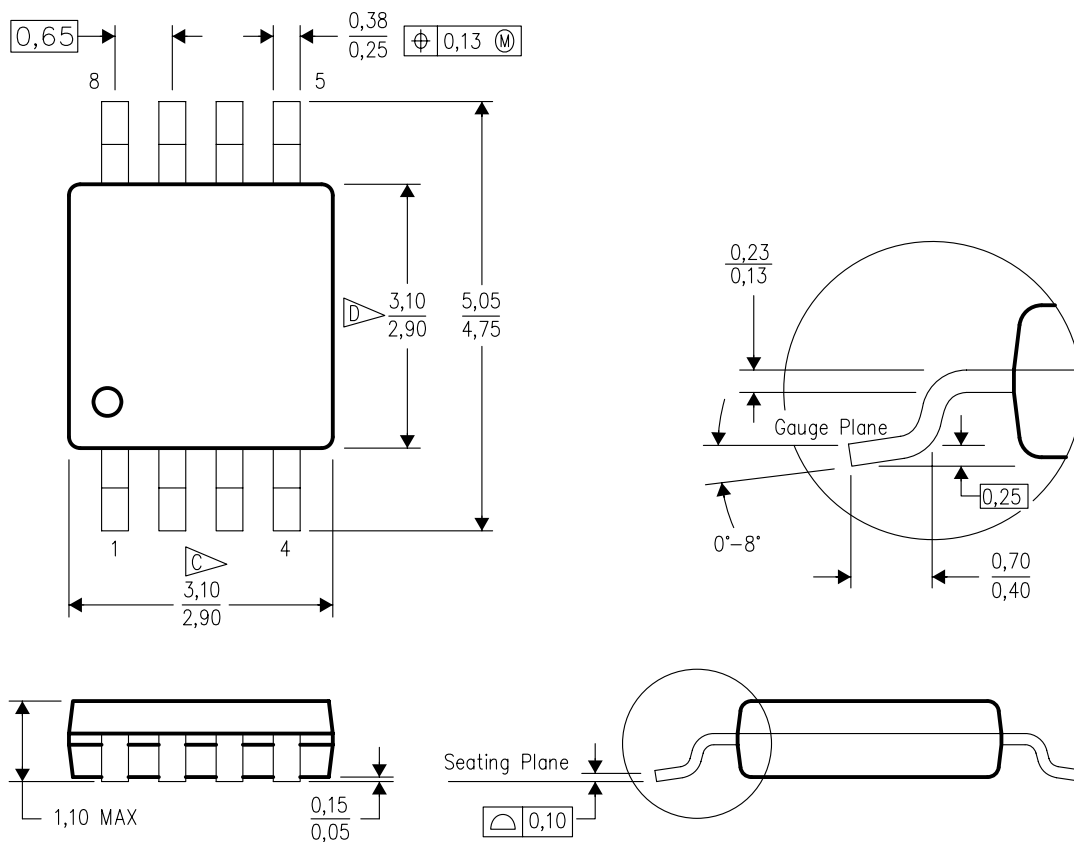
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



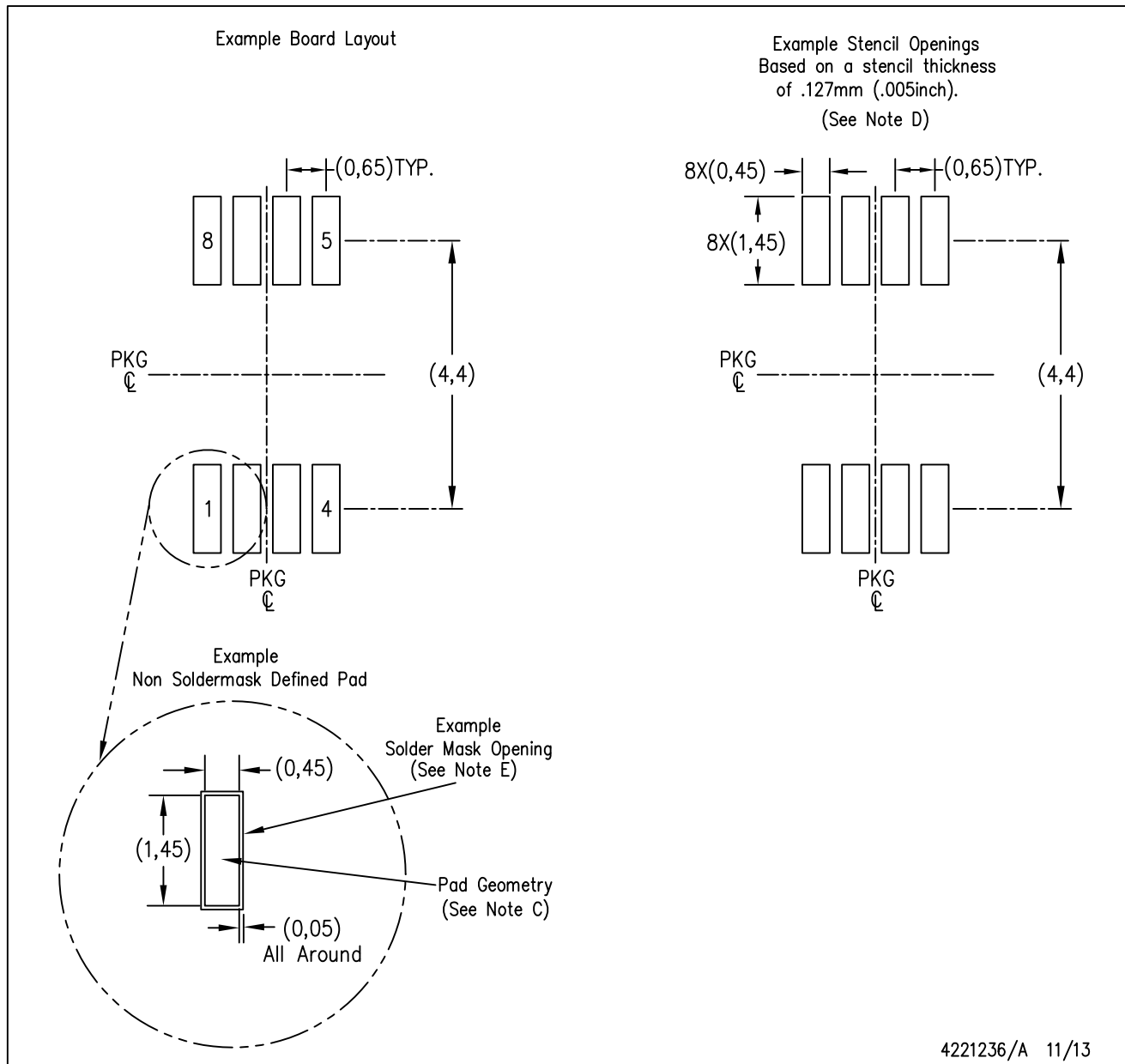
4073329/E 05/06

NOTES:

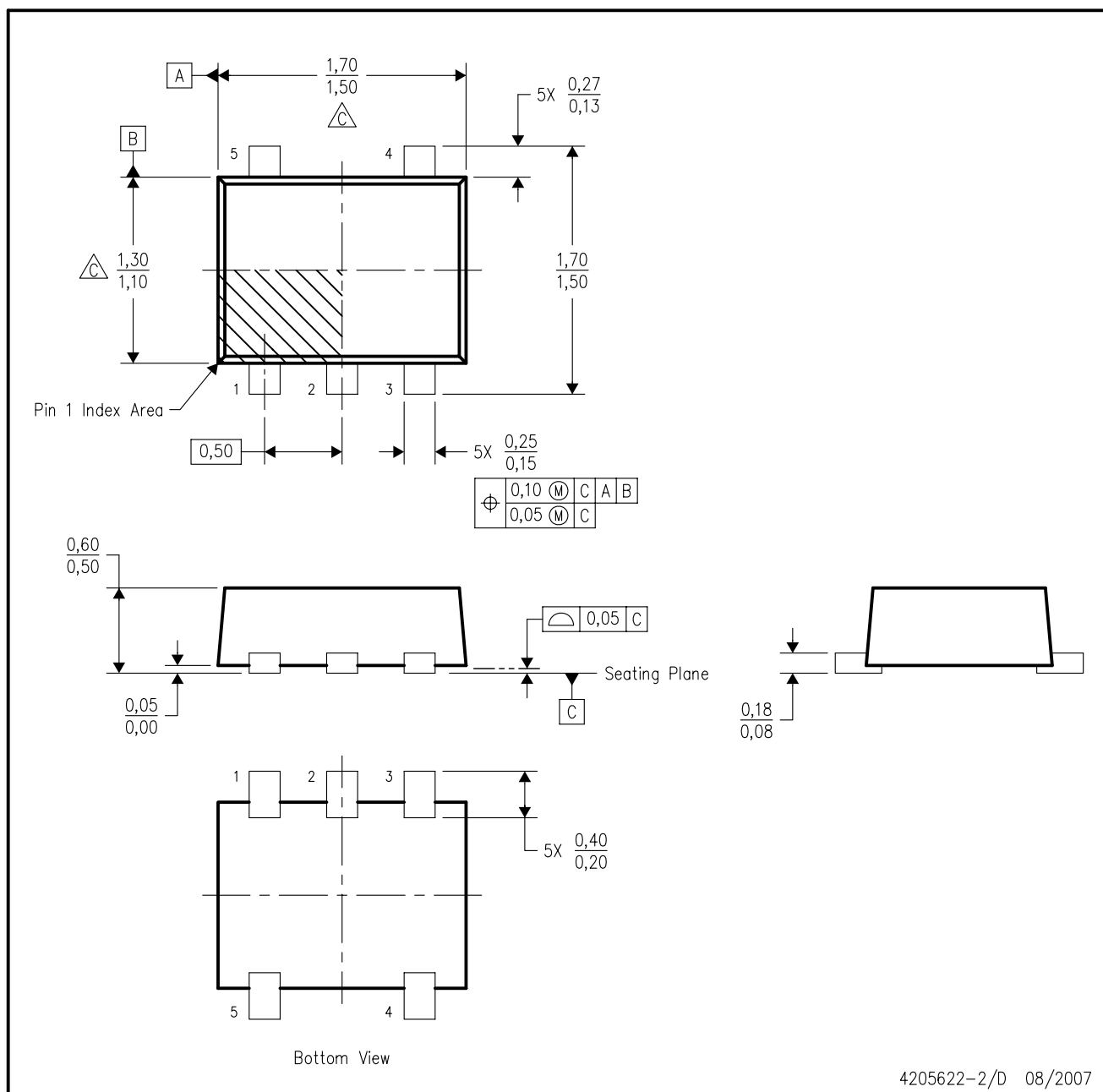
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- ☒ C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- ☐ D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGK (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



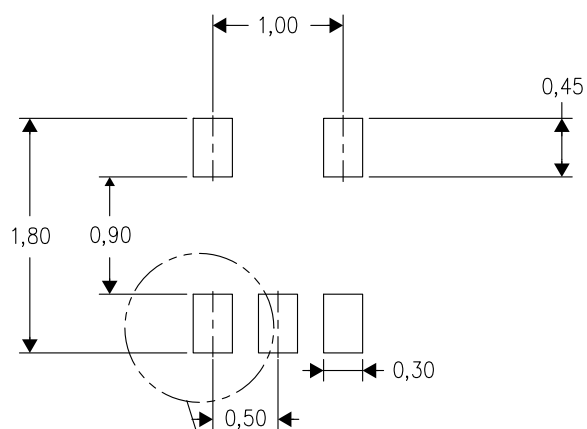
4205622-2/D 08/2007

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
 - D. JEDEC package registration is pending.

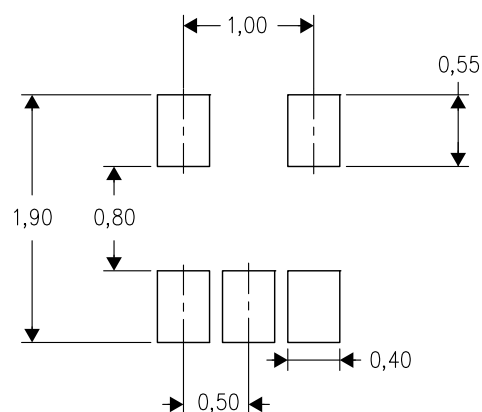
DRL (R-PDSO-N5)

PLASTIC SMALL OUTLINE

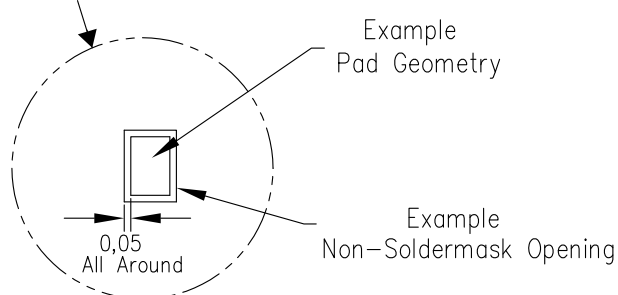
Example Board Layout



Example Stencil Design
(Note E)



Example
Non-Soldermask Defined Pad



Example
Pad Geometry

Example
Non-Soldermask Opening

4208207-2/E 06/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

PW (R-PDSO-G14)

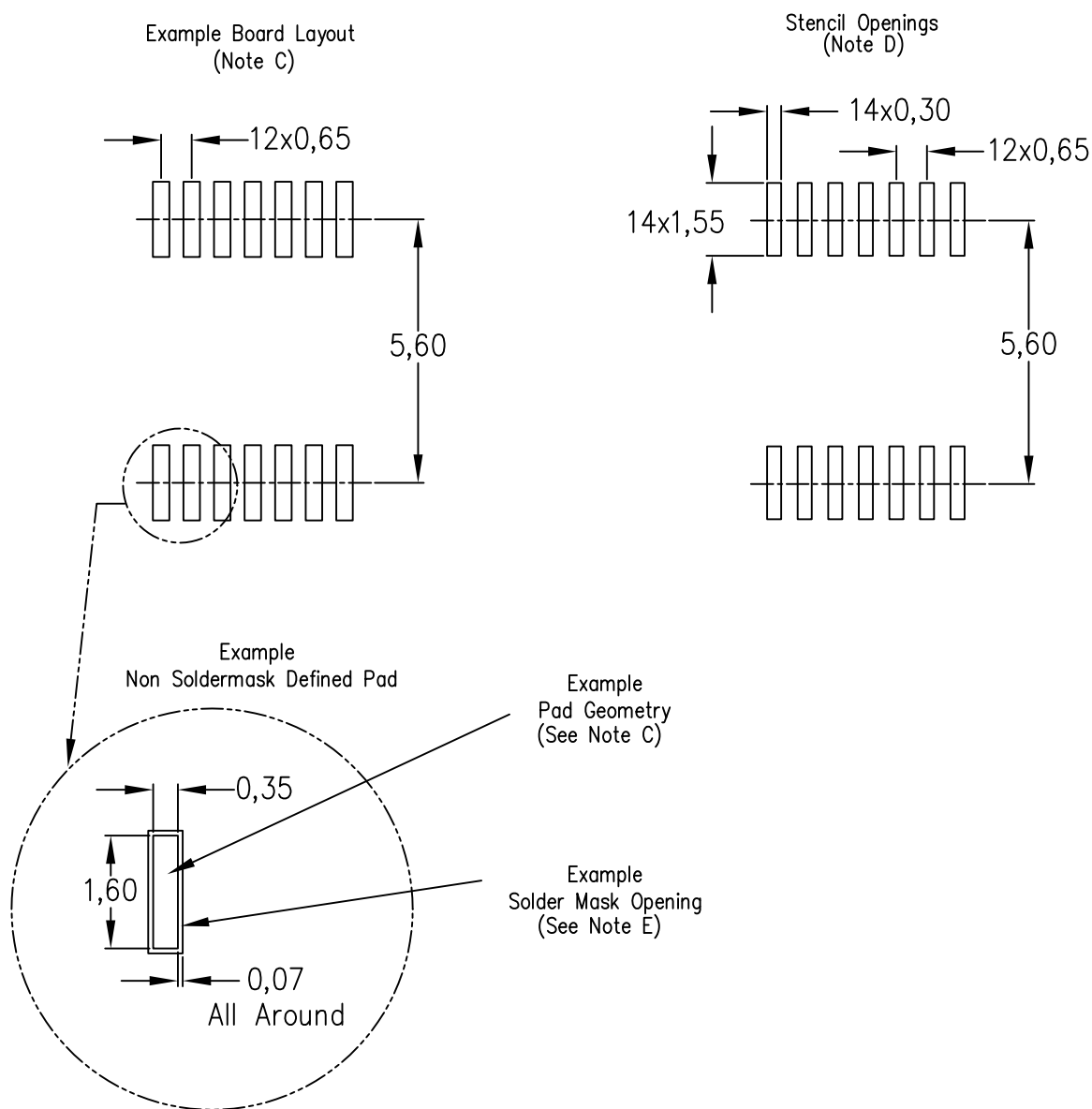
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

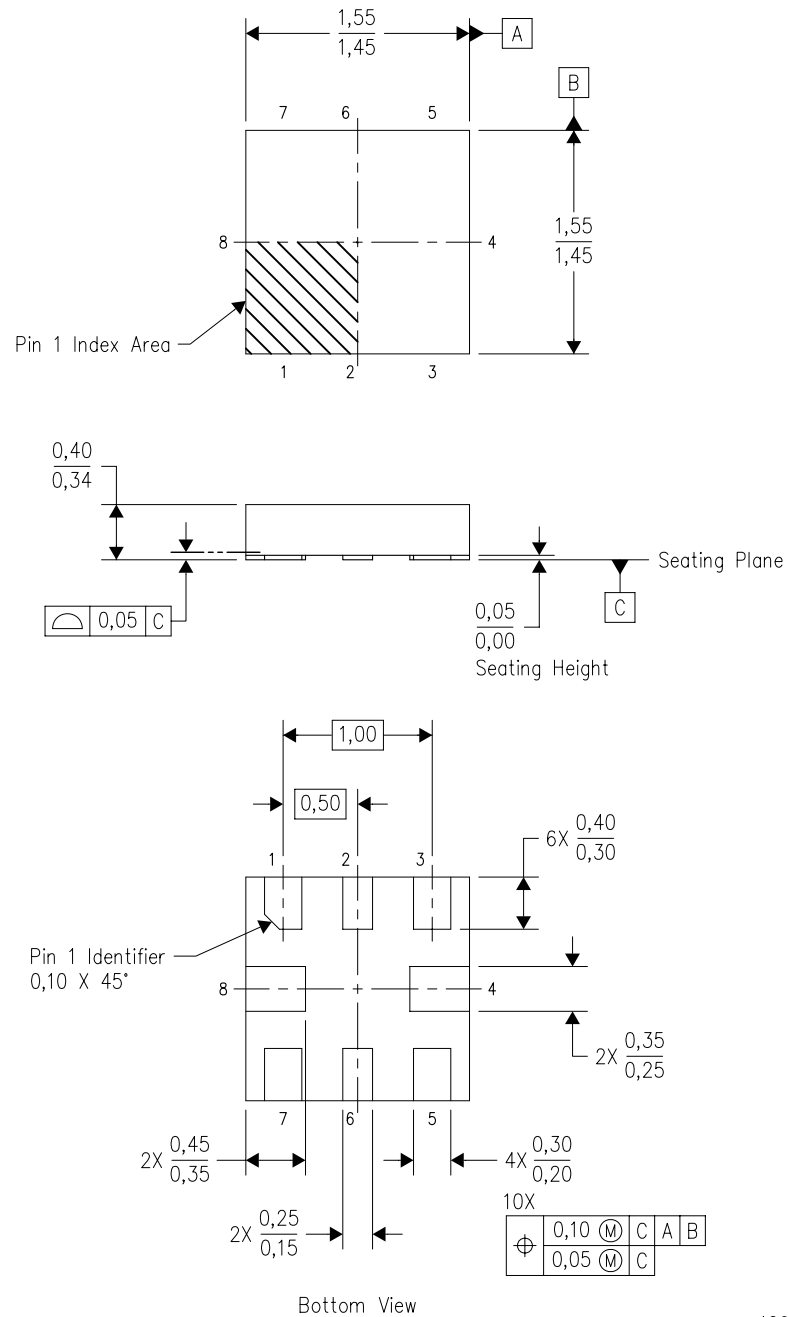


4211284-2/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RUG (S-PQFP-N8)

PLASTIC QUAD FLATPACK

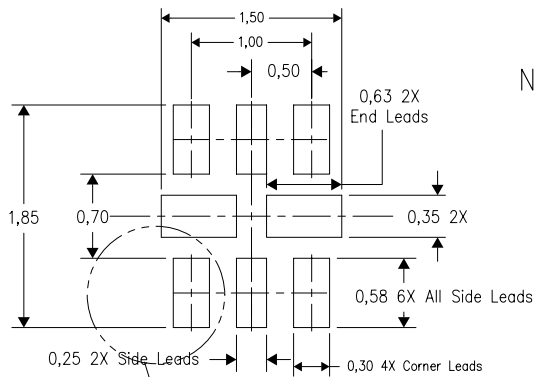


4208528-2/B 04/2008

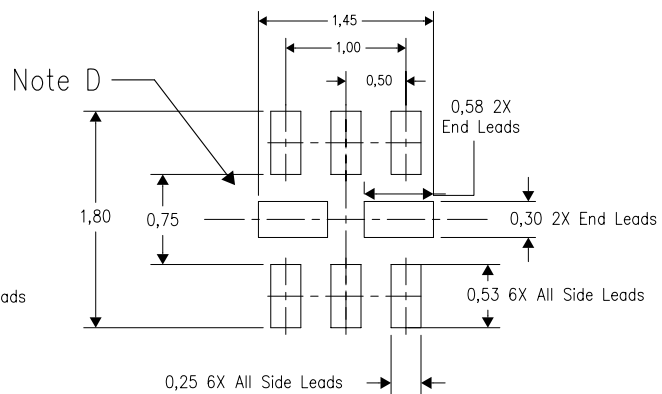
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - D. This package complies to JEDEC MO-288 variation X2ECD.

RUG (R-PQFP-N8)

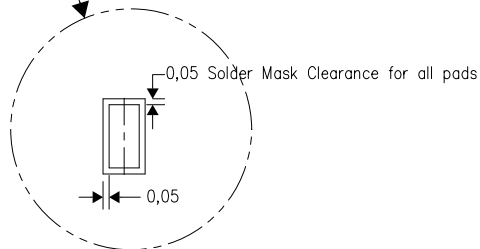
Example Board Layout



Example Stencil Design
(Note E)



Note D



4210299-2/A 06/09

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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