



## LMx58, LMx58x, LM2904, LM2904V Dual Operational Amplifiers

### 1 Features

- Wide Supply Ranges
  - Single Supply: 3 V to 32 V (26 V for LM2904)
  - Dual Supplies:  $\pm 1.5$  V to  $\pm 16$  V ( $\pm 13$  V for LM2904)
- Low Supply-Current Drain, Independent of Supply Voltage: 0.7 mA Typical
- Wide Unity Gain Bandwidth: 0.7 MHz
- Common-Mode Input Voltage Range Includes Ground, Allowing Direct Sensing Near Ground
- Low Input Bias and Offset Parameters
  - Input Offset Voltage: 3 mV Typical  
A Versions: 2 mV Typical
  - Input Offset Current: 2 nA Typical
  - Input Bias Current: 20 nA Typical  
A Versions: 15 nA Typical
- Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage: 32 V (26 V for LM2904)
- Open-Loop Differential Voltage Gain: 100 dB Typical
- Internal Frequency Compensation
- On Products Compliant to MIL-PRF-38535, All Parameters are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

### 2 Applications

- Blu-ray Players and Home Theaters
- Chemical and Gas Sensors
- DVD Recorder and Players
- Digital Multimeter: Bench and Systems
- Digital Multimeter: Handhelds
- Field Transmitter: Temperature Sensors
- Motor Control: AC Induction, Brushed DC, Brushless DC, High-Voltage, Low-Voltage, Permanent Magnet, and Stepper Motor
- Oscilloscopes
- TV: LCD and Digital
- Temperature Sensors or Controllers Using Modbus
- Weigh Scales

### 3 Description

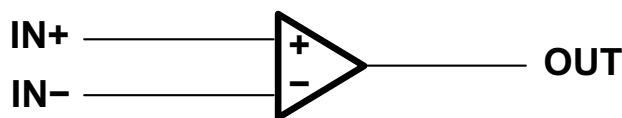
These devices consist of two independent, high-gain frequency-compensated operational amplifiers designed to operate from a single supply or split supply over a wide range of voltages.

Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMx58, LMx58x, LM2904, LM2904V	VSSOP (8)	3.00 mm × 3.00 mm
	SOIC (8)	4.90 mm × 3.90 mm
	SO (8)	5.20 mm × 5.30 mm
	TSSOP (8)	3.00 mm × 4.40 mm
	PDIP (8)	9.81 mm × 6.35 mm
LMx58, LMx58x, LM2904V	CDIP (8)	9.60 mm × 6.67 mm
	LCCC (20)	8.89 mm × 8.89 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Symbol (Each Amplifier)



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## 4 Revision History

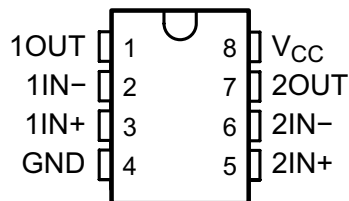
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision S (January 2014) to Revision T	Page
<ul style="list-style-type: none"> <li>Added <i>Applications</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....</li> </ul>	<b>1</b>

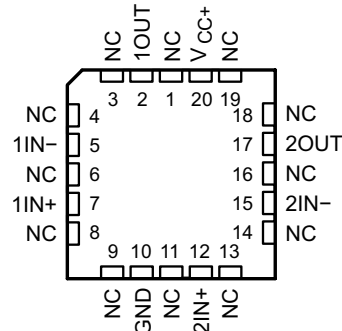
Changes from Revision R (July 2010) to Revision S	Page
<ul style="list-style-type: none"> <li>Converted this data sheet from the QS format to DocZone using the PDF on the web .....</li> <li>Deleted <i>Ordering Information</i> table .....</li> <li>Updated <i>Features</i> to include Military Disclaimer .....</li> <li>Added Typical Characteristics section .....</li> <li>Added ESD warning .....</li> </ul>	<b>1</b> <b>1</b> <b>1</b> <b>9</b> <b>17</b>

## 5 Pin Configuration and Functions

**D, DGK, P, PS, PW and JG Package  
8-Pin SOIC, VSSOP, PDIP, SO, TSSOP and CDIP  
(Top View)**



**FK Package  
20-Pin LCCC  
(Top View)**



NC - No internal connection

### Pin Functions

PIN			I/O	DESCRIPTION
NAME	LCCC NO.	SOIC, SSOP, CDIP, PDIP SO, TSSOP, CFP NO.		
1IN-	5	2	I	Negative input
1IN+	7	3	I	Positive input
1OUT	2	1	O	Output
2IN-	15	6	I	Negative input
2IN+	12	5	I	Positive input
2OUT	17	7	O	Output
GND	10	4	—	Ground
NC	1	—	—	Do not connect
	3			
	4			
	6			
	8			
	9			
	11			
	13			
	14			
	16			
	18			
	19			
V <sub>CC</sub>	—	8	—	Power supply
V <sub>CC+</sub>	20	—	—	Power supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			LMx58, LMx58x, LM2904V		LM2904		UNIT
			MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage <sup>(2)</sup>		–0.3	±16 or 32	–0.3	±13 or 26	V
V <sub>ID</sub>	Differential input voltage <sup>(3)</sup>		–32	32	–26	26	V
V <sub>I</sub>	either input Input voltage		–0.3	32	–0.3	26	V
	Duration of output short circuit (one amplifier) to ground at (or below) T <sub>A</sub> = 25°C, V <sub>CC</sub> ≤ 15 V <sup>(4)</sup>		Unlimited		Unlimited		s
T <sub>A</sub>	Operating free air temperature	LM158, LM158A	–55	125			°C
		LM258, LM258A	–25	85			
		LM358, LM358A	0	70			
		LM2904	–40	125	–40	125	
T <sub>J</sub>	Operating virtual junction temperature			150		150	°C
	Case temperature for 60 seconds	FK package		260			°C
	Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds	JG package		300		300	°C
T <sub>stg</sub>	Storage temperature		–65	150	–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values (except differential voltages and V<sub>CC</sub> specified for the measurement of I<sub>OS</sub>) are with respect to the network GND.
- (3) Differential voltages are at IN+, with respect to IN–.
- (4) Short circuits from outputs to V<sub>CC</sub> can cause excessive heating and eventual destruction.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			LMx58, LMx58x, LM2904V		LM2904		UNIT
			MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage		3	30	3	26	V
V <sub>CM</sub>	Common-mode voltage		0	V <sub>CC</sub> – 2	0	V <sub>CC</sub> – 2	V
T <sub>A</sub>	Operating free air temperature	LM158	–55	125			°C
		LM2904	–40	125	–40	125	
		LM358	0	70			
		LM258	–25	85			

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		LMx58, LMx58x, LM2904V, LM2904					LMx58, LMx58x, LM2904 V	LMx58, LMx58x, LM2904 V	UNIT
		D (SOIC)	DGK (VSSOP)	P (PDIP)	PS (SO)	PW (TSSOP)	FK (LCCC)	JG (CDIP)	
		8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	20 PINS	8 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	97	172	85	95	149	—	—	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	72.2	—	—	—	—	5.61	14.5	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics for LMx58

at specified free-air temperature, V<sub>CC</sub> = 5 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>(1)</sup>		T <sub>A</sub> <sup>(2)</sup>	LM158 LM258			LM358			UNIT
				MIN	TYP <sup>(3)</sup>	MAX	MIN	TYP <sup>(3)</sup>	MAX	
V <sub>IO</sub>	Input offset voltage	V <sub>CC</sub> = 5 V to MAX, V <sub>IC</sub> = V <sub>ICR(min)</sub> , V <sub>O</sub> = 1.4 V	25°C	3	5		3	7		mV
			Full range		7			9		
αV <sub>IO</sub>	Average temperature coefficient of input offset voltage		Full range	7			7			μV/°C
I <sub>IO</sub>	Input offset current	V <sub>O</sub> = 1.4 V	25°C	2	30		2	50		nA
			Full range		100			150		
αI <sub>IO</sub>	Average temperature coefficient of input offset current		Full range	10			10			pA/°C
I <sub>IB</sub>	Input bias current	V <sub>O</sub> = 1.4 V	25°C	–20	–150		–20	–250		nA
			Full range		–300			–500		
V <sub>ICR</sub>	Common-mode input voltage range	V <sub>CC</sub> = 5 V to MAX	25°C	0 to V <sub>CC</sub> – 1.5			0 to V <sub>CC</sub> – 1.5			V
			Full range	0 to V <sub>CC</sub> – 2			0 to V <sub>CC</sub> – 2			
V <sub>OH</sub>	High-level output voltage	R <sub>L</sub> ≥ 2 kΩ	25°C	V <sub>CC</sub> – 1.5			V <sub>CC</sub> – 1.5			V
		R <sub>L</sub> ≥ 10 kΩ	25°C							
		V <sub>CC</sub> = MAX	Full range	26			26			
			Full range	27	28		27	28		
V <sub>OL</sub>	Low-level output voltage	R <sub>L</sub> ≤ 10 kΩ	Full range	5	20		5	20		mV
A <sub>VD</sub>	Large-signal differential voltage amplification	V <sub>CC</sub> = 15 V, V <sub>ID</sub> = 1 V to 11 V, R <sub>L</sub> ≥ 2 kΩ	25°C	50	100		25	100		V/mV
			Full range	25			15			
CMRR	Common-mode rejection ratio	V <sub>CC</sub> = 5 V to MAX, V <sub>IC</sub> = V <sub>ICR(min)</sub>	25°C	70	80		65	80		dB
k <sub>SVR</sub>	Supply-voltage rejection ratio (ΔV <sub>DD</sub> /ΔV <sub>IO</sub> )	V <sub>CC</sub> = 5 V to MAX	25°C	65	100		65	100		dB
V <sub>O1</sub> /V <sub>O2</sub>	Crosstalk attenuation	f = 1 kHz to 20 kHz	25°C	120			120			dB
I <sub>O</sub>	Output current	V <sub>CC</sub> = 15 V, V <sub>ID</sub> = 1 V, V <sub>O</sub> = 0	25°C	–20	–30		–20	–30		mA
			Full range	–10			–10			
		V <sub>CC</sub> = 15 V, V <sub>ID</sub> = –1 V, V <sub>O</sub> = 15 V	25°C	10	20		10	20		
			Full range	5			5			
		V <sub>ID</sub> = –1 V, V <sub>O</sub> = 200 mV	25°C	12	30		12	30		μA
I <sub>OS</sub>	Short-circuit output current	V <sub>CC</sub> at 5 V, GND at –5 V, V <sub>O</sub> = 0	25°C	±40	±60		±40	±60		mA
I <sub>CC</sub>	Supply current (two amplifiers)	V <sub>O</sub> = 2.5 V, No load	Full range	0.7	1.2		0.7	1.2		mA
		V <sub>CC</sub> = MAX, V <sub>O</sub> = 0.5 V <sub>CC</sub> , No load	Full range	1	2		1	2		

(1) All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified. MAX V<sub>CC</sub> for testing purposes is 26 V for LM2902 and 30 V for the others.

(2) Full range is –55°C to 125°C for LM158, –25°C to 85°C for LM258, and 0°C to 70°C for LM358, and –40°C to 125°C for LM2904.

(3) All typical values are at T<sub>A</sub> = 25°C

## 6.6 Electrical Characteristics for LM2904

at specified free-air temperature,  $V_{CC} = 5\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>(1)</sup>		T <sub>A</sub> <sup>(2)</sup>	LM2904		UNIT
					MIN	TYP <sup>(3)</sup>	
V <sub>IO</sub>	Input offset voltage	V <sub>CC</sub> = 5 V to MAX, V <sub>IC</sub> = V <sub>ICR(min)</sub> , V <sub>O</sub> = 1.4 V	Non-A-suffix devices	25°C	3	7	mV
				Full range		10	
		A-suffix devices	25°C	1	2		
			Full range		4		
αV <sub>IO</sub>	Average temperature coefficient of input offset voltage			Full range	7		μV/°C
I <sub>IO</sub>	Input offset current	V <sub>O</sub> = 1.4 V	Non-V device	25°C	2	50	nA
				Full range		300	
		V-suffix device	25°C	2	50		
			Full range		150		
αI <sub>IO</sub>	Average temperature coefficient of input offset current			Full range	10		pA/°C
I <sub>IB</sub>	Input bias current	V <sub>O</sub> = 1.4 V		25°C	–20	–250	nA
				Full range		–500	
V <sub>ICR</sub>	Common-mode input voltage range	V <sub>CC</sub> = 5 V to MAX		25°C	0 to V <sub>CC</sub> – 1.5		V
				Full range	0 to V <sub>CC</sub> – 2		
V <sub>OH</sub>	High-level output voltage	R <sub>L</sub> ≥ 10 kΩ		25°C	V <sub>CC</sub> – 1.5		V
		V <sub>CC</sub> = MAX, Non-V device	R <sub>L</sub> = 2 kΩ	Full range	22		
			R <sub>L</sub> ≥ 10 kΩ	Full range	23      24		
		V <sub>CC</sub> = MAX V-suffix device	R <sub>L</sub> = 2 kΩ	Full range	26		
			R <sub>L</sub> ≥ 10 kΩ	Full range	27      28		
V <sub>OL</sub>	Low-level output voltage	R <sub>L</sub> ≤ 10 kΩ		Full range	5	20	mV
A <sub>VD</sub>	Large-signal differential voltage amplification	V <sub>CC</sub> = 15 V, V <sub>O</sub> = 1 V to 11 V, R <sub>L</sub> ≥ 2 kΩ		25°C	25	100	V/mV
				Full range	15		
CMRR	Common-mode rejection ratio	V <sub>CC</sub> = 5V to MAX, V <sub>IC</sub> = V <sub>ICR(min)</sub>	Non-V device	25°C	50	80	dB
			V-suffix device	25°C	65	80	
k <sub>SVR</sub>	Supply-voltage rejection ratio (ΔV <sub>CC</sub> /ΔV <sub>IO</sub> )	V <sub>CC</sub> = 5 V to MAX		25°C	65	100	dB
V <sub>O1</sub> / V <sub>O2</sub>	Crosstalk attenuation	f = 1 kHz to 20 kHz		25°C	120		dB
I <sub>O</sub>	Output current	V <sub>CC</sub> = 15 V, V <sub>ID</sub> = 1 V, V <sub>O</sub> = 0	Source	25°C	–20	–30	mA
				Full range	–10		
		V <sub>CC</sub> = 15 V, V <sub>ID</sub> = –1 V, V <sub>O</sub> = 15 V	Sink	25°C	10	20	
				Full range	5		
		V <sub>ID</sub> = –1 V, V <sub>O</sub> = 200 mV	Non-V device	25°C	30		μA
V-suffix device	25°C	12      40					
I <sub>OS</sub>	Short-circuit output current	V <sub>CC</sub> at 5 V, V <sub>O</sub> = 0, GND at –5 V		25°C	±40	±60	mA
I <sub>CC</sub>	Supply current (four amplifiers)	V <sub>O</sub> = 2.5 V, No load		Full range	0.7	1.2	mA
		V <sub>CC</sub> = MAX, V <sub>O</sub> = 0.5 V <sub>CC</sub> , No load		Full range	1	2	

- (1) All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified. MAX  $V_{CC}$  for testing purposes is 26 V for LM2902 and 32 V for LM2902V.
- (2) Full range is –55°C to 125°C for LM158, –25°C to 85°C for LM258, 0°C to 70°C for LM358, and –40°C to 125°C for LM2904.
- (3) All typical values are at  $T_A = 25^\circ\text{C}$ .

## 6.7 Electrical Characteristics for LM158A and LM258A

at specified free-air temperature,  $V_{CC} = 5\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>(1)</sup>	$T_A$ <sup>(1)</sup>	LM158A			LM258A			UNIT
			MIN	TYP <sup>(2)</sup>	MAX	MIN	TYP <sup>(2)</sup>	MAX	
$V_{IO}$ Input offset voltage	$V_{CC} = 5\text{ V to } 30\text{ V},$ $V_{IC} = V_{ICR(min)},$ $V_O = 1.4\text{ V}$	25°C			2		2	3	mV
		Full range			4			4	

- (1) All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified. MAX  $V_{CC}$  for testing purposes is 26 V for LM2904 and 30 V for others.
- (2) All typical values are at  $T_A = 25^\circ\text{C}$ .

## Electrical Characteristics for LM158A and LM258A (continued)

at specified free-air temperature,  $V_{CC} = 5\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>(1)</sup>		T <sub>A</sub> <sup>(1)</sup>	LM158A			LM258A			UNIT		
					MIN	TYP <sup>(2)</sup>	MAX	MIN	TYP <sup>(2)</sup>	MAX			
αV <sub>IO</sub>	Average temperature coefficient of input offset voltage			Full range		7	15 <sup>(3)</sup>		7	15	μA/°C		
I <sub>IO</sub>	Input offset current	V <sub>O</sub> = 1.4 V		25°C		2	10		2	15	nA		
				Full range			30			30			
αI <sub>IO</sub>	Average temperature coefficient of input offset current			Full range		10	200		10	200	pA/°C		
I <sub>IB</sub>	Input bias current	V <sub>O</sub> = 1.4 V		25°C		–15	–50		–15	–80	nA		
				Full range			–100			–100			
V <sub>ICR</sub>	Common-mode input voltage range	V <sub>CC</sub> = 30 V		25°C		0 to V <sub>CC</sub> – 1.5			0 to V <sub>CC</sub> – 1.5		V		
				Full range		0 to V <sub>CC</sub> – 2			0 to V <sub>CC</sub> – 2				
V <sub>OH</sub>	High-level output voltage	R <sub>L</sub> ≥ 2 kΩ		25°C		V <sub>CC</sub> – 1.5			V <sub>CC</sub> – 1.5		V		
		V <sub>CC</sub> = 30 V	R <sub>L</sub> = 2kΩ	Full range		26			26				
			R <sub>L</sub> ≥ 10kΩ	Full range		27	28		27	28			
V <sub>OL</sub>	Low-level output voltage	R <sub>L</sub> ≤ 10 kΩ		Full range		5	20		5	20	mV		
A <sub>VD</sub>	Large-signal differential voltage amplification	V <sub>CC</sub> = 15 V, V <sub>O</sub> = 1 V to 11 V, R <sub>L</sub> ≥ 2 kΩ		25°C		50	100		50	100	V/mV		
				Full range		25			25				
CMRR	Common-mode rejection ratio			25°C		70	80		70	80	dB		
k <sub>SVR</sub>	Supply-voltage rejection ratio (ΔV <sub>D</sub> /ΔV <sub>IO</sub> )			25°C		65	100		65	100	dB		
V <sub>O1</sub> / V <sub>O2</sub>	Crosstalk attenuation	f = 1 kHz to 20 kHz		25°C		120			120		dB		
I <sub>O</sub>	Output current	V <sub>CC</sub> = 15 V, V <sub>ID</sub> = 1 V, V <sub>O</sub> = 0	Source	25°C		–20	–30	–60		–20	–30	–60	mA
				Full range		–10			–10				
		V <sub>CC</sub> = 15 V, V <sub>ID</sub> = –1 V, V <sub>O</sub> = 15 V	Sink	25°C		10	20		10	20			
				Full range		5			5				
		V <sub>ID</sub> = –1 V, V <sub>O</sub> = 200 mV		25°C		12	30		12	30	μA		
I <sub>OS</sub>	Short-circuit output current	V <sub>CC</sub> at 5 V, GND at –5 V, V <sub>O</sub> = 0		25°C		±40	±60		±40	±60	mA		
I <sub>CC</sub>	Supply current (four amplifiers)	V <sub>O</sub> = 2.5 V, No load		Full range		0.7	1.2		0.7	1.2	mA		
		V <sub>CC</sub> = MAX V, V <sub>O</sub> = 0.5 V, No load		Full range		1	2		1	2			

(3) On products compliant to MIL-PRF-38535, this parameter is not production tested.

## 6.8 Electrical Characteristics for LM358A

at specified free-air temperature,  $V_{CC} = 5\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>(1)</sup>	$T_A$ <sup>(2)</sup>	LM358A			UNIT
			MIN	TYP <sup>(3)</sup>	MAX	
$V_{IO}$	Input offset voltage	25°C		2	3	mV
		Full range			5	
$\alpha V_{IO}$	Average temperature coefficient of input offset voltage	Full range		7	20	$\mu\text{A}/^\circ\text{C}$
$I_{IO}$	Input offset current	25°C		2	30	nA
		Full range			75	
$\alpha I_{IO}$	Average temperature coefficient of input offset current	Full range		10	300	$\text{pA}/^\circ\text{C}$

- All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified. MAX  $V_{CC}$  for testing purposes is  $26\text{ V}$  for LM2904 and  $30\text{ V}$  for others.
- All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified. MAX  $V_{CC}$  for testing purposes is  $26\text{ V}$  for LM2904 and  $30\text{ V}$  for others.
- All typical values are at  $T_A = 25^\circ\text{C}$ .

## Electrical Characteristics for LM358A (continued)

at specified free-air temperature,  $V_{CC} = 5\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>(1)</sup>		T <sub>A</sub> <sup>(2)</sup>	LM358A			UNIT
					MIN	TYP <sup>(3)</sup>	MAX	
I <sub>IB</sub>	Input bias current	V <sub>O</sub> = 1.4 V		25°C		–15	–100	nA
				Full range			–200	
V <sub>ICR</sub>	Common-mode input voltage range	V <sub>CC</sub> = 30 V		25°C	0 to V <sub>CC</sub> – 1.5			V
				Full range	0 to V <sub>CC</sub> – 2			
V <sub>OH</sub>	High-level output voltage	R <sub>L</sub> ≥ 2 kΩ		25°C	V <sub>CC</sub> – 1.5			V
		V <sub>CC</sub> = 30 V	R <sub>L</sub> = 2kΩ	Full range	26			
			R <sub>L</sub> ≥ 10kΩ	Full range	27            28			
V <sub>OL</sub>	Low-level output voltage	R <sub>L</sub> ≤ 10 kΩ		Full range	5            20			mV
A <sub>VD</sub>	Large-signal differential voltage amplification	V <sub>CC</sub> = 15 V, V <sub>O</sub> = 1 V to 11 V, R <sub>L</sub> ≥ 2 kΩ		25°C	25            100			V/mV
				Full range	15			
CMRR	Common-mode rejection ratio			25°C	65            80			dB
k <sub>SVR</sub>	Supply-voltage rejection ratio (ΔV <sub>DD</sub> /ΔV <sub>IO</sub> )			25°C	65            100			dB
V <sub>O1</sub> / V <sub>O2</sub>	Crosstalk attenuation	f = 1 kHz to 20 kHz		25°C	120			dB
I <sub>O</sub>	Output current	V <sub>CC</sub> = 15 V, V <sub>ID</sub> = 1 V, V <sub>O</sub> = 0	Source	25°C	–20            –30            –60			mA
				Full range	–10			
		V <sub>CC</sub> = 15 V, V <sub>ID</sub> = –1 V, V <sub>O</sub> = 15 V	Sink	25°C	10            20			
				Full range	5			
		V <sub>ID</sub> = –1 V, V <sub>O</sub> = 200 mV		25°C	30			μA
I <sub>OS</sub>	Short-circuit output current	V <sub>CC</sub> at 5 V, GND at –5 V, V <sub>O</sub> = 0		25°C	±40            ±60			mA
I <sub>CC</sub>	Supply current (four amplifiers)	V <sub>O</sub> = 2.5 V, No load		Full range	0.7            1.2			mA
		V <sub>CC</sub> = MAX V, V <sub>O</sub> = 0.5 V, No load		Full range	1            2			

## 6.9 Operating Conditions

$V_{CC} = \pm 15\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
SR Slew rate at unity gain	$R_L = 1\text{ M}\Omega$ , $C_L = 30\text{ pF}$ , $V_I = \pm 10\text{ V}$ (see <a href="#">Figure 11</a> )	0.3	V/ $\mu\text{s}$
$B_1$ Unity-gain bandwidth	$R_L = 1\text{ M}\Omega$ , $C_L = 20\text{ pF}$ (see <a href="#">Figure 11</a> )	0.7	MHz
$V_n$ Equivalent input noise voltage	$R_S = 100\text{ }\Omega$ , $V_I = 0\text{ V}$ , $f = 1\text{ kHz}$ (see <a href="#">Figure 12</a> )	40	nV/ $\sqrt{\text{Hz}}$



## 6.10 Typical Characteristics

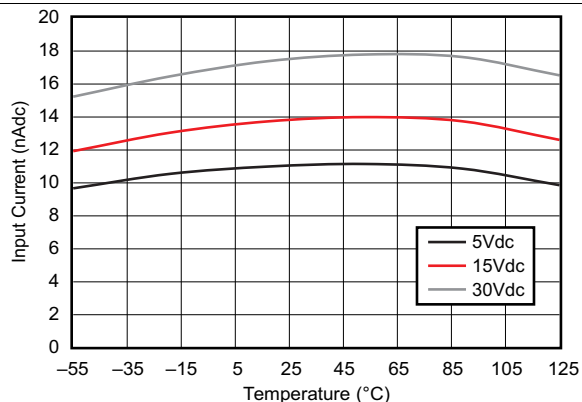


Figure 1. Input Current vs. Temperature

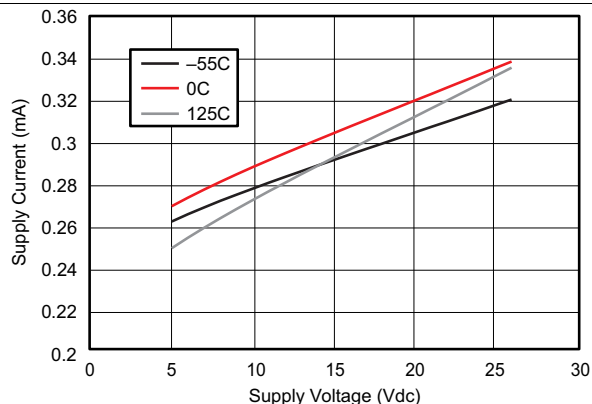


Figure 2. Supply Current vs. Supply Voltage

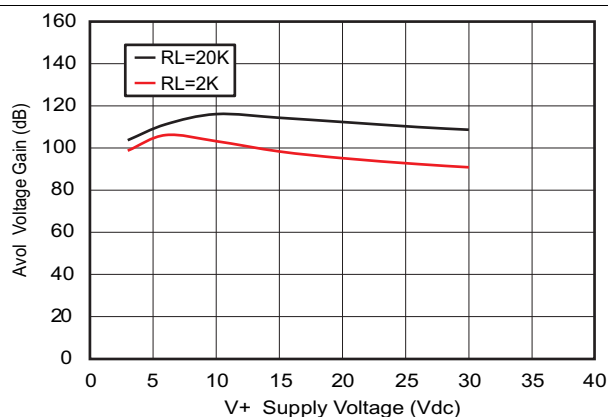


Figure 3. Voltage Gain vs. Supply Voltage

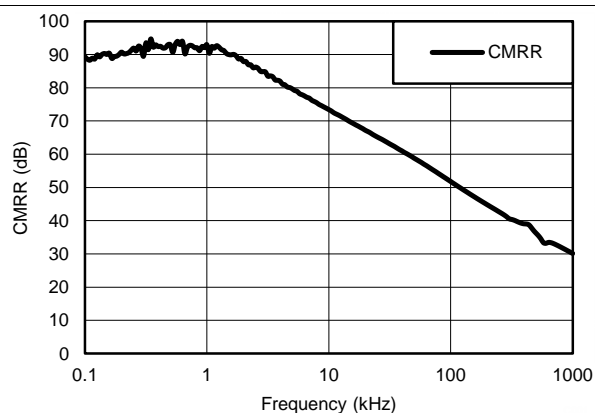


Figure 4. Common-mode Rejection Ratio vs. Frequency

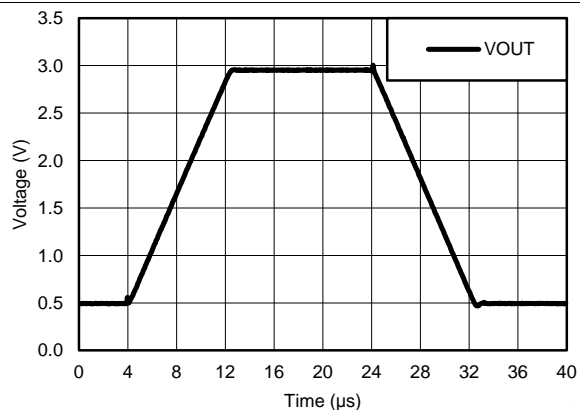


Figure 5. Voltage Follower Large Signal Response (50 pF)

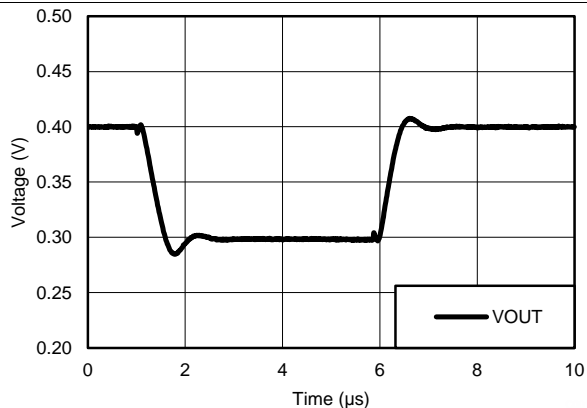


Figure 6. Voltage Follower Small Signal Response (50 pF)

## Typical Characteristics (continued)

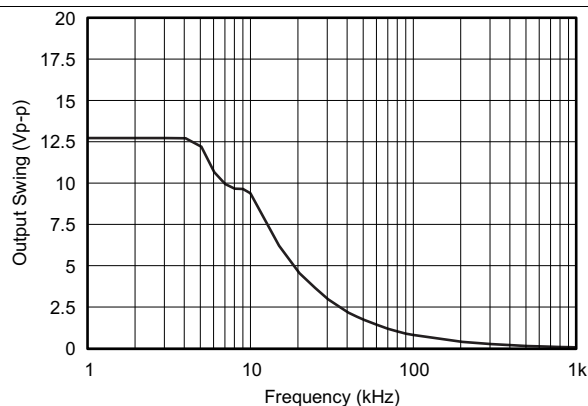


Figure 7. Maximum Output Swing vs. Frequency  
( $V_{CC} = 15\text{ V}$ )

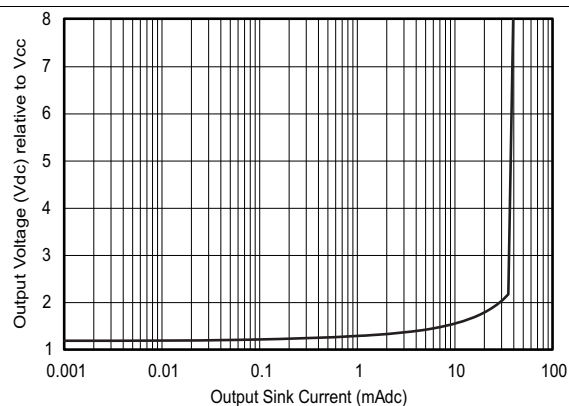


Figure 8. Output Sourcing Characteristics

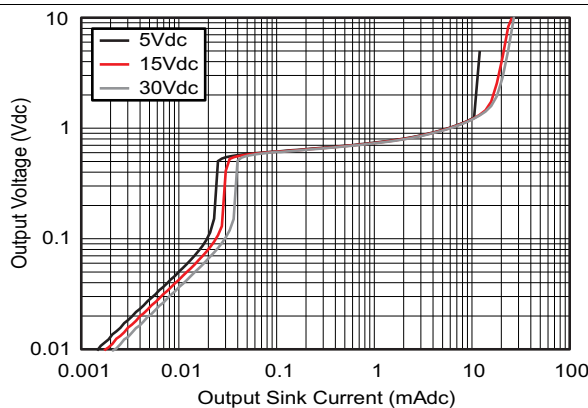


Figure 9. Output Sinking Characteristics

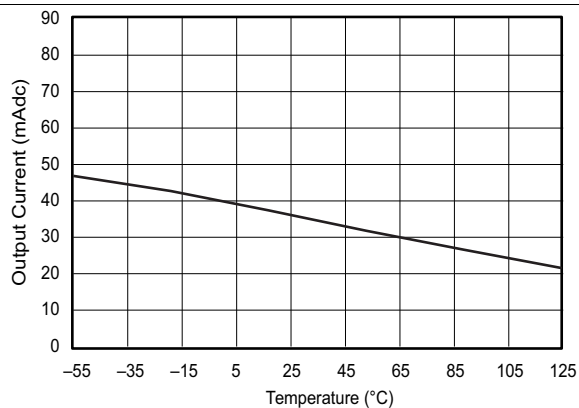


Figure 10. Source Current Limiting

## 7 Parameter Measurement Information

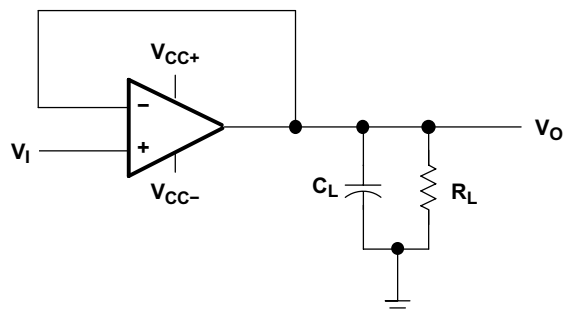


Figure 11. Unity-Gain Amplifier

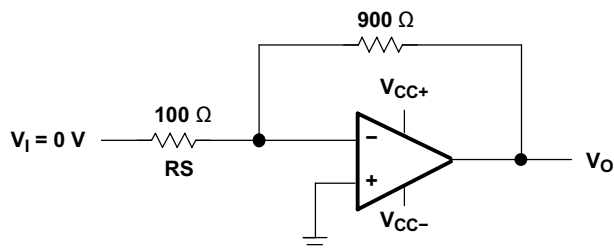


Figure 12. Noise-Test Circuit

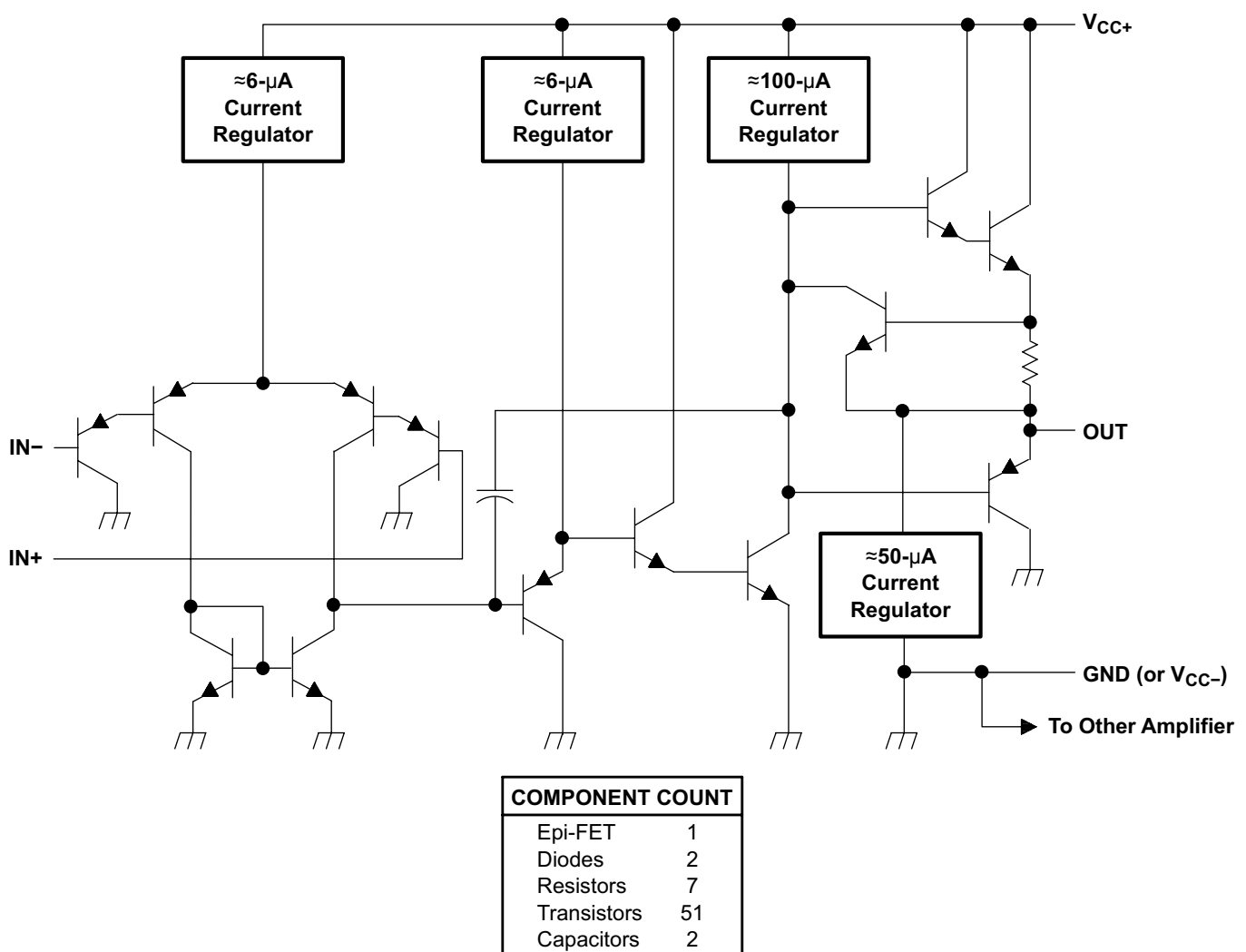
## 8 Detailed Description

### 8.1 Overview

These devices consist of two independent, high-gain frequency-compensated operational amplifiers designed to operate from a single supply over a wide range of voltages. Operation from split supplies also is possible if the difference between the two supplies is 3 V to 32 V (3 V to 26 V for the LM2904 device), and  $V_{CC}$  is at least 1.5 V more positive than the input common-mode voltage. The low supply-current drain is independent of the magnitude of the supply voltage.

Applications include transducer amplifiers, DC amplification blocks, and all the conventional operational amplifier circuits that now can be implemented more easily in single-supply-voltage systems. For example, these devices can be operated directly from the standard 5-V supply used in digital systems and easily can provide the required interface electronics without additional  $\pm 5$ -V supplies.

### 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Unity-Gain Bandwidth

The unity-gain bandwidth is the frequency up to which an amplifier with a unity gain may be operated without greatly distorting the signal. These devices have a 0.7-MHz unity-gain bandwidth.

### 8.3.2 Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. These devices have a 0.3-V/ $\mu$ s slew rate.

### 8.3.3 Input Common Mode Range

The valid common mode range is from device ground to  $V_{CC} - 1.5\text{ V}$  ( $V_{CC} - 2\text{ V}$  across temperature). Inputs may exceed  $V_{CC}$  up to the maximum  $V_{CC}$  without device damage. At least one input must be in the valid input common mode range for output to be correct phase. If both inputs exceed valid range then output phase is undefined. If either input is less than  $-0.3\text{ V}$  then input current should be limited to 1mA and output phase is undefined.

## 8.4 Device Functional Modes

These devices are powered on when the supply is connected. This device can be operated as a single supply operational amplifier or dual supply amplifier depending on the application.

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The LMx58 and LM2904 operational amplifiers are useful in a wide range of signal conditioning applications. Inputs can be powered before  $V_{CC}$  for flexibility in multiple supply circuits.

### 9.2 Typical Application

A typical application for an operational amplifier in an inverting amplifier. This amplifier takes a positive voltage on the input, and makes it a negative voltage of the same magnitude. In the same manner, it also makes negative voltages positive.

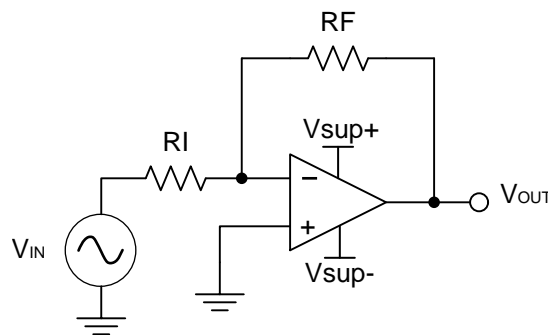


Figure 13. Application Schematic

#### 9.2.1 Design Requirements

The supply voltage must be chosen such that it is larger than the input voltage range and output range. For instance, this application will scale a signal of  $\pm 0.5$  V to  $\pm 1.8$  V. Setting the supply at  $\pm 12$  V is sufficient to accommodate this application.

#### 9.2.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier using [Equation 1](#) and [Equation 2](#):

$$A_v = \frac{V_{OUT}}{V_{IN}} \quad (1)$$

$$A_v = \frac{1.8}{-0.5} = -3.6 \quad (2)$$

Once the desired gain is determined, choose a value for  $R_I$  or  $R_F$ . Choosing a value in the kilohm range is desirable because the amplifier circuit will use currents in the milliamp range. This ensures the part will not draw too much current. This example will choose 10 k $\Omega$  for  $R_I$  which means 36 k $\Omega$  will be used for  $R_F$ . This was determined by [Equation 3](#).

$$A_v = -\frac{R_F}{R_I} \quad (3)$$

## Typical Application (continued)

### 9.2.3 Application Curve

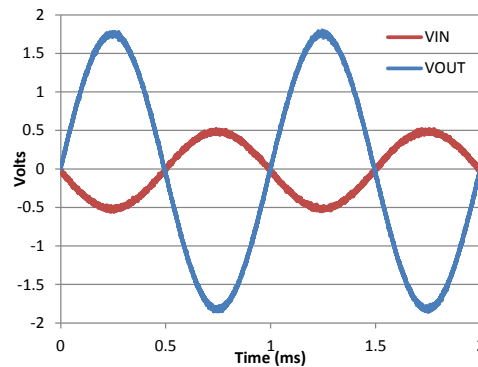


Figure 14. Input and Output Voltages of the Inverting Amplifier

## 10 Power Supply Recommendations

### CAUTION

Supply voltages larger than 32 V for a single supply (26 V for the LM2904), or outside the range of  $\pm 16$  V for a dual supply ( $\pm 13$  V for the LM2904) can permanently damage the device (see the [Absolute Maximum Ratings](#)).

Place 0.1- $\mu$ F bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the [Layout](#).

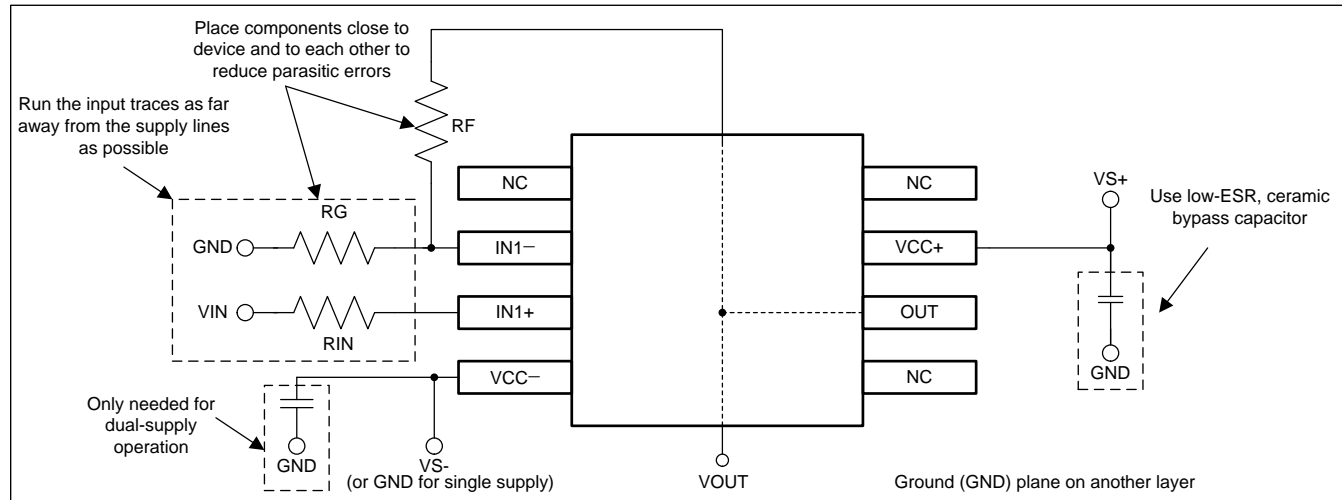
## 11 Layout

### 11.1 Layout Guidelines

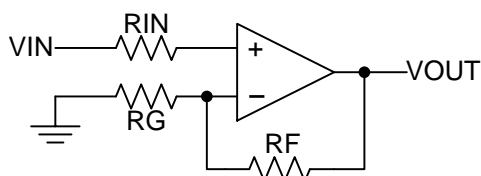
For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1- $\mu$ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in [Layout Examples](#).
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

## 11.2 Layout Examples



**Figure 15. Operational Amplifier Board Layout for Noninverting Configuration**



**Figure 16. Operational Amplifier Schematic for Noninverting Configuration**



## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

- *Circuit Board Layout Techniques*, [SLOA089](#).

### 12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 1. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM158	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
LM158A	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
LM258	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
LM258A	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
LM358	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
LM358A	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
LM2904	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
LM2904V	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 12.3 Trademarks

All trademarks are the property of their respective owners.

### 12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-87710012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 87710012A LM158FKB	<a href="#">Samples</a>
5962-8771001PA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	8771001PA LM158	<a href="#">Samples</a>
5962-87710022A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 87710022A LM158AFKB	<a href="#">Samples</a>
5962-8771002PA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	8771002PA LM158A	<a href="#">Samples</a>
LM158AFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 87710022A LM158AFKB	<a href="#">Samples</a>
LM158AJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	LM158AJG	<a href="#">Samples</a>
LM158AJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	8771002PA LM158A	<a href="#">Samples</a>
LM158FKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 87710012A LM158FKB	<a href="#">Samples</a>
LM158JG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	LM158JG	<a href="#">Samples</a>
LM158JGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	8771001PA LM158	<a href="#">Samples</a>
LM258AD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM258A	<a href="#">Samples</a>
LM258ADGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU NIPDAUAG	Level-1-260C-UNLIM	-25 to 85	(M3L ~ M3P ~ M3S ~ M3U)	<a href="#">Samples</a>
LM258ADGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	(M3L ~ M3P ~ M3S ~ M3U)	<a href="#">Samples</a>
LM258ADR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-25 to 85	LM258A	<a href="#">Samples</a>
LM258ADRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM258A	<a href="#">Samples</a>
LM258ADRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM258A	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM258AP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU   CU SN	N / A for Pkg Type	-25 to 85	LM258AP	<a href="#">Samples</a>
LM258APE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-25 to 85	LM258AP	<a href="#">Samples</a>
LM258D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM258	<a href="#">Samples</a>
LM258DE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM258	<a href="#">Samples</a>
LM258DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM258	<a href="#">Samples</a>
LM258DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU NIPDAUAG	Level-1-260C-UNLIM	-25 to 85	(M2L ~ M2P ~ M2S ~ M2U)	<a href="#">Samples</a>
LM258DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	(M2L ~ M2P ~ M2S ~ M2U)	<a href="#">Samples</a>
LM258DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-25 to 85	LM258	<a href="#">Samples</a>
LM258DRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM258	<a href="#">Samples</a>
LM258DRG3	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-25 to 85	LM258	<a href="#">Samples</a>
LM258DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM258	<a href="#">Samples</a>
LM258P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU   CU SN	N / A for Pkg Type	-25 to 85	LM258P	<a href="#">Samples</a>
LM258PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-25 to 85	LM258P	<a href="#">Samples</a>
LM2904AVQDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904AV	<a href="#">Samples</a>
LM2904AVQDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904AV	<a href="#">Samples</a>
LM2904AVQPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904AV	<a href="#">Samples</a>
LM2904AVQPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904AV	<a href="#">Samples</a>
LM2904D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2904	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2904DE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2904	<a href="#">Samples</a>
LM2904DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2904	<a href="#">Samples</a>
LM2904DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(MBL ~ MBP ~ MBS ~ MBU)	<a href="#">Samples</a>
LM2904DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(MBL ~ MBP ~ MBS ~ MBU)	<a href="#">Samples</a>
LM2904DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-40 to 125	LM2904	<a href="#">Samples</a>
LM2904DRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2904	<a href="#">Samples</a>
LM2904DRG3	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM2904	<a href="#">Samples</a>
LM2904DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2904	<a href="#">Samples</a>
LM2904P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU   CU SN	N / A for Pkg Type	-40 to 125	LM2904P	<a href="#">Samples</a>
LM2904PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	LM2904P	<a href="#">Samples</a>
LM2904PSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904	<a href="#">Samples</a>
LM2904PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904	<a href="#">Samples</a>
LM2904PWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904	<a href="#">Samples</a>
LM2904PWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI	-40 to 125		
LM2904PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-40 to 125	L2904	<a href="#">Samples</a>
LM2904PWRG3	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L2904	<a href="#">Samples</a>
LM2904PWRG4-JF	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		L2904	<a href="#">Samples</a>
LM2904QD	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 125		
LM2904QDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904Q1	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2904QDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904Q1	<a href="#">Samples</a>
LM2904QP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI	-40 to 125		
LM2904VQDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904V	<a href="#">Samples</a>
LM2904VQDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904V	<a href="#">Samples</a>
LM2904VQPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904V	<a href="#">Samples</a>
LM2904VQPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904V	<a href="#">Samples</a>
LM358AD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358A	<a href="#">Samples</a>
LM358ADE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358A	<a href="#">Samples</a>
LM358ADG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358A	<a href="#">Samples</a>
LM358ADGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	(M6L ~ M6P ~ M6S ~ M6U)	<a href="#">Samples</a>
LM358ADGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	(M6L ~ M6P ~ M6S ~ M6U)	<a href="#">Samples</a>
LM358ADR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	0 to 70	LM358A	<a href="#">Samples</a>
LM358ADRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358A	<a href="#">Samples</a>
LM358ADRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358A	<a href="#">Samples</a>
LM358AP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU   CU SN	N / A for Pkg Type	0 to 70	LM358AP	<a href="#">Samples</a>
LM358APE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	LM358AP	<a href="#">Samples</a>
LM358APW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	L358A	<a href="#">Samples</a>
LM358APWE4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	L358A	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM358APWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	0 to 70	L358A	<a href="#">Samples</a>
LM358APWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	L358A	<a href="#">Samples</a>
LM358D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358	<a href="#">Samples</a>
LM358DE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358	<a href="#">Samples</a>
LM358DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358	<a href="#">Samples</a>
LM358DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	(M5L ~ M5P ~ M5S ~ M5U)	<a href="#">Samples</a>
LM358DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	(M5L ~ M5P ~ M5S ~ M5U)	<a href="#">Samples</a>
LM358DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	0 to 70	LM358	<a href="#">Samples</a>
LM358DRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358	<a href="#">Samples</a>
LM358DRG3	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM358	<a href="#">Samples</a>
LM358DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358	<a href="#">Samples</a>
LM358P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU   CU SN	N / A for Pkg Type	0 to 70	LM358P	<a href="#">Samples</a>
LM358PE3	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 70	LM358P	<a href="#">Samples</a>
LM358PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	LM358P	<a href="#">Samples</a>
LM358PSLE	OBSOLETE	SO	PS	8		TBD	Call TI	Call TI	0 to 70		
LM358PSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	L358	<a href="#">Samples</a>
LM358PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	L358	<a href="#">Samples</a>
LM358PWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	L358	<a href="#">Samples</a>
LM358PWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI	0 to 70		

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM358PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	0 to 70	L358	<a href="#">Samples</a>
LM358PWRG3	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	L358	<a href="#">Samples</a>
LM358PWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	L358	<a href="#">Samples</a>
LM358PWRG4-JF	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		L358	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF LM258A, LM2904 :**

- Automotive: [LM2904-Q1](#)
- Enhanced Product: [LM258A-EP](#)

**NOTE: Qualified Version Definitions:**

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications



**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM258ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM258ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM258ADR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM258ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM258DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM258DR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM258DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258DRG3	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM258DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904AVQPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904AVQPWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2904DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2904DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904DRG3	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM2904DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904PSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
LM2904PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904PWRG3	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904VQPWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM358ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM358ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358ADR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM358ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358APWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358APWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM358DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM358DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358DRG3	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM358DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358PSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
LM358PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358PWRG3	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



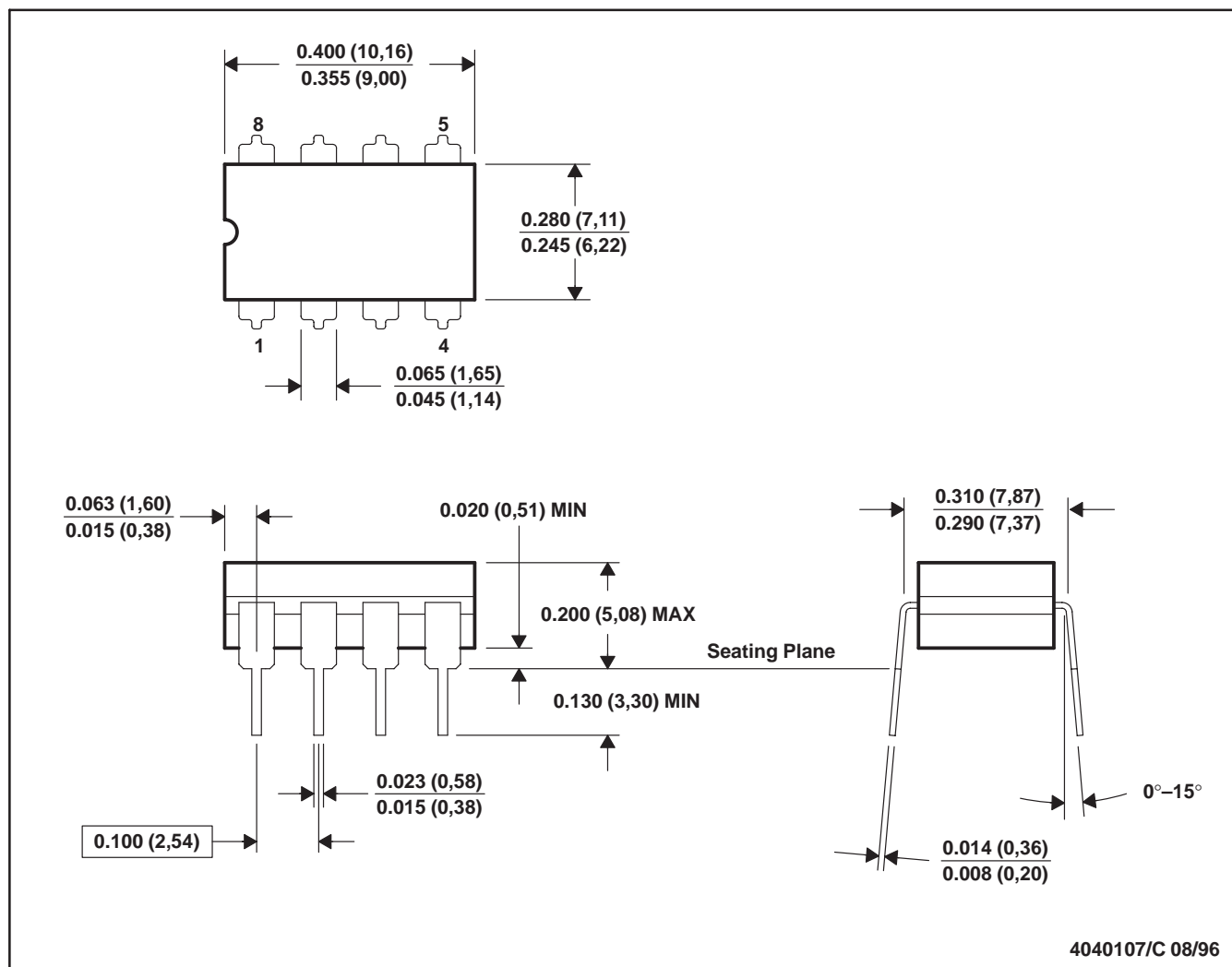
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM258ADGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
LM258ADGKR	VSSOP	DGK	8	2500	332.0	358.0	35.0
LM258ADR	SOIC	D	8	2500	364.0	364.0	27.0
LM258ADR	SOIC	D	8	2500	340.5	338.1	20.6
LM258ADR	SOIC	D	8	2500	367.0	367.0	35.0
LM258ADRG4	SOIC	D	8	2500	367.0	367.0	35.0
LM258ADRG4	SOIC	D	8	2500	340.5	338.1	20.6
LM258DGKR	VSSOP	DGK	8	2500	332.0	358.0	35.0
LM258DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
LM258DR	SOIC	D	8	2500	364.0	364.0	27.0
LM258DR	SOIC	D	8	2500	340.5	338.1	20.6
LM258DR	SOIC	D	8	2500	367.0	367.0	35.0
LM258DRG3	SOIC	D	8	2500	364.0	364.0	27.0
LM258DRG4	SOIC	D	8	2500	367.0	367.0	35.0
LM2904AVQPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
LM2904AVQPWRG4	TSSOP	PW	8	2000	367.0	367.0	35.0
LM2904DGKR	VSSOP	DGK	8	2500	332.0	358.0	35.0
LM2904DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
LM2904DR	SOIC	D	8	2500	367.0	367.0	35.0
LM2904DRG3	SOIC	D	8	2500	364.0	364.0	27.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2904DRG4	SOIC	D	8	2500	340.5	338.1	20.6
LM2904DRG4	SOIC	D	8	2500	367.0	367.0	35.0
LM2904PSR	SO	PS	8	2000	367.0	367.0	38.0
LM2904PWR	TSSOP	PW	8	2000	364.0	364.0	27.0
LM2904PWRG3	TSSOP	PW	8	2000	364.0	364.0	27.0
LM2904QDR	SOIC	D	8	2500	367.0	367.0	35.0
LM2904VQPWRG4	TSSOP	PW	8	2000	367.0	367.0	35.0
LM358ADGKR	VSSOP	DGK	8	2500	332.0	358.0	35.0
LM358ADGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
LM358ADR	SOIC	D	8	2500	340.5	338.1	20.6
LM358ADR	SOIC	D	8	2500	364.0	364.0	27.0
LM358ADRG4	SOIC	D	8	2500	340.5	338.1	20.6
LM358ADRG4	SOIC	D	8	2500	367.0	367.0	35.0
LM358APWR	TSSOP	PW	8	2000	367.0	367.0	35.0
LM358APWR	TSSOP	PW	8	2000	364.0	364.0	27.0
LM358DGKR	VSSOP	DGK	8	2500	332.0	358.0	35.0
LM358DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
LM358DR	SOIC	D	8	2500	340.5	338.1	20.6
LM358DR	SOIC	D	8	2500	367.0	367.0	35.0
LM358DRG3	SOIC	D	8	2500	364.0	364.0	27.0
LM358DRG4	SOIC	D	8	2500	367.0	367.0	35.0
LM358DRG4	SOIC	D	8	2500	340.5	338.1	20.6
LM358PSR	SO	PS	8	2000	367.0	367.0	38.0
LM358PWR	TSSOP	PW	8	2000	364.0	364.0	27.0
LM358PWRG3	TSSOP	PW	8	2000	364.0	364.0	27.0

## JG (R-GDIP-T8)

## CERAMIC DUAL-IN-LINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification.
  - E. Falls within MIL STD 1835 GDIP1-T8

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

## DGK (S-PDSO-G8)

## PLASTIC SMALL-OUTLINE PACKAGE



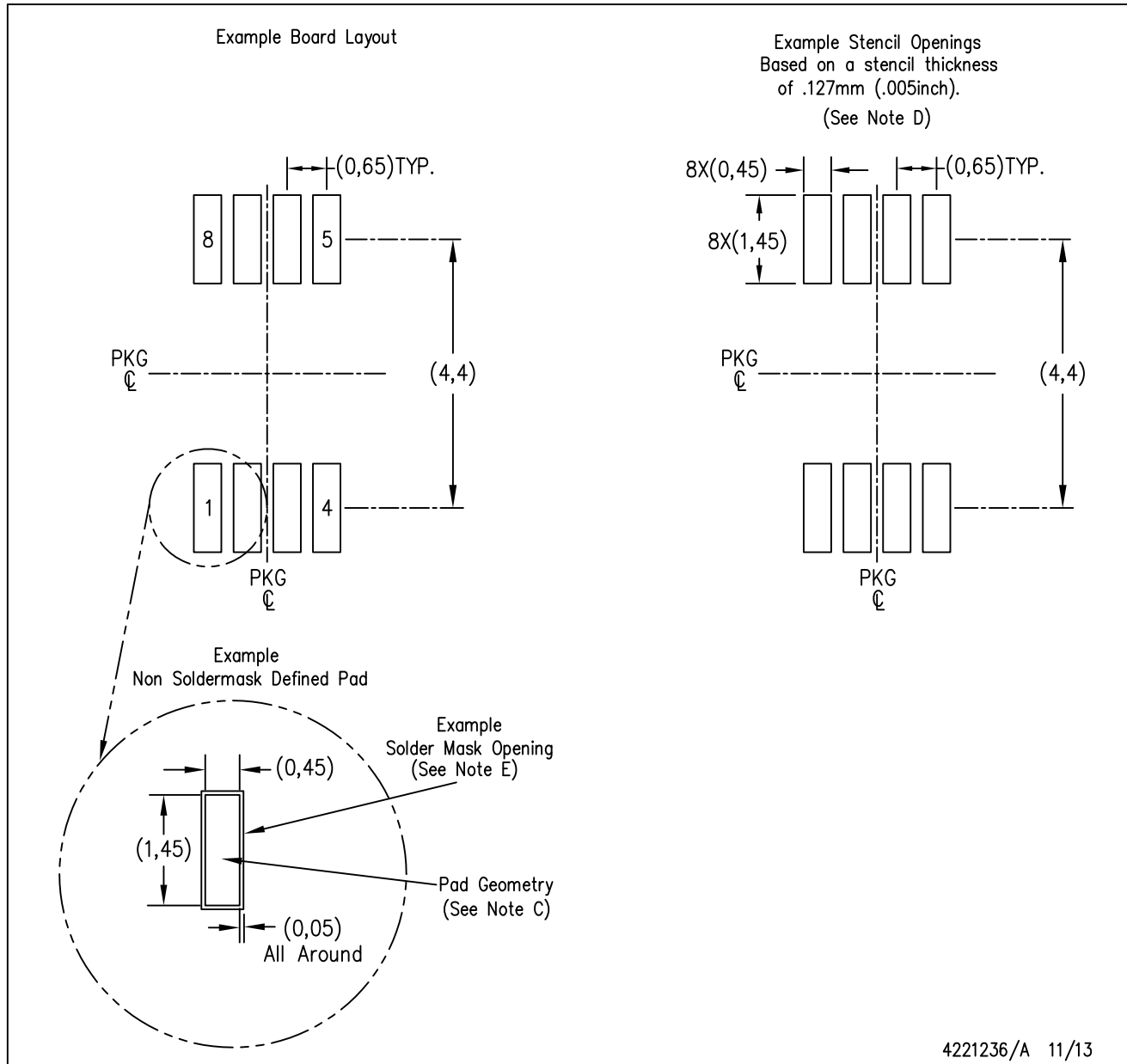
## NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.



DGK (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

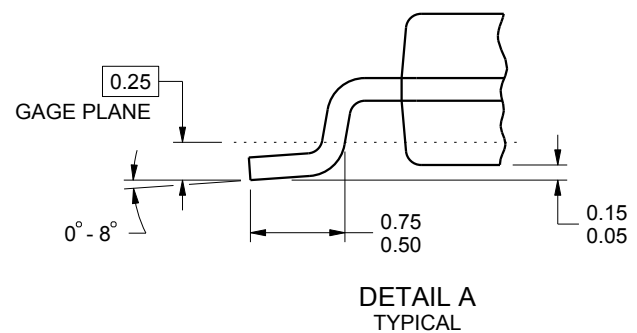
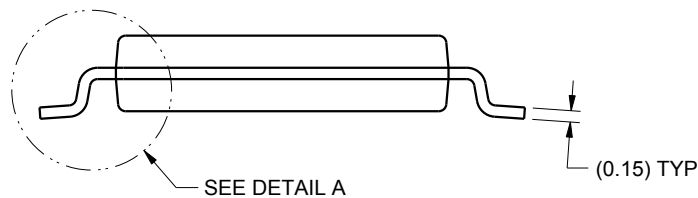
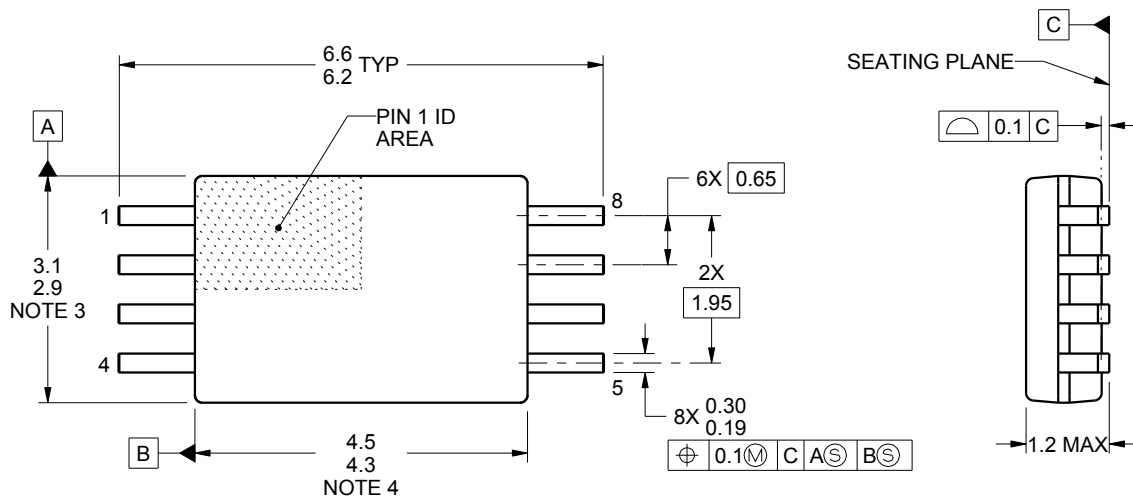
PW0008A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

### NOTES:

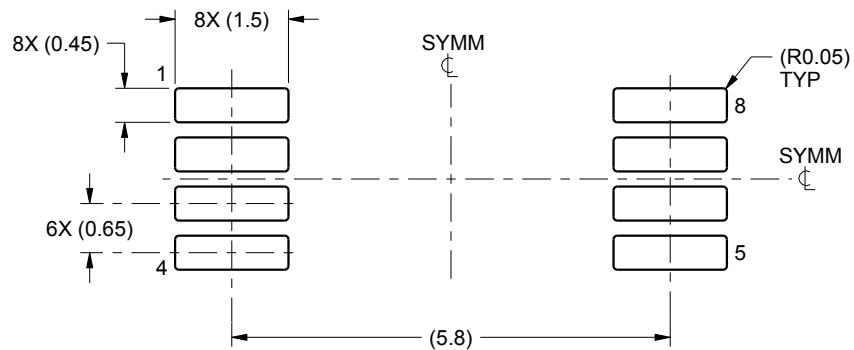
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

# EXAMPLE BOARD LAYOUT

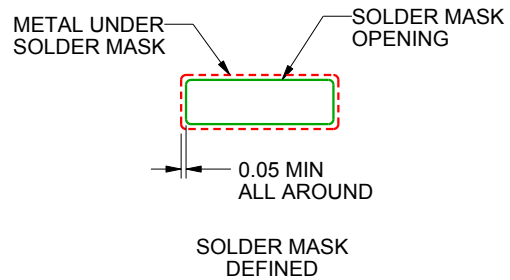
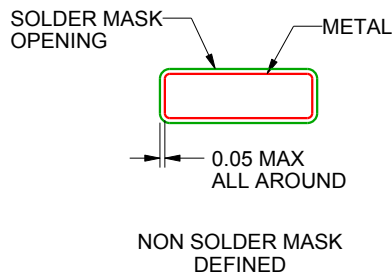
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

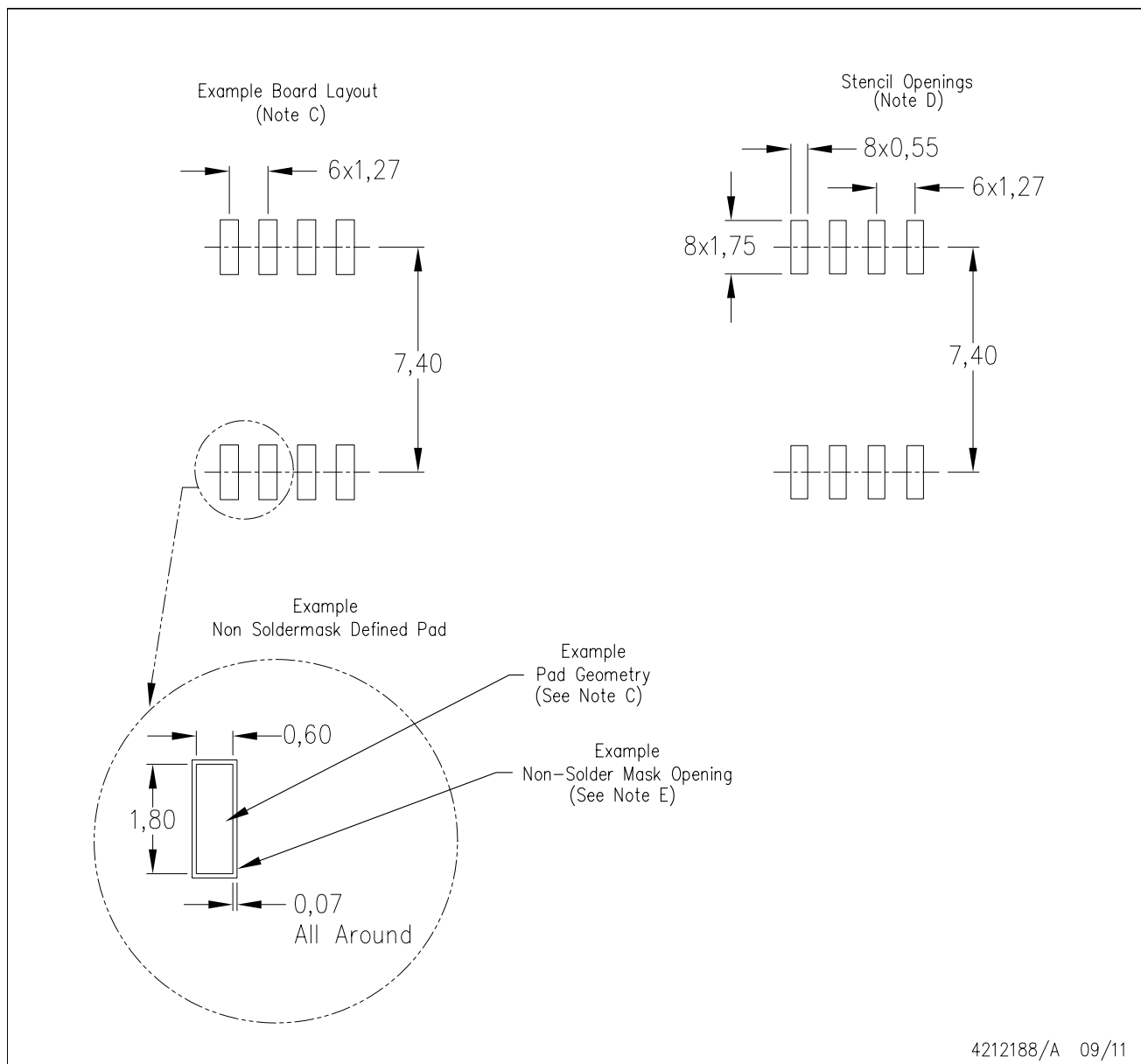
PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



4040063/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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