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Optimized all Hardware Edge Node, 10BASE-T1S Ethernet to the Edge Bus (E^2B) Transceiver

FEATURES

- 10BASE-T1S IEEE 802.3-2022 compliant PHY with support for PLCA and an integrated MAC
- 10BASE-T1S PHY operating modes
  - Point-to-point half-duplex (≥ 15 m)
  - Multidrop configuration half-duplex (≥ 25 m, ≥ 8 nodes)
- PLCA features: PLCA coordinator, burst mode, precedence mode, and multiple PLCA IDs
- MAC Features
  - AD3300 only: OPEN Alliance 10BASE-T1x MAC-PHY serial interface
  - AD3300 only: Transmit priority queues
  - 16 MAC address filters
- IEEE 802.1AS / IEEE 1588 support for TSN using the gPTP combined with sensor timestamping and actuator synchronization
- Low Complexity Ethernet Engine
  - Provides a deterministic, low-latency data path between 10BASE-T1S to the SAIF
  - 12 SAIF pins support simultaneous operation of several common sensor/actuator interface standards and functions, including SPI, I^2C, UART, PWM, GPIO, Flexible I/O, and bridge to LIN
  - SMC enables periodic read and write functions on all interfaces
  - AD3300 supports dual mode: MAC-PHY and LCE operation simultaneously
  - AD3304/5 only: Bridge to ISELED and ILaS
- OPEN Alliance features sleep/wake-up, topology discovery, and advanced diagnostics
  - Enable output pin (EN) to power down the regulated supply inputs in sleep mode
  - Support for local (WAKE input pin) and network (wake-up pulse) wake
- Suitable for 12 V, 24 V, 48 V automotive electrical systems or operating from 5 V levels only
- Detection capability for over voltage and under voltage events when monitoring the VBAT pin
- General-purpose ADC
- SSC for handling fault conditions
- Low-current 3.3 V LDO using the LVDD pin as an output
- Compatible with power delivery over data cable
- Provides robust EMC/EMI performance
  - Low cost bus interface network with no external ESD components required
  - Enhanced noise immunity providing additional performance for noisy environments
- Low power consumption: maximum current of 50 mA in functional modes of operation and 40 µA in sleep mode
- 1.8 V to 3.3 V I/O logic levels with support for 5 V inputs
- −40°C to +150°C junction temperature range
- Small package: 4 mm x 4 mm 24-lead LFCSP (QFN) package
- AEC-Q100 qualified for automotive applications

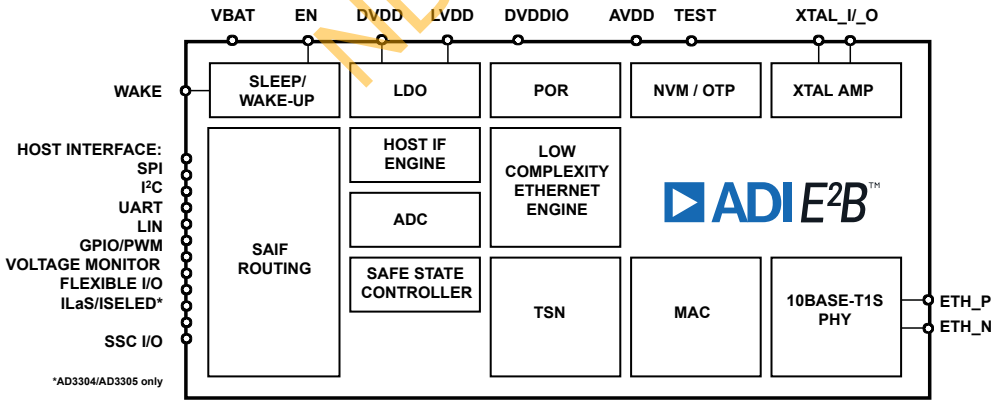

Figure 1. AD3301/4/5 Functional Block Diagram

Optimized all Hardware Edge Node, 10BASE-T1S Ethernet to the Edge Bus (E^{2}B) Transceiver

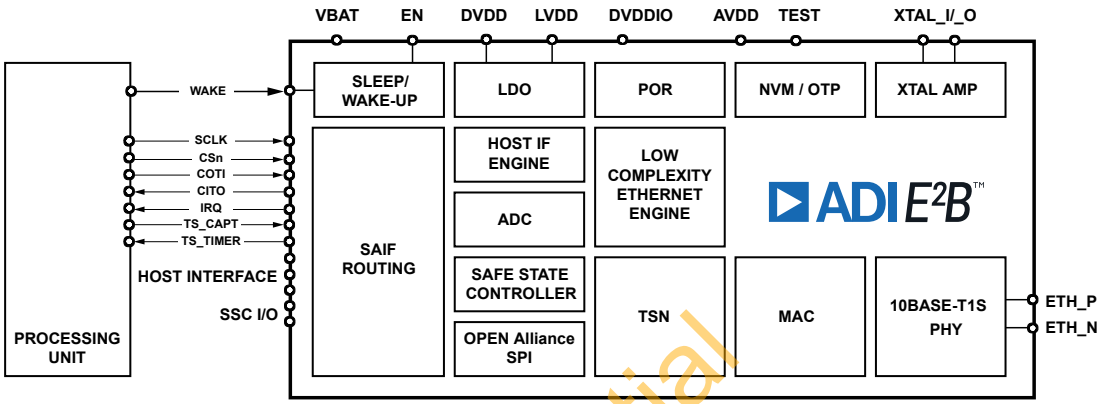

Figure 2. AD3300 Functional Block Diagram (Dual mode)

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APPLICATIONS

- Automotive internal and external lighting
- Automotive body and chassis domain control
- Automotive sensor and actuator networking
- Automotive Ethernet based zonal architectures
- Automotive in-vehicle networking

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05/2024—Revision Sp0: Initial Version

GENERAL DESCRIPTION

The AD3300/AD3301/AD3304/AD3305 are highly optimized, all hardware remote devices for 10BASE-T1S Ethernet connectivity to remote sensors and actuators. They provide the ability to remove microcontrollers from edge nodes in automotive applications.

The PHY is compliant with the IEEE 802.3™-2022 Ethernet standard for short reach 10 Mbps single pair Ethernet, and operates in point-to-point (half-duplex) configurations up to at least 15 m and multidrop configurations up to at least 25 m with up to at least 8 nodes.

Physical layer collision avoidance (PLCA) is supported for improving latency and throughput performance in a half-duplex communication system. The PLCA block includes PLCA coordinator mode, burst mode, and precedence mode. Multiple PLCA IDs reduce latency as certain nodes can be prioritized using more than one transmit opportunity within a PLCA cycle.

OPEN Alliance TC10/TC14 features include:

- Sleep/Wake-up
- Topology Discovery
- Advanced diagnostics including dynamic channel quality (DCQ) and signal quality index (SQI)

The transceiver contains an integrated media access control (MAC) interface with 16 MAC address filters.

Only the AD3300 model allows direct connectivity with a host controller via an OPEN Alliance 10BASE-T1x MAC-PHY Serial Interface. This SPI enables the use of lower capability processors without an integrated MAC, which provides for the lowest overall system level power consumption. Incoming Ethernet frames can be assigned to different transmit priority queues. Full switching capability between the 10BASE-T1S network interface, OA-SPI, and SAIF is supported. This enables, for example, a processor shared access to the 10BASE-T1S network in conjunction with the LCE (dual mode).

The AD3300 default configuration has the MAC-PHY OA-SPI interface disabled (LCE only mode). The user must enable the MAC-PHY OA-SPI interface over the network via an E^{2}B message, setting the node to dual mode access. For systems requiring local microcontroller OA-SPI interface access on power-up, the dual mode configuration can be programmed into the OTP.

Time-sensitive networking (TSN) is supported using the IEEE 802.1AS™ / IEEE 1588™ engine to synchronize with a generalized precision time protocol (gPTP) grandmaster. gPTP enables high-precision clock recovery with ultra-low jitter for synchronization to a common network time and timestamping of sensor data.

Over voltage (OV) and under voltage (UV) events can be detected when monitoring the battery via the VBAT pin using programmable over voltage and under voltage thresholds.

The integrated safe state controller (SSC) can monitor fault detection mechanisms and place the device in a safely defined mode of operation in the event of a fault condition. This ensures that the 10BASE-T1S node enters a pre-defined state in the event of a local fault.

In addition, E^{2}B™ simplifies the networking of sensors and actuators in the vehicle by integrating a low complexity Ethernet (LCE) hardware engine, removing the need for microcontrollers in sensor and actuator nodes. This offers the ability to implement an all-hardware edge node, greatly simplifying edge node implementation.

A system utilizing E^{2}B comprises a controller node with a 10BASE-T1S interface along with one or more AD3300/1/4/5 devices. All AD3300/1/4/5 devices operate in remote mode (LCE running E^{2}B protocol), bridging directly from the IEEE 10BASE-T1S network to sensors and/or actuators. All software can be removed from the edge nodes and centralized either in the controller node or in another node/device on the Ethernet network. An E^{2}B network example is shown in Figure 3.

The E^{2}B transport protocol (EBTP) specifies a highly optimized remote control protocol (RCP) to transport control and interface data over a network between E^{2}B capable entities. These entities include, but are not limited to, E^{2}B transceivers and T1S compliant MAC-PHYs combined with a controller running the E^{2}B transport protocol driver. The E^{2}B software uses this protocol to configure all E^{2}B remote nodes and to packet or parse E^{2}B data within Ethernet frames. This enables efficient communication to/from the remote nodes. The E^{2}B software layer can be run on a controller node connected directly to the IEEE 10BASE-T1S bus / network. Or alternatively on a zonal or central processing unit that may be connected through one or more Ethernet switch devices.

The AD3300/1/4/5 consume Ethernet frames generated by the E^{2}B software layer in the controller node. These frames may contain status requests, configuration commands, or data frames for connected actuators. Responses for status requests and configuration frames or data from connected sensors are automatically transmitted back to the E^{2}B controller node.

If the frames contain data for the connected sensor/actuator interface (SAIF), the E^{2}B remote node outputs this data via the pre-configured pins. If a response is captured and an acknowledgment is required, the E^{2}B remote node prepares the response frame which is transmitted back to the E^{2}B controller node.

All of the Ethernet frame parsing and response frame generation is performed exclusively in hardware (no software stack needed) by the AD3300/1/4/5. This means that no external processor is required at the sensor/actuator to enable the connection to the IEEE 10BASE-T1S network. The resulting network can be used to create both simple and complex control loops.

GENERAL DESCRIPTION

The AD3300/1/4/5 supports many common automotive sensor/actuator interface protocols, for example SPI, I²C, UART, GPIO, and PWM. Additional interfaces can be implemented using Flexible I/O. Bridging to several commonly used automotive networking protocols such as LIN is supported as well.

Additionally, the AD3304/5 supports other internal lighting network protocols such as ISELED[1] and ILaS[2]

The scannable memory controller (SMC) block enables simple functions to be repeated on a defined time interval. The SMC provides flexibility and adaptability, allowing the system to respond to changes in conditions or requirements effectively without any instruction from the software other than the configuration, reducing traffic on the Ethernet bus.

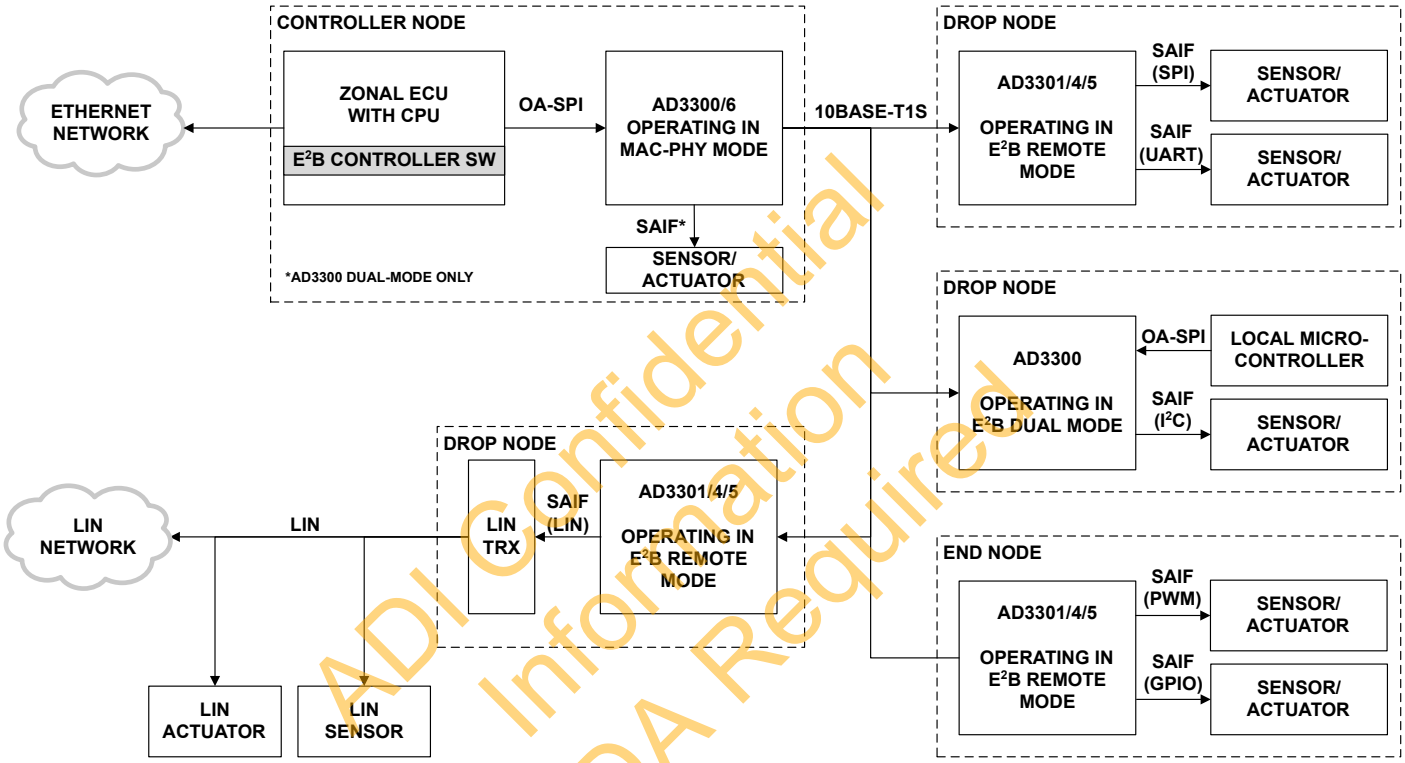

Figure 3. Example Conceptual E²B Network

EXTERNAL SPECIFICATIONS

The AD3300/AD3301/AD3304/AD3305 10BASE-T1S transceivers conform to the specifications listed below.

- IEEE Standard 802.3™-2022
- IEEE 802.3 Clause 148 PLCA Reconciliation Sublayer (RS)
- OPEN Alliance 10BASE-T1x MAC-PHY Serial Interface V1.1
- OPEN Alliance TC10/TC14 10BASE-T1S Sleep/Wake-up version 1.0
- OPEN Alliance TC14 10BASE-T1S Topology Discovery Specification version 1.0
- OPEN Alliance TC14 Advanced diagnostic features for 10BASE-T1S automotive Ethernet PHYs version 1.1
- AD3300/1/4/5 is compatible with the I²C-bus specification v2.1
- AD3300/1/4/5 conforms to the LIN specification v2.2
- AD3304/5 is compatible with ISELED and ILaS interface by INOVA Semiconductors

[1] Protocol: Integrated Smart Ecosystem Light Emitting Diode.
[2] Field Bus: ISELED Light and Sensor.

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OPERATING CONDITIONS

AVDD = 4.75 V to 5.25 V; DVDDIO = 1.71 V to 3.47 V; DVDD and LVDD from internal LDO; All specifications at −40°C to +150°C junction temperature, unless otherwise noted.

Table 1. Operating Conditions

Parameter	Symbol	Conditions / Comments	Min	Typ	Max	Unit
POWER REQUIREMENTS						
Digital Core Power Supply	V_{DVDD}	Power supply output. Generated from internal LDO		1.1		V
Low-voltage Supply	V_{LVDD}[1]	Power supply output. Generated from internal LDO	3.05	3.3	3.45	V
Digital Input and Output Power Supply	V_{DVDDIO}	Power supply input. Can be supplied from LVDD[1]	1.71		3.47	V
Analog Power Supply	V_{AVDD}	Power supply input	4.75	5	5.25	V
Always-on Domain Supply	V_{VBAT}	Power supply input	4.5		70	V
POWER ON RESET						
Exit From Reset	V_{VBAT}	Always-on domain functional	3.2		3.9	V
	V_{AVDD}	All other IC domains functional	4.2		4.7	V
Entry Into Reset	V_{VBAT}	Independent from AVDD: Complete IC in reset	3.2		3.9	V
	V_{AVDD}	Complete IC in reset excluding always-on domain	4.2		4.7	V
TEMPERATURE						
Junction Temperature for OTP Programming	T_J		-40		+120	°C
Junction Temperature	T_J		-40		+150	°C
REFERENCE CLOCK INPUT						
Transconductance	g_M			6.25		mS
External Crystal (XTAL)		Requirements for an external crystal used on XTAL_I/ CLK_IN pin and XTAL_O pin				
Crystal Frequency				25		MHz
Crystal Frequency Tolerance		Over full temperature range and life-time	-100		+100	ppm
Crystal Shunt Capacitance	C_{SHUNT}				3	pF
Crystal Load Capacitance[2]	C_{LOAD}				12	pF
Crystal Equivalent Series Resistance (ESR)	R_s				100	Ω
External Clock Input (CLK_IN)		When driving XTAL_I with an oscillator				
Clock Input Frequency				25		MHz
Clock Input Frequency Tolerance		Over full temperature range and lifetime	-100		+100	ppm
Clock Input Voltage Range		DC-coupled sine or square wave at XTAL_I/CLK_IN pin	0.8		1.1	Vp-p
Clock Input Duty Cycle			40		60	%

[1] Maximum 10 mA DC current.

[2] Load capacitance $C_{LOAD} = (C1 \times C2)/(C1 + C2) + C_{STRAY}$, where C_{STRAY} is the stray capacitance including routing and package parasitics. C1 and C2 are the capacitors loaded on PCB.

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ELECTRICAL CHARACTERISTICS

The digital inputs are 5 V tolerant.

Limited support for 5 V open drain outputs (I^2C, ISELED and Flexible I/O only).

Table 2. Electrical Characteristics

Parameter	Symbol	Conditions / Comments	Min	Typ	Max	Unit
DIGITAL INPUTS		SAIF[11:0] / OA-SPI[1]				
Input High Voltage	V_{IH}	DVDDIO: 2.5 V to 3.3 V	DVDDIO × 0.7		5.5	V
		DVDDIO: 1.8 V to < 2.5 V	DVDDIO × 0.7		4.5	V
Input Low Voltage	V_{IL}		−0.3		DVDDIO × 0.3	V
Input Pull-up Resistance	R_{PU}	DVDDIO = 3.63 V, V_{PAD} = 0 V	15		30	kΩ
Input Pull-down Resistance	R_{PD}	DVDDIO = 3.63 V, V_{PAD} = 3.63 V	15		30	kΩ
		DVDDIO = 3.63 V, V_{PAD} = 5.5 V	22		40	kΩ
Input Leakage Current	I_{IN}		-2		+2	µA
DIGITAL INPUTS		WAKE				
WAKE Input Threshold		Active high	0.95	1	1.05	V
		Active low[2]	0.9		1	V
Input Leakage Current	I_{IN}	WAKE: 0 V to 70 V	-1		+1	µA
ADC		SAIF[5:0]				
Input Range			0		3.6	V
Input Absolute Error					±50	mV
Input Voltage Sensitivity				±8		mV
DC Signal Voltage Input Bandwidth					20	kHz
ADC Resolution					12	bit
Sample Rate					500	kSPS
Input Impedance			1			MΩ
TEMPERATURE SENSOR						
Temperature Range			-40		150	°C
Temperature Accuracy					±20	°C
DIGITAL OUTPUTS						
Output High Voltage	V_{OH}	SAIF[11:0]				
		Load condition = 2 mA	DVDDIO – 0.4			V
		EN				
		Load condition = 25 µA	2.5		3.6	V
Output Low Voltage	V_{OL}	SAIF[11:0]				
		Load condition = 2 mA			0.4	V
		EN				
		Load condition = 250 µA			0.4	V
High Impedance Leakage Current	I_{LEAK}		-2		+5	µA
DIGITAL I/O		SAIF[11:0]				
Pin Capacitance	C_{PIN}				7	pF
10BASE-T1S PHY		ETHP, ETHN				
Differential Capacitance		Measurement frequency = 10 MHz		4[3]	7[4]	pF
Output Signal Swing		Driving the 50 Ω differential load	0.8	1	1.2	V_{P-P}

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[1] AD3300 only.

[2] 40 mV to 50 mV hysteresis on the WAKE input pin.

[3] V_{CM} = 2.5 V, Temp. = +25°C, IC powered.

[4] V_{CM} = -5 V to +10 V, Temp. = -40°C to +150°C, IC powered and unpowered.

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POWER CONSUMPTION CHARACTERISTICS

Table 3. Power Consumption Characteristics

Parameter	Symbol	Conditions / Comments	Min	Typ	Max	Unit
Battery Power Supply	I_{VBAT}			28	40	µA
DVDDIO Current Consumption[1]	I_{DVDDIO}	The DVDDIO current is determined by a number of external factors[2]				
Analog Power Supply Standby Mode	I_{AVDD}			2.3	3	mA
Analog Power Supply Active Mode[3]	I_{AVDD}				48	mA
Analog Power Supply Active Mode[4]	I_{AVDD}	Transmitting			50	mA
		Receiving			30	mA
Battery Power Supply Sleep Mode	$I_{VBATSleep}$			28	40	µA
Analog Power Supply Sleep Mode[5]	$I_{AVDDSleep}$				50	µA

1 When sourcing from LVDD, do not exceed the DC current limit of 10 mA.

2 See DVDDIO Current.

3 MAC-PHY with 10 Mbps Ethernet throughput, 15 MHz OA-SPI clock.

4 Remote node.

5 Typically AVDD supply is turned off using EN pin function saving AVDD current when in sleep mode.

DVDDIO Current

I_{DVDDIO} is application specific, but is typically dominated by the sum of Output Dynamic Current and Input Dynamic Current:

$$I_{DVDDIO} = I_{OD} + I_{ID}$$

The on-chip I/O current I_{DVDDIO} is based on dynamic switching currents on the digital I/O pins.

The dynamic current, due to switching activity on an output pin, is calculated using the following equation:

$$Output \quad Dynamic \quad Current \quad (I_{OD}) = (C_{PIN} + C_L) \times V_{DVDDIO} \times f$$

Where:

- C_{PIN} = dynamic, transient power dissipation capacitance internal to the transceiver output pins (see Table 2).
- C_L = total load capacitance that an output pin sees outside the transceiver.
- V_{DVDDIO} = DVDDIO supply voltage.
- f = frequency of switching on the pin.

The dynamic current, due to switching activity on an input pin, is calculated using the following equation:

$$Input \quad Dynamic \quad Current \quad (I_{ID}) = C_{PIN} \times V_{DVDDIO} \times f$$

Where:

- C_{PIN} = dynamic, transient power dissipation capacitance internal to the transceiver input pins (see Table 2).
- V_{DVDDIO} = DVDDIO supply voltage.
- f = frequency of switching on the pin.

Further aspects that may need to be taken into account include the contributions due to additional resistive loads (either internal or external pull-up/pull-down) and any open-drain configuration of output drivers.

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OPEN ALLIANCE SPI I/O TIMING SPECIFICATIONS

Table 4. OA-SPI Timing Specifications

Parameter	Symbol	Conditions / Comments	DVDDIO = 1.8 V		DVDDIO = 3.3 V		Unit
			Min	Max	Min	Max	
OPEN Alliance compliant SPI (OA-SPI)		OPEN Alliance SPI pins (SCLK, $\overline{IRQ}$, $\overline{CS}$, CITO, and COTI)					
SCLK Frequency			8	22.5	8	25	MHz
SCLK Frequency		Dual mode[1]	8	15	8	15	MHz
SCLK Duty Cycle			25/75	75/25	25/75	75/25	%
$\overline{CS}$ High Time	t_{25}	SCLK frequency = 15 MHz	120		120		ns
$\overline{CS}$ Setup Time	t_{26}	SCLK frequency = 15 MHz	17		17		ns
$\overline{CS}$ Hold Time	t_{27}	SCLK frequency = 15 MHz	17		17		ns
COTI Input Setup Time Before Sample Edge	t_{28}	SCLK frequency = 15 MHz	5		5		ns
COTI Input Hold Time After Sample Edge	t_{29}	SCLK frequency = 15 MHz	5		5		ns
CITO Output Valid (Delay After Drive Edge)	t_{30}	SCLK frequency = 15 MHz		14		12	ns
CITO Output Hold Time After Drive Edge	t_{31}	SCLK frequency = 15 MHz	5		4		ns
CITO Output Disable Time	t_{32}	SCLK frequency = 15 MHz		20		20	ns
CITO Output Valid (Delay After $\overline{CS}$ Edge)	t_{33}	SCLK frequency = 15 MHz		15		12	ns

[1] AD3300 model only.

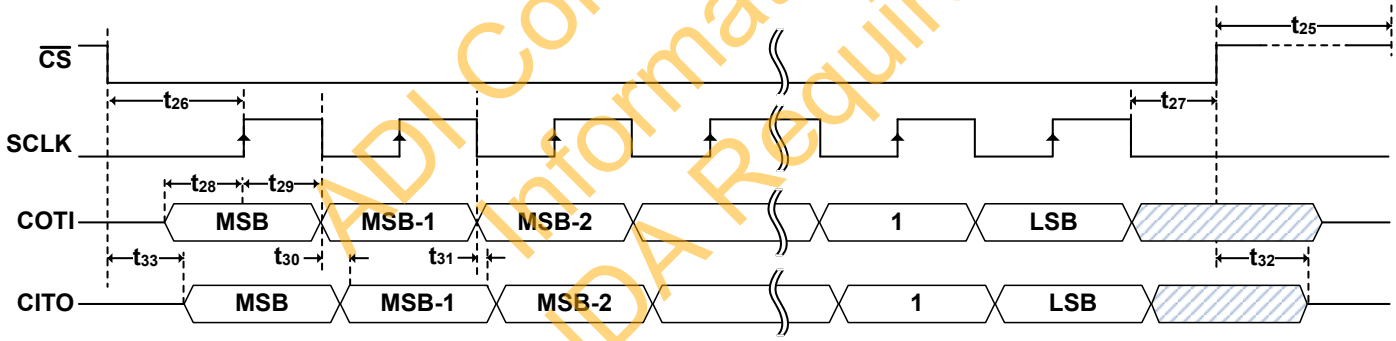

Figure 4. OPEN Alliance 10BASE-T1x MAC-PHY Serial Interface Timing

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SAIF I/O TIMING SPECIFICATIONS

Note: All output timings are derived from an internal 100 MHz clock (10 ns period). Accuracy of output timings is optimized using periods or bit times being a multiple of 10 ns.

Note: Higher frequencies may require the highest drive strength setting depending on the system design.

SAIF Interfaces Timing Specifications

Table 5. SAIF Timing Specifications

Parameter	Symbol	Conditions / Comments	Min	Typ	Max	Unit
TS_CAPT						
Pulse Width			80			ns
TS_TIMER						
Period			32		8,589,934,560	ns
Period Error[1]				0		ns
Jitter Error[2]			-2		2	ns
Jitter Error[3]			-12		12	ns
Jitter Error[4]			-25		25	ns
SAIF = UART		SAIF[11:0] configured for UART interface (UART_RX and UART_TX)				
Baud Rate			600		6250000	bps
Baud Rate Error		For standard baud rates in the supported range up to 921600 bps	-1		1	%
Baud Rate Error		For standard baud rates above 921600 bps	-2		2	%
SAIF = PWM		SAIF[11:0] configured for pulse width modulation interface (PWM[11:0])				
Frequency Range			0.1		$1.0x10^6$	Hz
Frequency Accuracy				2000	15000	ppm
Frequency Jitter				3000	15000	ppm
Duty Cycle			0		100	%
Duty Cycle Resolution				0.78125		%
Duty Cycle Accuracy				4000	15000	ppm
Duty Cycle Jitter				3000	15000	ppm
SAIF = Clock Generator		SAIF[11:0] configured for clock generation mode				
Frequency Range		Fixed frequencies from look-up table	0.25		25	MHz
Frequency Accuracy				10	200	ppm
Frequency Jitter					1	ns
Duty Cycle			45/55	50/50	55/45	%
SAIF = LIN Controller		SAIF[11:0] configured for LIN interface (LIN_EN, LIN_TXD, LIN_RXD)				
Bit Rate			1		20	kbps
SAIF = ISELED / ILaS[5]		SAIF[11:0] configured for INOVA Semiconductors compatible ISELED or ILaS interface				
Bit Width (Downstream)	t_{BW_DS}			500		ns
Bit Width (Upstream)	t_{BW_US}		384		714	ns

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Table 5. SAIF Timing Specifications (Continued)

Parameter	Symbol	Conditions / Comments	Min	Typ	Max	Unit
Frame Downstream	t_{Frame}	CRC enabled		80 x t_{BW}		
		CRC disabled		70 x t_{BW}		
Frame Synchronization	t_{Frame_S}			15 x t_{BW}		
Frequency Synchronization	t_{Freq_S}			5 x t_{BW}		
Service Data Unit Downstream	t_{SDU}			50 x t_{BW}		

[1] Linked to gPTP grandmaster clock when gPTP functionality is used.

[2] TS_TIMER_HI + TS_TIMER_LO Period = Multiples of 80 ns. For example 80 ns, 160 ns, 240 ns.

[3] TS_TIMER_HI + TS_TIMER_LO Period = Multiples of 32 ns.

[4] TS_TIMER_HI + TS_TIMER_LO Period - QE_CORR = All other integer values which are non-multiples of 32 ns or 80 ns.

[5] Only available on AD3304/5 product models.

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SPI Controller Mode Timing Specifications

Note: Clock switching characteristics require a period based on a multiple of 10 ns.

Note: Accuracy is improved when using a half-period being a multiple of 10 ns.

Table 6. SPI Controller Mode Timing Specifications

Parameter	Symbol	Conditions / Comments	Min	Typ	Max	Unit
SAIF = SPI Controller		SAIF[11:0] configured for SPI Controller Mode (SCLK, $\overline{CS}$n[1], COTI and CITO)				
Timing Requirements						
Data Input Setup Time Before SCLK Edge	t_{DSU}	DVDDIO = 3.3 V	5			ns
Data Input Hold Time After SCLK Edge	t_{DHD}	DVDDIO = 3.3 V	10			ns
Switching Characteristics						
SCLK Frequency	f_{SCLK}		0.1		20	MHz
CS Setup Time Before SCLK Edge	t_{CS}		See [2]			ns
CS Hold Time After SCLK Edge	t_{SFS}		See [3]		See [4]	ns
LOW Period of the SCLK[5]	t_{SL}		18.5			ns
HIGH Period of the SCLK[5]	t_{SH}		18.5			ns
Data Output Valid After SCLK Edge	t_{DAV}			±8		ns
Data Output Setup Time Before SCLK Edge	t_{DOSU}			0		ns
Data Output Fall Time	t_{DF}				2.5	ns
Data Output Rise Time	t_{DR}				2.5	ns
SCLK Rise Time	t_{SR}				2.4	ns
SCLK Fall Time	t_{SF}				2.4	ns

1 n = up to 8, default: active low, polarity configurable.

2 $(CSB\_TO\_SCLK - 1) \times BAUD\_RATE\_PERIOD$.

3 $(INTERBYTE\_SPACING \times 10ns) + ((SCLK\_TO\_CSB - 1) \times BAUD\_RATE\_PERIOD)$.

4 $(INTERBYTE\_SPACING \times 10ns) + \left(ceil\left({}^{550ns}/_{BAUD\_RATE\_PERIOD}\right) \times BAUD\_RATE\_PERIOD\right)$.

5 The final SCLK period in a SPI transaction may be substantially longer than nominally expected.

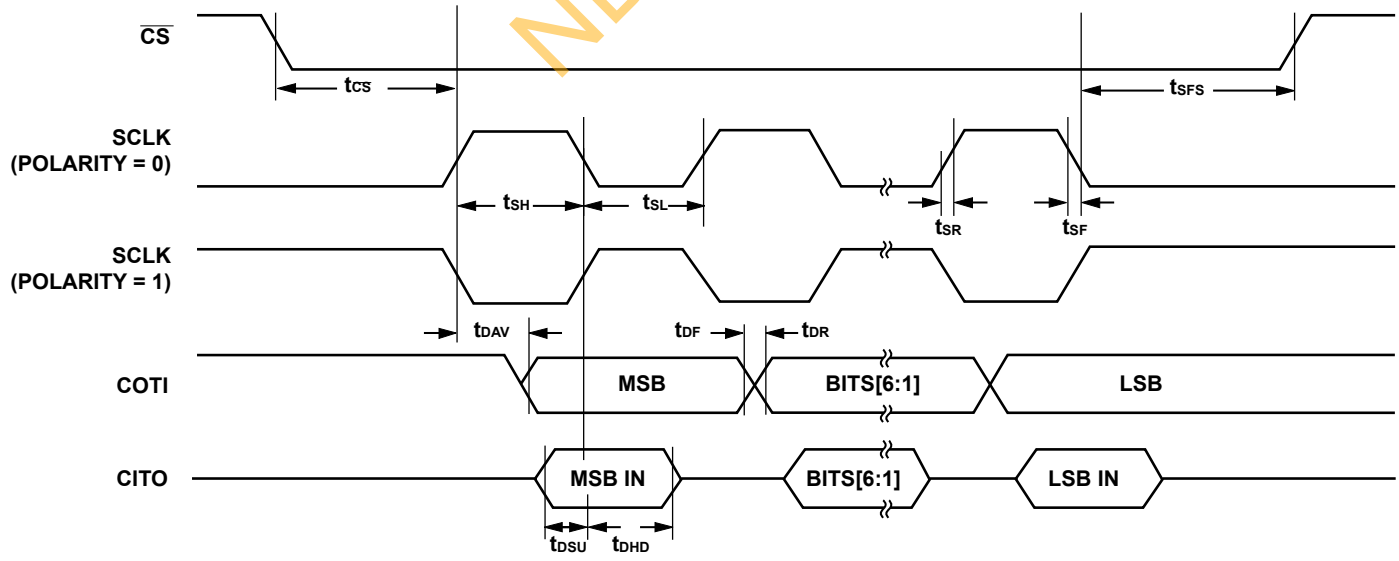


Figure 5. SPI Controller Mode Timing (Phase Mode = 1)

SPECIFICATIONS

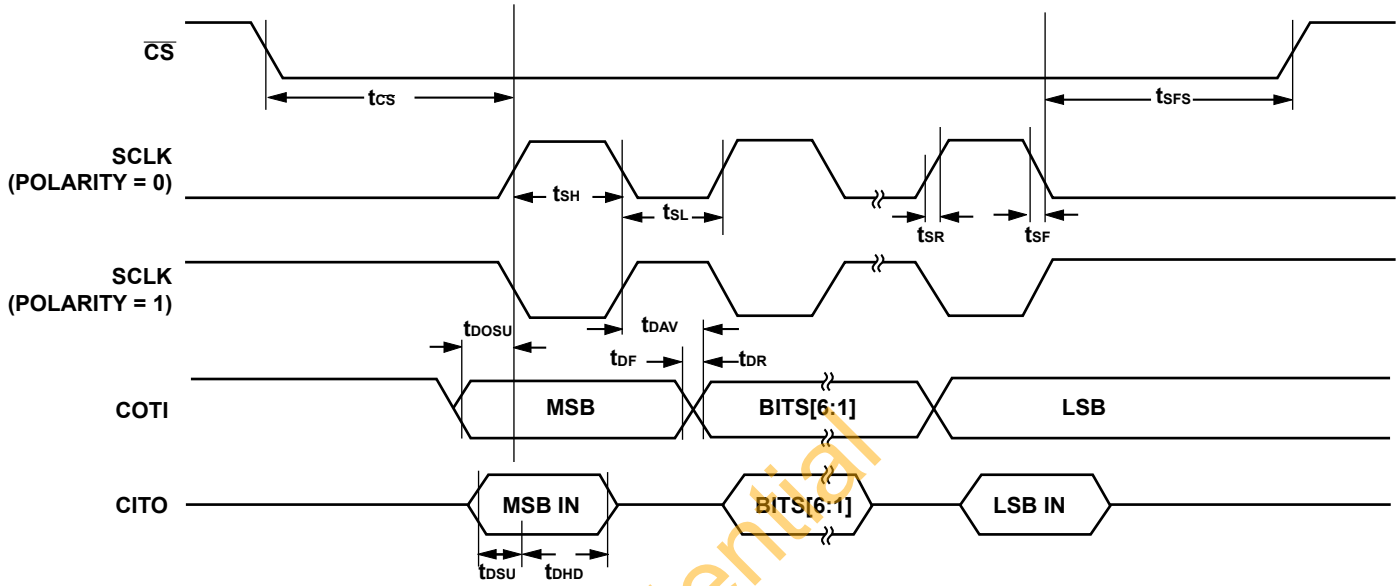


Figure 6. SPI Controller Mode Timing (Phase Mode = 0)

SPECIFICATIONS

I²C Controller Mode Timing Specifications

Table 7. I²C Controller Mode Timing Specifications

Parameter	Symbol	Conditions / Comments	Standard Mode		Fast Mode		Fast Mode Plus		Unit
			Min	Max	Min	Max	Min	Max	
SAIF = I²C Controller[1]		SAIF[10:9] configured for I²C Controller Mode (SDA and SCL). Drive-strength = 20 mA, and DVDDIO = 3.3 V required							
Serial Clock (SCL) Frequency	f_{SCL}		0	100	0	400	0	1000	kHz
Hold Time (Repeated) START Condition	$t_{HD;STA}$	After this period, the first clock pulse is generated	4.0		0.6		0.26		µs
LOW Period of SCL	t_{LOW}		4.7		1.3		0.5		µs
HIGH Period of SCL	t_{HIGH}		4.0		0.6		0.26		µs
Set-up Time for a Repeated START Condition	$t_{SU;STA}$		3.25		0.6		0.26		µs
Data Hold Time	$t_{HD;DAT}$		0		0		0		µs
Data Set-up Time	$t_{SU;DAT}$		250		100		50		ns
Rise Time of Both SDA and SCL Signals	t_r[2]		105	1000	105	300	105	120	ns
Fall Time of Both SDA and SCL Signals	t_f			300		300		120	ns
Set-up Time for STOP Condition	$t_{SU;STO}$		2.9		0.37		0.23		µs
Bus Free Time Between a STOP and START Condition	t_{BUF}		4.7		1.3		0.5		µs
Data Valid Time	$t_{VD;DAT}$			3.45		0.9		0.45	µs
Data Valid Acknowledge Time	$t_{VD;ACK}$			3.45		0.9		0.45	µs

[1] Clock stretching is not supported after the ACK-bit and immediately before STOP condition.

[2] Minimum rise time must be guaranteed by system implementation considering pull-up resistors and bus capacitance: $t_r = 0.8473 \times (C_b \times R_p)$.

SPECIFICATIONS

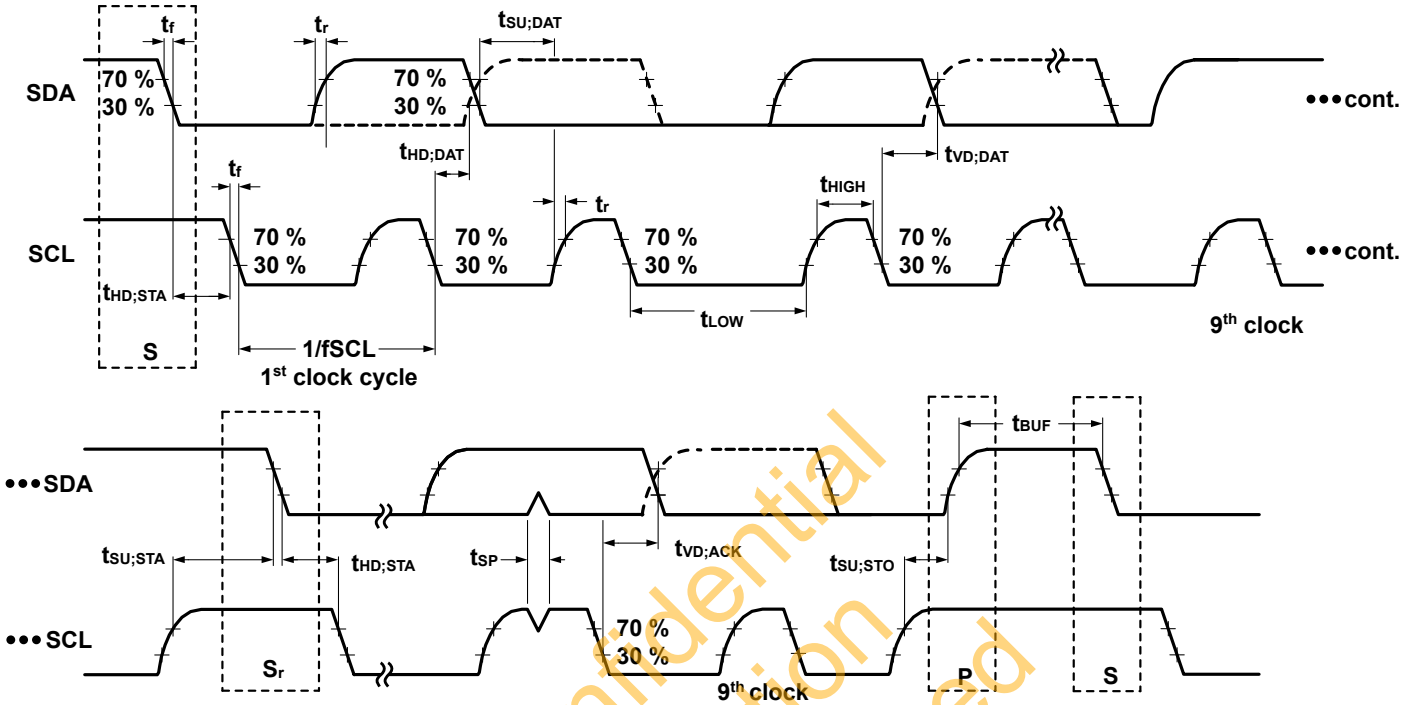


Figure 7. I²C Controller Mode Timing

SPECIFICATIONS

SYSTEM SPECIFICATIONS

Table 8. System Specifications

Parameter	System Specification
System EMI/EMC	Meets or exceeds industry specifications for robustness (ISO 11452-2, ISO 11452-4, ISO 7637-3, ISO7637-2, SAEJ2962-3) and emissions (CISPR25, SAEJ2962-3)
System ESD Rating	Meets ISO 10605 severity levels (±12 kV) on the 10BASE-T1S interface without any external ESD protection

ABSOLUTE MAXIMUM RATINGS

Table 9. Tolerant Voltage on Digital I/O Pins for Different Power Supplies

Voltage	Minimum DVDDIO	Maximum digital I/O voltage
3.3 V operation	2.97 V	5.5 V
	0 V	3.63 V
2.5 V operation	2.25 V	5.5 V
	0 V	3.63 V
1.8 V operation[1]	1.62 V	4.5 V
	0 V	3.63 V

[1] Not tolerant to 5 V input voltage.

Table 10. Absolute Maximum Ratings

Parameter	Rating
DVDDIO to GND	3.63 V
AVDD to GND	5.5 V
VBAT to GND	70 V
WAKE to GND	70 V
XTAL_I/CLKIN to GND	-0.3 V to +1.8 V
XTAL_O to GND	-0.3 V to +1.35 V
ETH_P/ETH_N (Common Mode)[1]	±20 V
Storage temperature range	−60°C to +150°C
Solder reflow, per JEDEC J-STD-020	260°C
Junction temperature while biased	−40°C to +150°C

[1] Maximum ETH_P/ETH_N receiver common mode DC offset. The ETH_P/ETH_N transmitter should not be enabled if driving into a low impedance DC load. This can result in device damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to the printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

The thermal characteristics provided in this section are provided for package comparison and estimation purposes only. They are not intended for accurate system temperature calculation. Thermal simulation is required for accurate temperature analysis that accounts for all the impacts of each specific 3D system design, including, but not limited to other heat sources, the use of heat-sinks, and the system enclosure.

Thermal data is generated according to the JEDEC JESD51 series of specifications:

- θ_{JA} is the junction to ambient thermal resistance in natural convection.
- θ_{JMA} is the junction to ambient thermal resistance in moving air.
- θ_{JB} is the junction to board thermal resistance.
- θ_{JC} is the junction to case thermal resistance.
- Ψ_{JT} is the junction to top thermal characterization parameter.
- Ψ_{JB} is the junction to board thermal characterization parameter.

Table 11. Thermal Resistance

Parameter	Unit	Air flow conditions			
		No airflow	1 m/s	2 m/s	3 m/s
θ_{JA}	(°C/W)	70.8 [1]	56.1 [4]	53.6 [4]	52.0 [4]
Ψ_{JT}[1]	(°C/W)	2.4	-	-	-
Ψ_{JB}[1]	(°C/W)	37.6	-	-	-
θ_{JB}[2]	(°C/W)	38.9	-	-	-
θ_{JC}[3]	(°C/W)	51.7	-	-	-

1. Simulated data based on JEDEC 2s2p thermal test board with 4 thermal vias under the exposed paddle in a JEDEC Natural Convection environment.
2. Simulated data based on JEDEC 2s2p thermal test board with 4 thermal vias under the exposed paddle in a JEDEC Junction To Board environment.
3. Simulated using a JEDEC 1s thermal test board with a cold plate attached to the package top and measured at the package top surface.
4. Simulated data based on JEDEC 2s2p thermal test board with 4 thermal vias under the exposed paddle in a JEDEC Forced Convection environment.

When using the device, the T_{JMAX} must not go above 150°C. The following equation calculates the junction temperature using the measured package surface temperature and applies only when not using a heat sink on the DUT:

$$T_J = T_S + (\Psi_{JT} \times W_{TOTAL}).$$

Where: T_J is the junction temperature of the DUT. T_S is the package surface temperature (°C). W_{TOTAL} is the total power consumption of the DUT.

$$W_{TOTAL} = ((\text{VBAT} \times I_{VBAT}) + (DVDDIO \times I_{DVDDIO}) + (\text{AVDD} \times I_{AVDD}).$$

Values of θ_{JA} are provided for package comparison and PCB design considerations. Use θ_{JA} for a first-order approximation of T_J by the following equation:

$$TJ = T_A + (\theta JA \times W_{TOTAL}).$$

Where T_A = ambient temperature (°C).

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD-protected area only. Human body model (HBM) ratings are per ANSI/ESDA/ JEDEC JS-001.

ABSOLUTE MAXIMUM RATINGS

Field induced charged device model (FICDM) ratings are per ANSI/ESDA/JEDEC JS-002.

Table 12. AD3300/AD3301/AD3304/AD3305, 24-lead [LFCSP] – ETH_P, ETH_N pins

ESD Model	Withstand Threshold (V)	Class
HBM[1]	±8 k	2

[1] HBM level is relative to GND paddle reference.

Table 13. AD3300/AD3301/AD3304/AD3305, 24-lead [LFCSP]

ESD Model	Withstand Threshold (V)	Class
HBM	±2.5 k	2
FICDM	±500	C2a

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

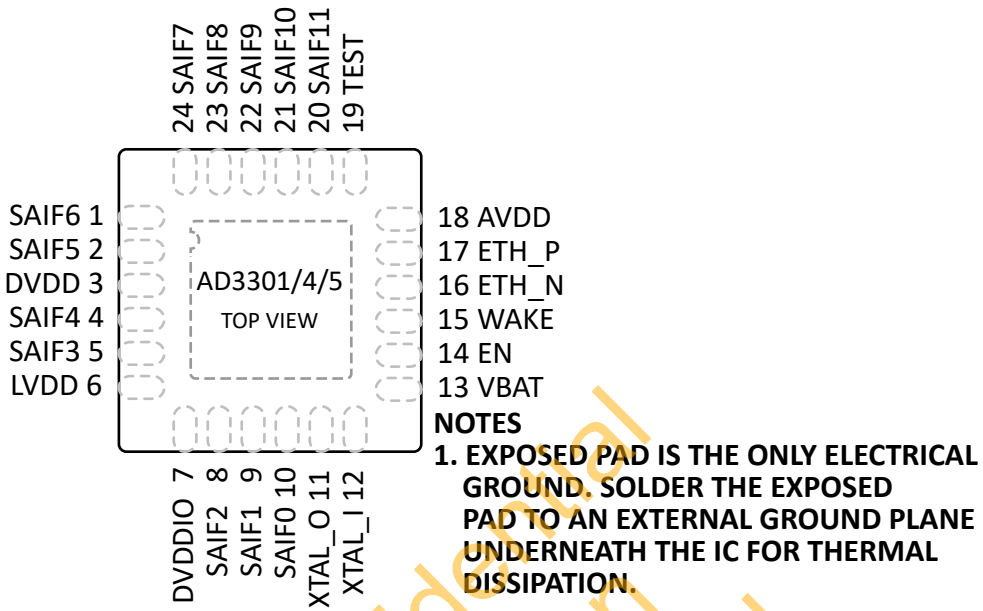


Figure 8. AD3301/4/5 Pin Configuration

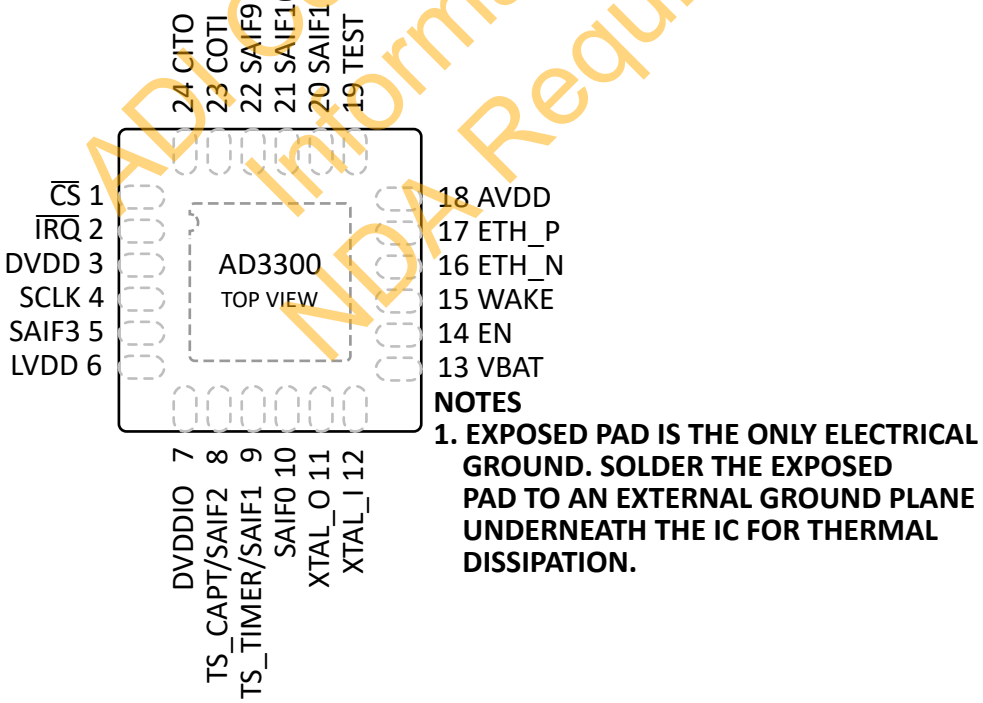


Figure 9. AD3300 Dual Mode Pin Configuration

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 14. AD3300/AD3301/AD3304/AD3305 Pin Function Descriptions

Pin No	Mnemonic	Type	Description
1	SAIF6/$\overline{CS}$	Digital input/output	Multipurpose input/output pin used for the sensor/actuator interface. Also serves as SPI chip select ($\overline{CS}$) input (active low) when OA-SPI interface is enabled.[1] **Note:** Optional: 10 kΩ pull-up resistor.
2	SAIF5/$\overline{IRQ}$	Digital input/output	Multipurpose input/output pin used for the sensor/actuator interface. Also serves as interrupt output when OA-SPI interface is enabled.[1]
3	DVDD	Power	Decoupling for the internally generated digital core power supply (1.1 V). Requires a 10 nF and 1 µF decoupling capacitor.
4	SAIF4/SCLK	Digital input/output	Multipurpose input/output pin used for the sensor/actuator interface. Also serves as SPI serial clock (SCLK) input when OA-SPI interface is enabled.[1] **Note:** Optional: 10 kΩ pull-down resistor.
5	SAIF3	Digital input/output	Multipurpose input/output pin used for the sensor/actuator interface.
6	LVDD	Power	Decoupling for the internally generated 3.3 V, regulated from AVDD, and used to power the analog logic. LVDD can be used to drive DVDDIO at 3.3 V and / or to source an off-chip supply if desired. The DC current in total (DVDDIO + off-chip) that can be supplied from this pin is 10 mA. Requires a 100 nF and 2.2 µF decoupling capacitor.
7	DVDDIO	Power	Separate supply for the I/O circuitry, to allow the digital I/O level to be controlled as suits the application. It can run from 1.8 V to 3.3 V. Requires a 100 nF and 4.7 µF decoupling capacitor.
8	SAIF2/ TS_CAPT	Digital input/output	Multipurpose input/output pin used for the sensor/actuator interface. Also serves as input for the synchronized timer to trigger the capture of a timestamp when OA-SPI interface is enabled (optional).[1] DNC when not used.
9	SAIF1/ TS_TIMER	Digital input/output	Multipurpose input/output pin used for the sensor/actuator interface. Also serves as the output of the synchronized timer when OA-SPI interface is enabled (optional).[1] DNC when not used.
10	SAIF0	Digital input/output	Multipurpose input/output pin used for the sensor/actuator interface.
11	XTAL_O	Analog output	Crystal amplifier (25 MHz) output pin.
12	XTAL_I	Analog input	Crystal amplifier (25 MHz) input pin. Direct clock reference (25 MHz) input pin.
13	VBAT	Power	Supply input for the always-on domain. It can connect to 5 V or battery supply. Requires a filter network (100 Ω resistor and 10 µF capacitor) that prevents damage or malfunction during electrical events or electrical event testing. An additional 100 nF capacitor can be used for improved noise immunity.
14	EN	Digital output	An output pin is asserted when the 10BASE-T1S transceiver is in an Awake mode (see Operating Modes); it can be used as an active-high enable or an active-low inhibit. For example, for an external DC/DC regulator generating the AVDD supply. Always driven, DNC or connect to a test point when not used. **Note:** It is not recommended to pull this pin to GND using a resistor. Ensure load not exceeding the driving capability of this pin (see Table 2).
15	WAKE	Digital input	Input that can be used for an external device to trigger the 10BASE-T1S transceiver to exit the sleep mode. WAKE is triggered by a positive edge > 1 V. Default: disabled. **Note:** Optional: 10 kΩ pull-down resistor. Do not leave floating/unconnected. Short to GND when not used. When connecting externally (off-PCB), the pin will need an off-chip filter for EMI protection).
16	ETH_N	Analog input/output	10BASE-T1S negative differential pin. **Note:** Differential signal, symmetric design.
17	ETH_P	Analog input/output	10BASE-T1S positive differential pin. **Note:** Same as ETH_N.
18	AVDD	Power	5 V supply input; it can be powered off when the 10BASE-T1S transceiver is not in an Awake mode (see Operating Modes) to save power. Requires a 100 nF and 4.7 µF decoupling capacitor.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 14. AD3300/AD3301/AD3304/AD3305 Pin Function Descriptions (Continued)

Pin No	Mnemonic	Type	Description
19	TEST	Digital input	Short to GND. **Note:** Do not leave floating/unconnected.
20	SAIF11	Digital input/output	Multipurpose input/output pin used for sensor/actuator interface.
21	SAIF10	Digital input/output	Multipurpose input/output pin used for sensor/actuator interface. Pull pin high or low with an external resistor to set bit3 of the MAC address and/or PLCA ID[2]. Pin level must remain steady until the initial SW configuration is complete and the MAC address and/or PLCA ID is stored. Supports true open drain functionality (increased drive strength and inbuilt I^2C glitch filter on the input side) for I^2C compatibility. **Note:** Add weak pulling resistors to enable override, for example,100 kΩ.
22	SAIF9	Digital input/output	Multipurpose input/output pin used for sensor/actuator interface. Pull pin high or low with an external resistor to set bit2 of the MAC address and/or PLCA ID[2]. Pin level must remain steady until the initial SW configuration is complete and the MAC address and/or PLCA ID is stored. **Note:** Add weak pulling resistors to enable override, for example, 100 kΩ. Supports true open drain functionality (increased drive strength and inbuilt I^2C glitch filter on the input side) for I^2C compatibility.
23	SAIF8/COTI	Digital input/output	Multipurpose input/output pin used for sensor/actuator interface. Pull pin high or low with an external resistor to set bit1 of the MAC address and/or PLCA ID[2]. Pin level must remain steady until the initial SW configuration is complete and the MAC address and/or PLCA ID is stored. **Note:** Add weak pulling resistors to enable override, for example, 100 kΩ. Also serves as SPI COTI (controller output target input) signal when OA-SPI interface is enabled.[1] **Note:** Optional: 10 kΩ pull-down resistor.
24	SAIF7/CITO	Digital input/output	Multipurpose input/output pin used for sensor/actuator interface. Pull pin high or low with an external resistor to set bit0 of the MAC address and/or PLCA ID[2]. Pin level must remain steady until the initial software configuration is complete and the MAC address and/or PLCA ID is stored. **Note:** Add weak pulling resistors to enable override, for example, 100 kΩ. Also serves as SPI CITO (controller input target output) signal when OA-SPI interface is enabled.[1] **Note:** Optional: 33 Ω series resistor at the source side of the signal.
EXP_PAD	GND	Ground	Exposed paddle. Connect to ground.

Any SAIF can be left unconnected. The pins are three-stated when not enabled in pin multiplexing.

All other pins must be connected as per the description.

[1] AD3300 only

[2] The 4 LSBs of the PLCA ID is determined by sampling those pins and then providing the value using a look-up table (LUT). By default (unprogrammed OTP), the PLCA ID's are 1:1 (matching the MAC address LSBs). If a different PLCA ID mapping is needed, the OTP LUT must be programmed accordingly.

The following sections provide information on typical power configurations as well as board layout guidelines.

POWER CONFIGURATIONS

There are two power configurations to consider for the AD3300/AD3301/AD3304/AD3305 transceiver: battery power and 5 V power.

In the battery power configuration, the following attributes must be considered:

- Application of UVLO and OVLO thresholds are disabled by default from boot.
- UVLO and OVLO thresholds can be programmed into OTP for end use and applied upon boot.
- The battery supply feeds the VBAT pin of AD3300/AD3301/AD3304/AD3305 and powers the DC/DC regulator.
- AD3300/AD3301/AD3304/AD3305 always-on domain is kept powered via the VBAT pin.
- Always-on domain enables sleep/wake-up functions.
- AD3300/AD3301/AD3304/AD3305 can monitor the VBAT voltage level for over voltage (OV) and under voltage (UV) events.
- AD3300/AD3301/AD3304/AD3305 can decide whether or not to enter the sleep mode thereby disabling the DC/DC regulator 5 V output.

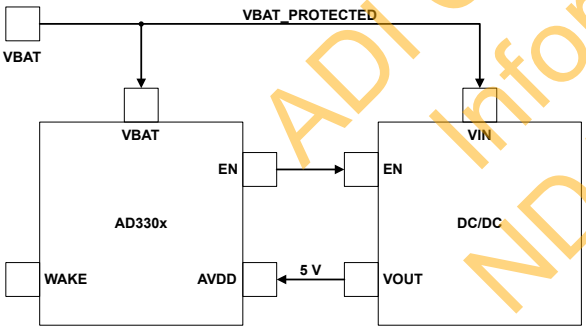


Figure 10. Battery Power Configuration

In the 5 V power configuration figure, the 5 V rail feeds both the VBAT and AVDD pins. VBAT monitoring is not supported.

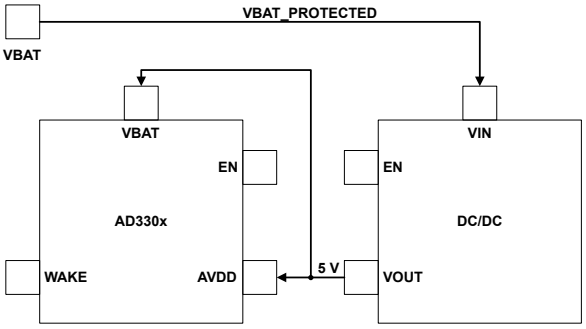


Figure 11. 5 V Power Configuration

LAYOUT GUIDELINES

The layout of the AD3300/AD3301/AD3304/AD3305 10BASE-T1S transceiver devices must be executed in line with the following specific requirements. These requirements are critical for systems aiming to achieve compliance with automotive EMC standards. Further to these specific requirements, best layout practices should always be followed. The following figure shows the placement of the 10BASE-T1S network components like the common-mode choke and AC-coupling capacitors.

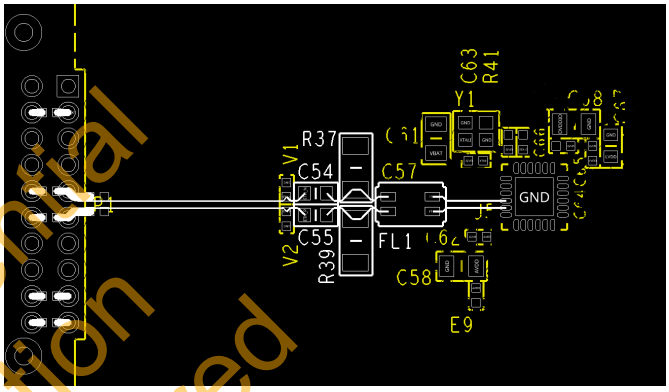


Figure 12. T1S Termination Network and Connectors, Combined View

10BASE-T1S Connector Pinout Guidelines

The following points should be considered for the 10BASE-T1S connector pinout:

- The connector pitch (distance between the pair of pins) should be between 2 mm and 4 mm. A higher pitch than 4 mm and / or additional untwist of the cable causes high impedance mismatch.
- Spare pins around Ethernet pins are recommended; at least one pin on both sides.
- If power/ground wire to the node is also on the same row, it is recommended to place those wires at least 2-pins away.
- On two-row connectors, the pins under ETH pair can be another ETH pair (for example daisy-chain).
- Another balanced differential bus can also be used.
- Do not connect single-ended signals on these pins (for example ground, power or LIN).
- In the case of daisy chain implementation at the connector level for the same Ethernet PHY, vertical cascading is recommended.
- Immediate adjacent horizontal cascading of 2-pairs should be avoided, this will lead to imbalance and asymmetry. When not possible otherwise, one-pin spacing should be respected, maintaining symmetry.
- In case of two Ethernet PHYs on the same ECU, two Ethernet signal pairs can be cascaded vertically, below each other. If placed horizontally, it is recommended to have one empty pin between the Ethernet signal pairs.

DESIGNER REFERENCE

- There should not be any flooding/pours (ground, power or other) in the area of the connector pin courtyard. This rule is applicable for all layers, if the connector is a through-hole part.
- Track/trace the signals Ethernet P, Ethernet N, power, and ground, but no flooding is wanted.
- AD3300/AD3301/AD3304/AD3305 reference hardware uses a through hole NanoMQS connector by TE. The connector choice should consider RF parameters effecting the link segment: CIDM, Intra pair skew, Insertion Loss, Return Loss, LCL, LCTL, ANEXT, AFEXT. The 10BASE-T1S System Implementation Specification and the IEEE Std 802.3-2022 Specification refers to ECU connectors for 10BASE-T1S interfaces.

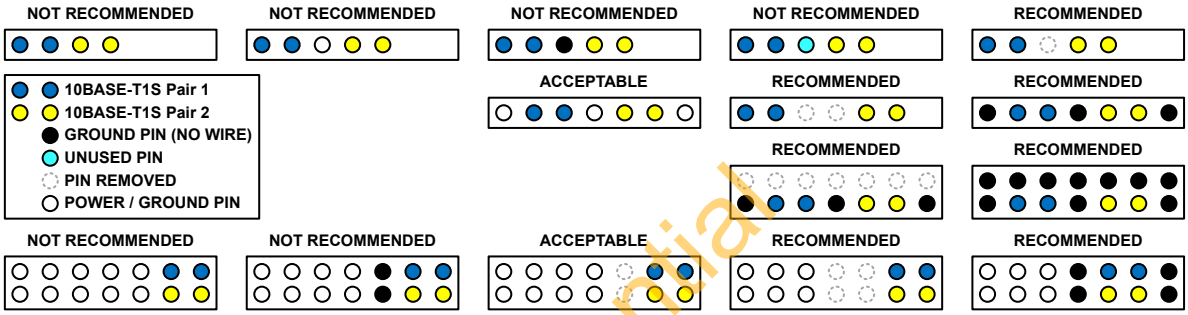


Figure 13. Connector Pinout Guidelines Summary Diagram

Passive Device Placement and Layout

Place decoupling capacitors for any power pin on the same side of the PCB as the transceiver with the smaller capacitor closest to the respective pin. The following figure shows the placement of the AD3300/AD3301/AD3304/AD3305 power decoupling components.

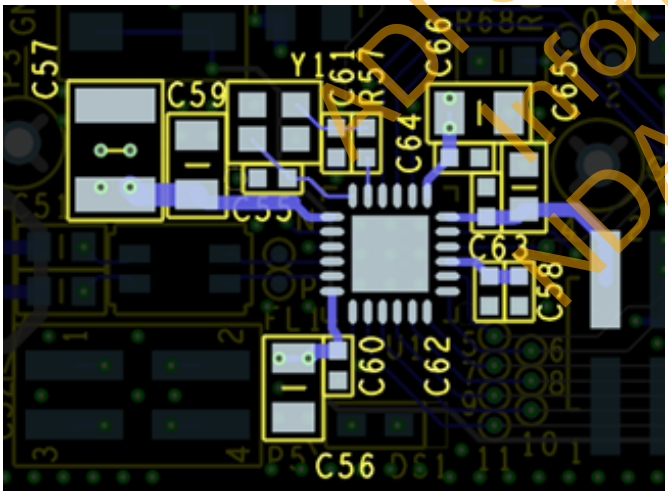


Figure 14. Power decoupling components

Common-Mode Choke Parasitic Capacitance

The following points should be considered for the board design:

- Refer to Open Alliance CMC specification
- The parasitic capacitance between the common mode choke and adjacent ground planes must be minimized to ensure that the common-mode choke rejects common-mode noise across the specified frequency range.
- High speed layout techniques should be used to minimize the parasitic capacitance of the landing pads and the choke's body to the ground plane below the component.
- Minimizing parasitic capacitance supports the goal of maximizing the differential bandwidth with minimum insertion loss.
- Use ground relief in the ground plane underneath the choke for reducing parasitic capacitance to ground.

Power Supply Requirements

For specific power supply values, see the Power Consumption Characteristics. The general rules for managing the power supply are:

- The requirements for the AD3300/AD3301/AD3304/AD3305 power supply pin filtering are found in the Bill of Material (BoM).The passive components (termination resistors and ac-coupling capacitors) must be sized to adequately handle BCI events.
- Ensure that the digital and analog power supplies are isolated to minimize potential coupling paths between the noisy and sensitive power supplies.
- Employ double vias if possible, when connecting AD3300/AD3301/AD3304/AD3305 supplies to minimize the supply inductance. In situations where this is not possible, analog supplies take priority.

General Layout Guidelines

Taking the previously outlined slots into account, take care to ensure the voids in any plane are not large enough to unintentionally disrupt the path for power and/or return currents, on the plane. The following figure shows an example of a situation to avoid.

DESIGNER REFERENCE

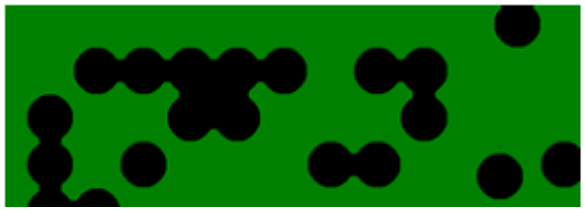


Figure 15. Unintentional Disrupted Power Plane

General Requirements

- The AD3300/AD3301/AD3304/AD3305 contains a common ground thermal exposed pad. The exposed pad must be connected directly to a solid, contiguous ground plane through a thermal via array.
- Carefully consider the return currents for signals on the PCB and simplify their path using techniques such as employing planar capacitors and using stitching vias.

Component Placement Notes

- Ideally, place common mode choke, AC coupling caps and termination on the same side of the PCB as the AD3300/AD3301/AD3304/AD3305 device.
- Keep decoupling caps close and on same the side of the PCB as the AD3300/AD3301/AD3304/AD3305 device.
- Keep crystal resonator close and on the same side of the PCB as the AD3300/AD3301/AD3304/AD3305 device.

DUT Area

- For proper thermal management, the AD3300/AD3301/AD3304/AD3305 device must have its ground paddle connected to a continuous PCB ground plane.
- Use stitching into internal layers to sink heat (9 vias – 3 x 3).

Performance Requirements

- Each single-ended Ethernet signal trace has impedance control of 50 Ω. The preferred option for optimal EMC performance is stripline routing but microstrip routing may also be used. Refer to the Altium Guidelines for more information.

Routing Notes

- Ethernet P and Ethernet N: Reduce stub length as much as possible.
- Ethernet P and Ethernet N: On the trace routing try to minimize single ended and differential capacitance.
- Length match Ethernet P and Ethernet N. Try not to introduce imbalance in length and also imbalance in coupling to neighboring nets/potentials. To match the trace lengths, different routing techniques can be used. It is recommended to apply those techniques on the same end of the length-matched pair.
- Match any vias in the signal route with the same impedance of the signal line. Typical target 50 Ω impedance.
- When placing signal vias, it is recommended to place ground, or return, vias close by in order to provide a short path to ground.

Plane Notes

- AD3300/AD3301/AD3304/AD3305 reference hardware has implemented a copper ground plane void underneath the common mode choke (three layers deep).
- The internal ground layer reference immediately below the common-mode choke which is on an external layer should have an area of ground cut-out that matches the dimension of the courtyard of the common-mode choke.

ELECTROMAGNETIC COMPATIBILITY (EMC)

This section provides information on EMC performance.

Information on the exact testing methods and results are available in a comprehensive EMC report, which is available on request from a local Analog Devices sales team or Analog Devices sales office. The transceiver features that influence the EMC performance are listed below.

Table 15. Device Features for EMC Performance

Block	Emissions Aid	Immunity Aid
Differential signaling	Yes	Yes
10BASE-T1S link encoding	Yes	Yes
Termination scheme:		
Common-mode choke	Yes	Yes
On-chip ESD protection	No	Yes

POWER SUPPLY REQUIREMENTS

OPERATING MODES

The operating modes of the AD3300/AD3301/AD3304/AD3305 are the always-on reset (initial state), awake (reset, normal, and standby), sleep, and lockout.

Always-on reset mode is triggered when VBAT reset threshold is asserted. The IC is in reset in always-on reset mode.

In reset mode all circuitry is in a power down or reset state apart from the always-on circuitry. Reset mode is the initial awake state. In this mode all SAIF are in tri-state.

Normal mode is the default mode of operation. The AD3300/AD3301/AD3304/AD3305 is fully functional in this mode, able to activate any functional feature and to interact with all interfaces connected to it.

Standby mode keeps the AD3300/AD3301/AD3304/AD3305 awake with all circuitry powered but biased for low activity. The benefit versus sleep mode is much faster boot time to normal mode.

Sleep mode is a very low power state. Only the always-on circuitry, including the sleep/wake-up controller, is powered.

Lockout mode is reached when UVLO or OVLO VBAT thresholds are asserted. This mode puts the AD3300/AD3301/AD3304/AD3305 in a low power state, regardless of the awake mode the AD3300/AD3301/AD3304/AD3305 is in. Once the UVLO or OVLO condition has been de-asserted, the AD3300/AD3301/AD3304/AD3305 returns to the awake mode initial state of reset. If during lockout mode, the VBAT RESET threshold is asserted, this will put the AD3300/AD3301/AD3304/AD3305 in always-on reset mode. The wake-up controller is not active in lockout mode.

Note: The EN output pin is asserted when the AD3300/AD3301/AD3304/AD3305 is in an awake mode.

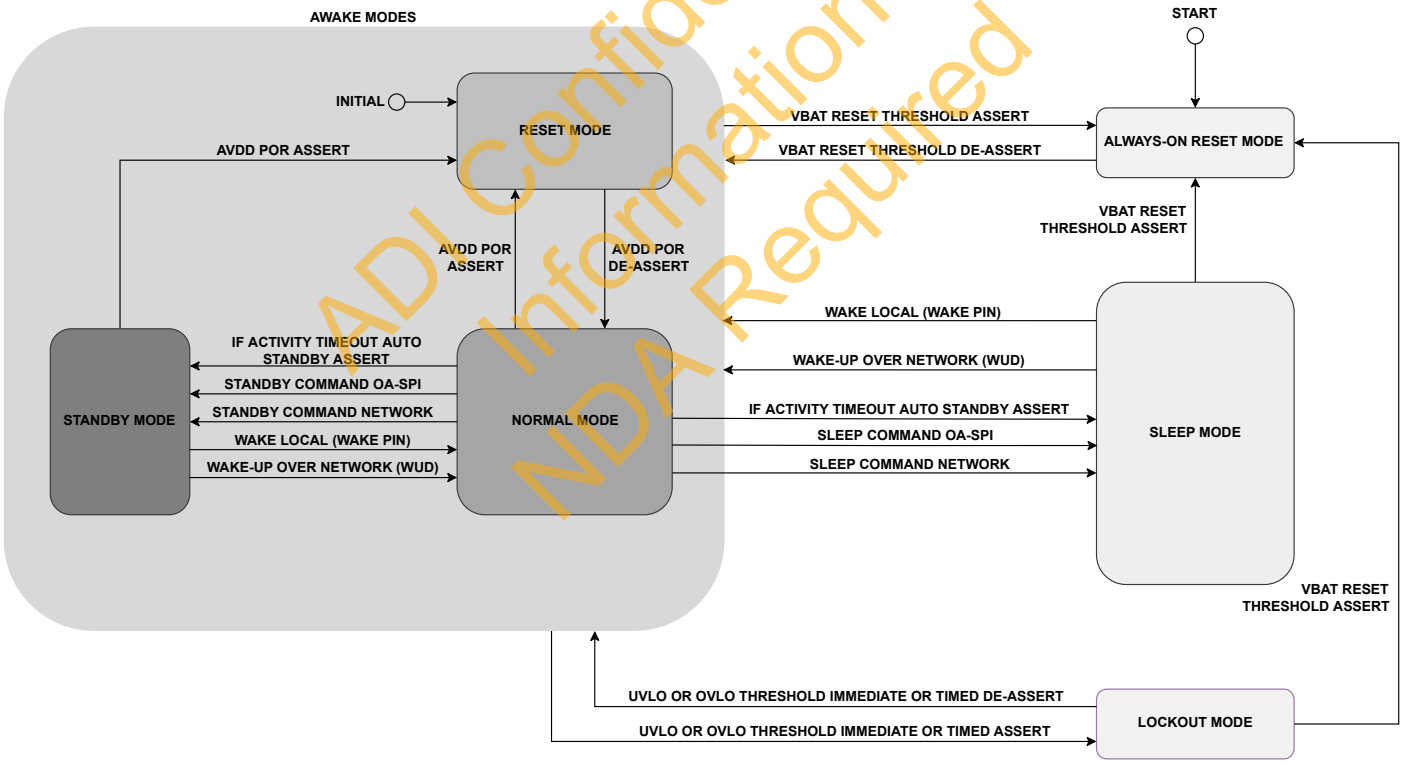


Figure 16. Operating Mode State Diagram

POWER-UP SEQUENCE

There are no power-up sequence requirements between the VBAT, AVDD, and DVDDIO supply when using up to 3.3 V I/O supply.

When using 5 V I/O logic, the DVDDIO supply must be >2.5 V before any 5 V logic signal is driven into the AD3300/AD3301/AD3304/AD3305 device. This also applies to when the DVDDIO supply is being powered from LVDD 3.3 V supply. Failure to do this will exceed the absolute maximum ratings of the AD3300/AD3301/AD3304/AD3305 device.

XTAL_I input must be present no later than 0.5 s after power-on.

POWER SUPPLY REQUIREMENTS

Note: Ensure that AVDD supply can handle 120 mA of in-rush current on start-up.

POWER-DOWN SEQUENCE

There are no power-down sequence requirements between the VBAT, AVDD, and DVDDIO supply. DVDDIO supply must remain >2.5 V as long as 5 V I/O signals are driven into the AD3300/AD3301/AD3304/AD3305 digital inputs.

REMOTE NODE INTERFACES

Table 16 provides the list of the remote node interfaces available on the AD3300/1/4/5. Up to four different serial interfaces can be configured for concurrent operation. Internal multiplexing allows any remote node interface pins to be assigned to any of the twelve sensor/actuator interface pins - SAIF[11:0].

Table 16. Supported Remote Node Interfaces

Remote Node Interface	Number of Interfaces Available	Interface Pin Type	Pin Direction
SPI Controller	1	$\overline{\text{SPI\_CS}}$[1] SPI_SCLK SPI_COTI SPI_CITO SPI_IRQ (Optional)	Output Output Output Input Input
I^2C Controller	1	I2C_SCL I2C_SDA	Output Input/Output
LIN Controller	2	LIN_EN LIN_TXD LIN_RXD	Output Output Input
Port Controller[2]			
GPIO	12	GPIO[11:0]	Input/Output
PWM	12	PWM[11:0]	Output
UART	1	UART_RX UART_TX	Input Output
ADC	1[3]	SAIF[5:0] VBAT[4], DVDDIO, LVDD, DVDD, AVDD[5]	Input Input[6]
Flexible I/O	2	SAIF[11:0]	Input/Output
ISELED or ILaS	2[7] or 4[8]	SIOP SION	Input/Output Input/Output

1 Up to 8 chip select signals supported.

2 The port controller interface supports GPIO, PWM, and fixed clock functions.

3 All SAIF and voltages listed can be monitored simultaneously.

4 Attenuated 20x.

5 Attenuated 3x.

6 Internally routed to ADC.

7 Only available on AD3304/5.

8 Only available on AD3305.

Note: The 10BASE-T1S network throughput may limit the data rate of different interfaces when operating simultaneously.

The list below provides some example configurations of different interface types operating simultaneously:

- Port controller configured for 12x GPIOs = 12x SAIF pins used
- Port controller configured for 3x GPIOs (3 pins) and 2x PWM (2 pins) + 1x LIN (3 pins) + 1x ISELED (2 pins) + I^2C (2 pins) = 12x SAIF pins used
- 1x SPI (4 pins) + 1x LIN (3 pins) + 1x I^2C (2 pins) + 1x ISELED (2 pins) = 11x SAIF pins used
- 1x SPI (4 pins) + 1x LIN (3 pins) + 1x UART (2 pins) = 9x SAIF pins used

TYPICAL CONNECTION DIAGRAMS

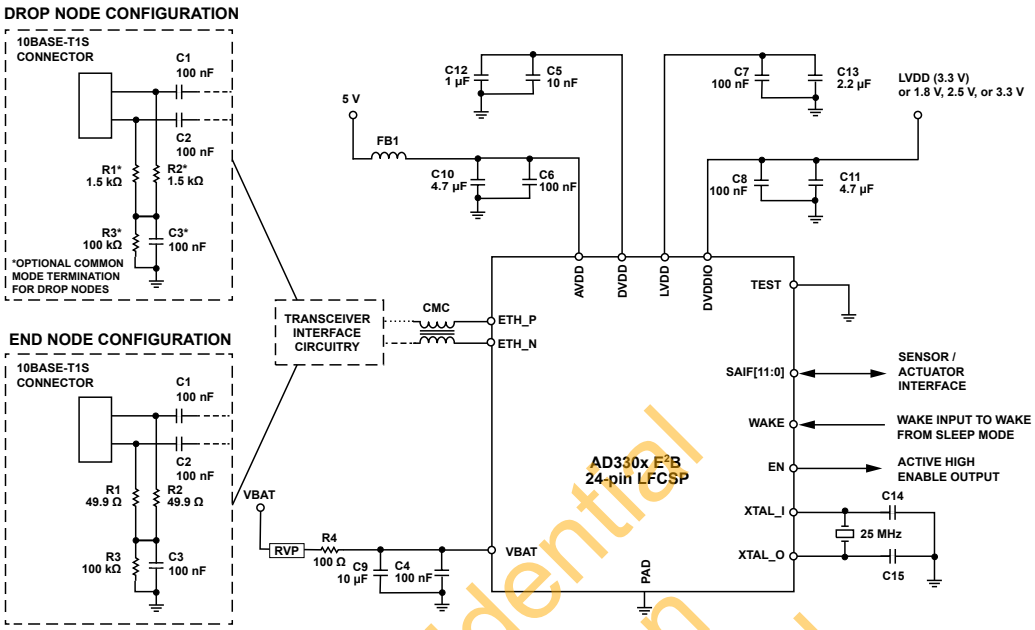


Figure 17. Typical Connection Diagram with 10BASE-T1S in Remote Mode

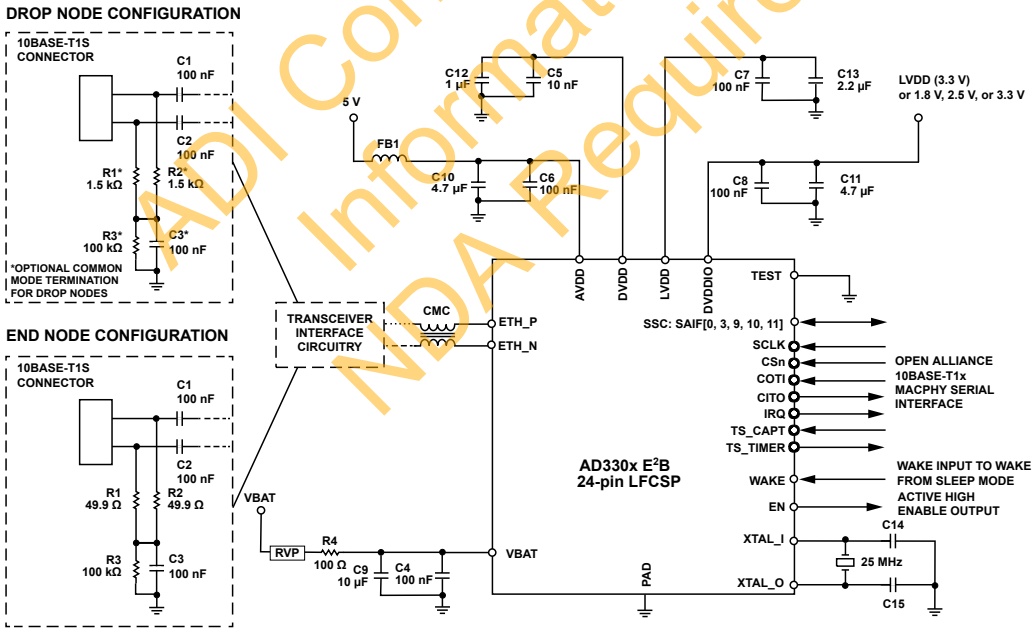


Figure 18. Typical Connection Diagram with 10BASE-T1S in Dual Mode

TYPICAL CONNECTION DIAGRAMS

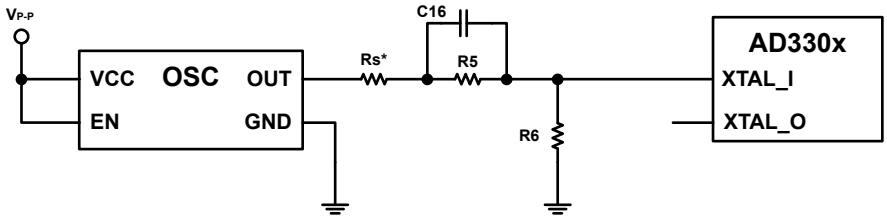


Figure 19. Typical Oscillator Connection Diagram

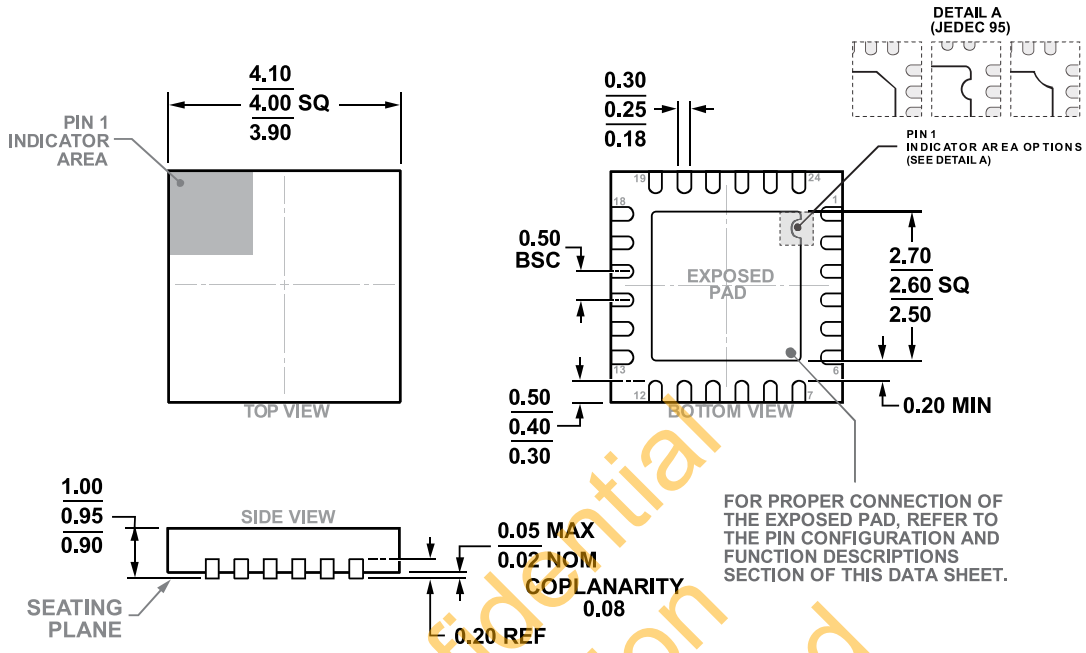
Table 17. Oscillator Circuit Component Selection

Clock V_{P-P}	R5	R6	C16	Rs
3.3 V	3.6 kΩ	1.8 kΩ	5 pF	100 Ω
2.5 V	3.6 kΩ	2.4 kΩ	7 pF	100 Ω
1.8 V	3.6 kΩ	4.5 kΩ	15 pF	100 Ω

Note: Assumes a parasitic input capacitance (PCB + Pin) of ~10 pF.

Note: Rs: Series damping resistor, application specific, recommended value.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-8

Figure 20. 24-lead Lead Frame Chip Scale Package [LFCSP]
4 x 4 mm Body and 0.95 mm Package Height
(CP-24-17)
Dimensions are shown in millimeters

OUTLINE DIMENSIONS

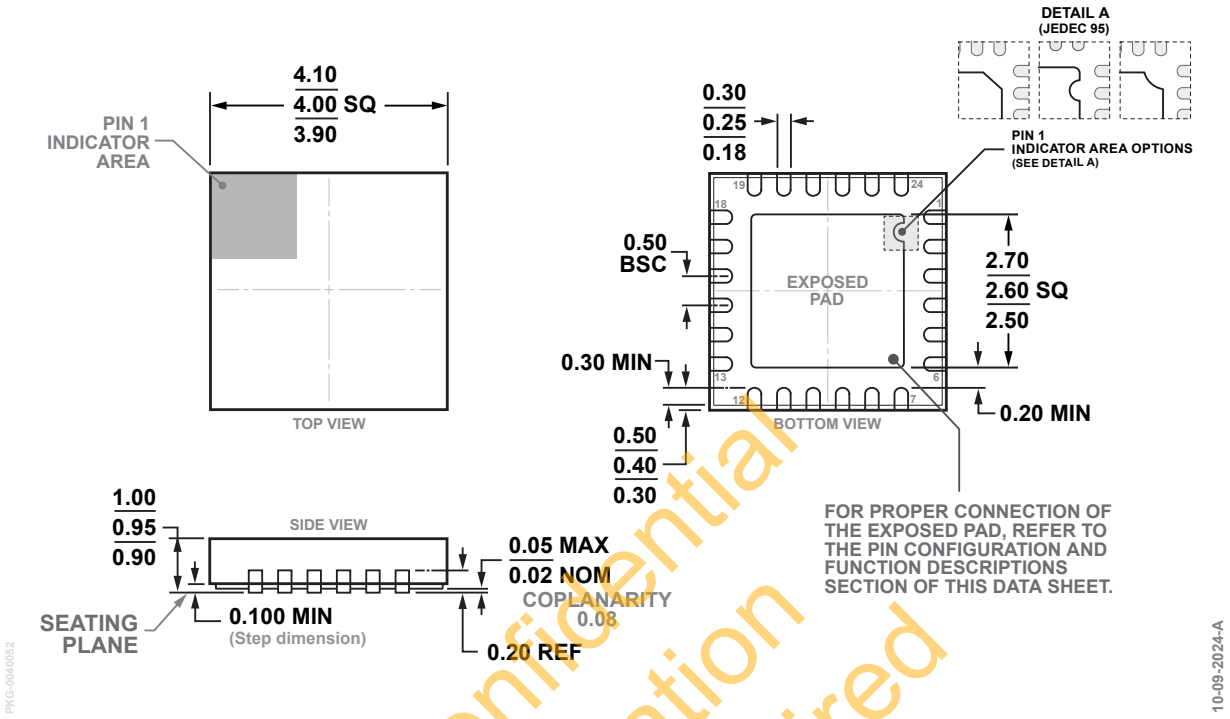


Figure 21. 24-lead Lead Frame Chip Scale Package [LFCSP_SS]
4 x 4 mm Body, With Side Solderable Leads
(CS-24-2)
Dimensions are shown in millimeters

For the latest package outline information and land patterns (footprints), go to Package Index.

AUTOMOTIVE PRODUCTS

All automotive-qualified models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models. Only the automotive-grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information.

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I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

Updated: February 17, 2025

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
AD3300WBCPZ	-40°C to +150°C	24-Lead LFSCP (4mm x 4mm x 0.95mm w/ EP)	TRAY, 490	CP-24-17
AD3300WBCPZ-RL	-40°C to +150°C	24-Lead LFSCP (4mm x 4mm x 0.95mm w/ EP)	REEL, 5000	CP-24-17
AD3301WBCPZ	-40°C to +150°C	24-Lead LFSCP (4mm x 4mm x 0.95mm w/ EP)	TRAY, 490	CP-24-17
AD3301WBCPZ-RL	-40°C to +150°C	24-Lead LFSCP (4mm x 4mm x 0.95mm w/ EP)	REEL, 5000	CP-24-17
AD3301WBCSZ	-40°C to +150°C	24-Lead LFSCP_SS (4mm x 4mm x 0.95mm w/ EP)	TRAY, 490	CS-24-2
AD3301WBCSZ-RL	-40°C to +150°C	24-Lead LFSCP_SS (4mm x 4mm x 0.95mm w/ EP)	REEL, 5000	CS-24-2
AD3304WBCPZ	-40°C to +150°C	24-Lead LFSCP (4mm x 4mm x 0.95mm w/ EP)	TRAY, 490	CP-24-17
AD3304WBCPZ-RL	-40°C to +150°C	24-Lead LFSCP (4mm x 4mm x 0.95mm w/ EP)	REEL, 5000	CP-24-17
AD3305WBCPZ	-40°C to +150°C	24-Lead LFSCP (4mm x 4mm x 0.95mm w/ EP)	TRAY, 490	CP-24-17
AD3305WBCPZ-RL	-40°C to +150°C	24-Lead LFSCP (4mm x 4mm x 0.95mm w/ EP)	REEL, 5000	CP-24-17

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model	Description
EVAL-AD3301KTZ	E²B Remote Node Generic
EVAL-AD3304KTZ	E²B Remote Node 2 ISELED/ILaS Channels
EVAL-AD3305KTZ	E²B Remote Node 4 ISELED/ILaS Channels
EVAL-AD3300KTZ	E²B Dual Mode Controller Node