LABORATORY PRACTICE – II

EN2090

SEMESTER 3

High Frequency Amplifier

Final Report

GROUP 20

Group Members

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Content

ABSTRACT

The project's aim is to create a High Frequency Amplifier which can drive a load of 8 ohms, such as a headphone with a power amplified signal. It must be capable to amplify signals of the high frequency range from 20kHz to 100kHz. Designed amplifier has mainly two stages with an intermediate impedance matching stage. The first stage is the pre-amplifying stage. It is a BJT transistor in the common emitter configuration. The second stage is the push pull power amplifying stage. Those two stages are combined using the impedance matching stage.

INTRODUCTION

This section describes the given objectives and specification of the project.

OBJECTIVE

The goal is to design and build a high-frequency amplifier capable of driving a 8 ohm head phone with minimal waveform distortion and amplitude reduction.

The design requirements for the amplifier to be built are as follows.

1. Drive a load impedance of 8Ω (headphone).
2. The design must be compatible with working 12V.
3. Amplify a sine wave of 0.1V (peak-peak voltage).
4. Work in the frequency range of 20 kHz – 100kHz (Bandwidth requirement).
5. Consist of minimum 3 transistors (usage of op-amps is prohibited).

And a datasheet must be provided for the designed amplifier.

The following are the parameters that must be determined for the product's data sheet:

1. Open Circuit Gain
2. Gain (with 8Ω load)
3. Bandwidth
4. Input Resistance
5. Output Resistance
6. Maximum Load Current
7. Harmonic Distortion

SUMMARY OF THE REPORT

This report describes a brief description about all the amplifiers firstly then the designed stages of High frequency power amplifier. Those are ,

voltage amplification stage, impedance matching stage and the current amplification stage. And also simulation schematic diagram of Multisim, enclosure solid work design, photo type printed PCB images and the Data sheet of the design are included.

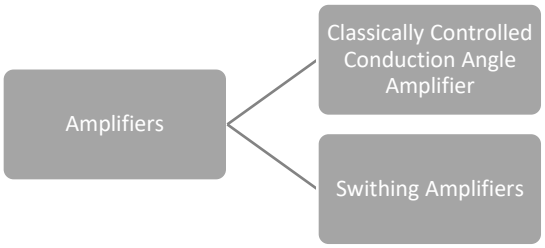
METHODOLOGY

Under this section we mainly focus on the approach that we used to implement our High Frequency amplifier and theory related to the amplifying.

On this point forward we discuss about Common Classification of amplifiers, Class A amplifiers, Class A amplifier configuration, Class B amplifiers, Disadvantages of Amplifier and Class AB amplifier and its implementation.

Amplifier Classes

We can divide amplifiers into 2 major classes.



For our High Frequency Amplifier, we used classically controlled conduction Angle Amplifiers. This Amplifier further can be divided into 4 categories. They are Class A, Class B, Class AB, Class C. To fulfill the purposes of the Amplifier Class A, High Impedance Amplifier (Common Collector Configuration of NPN BJT) and Class AB Amplifier as power amplifier has been used.

Angle Amplifier classes

Class A

Mostly used amplifier class is Class A Amplifiers. Using Bipolar Junction Transistor, Field Effect Transistors Class A amplifiers can be implemented. This type of amplifiers biased around the Q point. Probably Q point is kept at middle of the load line to avoid cutoff or the saturation regions of the signals.

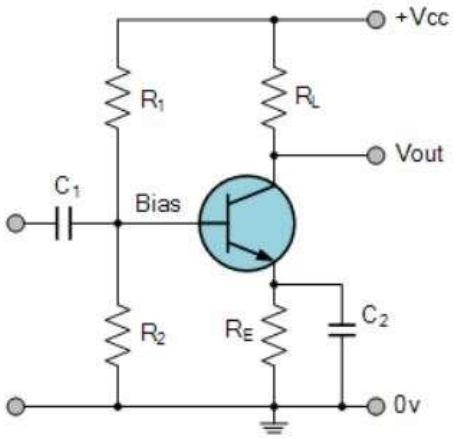
Class A Amplifiers are using mainly because of their linearity, and high gain as well as low distortion level. But can't turn off is a disadvantage of Class A Amplifiers. Class A Amplifiers can be used in configurations such as

- Common Emitter Configuration
- Common Collector Configuration
- Common Base configuration

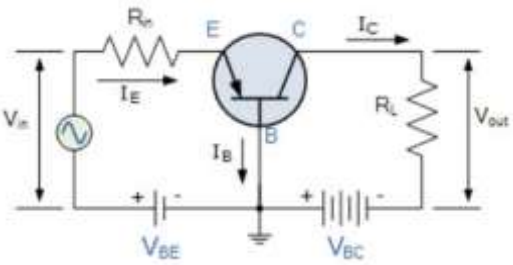
Where these configurations depend on the need of the amplifier. For example, if we need better current and voltage gain, we need to use Common Emitter Configuration.

Brief comparison between above configurations can be shown as below.

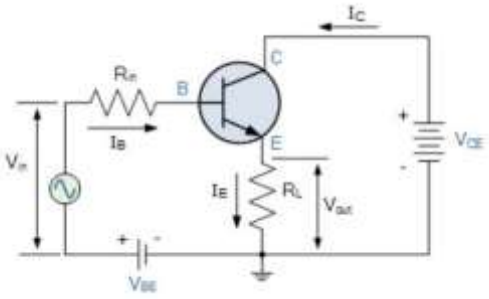
Configuration	Voltage Gain	Current Gain
Common Emitter	About 500 times	Moderate
Common Base	About 150 times	Less than unity
Common Collector	Below 1	Very High



(Common Emitter Configuration)

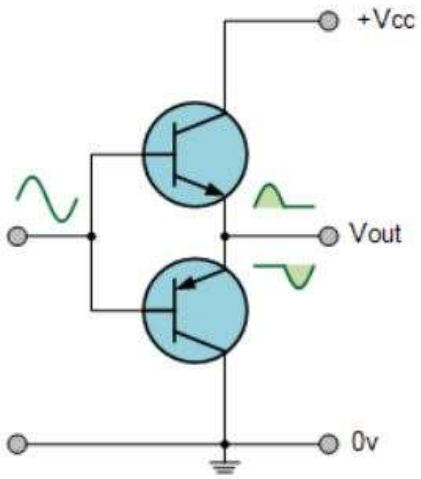


(Common Base Configuration)



(Common Collector Configuration)

Class B Amplifier

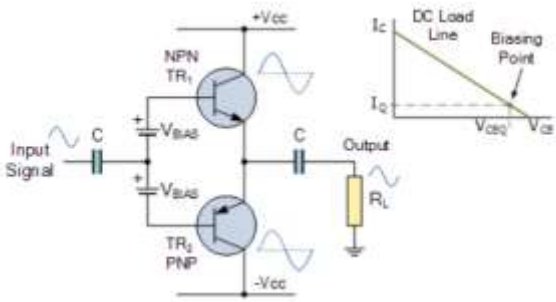


As shown in above picture, Class B amplifiers use 2 transistors. 1 NPN transistor and 1 PNP transistor in push pull arrangement. Because of there is no DC bias, quiescent current become zero. Although Class B amplifier has higher efficiency, DC power is small.

If the input signal is positive, positive biased transistor start conducting. At that time negative biased remain turned off. In the negative half cycle negative biased transistor start conducting. Meanwhile Positive biased transistor remain turned off. Likewise these transistors conducts one at a time. But at the output stage device combines both half cycles together. Although this design in more efficient, this Class B amplifier cause distortions. This distortion is called crossover distortion. Cross over distortion happens when signal cross the zero. Transistor dead band from –0.7 to +0.7.

Class AB Amplifier

Class AB amplifiers are commonly using in power amplification in Audio power amplification. Class AB amplifiers can avoid the dead zone and crossover distortion.



Here to avoid cross over distortion and dead zone we bias 2 power transistors using to external batteries. For Our Circuit we used Biasing circuit using BC547B transistor and Capacitor which connected between collector and emitter of the transistor

High Frequency Amplifier Stages

Stage 1 – Pre-Amplifier

The first stage is used to get a sufficient volage gain that can be passed through rest of the stages. We used class A common emitter amplifier as the pre amplifier stage in order to amplify the voltage of the input signal. Since class A amplifier type fully amplify the input signal and we can get large voltage gain it is the most suitable type for the pre amplifier stage.

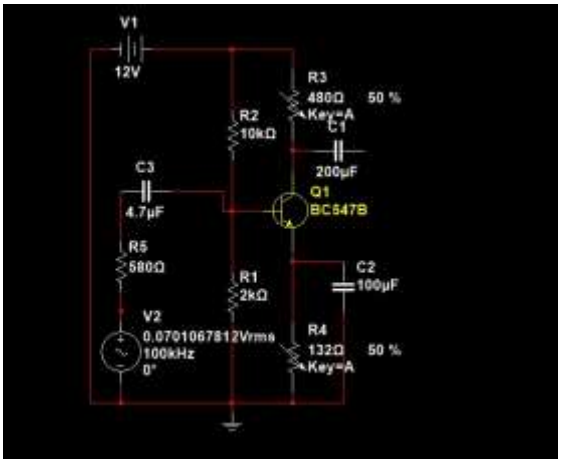


Figure: circuit diagram

Initial Calculations

The base was biased to the voltage of 2v. (RB1 = 10kΩ RB2 = 2kΩ)

Assuming that base current is negligible. Therefore VB = 2v

Assuming VBE = 0.7v. Then VE = 1.3v

We selected emitter resistance such that IE = 20mA. Then RE = 66Ω and IC = 20mA

VCE is set to round 6v to allow for the full swing of the voltage during operation to get the maximum gain without distortion.

Therefore RC = (12 – 7.3)/20 = 240Ω

We calculated some of the parameters initially using the hybrid π model. However, many of these parameters not agree with the practical values and later were discarded.

Rπ = VT/IB = 26mV/(20mA/300) = 390Ω

Therefore, input resistance

Rin = RB1//RB2//rπ = 390Ω

Open circuit voltage gain (AVO) = β*RC/Rin = 180

Device selection

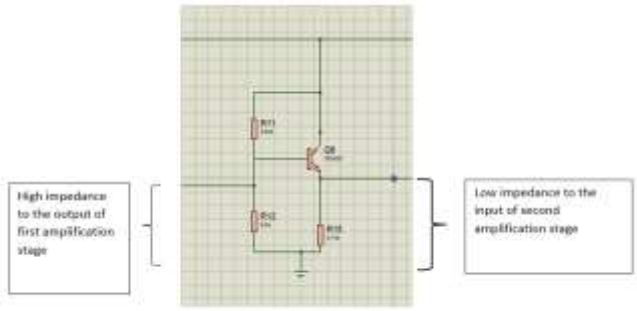
Component	Value	Description
BC547B npn transistor	1	BC547B has a relatively high h_{fe} value and the transistors has a high bandwidth and fast switching enabling to handle high frequency signals
Capacitors	0.47µF, 220µF, 100µF	Capacitors are used to block the DC from the input and output side and ground the emitter resistance to the AC signals
Resistors	10kΩ, 2kΩ, 132Ω, 480Ω	
Heat sinks		Heat sinks are used to remove the heat generated in the amplifier

Stage 2 - Impedance matching stage

Impedance matching of the input and the output is necessary because the gain of a single amplifier is not sufficient for the given power amplification task. Therefore, we designed two main amplification stages which are connected in cascade. The first stage is the voltage amplification stage as mention above and the second stage is the power amplification stage which can amplify the current. This voltage amplification stage cannot be directly connected to the power amplification stage because the voltage gain is reduced due to the load(power amplification stage). Therefore high impedance is needed to be connected to the output of the first stage(Voltage amplification stage) and low impedance is needed to be connected to the input of the power amplification stage.

The common collector setup commonly known as emitter follower has used as the intermediate stage for the impedance matching task. Because this setup has a high input impedance and a low output impedance with practically unit gain.

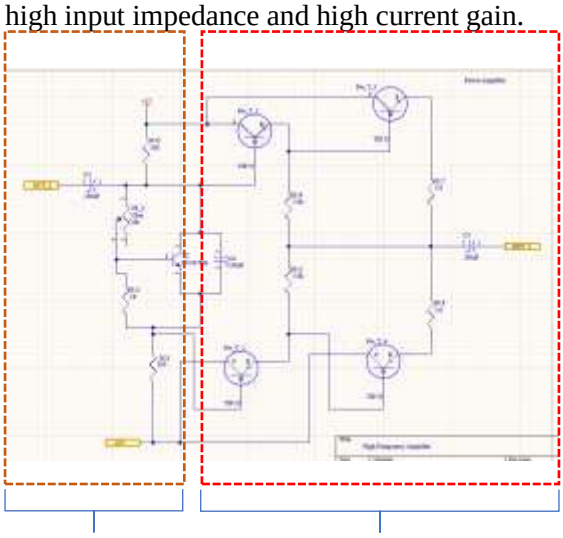
As a result of this stage current amplification stage can be fed up with a sufficient amplified voltage.



Stage 3 - Power Amplification

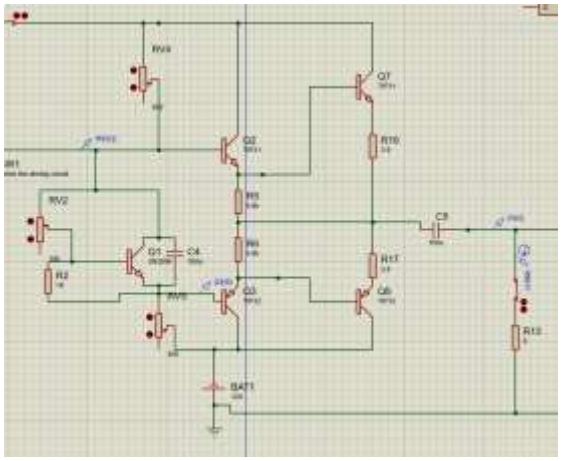
Even though the signal is amplified by the *Pre-Amplifier*, it cannot supply enough current to maintain the high voltage, with a small load. Therefore, a *Power Amplification* stage is added to the circuit.

The pre-amplified circuit is designed with high input impedance and high current gain.



Biasing Circuit

Current Amplifying Circuit



Since the current can be handled by a single power transistor is limited and to improve the full power efficiency, the push pull configuration is being used. TIP31 is the NPN and TIP32 is the PNP used.

The positive half cycle is amplified by the NPN transistor, and the negative half cycle is amplified by the PNP transistor

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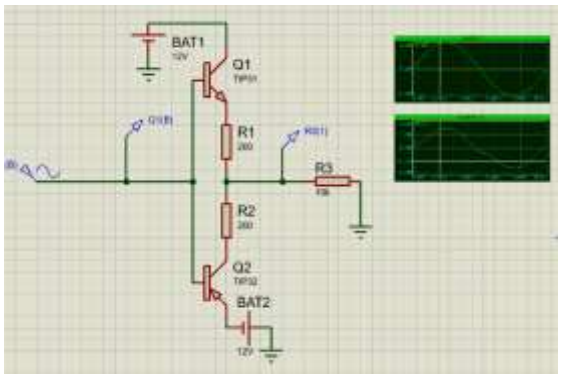
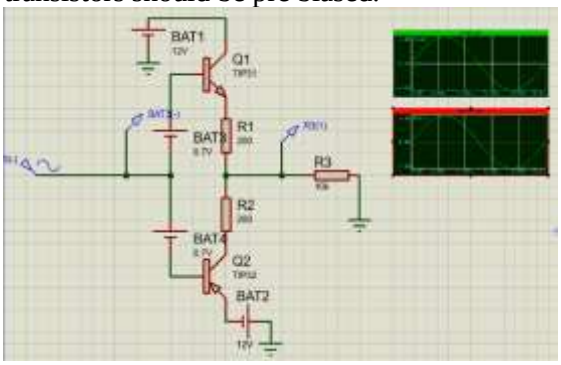


As shown in the output graph, the output signal is distorted. Until the input magnitude surpasses the VBE values of transistors. Therefore, the power transistors have to be biased initially.

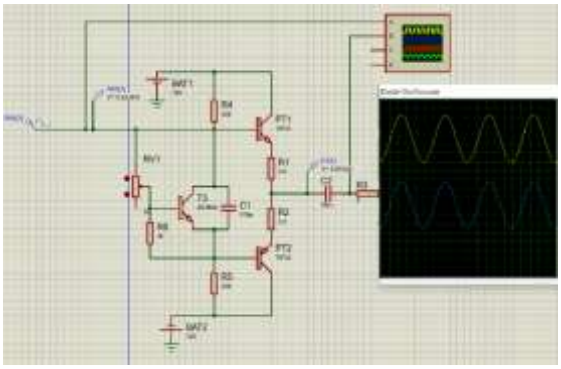
Biasing circuit

To overcome the cut off issue, the power transistors should be pre biased.



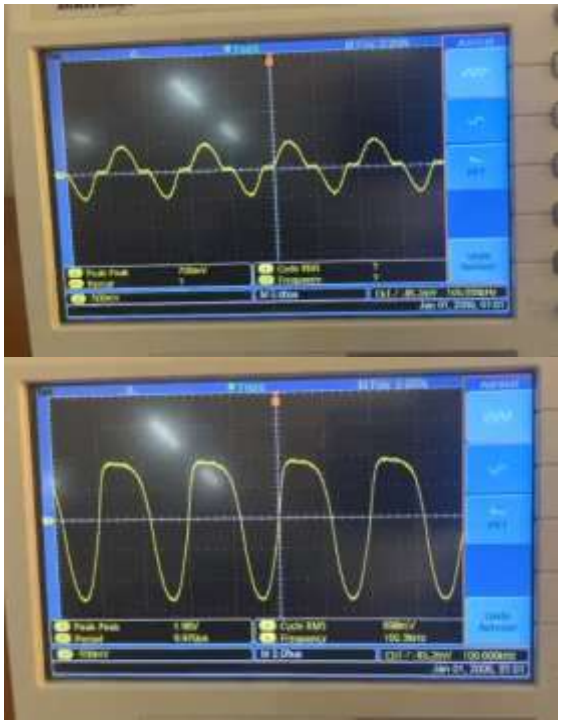
This can be achieved by setting a fixed bias. But in a practical circuit, the VBE varies with the temperature and other external factors.

As the solution, an Active Biasing Circuit is used.



R6 will have the VBE of T3 (let's say 0.7). Since the IB current of T3 is low, VR1 and R6 will operate as series resistors. By varying the VR1 value, we can adjust the biasing voltage across C1. The R4 and R5 help to maintain a constant border from the supply voltages.

In the practical circuit, by adjusting the VR1, we can shift the push pull circuit to B, AB and A types. By keeping R1 & R2 low, we can reduce the voltage drop and increase the output voltage.



Current Amplifying circuit

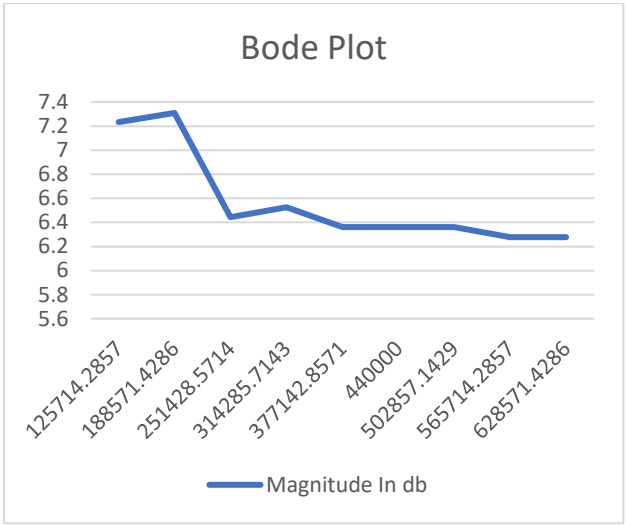
As the current amplifying circuit, two push pull stages have been used to increase the current gain. A portion of first stage emitter current is fed to the second stage bases. It increases the power amplifier gain as well as the impedance. The graph below is the output with only one stage.

The graph below is the output when the second stage is connected. Practically it is more convenient. This increases the circuit input impedance as well.

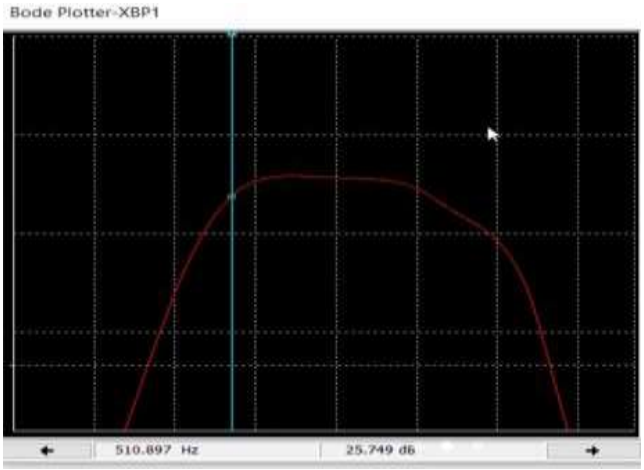
Bode Plot Using

Frequency Input(kHz)	Vout	Magnitude In db	Omega Value
20	2.3	7.23455672	125714.2857
30	2.32	7.309759698	188571.4286
40	2.1	6.444385895	251428.5714
50	2.12	6.526717219	314285.7143
60	2.08	6.361266699	377142.8571
70	2.08	6.361266699	440000
80	2.08	6.361266699	502857.1429
90	2.06	6.277344407	565714.2857
100	2.06	6.277344407	628571.4286

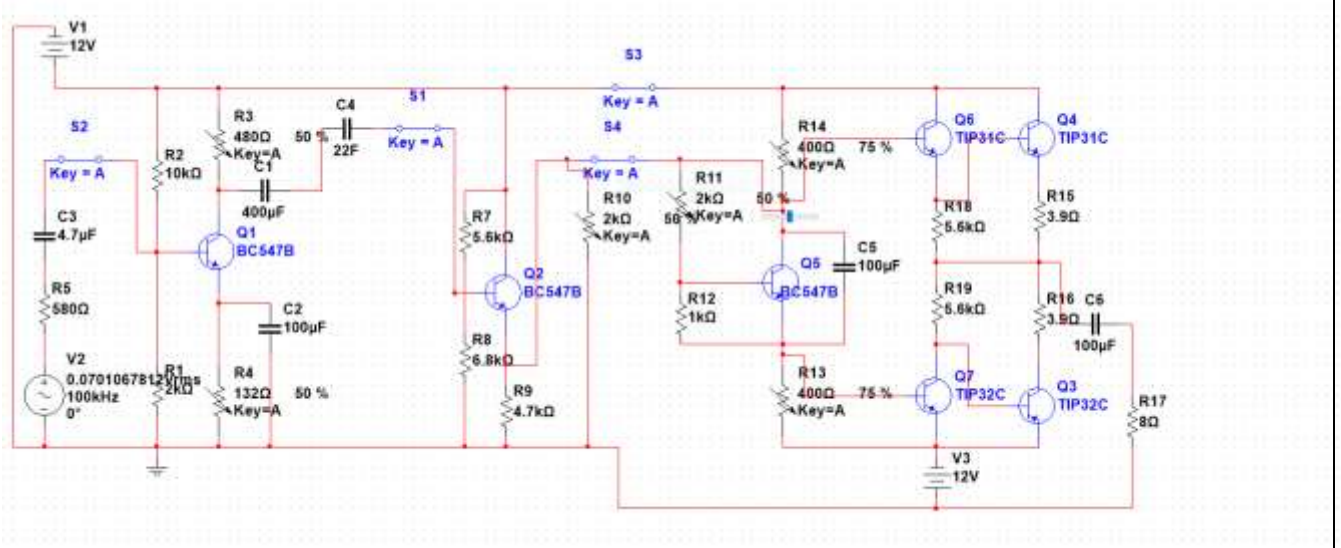
Magnitude (dB) =20log$_{10}$(X)



Body Plot Using Multisim simulation

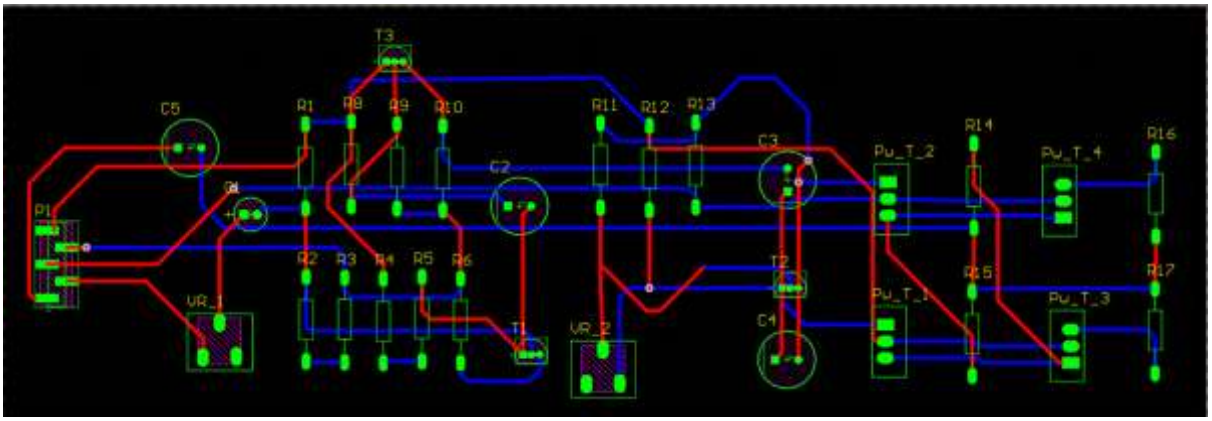


Final Circuit design



Printed Circuit Board

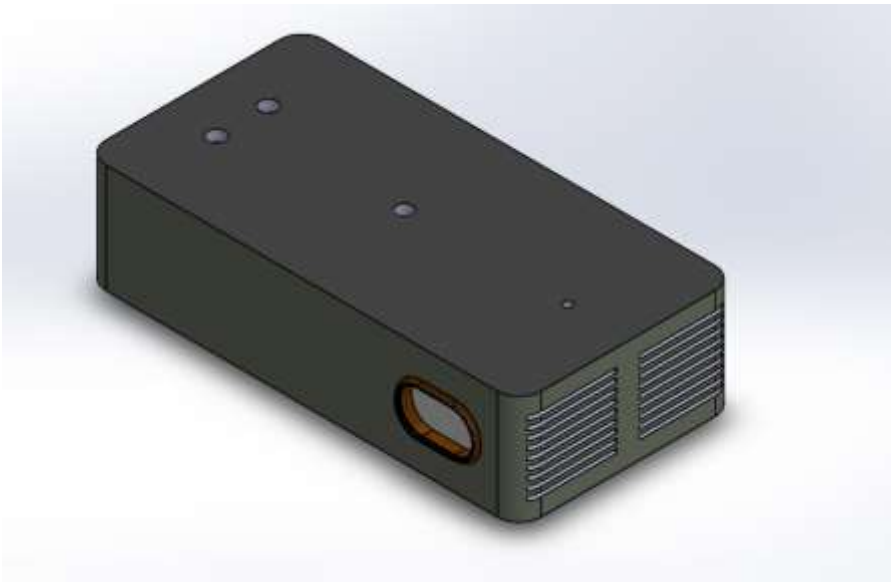
Altium Design



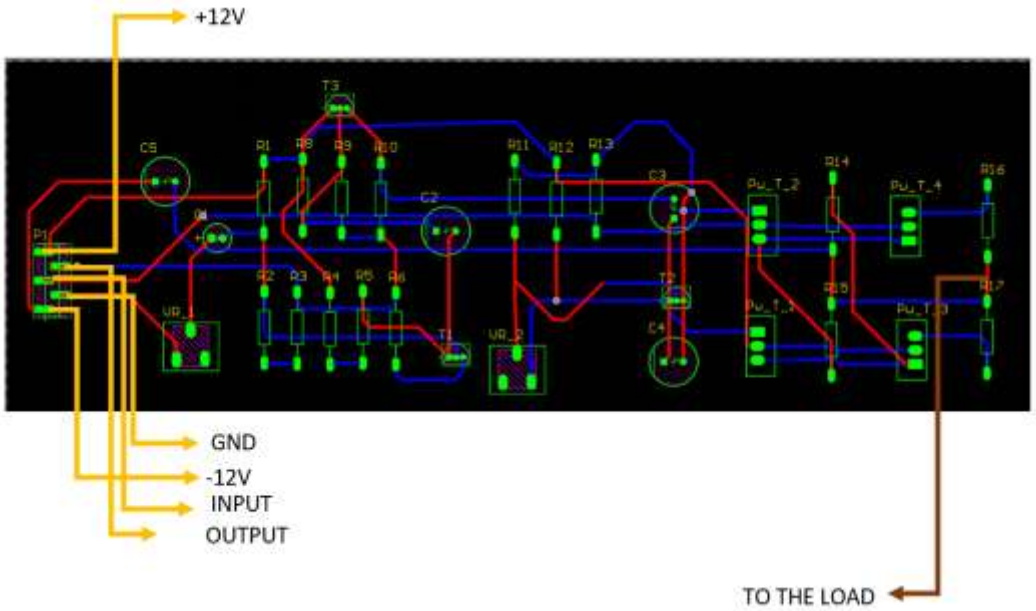
Implemented PCB

ENCLOSURE DESIGN

As we are using many TIP3X power transistors heat generation is high. So we decided to put many ventilation holes to keep environment cool inside the enclosure



Pin Diagram of PCB



Electrical Specification

PARAMETER	CONDITION	MIN	TYPICAL	MAXIMUM	UNITS
OPERATING SUPPLY VOLTAGE				12	V
INPUT VOLTAGE (PK-PK)				0.1	V
VOLTAGE GAIN	R_L=8Ω				dB
BANDWIDTH			143.371		MHz
INPUT RESISTANCE	R_L -> ∞		34.987		Ω
OUTPUT RESISTANCE	Vs=0		23.392		MΩ
LOAD CURRENT	R_L=10Ω		102.5		mA
TOTAL HARMONIC DISTORTION	f = 20Hz		6.84		%
	f = 100kHz		17.094		%
	f = 200kHz		32.729		%

Conclusion

We met with objectives and tasks on the breadboard prototype. For the experiment we got the good results for the prototype on breadboard and dot board designs. We designed our own designs for PCB and Enclosure.

References

https://www.alldatasheet.com/datasheet-pdf/pdf/2776/MOSPEC/TIP31.html

https://www.alldatasheet.com/datasheet-pdf/pdf/2780/MOSPEC/TIP32.html

https://www.alldatasheet.com/datasheet-pdf/pdf/11551/ONSEMI/BC547.html

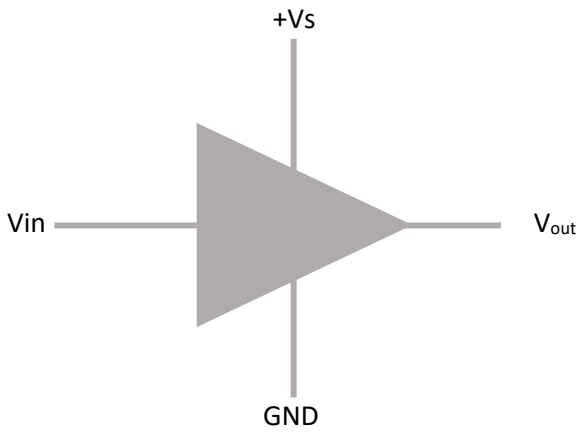
https://www.electronics-tutorials.ws/amplifier/class-ab-amplifier.html

Name	Index Number	Contribution
Rathnayake R.M.K.L.	190520D	Basic Implementation of Circuit on breadboard, Enclosure Design, Soldering PCB, Simulation on Multisim, Component Recognition, Mounting Components on PCB
Rathnayake R.M.L.W	190521G	Basic Implementation of Circuit on breadboard, PCB Design, Simulations on proteus, Soldering PCB, Component Recognition
Rodrigo K.M.P.M.	190527F	Simulation on Multisim, Contribution to Report, Bode plots, Enclosure Design,
Rodrigo M.D.A.C.	190528J	Basic Implementation of Circuit on breadboard, Mounting Components on PCB and Soldering, Proteus Simulation, Helping design PCB

APPENDIX 1

DATA SHEET OF HIGH FREQUENCY AMPLIFIER

BLOCK DIAGRAM OF HIGH FREQUENCY AMPLIFIER



INPUT CONDITIONS

Minimum Input 0.1V

Frequency Range 20Khz - 100kHz

OUTPUT CONDITIONS

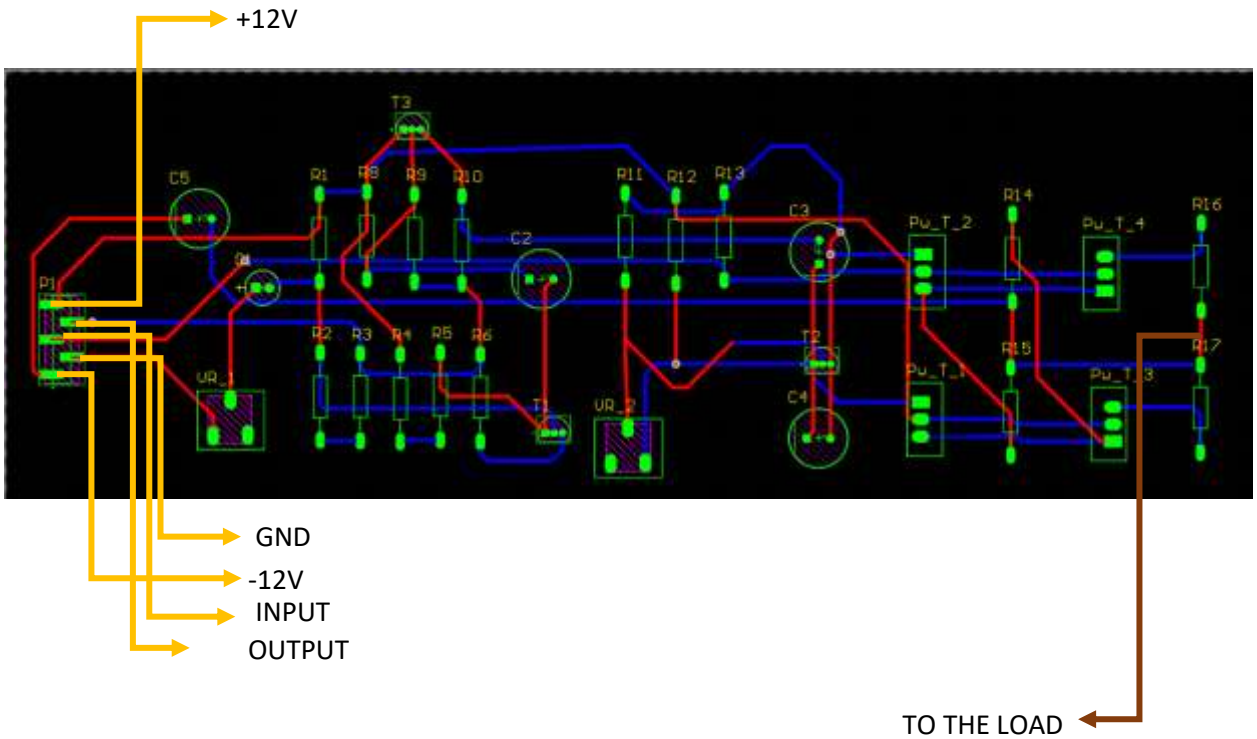
8ohm Load (Headphone)

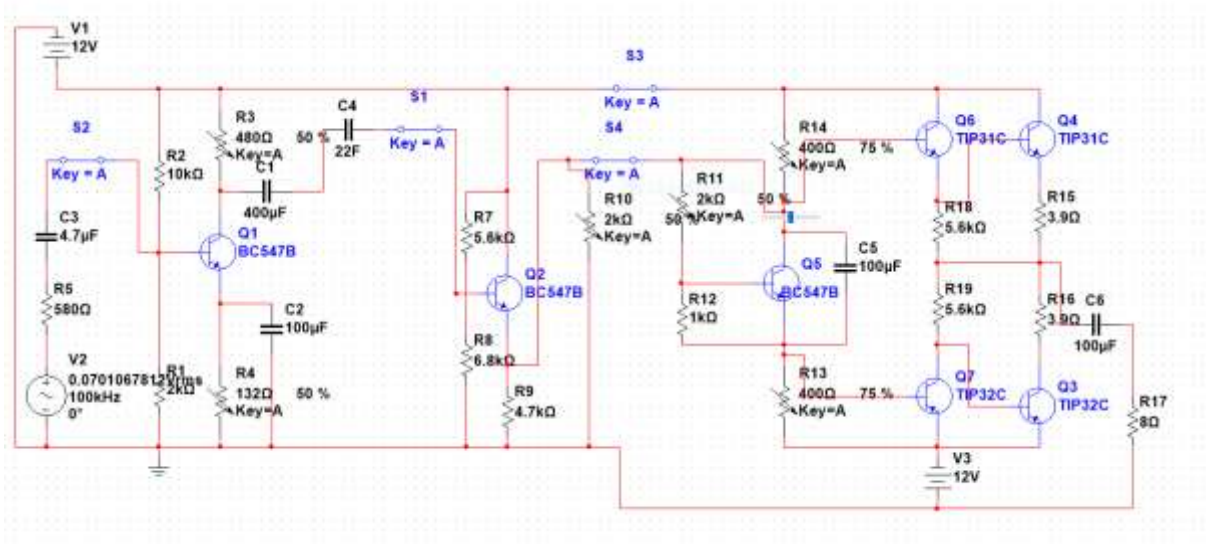
ELECTRICAL SPECIFICATION

PARAMETER	CONDITION	MIN	TYPICAL	MAXIMUM	UNITS
OPERATING SUPPLY VOLTAGE				12	V
INPUT VOLTAGE (PK-PK)				0.1	V
VOLTAGE GAIN	R_L=8Ω				dB
BANDWIDTH			143.371		MHz
POWER OUTPUT	R_L=10Ω				
INPUT RESISTANCE	R_L -> ∞		34.987		Ω
OUTPUT RESISTANCE	Vs=0		23.392		MΩ
LOAD CURRENT	R_L=10Ω		102.5		mA

TOTAL HARMONIC DISTORTION	f = 20Hz	6.84	%
	f = 100kHz	17.094	%
	f = 200kHz	32.729	%

Schematic and PCB





Bode Plots

Real Values

Frequency Input(kHz)	Vout	Magnitude In db	Omega Value
20	2.3	7.23455672	125714.2857
30	2.32	7.309759698	188571.4286
40	2.1	6.444385895	251428.5714
50	2.12	6.526717219	314285.7143
60	2.08	6.361266699	377142.8571
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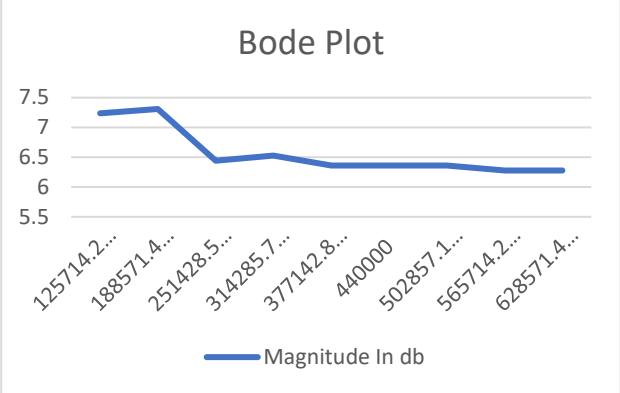
100	2.06	6.277344407	628571.4286



Bode Plot using Multisim