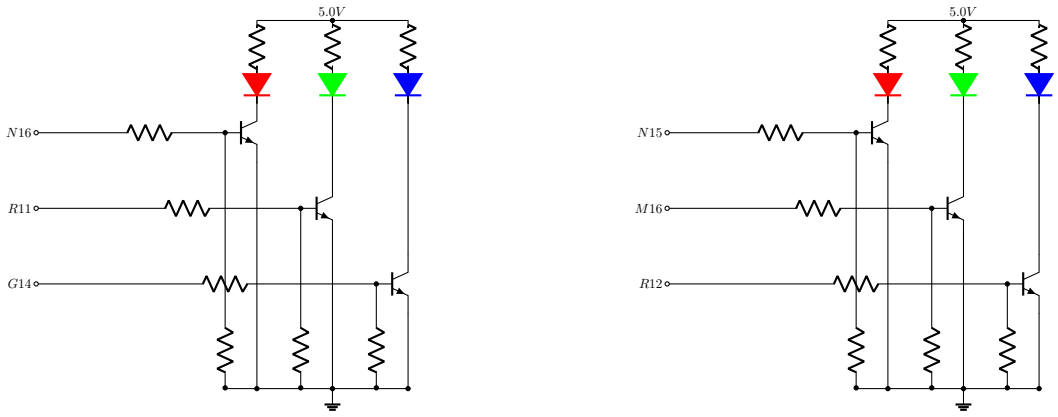
Experiment 4

Combinational Circuit Design: RGB LED using K-Maps

For this lab, we will design the driver circuit for the tri-color LEDs.

Overview of Tri-Color LEDs

Our board contains two tricolour LEDs. Each LED contains three smaller LEDs, i.e, one red, one green and one blue LED. The pin configurations of all the required components can be seen from the Nexys A7 reference manual in the **Basic I/O**.



(a) First RGB LED. (b) Second RGB LED.

Fig. 4.1: Configuration of tri-leds in the Nexys A7.

The Fig. 4.1 gives us the circuit diagram along with the pin configuration of the two LEDs on the FPGA board. Each LED of the RGB can be turned on by controlling the cathode of the respective LED. In order to turn on a LED, a high signal is required at the input which will be inverted using the transistor to turn on the LED. Hence, the transistor is going to act as a switch in the circuit.

Lab Task

For this lab, you are required to create a module containing two 2-bits inputs a and b such that we observe the following output on the tri-color LED.

$$F = \begin{cases} a > b & Purple \\ a = b & Yellow \\ a < b & Cyan \end{cases}$$

For this purpose, first develop the truth table according to the requirement (a[1], a[0], b[1] and b[0] will be the inputs and r, g and b will be the outputs) and then get the minimized expression for the output using K-maps. Next, implement the design using System Verilog. Simulate your design and program the bitstream on the FPGA.

The instruction manual is for the exclusive use of the students and trainees of University of Engineering and Technology, Lahore.
©2025 UET Lahore.

Deliverables

1. A report containing the following items:
   (a) Truth table of the circuit.
   (b) K-maps used to minimize the logic. Write down all prime and essential prime implicants of the function.
   (c) Circuit diagram of your reduced design inferred from K-Maps.
   (d) Circuit diagram inferred by the Xilinx Vivado. You can see the inferred circuit in "Schematic" under the process "Elaborated Design". Is it similar to the one you designed using K-maps?
   (e) Maximum combinational delay in Synthesis: Read the report of your circuit and describe which path has the maximum combinational delay?
   (f) Resource Utilization: Read the synthesis report and identify how many resources in the FPGA such as lookup tables (LUTs), input/output (IOs), etc., has been utilized.
2. System Verilog code for the circuit.
3. Synthesis of the circuit for the starter kit available in the lab. Tie inputs to the switches and output to the RGB LED available on the board.
4. Simulation of your design. Show it to the instructor.

Collaboration between students is encouraged, but blind code sharing/copying is not allowed. If you are unable to explain anything in your code, it will be assumed you have copied it. So make sure you know everything you have written in your code. We are least concerned about how you have learnt something as long as you have learnt it well.

Acknowledgments

The manual has been written by Dr. Ubaid Ullah Fayyaz and Mr. Ali Imran.

The instruction manual is for the exclusive use of the students of University of Engineering and Technology, Lahore.
©2025 UET Lahore.