1. Description
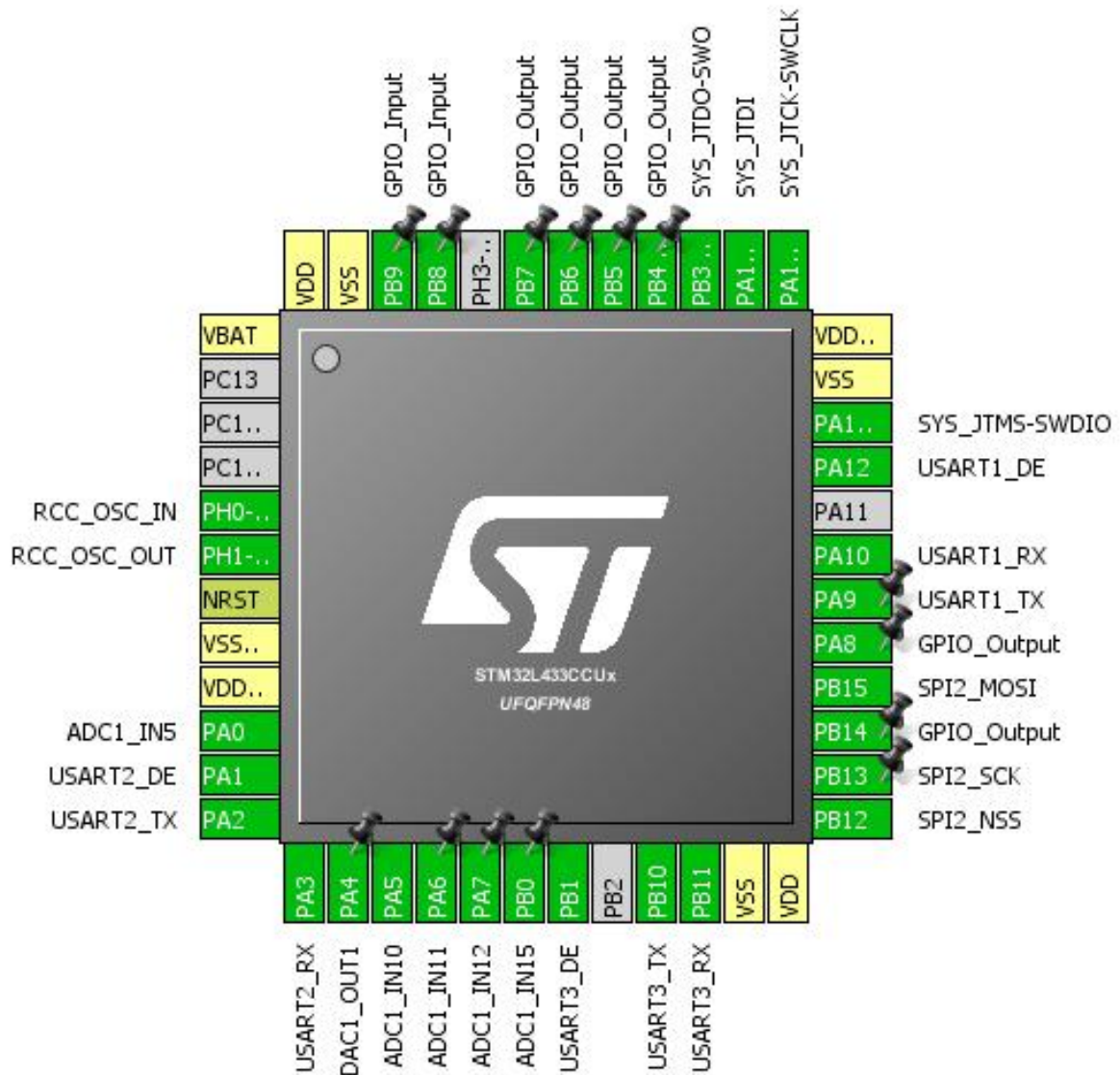
1.1. Project

Project Name	plc_1xx_L433
Board Name	plc_1xx_L433
Generated with:	STM32CubeMX 4.22.0
Date	08/17/2017

1.2. MCU

|	
MCU Series	STM32L4
MCU Line	STM32L4x3
MCU name	STM32L433CCUx
MCU Package	UFQFPN48
MCU Pin number	48

2. Pinout Configuration

3. Pins Configuration

Pin Number UFQFPN48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
5	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
6	PH1-OSC_OUT (PH1)	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	VSSA/VREF-	Power		
9	VDDA/VREF+	Power		
10	PA0	I/O	ADC1_IN5	
11	PA1	I/O	USART2_DE	
12	PA2	I/O	USART2_TX	
13	PA3	I/O	USART2_RX	
14	PA4	I/O	DAC1_OUT1	
15	PA5	I/O	ADC1_IN10	
16	PA6	I/O	ADC1_IN11	
17	PA7	I/O	ADC1_IN12	
18	PB0	I/O	ADC1_IN15	
19	PB1	I/O	USART3_DE	
21	PB10	I/O	USART3_TX	
22	PB11	I/O	USART3_RX	
23	VSS	Power		
24	VDD	Power		
25	PB12	I/O	SPI2_NSS	
26	PB13	I/O	SPI2_SCK	
27	PB14 *	I/O	GPIO_Output	
28	PB15	I/O	SPI2_MOSI	
29	PA8 *	I/O	GPIO_Output	
30	PA9	I/O	USART1_TX	
31	PA10	I/O	USART1_RX	
33	PA12	I/O	USART1_DE	
34	PA13 (JTMS-SWDIO)	I/O	SYS_JTMS-SWDIO	
35	VSS	Power		
36	VDDUSB	Power		
37	PA14 (JTCK-SWCLK)	I/O	SYS_JTCK-SWCLK	
38	PA15 (JTDI)	I/O	SYS_JTDI	
39	PB3 (JTDO-TRACESWO)	I/O	SYS_JTDO-SWO	
40	PB4 (NJTRST) *	I/O	GPIO_Output	
41	PB5 *	I/O	GPIO_Output	

Pin Number UFQFPN48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
42	PB6 *	I/O	GPIO_Output	
43	PB7 *	I/O	GPIO_Output	
45	PB8 *	I/O	GPIO_Input	
46	PB9 *	I/O	GPIO_Input	
47	VSS	Power		
48	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration
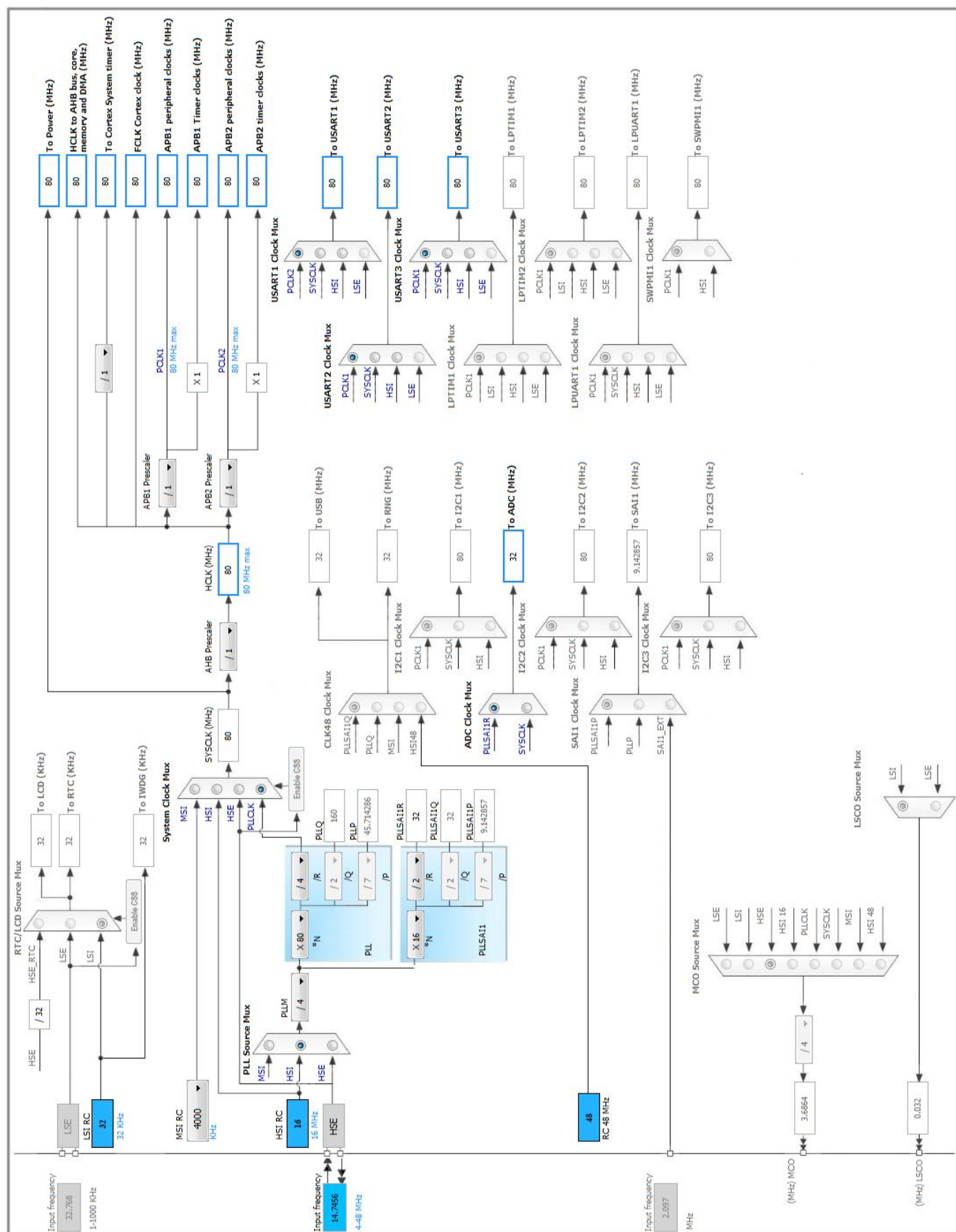
5. IPs and Middleware Configuration

5.1. ADC1

IN5: IN5 Single-ended
IN10: IN10 Single-ended
IN11: IN11 Single-ended
mode: IN12
IN15: IN15 Single-ended

5.1.1. Parameter Settings:

ADC_Settings:

Clock Prescaler	Asynchronous clock mode divided by 1
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	**Timer 6 Trigger Out event ***
External Trigger Conversion Edge	Trigger detection on the rising edge
Rank	1
Channel	Channel 5
Sampling Time	2.5 Cycles
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode   false

5.2. DAC1

OUT1 mode: Connected to external pin only

5.2.1. Parameter Settings:

DAC Out1 Settings:

Output Buffer	Enable
Trigger	None
User Trimming	Factory trimming
Sample And Hold	Sampleandhold Disable

5.3. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

5.3.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Disabled
Data Cache	Enabled
Flash Latency(WS)	4 WS (5 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
MSI Calibration Value	0
MSI Auto Calibration	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

5.4. SPI2

Mode: Transmit Only Master
Hardware NSS Signal: Hardware NSS Output Signal

5.4.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**40.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Output Hardware

5.5. SYS

Debug: JTAG (4 pins)
Timebase Source: TIM1

5.6. TIM2

Clock Source   : Internal Clock

5.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**8000 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**0xffffffff ***
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves

Trigger Event Selection TRGO   Reset (UG bit from TIMx_EGR)

5.7. TIM6

mode: Activated

5.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**80-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**3125 ***

Trigger Output (TRGO) Parameters:

Trigger Event Selection	**Update Event ***

5.8. TIM7

mode: Activated

5.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**8000-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**1000 ***

Trigger Output (TRGO) Parameters:

Trigger Event Selection	**Update Event ***

5.9. USART1

Mode: Asynchronous
mode: Hardware Flow Control (RS485)

5.9.1. Parameter Settings:

Basic Parameters:

Baud Rate	**9600** *
Word Length	**8 Bits (including Parity)** *
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
Polarity	High
Assertion Time	0
Deassertion Time	0

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

5.10. USART2

Mode: Asynchronous
mode: Hardware Flow Control (RS485)

5.10.1. Parameter Settings:

Basic Parameters:

Baud Rate	**9600** *
Word Length	**8 Bits (including Parity)** *
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
Polarity	High
Assertion Time	0
Deassertion Time	0

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

5.11. USART3

Mode: Asynchronous

mode: Hardware Flow Control (RS485)

5.11.1. Parameter Settings:

Basic Parameters:

Baud Rate	**9600** *
Word Length	**8 Bits (including Parity)** *
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
Polarity	High
Assertion Time	0
Deassertion Time	0

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

5.12. FREERTOS

mode: Enabled

5.12.1. Config parameters:

Versions:

FreeRTOS version	9.0.0
CMSIS-RTOS version	1.02

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Disabled
USE_COUNTING_SEMAPHORES	Disabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Enabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled

Memory management settings:

Memory Allocation	Dynamic
TOTAL_HEAP_SIZE	**15360 ***
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	**Enabled ***
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	**Enabled ***
USE_TRACE_FACILITY	Disabled

USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Disabled

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

5.12.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Disabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Disabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Disabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled

* User modified value

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0	ADC1_IN5	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
	PA5	ADC1_IN10	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
	PA6	ADC1_IN11	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
	PA7	ADC1_IN12	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
	PB0	ADC1_IN15	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
DAC1	PA4	DAC1_OUT1	Analog mode	No pull-up and no pull-down	n/a	
RCC	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
SPI2	PB12	SPI2_NSS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PB13	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PB15	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
SYS	PA13 (JTMS-SWDIO)	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14 (JTCK-SWCLK)	SYS_JTCK-SWCLK	n/a	n/a	n/a	
	PA15 (JTDI)	SYS_JTDI	n/a	n/a	n/a	
	PB3 (JTDO-TRACESWO)	SYS_JTDO-SWO	n/a	n/a	n/a	
USART1	PA9	USART1_TX	Alternate Function Push Pull	Pull-up	**Very High** *	
	PA10	USART1_RX	Alternate Function Push Pull	Pull-up	**Very High** *	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PA12	USART1_DE	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
USART2	PA1	USART2_DE	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PA2	USART2_TX	Alternate Function Push Pull	Pull-up	**Very High** *	
	PA3	USART2_RX	Alternate Function Push Pull	Pull-up	**Very High** *	
USART3	PB1	USART3_DE	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PB10	USART3_TX	Alternate Function Push Pull	Pull-up	**Very High** *	
	PB11	USART3_RX	Alternate Function Push Pull	Pull-up	**Very High** *	
GPIO	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PA8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB4 (NJTRST)	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB8	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PB9	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	

6.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA1_Channel1	Peripheral To Memory	Low

ADC1: DMA1_Channel1 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
DMA1 channel1 global interrupt	true	5	0
ADC1 global interrupt	true	5	0
TIM1 update interrupt and TIM16 global interrupt	true	0	0
USART1 global interrupt	true	5	0
USART2 global interrupt	true	5	0
USART3 global interrupt	true	5	0
TIM6 global interrupt, DAC channel1 and channel2 underrun error interrupts	true	5	0
TIM7 global interrupt	true	0	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/35/36/37/38	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM2 global interrupt	unused		
SPI2 global interrupt	unused		
FPU global interrupt	unused		

* User modified value

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32L4
Line	STM32L4x3
MCU	STM32L433CCUx
Datasheet	028794_Rev1

7.2. Parameter Selection

Temperature	25
Vdd	null

8. Software Project

8.1. Project Settings

Name	Value
Project Name	plc_1xx_L433
Project Folder	D:\Repos\PLC_1xx\plc_1xx_L433
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_L4 V1.8.1

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No