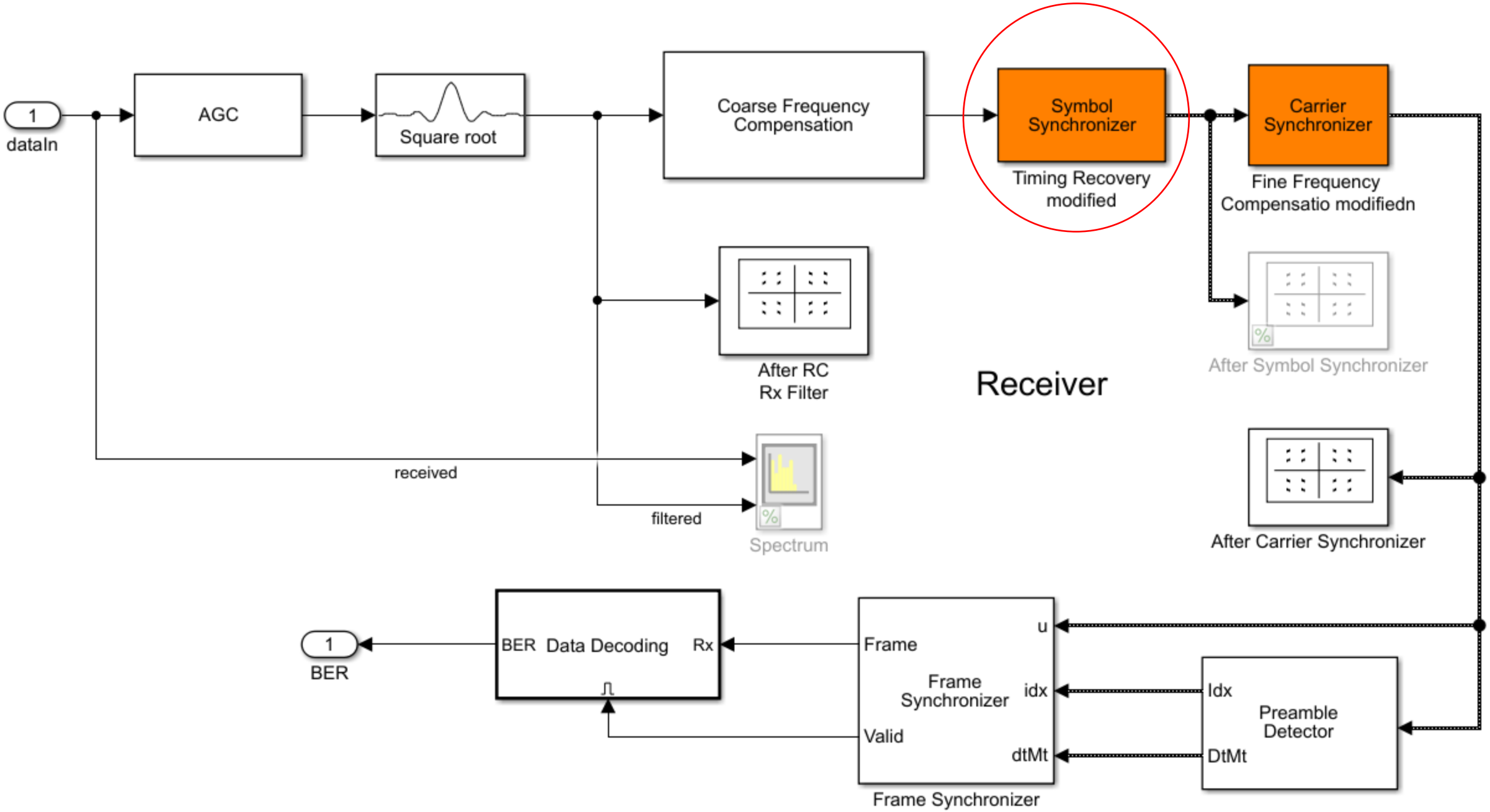
Synchronization blocks used in the QPSK lab demo

EE161: Digital Communication Systems

San José State University


1
dataIn
AGC
Square root
Coarse Frequency Compensation
Symbol Synchronizer
Timing Recovery modified
Carrier Synchronizer
Fine Frequency Compensatio modifiedn
After RC Rx Filter
After Symbol Synchronizer
Receiver
received
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Spectrum
After Carrier Synchronizer
1
BER
BER Data Decoding Rx
Frame
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idx
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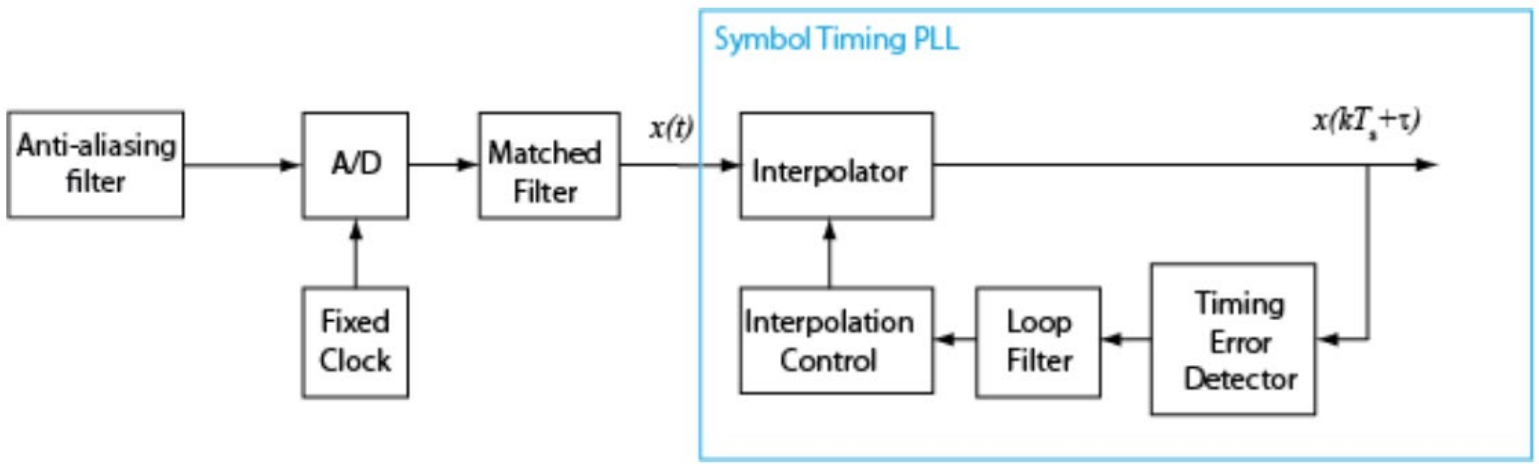
Frame Synchronizer
Idx
DtMt
Preamble Detector

Symbol Synchronization Overview

The symbol timing synchronizer algorithm is based on a phased lock loop (PLL) algorithm that consists of four components:

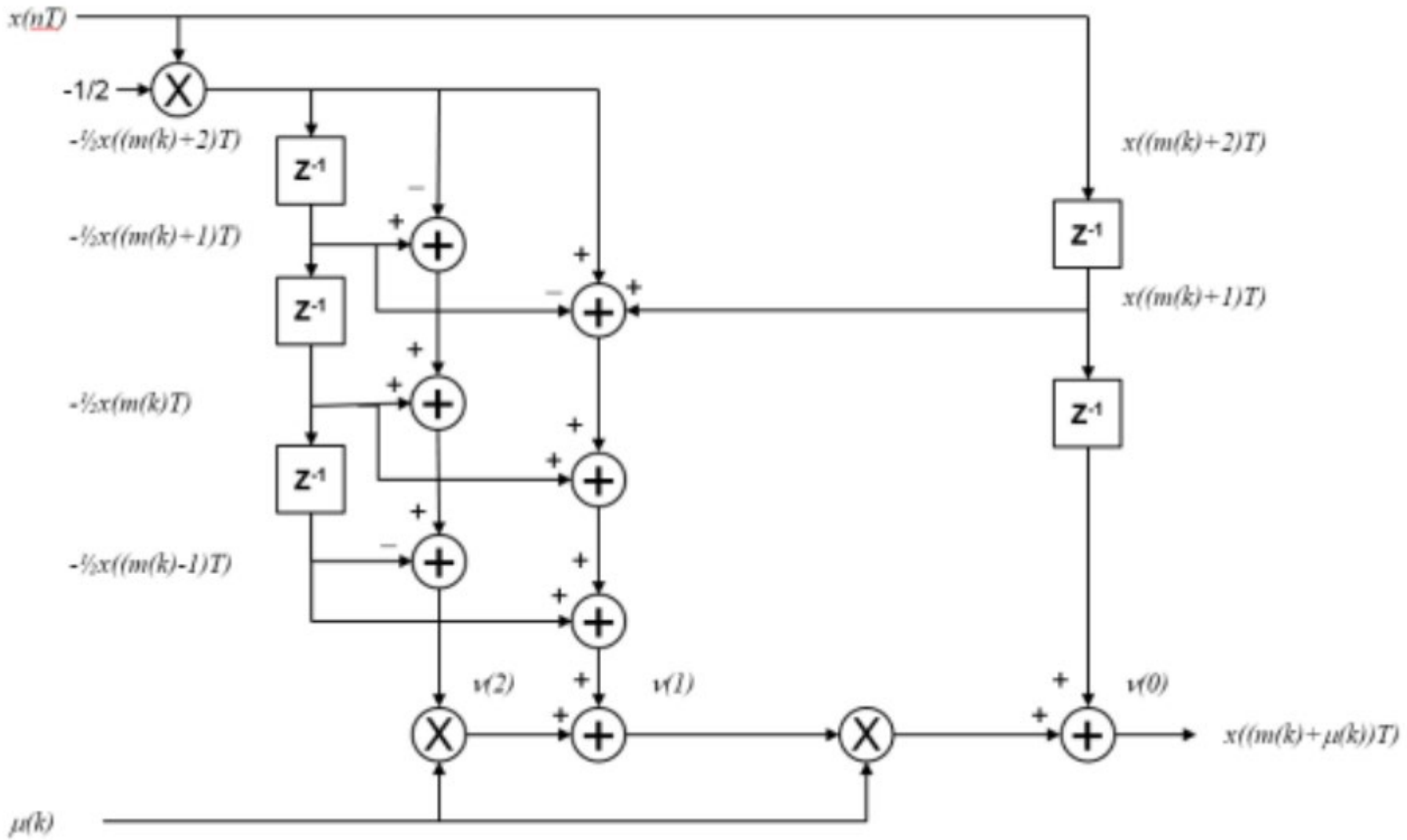
- A timing error detector (TED)
- An interpolator
- An interpolation controller
- A loop filter

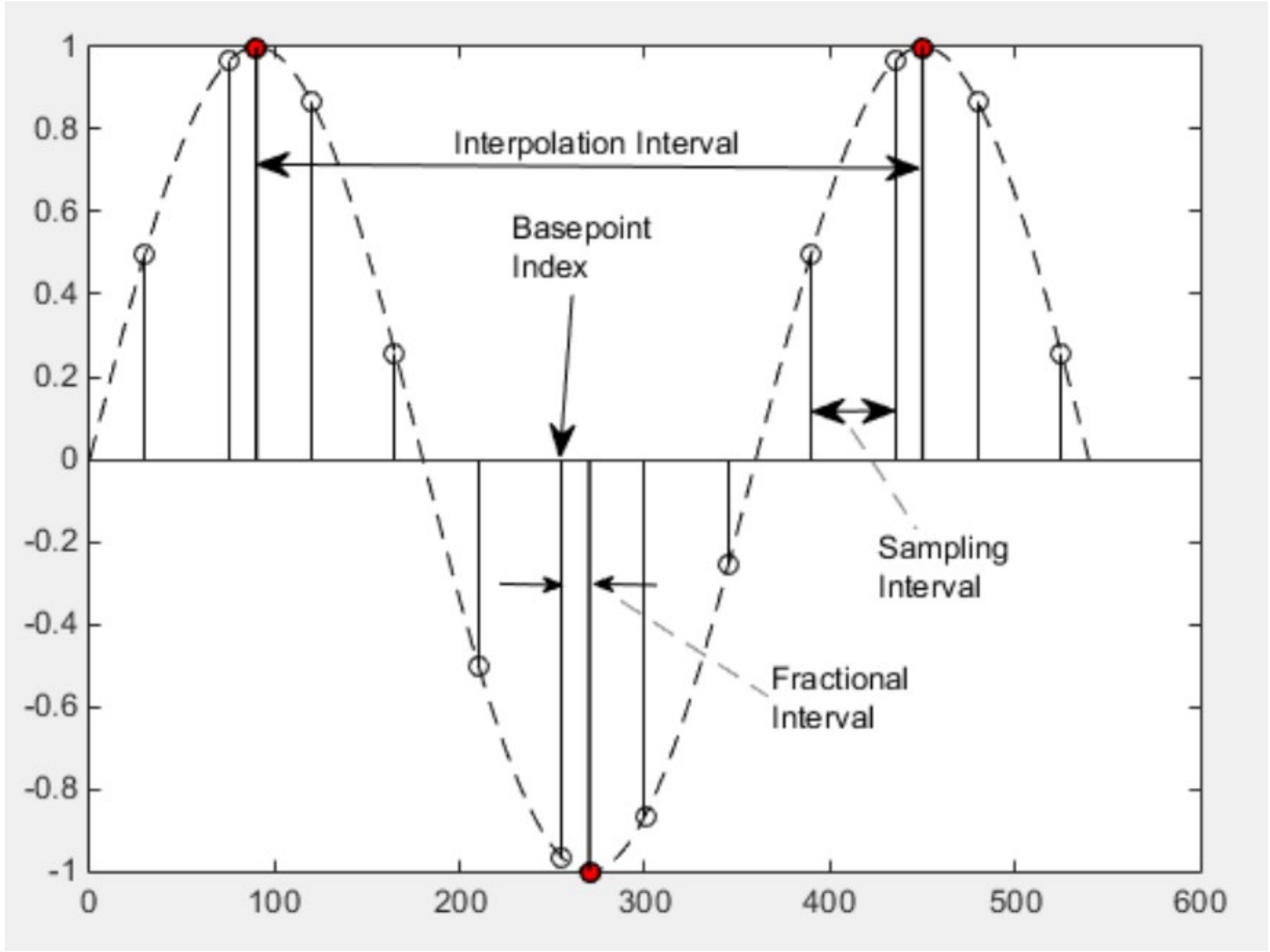


Timing Error Detection (TED)

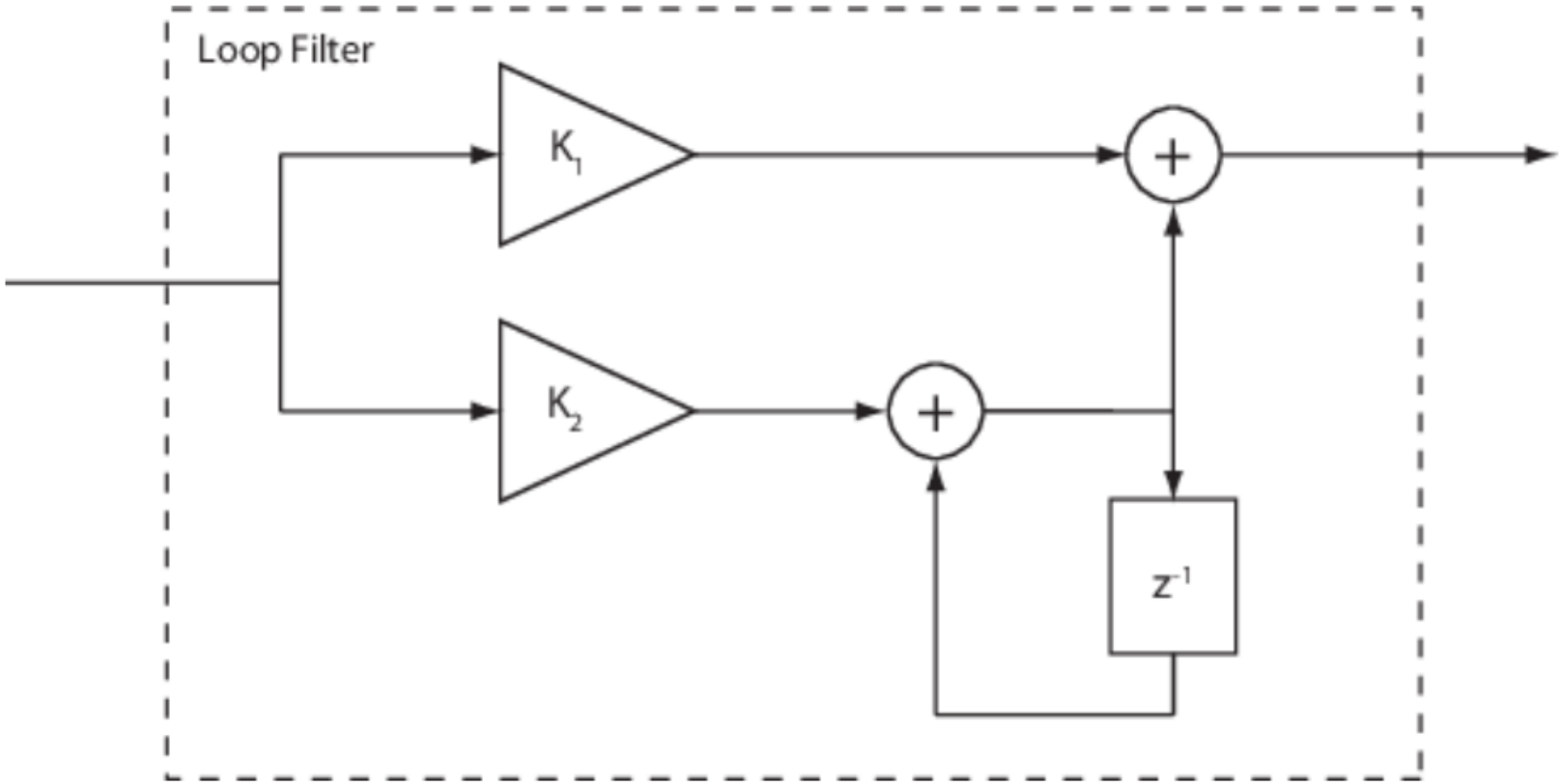
TED Method	Expression
Zero-crossing (decision-directed)	$e(k) = x\left((k-1/2)T_s + \widehat{\tau}\right)\left[\widehat{a}_0(k-1) - \widehat{a}_0(k)\right] + y\left((k-1/2)T_s + \widehat{\tau}\right)\left[\widehat{a}_1(k-1) - \widehat{a}_1(k)\right]$
Gardner (non-data-aided)	$e(k) = x\left((k-1/2)T_s + \widehat{\tau}\right)\left[x\left((k-1)T_s + \widehat{\tau}\right) - x(kT_s + \widehat{\tau})\right] + y\left((k-1/2)T_s + \widehat{\tau}\right)\left[y\left((k-1)T_s + \widehat{\tau}\right) - y(kT_s + \widehat{\tau})\right]$
Early-late (non-data-aided)	$e(k) = x(kT_s + \widehat{\tau})\left[x\left((k+1/2)T_s + \widehat{\tau}\right) - x\left((k-1/2)T_s + \widehat{\tau}\right)\right] + y(kT_s + \widehat{\tau})\left[y\left((k+1/2)T_s + \widehat{\tau}\right) - y\left((k-1/2)T_s + \widehat{\tau}\right)\right]$
Mueller-Muller (decision-directed)	$e(k) = \widehat{a}_0(k-1)x(kT_s + \widehat{\tau}) - \widehat{a}_0(k)x\left((k-1)T_s + \widehat{\tau}\right) + \widehat{a}_1(k-1)y(kT_s + \widehat{\tau}) - \widehat{a}_1(k)y\left((k-1)T_s + \widehat{\tau}\right)$

Interpolator




Interpolation Interval
Basepoint
Index
Sampling
Interval
Fractional
Interval
1
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
-1
0
100
200
300
400
500
600

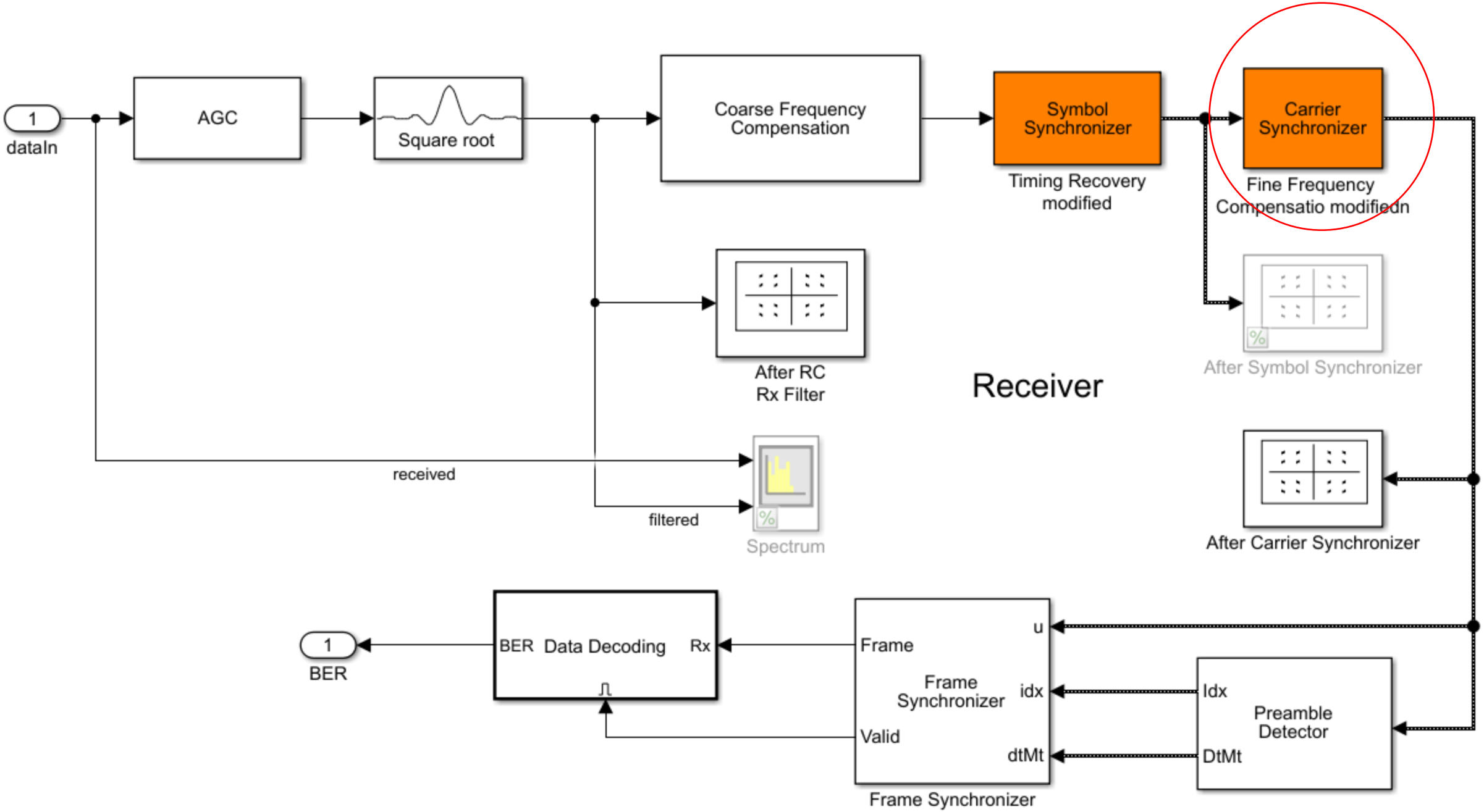
Loop Filter



References

[1] Rice, Michael. *Digital Communications: A Discrete-Time Approach*. Upper Saddle River, NJ: Prentice Hall, 2008.

[2] Mengali, Umberto and Aldo N. D'Andrea. *Synchronization Techniques for Digital Receivers*. New York: Plenum Press, 1997.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u
idx
dtMt
Frame Synchronizer
Idx
DtMt
Preamble Detector

Carrier Synchronizer

Compensate for carrier frequency offset

This block is similar in structure (phase-locked loop ot PLL) to the symbol synchronizer.

Frequency/phase correction is done by multiplying the incoming samples by a complex exponential with the negative of the estimated phase