ECSE-330, Introduction to Electronics (Fall 2015)

SPICE Assignment 1

Submission Guidelines:

1. Electronic submission through myCourses
2. On or before 11:55 pm, Friday, Nov. 13th, 2015
3. Submit in groups. Each group should contain 2 people and the group has to be the same throughout the term
4. Submit figures and files according to the requirement of each question

Question 1: Transconductance Amplifier

Consider the following transconductance amplifier in Fig. 1. Use the following values:

1. R_{sig} = 50 Ω, R_1 = R_2 = 100 kΩ, R_D = 10 kΩ, and R_L = 10 kΩ
2. C_1 = C_2 = 1 μF
3. g_m = 50 mA/V

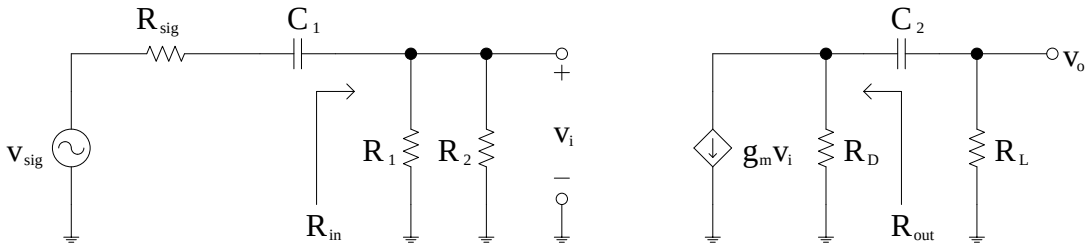

Figure 1: Transconductance Amplifier

(a) Provide the circuit diagram with nodes numbered, and the corresponding circuit (.cir) file

(b) Use a sinusoidal source v_{sig} with V_0 = 0 V, V_a = 1 V, freq = 10 Hz, t_d = 0 s, and damp = 0, then run transient analysis (.TRAN) from 0 to 1 s with time step size of 1 ms and provide the plots of the following parameters (and their peak-to-peak values): v_{sig}, v_i, v_o, and i_o.

(c) Use an AC source vsig with magnitude 1 V and phase 0 °, then run the AC frequency response (.AC DEC) from 10 Hz to 10 MHz with 10 points per decade. Provide the following plot (and find the 3 dB cutoff frequency on the plot): Av = v_o/v_{sig} in dB

(d) Find R_{in} and R_{out}. Provide the circuit diagrams, circuit (.cir) files, and figures showing R_{in} and R_{out}.

Question 2: Op-Amp Model

Fig. 2 shows an op-amp model with the following parameters:

R_{IN} = 1 MΩ, A_{OL} = 80 dB (what is this equivalent in V/V?), R_{OUT} = 50 Ω

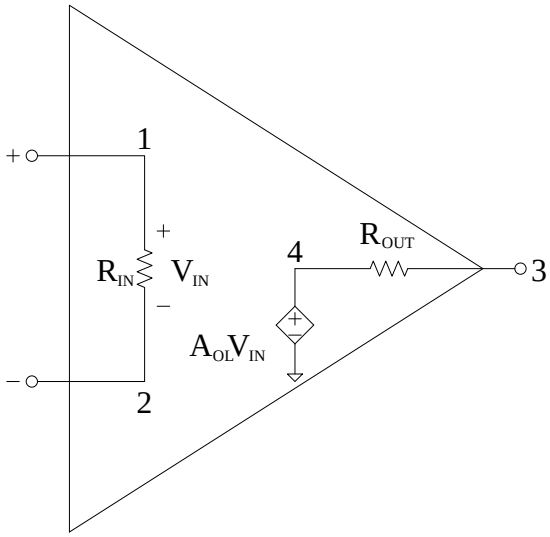

Figure 2: Op-Amp Model

Write the description for the parameters inside a sub-circuit:

```
*              non-inverting input
*              | inverting input
*              | | output
*              | | |
.SUBCKT opamp 1 2 3
     Description of the elements
.ENDS
```

You can use the model in your netlist in the following way (for example, in an inverting amplifier configuration where the inverting input is connected to ground):

```
*any name (after X)
*| non-inverting input
*| | inverting input
*| | | output
*| | | | model name
*| | | | |
X1 2 0 3 opamp
```

Build the standard testbench for the op-amp (as shown in Fig. 3) with:

1. Common voltage (V_{cm}, a DC volt source) at 1 V
2. Differential input voltage ($V_{in\text{-}diff}$, an AC volt source) with V_0 = 0 V, V_a = 5 mV, freq = 1 kHz, t_d = 0 s, and damp = 0
3. Load resistor R_L = 1 kΩ, and pick a reasonable value for R'

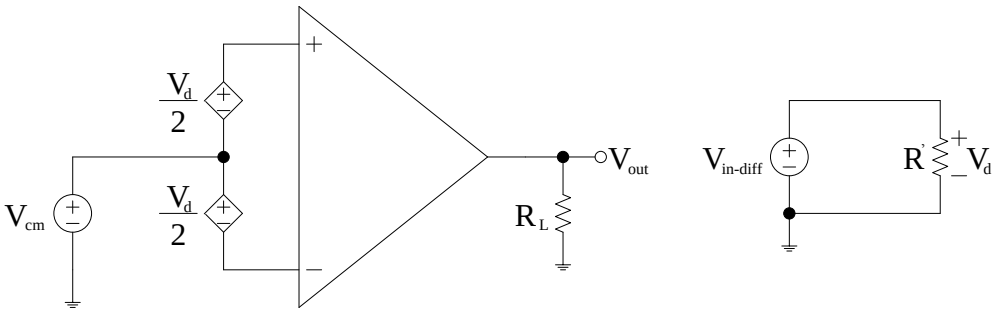

Figure 3: Standard Testbench for Op-Amp

Run a transient analysis (.TRAN) from 0 to 1 ms with a time step of size 1 μs, and provide:

1. Circuit diagram with nodes numbered, and the corresponding circuit (.CIR) file
2. Plot V_{in} (= $V_+ - V_-$) and V_{out} (separately, and clearly indicate the peak-to-peak values)

Question 3: Inverting Amplifier

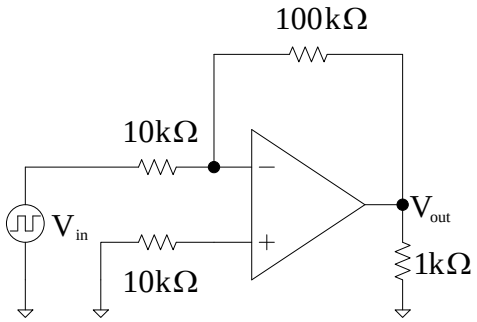

Figure 4: Inverting Amplifier

Fig. 4 shows an inverting amplifier (use the op-amp model from Question 2).

Use a pulse signal (PULSE (V_1 V_2 t_d t_r t_f PW T)) with V_1 = -5 mV, V_2 = 5 mv, t_d = 0 s, t_r = 10 µs, t_f = 10 µs, PW = 0.49 ms, T = 1 ms as V_{in}, then run a transient analysis (.TRAN) from 0 to 5 ms with a time step of size 1 µs, and provide:

1. Circuit diagram with nodes numbered, and the corresponding circuit (.CIR) file
2. Plot V_{in} and V_{out} (separately, and clearly indicate the peak-to-peak values)

Question 4: Non-Inverting Amplifier

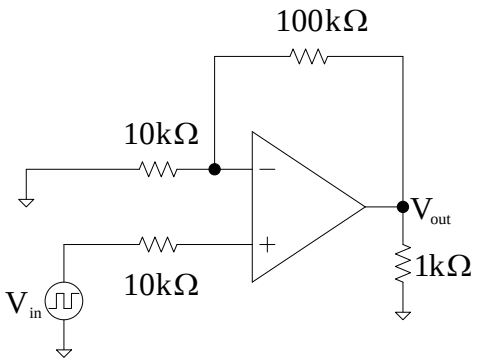

Figure 5: Non-Inverting Amplifier

Fig. 5 shows a non-inverting amplifier (use the op-amp model from Question 2).

Use a pulse signal (PULSE (V_1 V_2 t_d t_r t_f PW T)) with V_1 = -5 mV, V_2 = 5 mv, t_d = 0 s, t_r = 10 µs, t_f = 10 µs, PW = 0.49 ms, T = 1 ms as V_{in}, then run a transient analysis (.TRAN) from 0 to 5 ms with a time step of size 1 µs, and provide:

1. Circuit diagram with nodes numbered, and the corresponding circuit (.CIR) file
2. Plot V_{in} and V_{out} (separately, and clearly indicate the peak-to-peak values)

Question 5: Non-Inverting Amplifier with Diode in the Feedback Loop

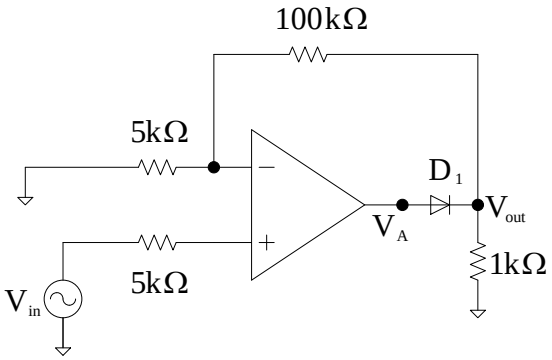

Figure 6: Non-Inverting Amplifier with Diode in the Feedback Loop

Fig. 6 shows a non-inverting amplifier (use the op-amp model from Question 2) with a diode in the feedback loop. Use the following model for the diode D_1:

```
.model dmodel d(Is=1e-9 n=1.8)
```

Use a sinusoidal signal (V_{in}) with V_0 = 0 V, V_a = 100 mv, freq = 1 kHz, t_d = 0 s, damp = 0, then run a transient analysis (.TRAN) from 0 to 5 ms with a time step of size 1 μs, and provide:

1. Circuit diagram with nodes numbered, and the corresponding circuit (.CIR) file
2. Plot V_{in}, V_{out}, V_A, V+ and V- (separately, and clearly indicate the peak-to-peak values)

Question 6: Biasing MOSFET Amplifier

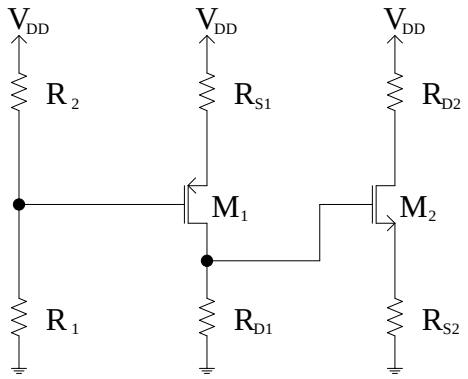

Figure 7: Biasing MOSFET Amplifier

Fig. 7 shows the DC biasing of two MOSFETs, which contains the following circuit elements:

1. $R_1 = R_2 = 10\ M\Omega$, $R_{D1} = 2.5\ k\Omega$, $R_{S1} = 1\ k\Omega$, $R_{D2} = 1\ k\Omega$ and $R_{S2} = 500\ \Omega$
2. M_1: L = 20 µm, W = 350 µm
3. M_2: L = 20 µm, W = 100 µm

SPICE description for NMOS:

```
*any name (after M)
*|    Drain
*|    | Gate
*|    | | Source
*|    | | | Substrate
*|    | | | |  MOS model
*|    | | | |  |          Length
*|    | | | |  |          |       Width
*|    | | | |  |          |       |
Mname d g s st model_name L=value W=value

.MODEL model_name NMOS parameter_name=value
```

SPICE description for PMOS:

```
*any name (after M)
*|    Drain
*|    | Gate
*|    | | Source
*|    | | | Substrate
*|    | | | |  MOS model
*|    | | | |  |          Length
*|    | | | |  |          |       Width
*|    | | | |  |          |       |
Mname d g s st model_name L=value W=value

.MODEL model_name NMOS parameter_name=value
```

Use the following models for NMOS (nfet) and PMOS (pfet):

```
.MODEL nfet NMOS LEVEL=3 PHI=0.600000 TOX=2.1200E-08
+ XJ=0.200000U TPG=1 VTO=0.7860 DELTA=6.9670E-01
+ LD=1.6470E-07 KP=9.6379E-05 UO=591.7 THETA=8.1220E-02
+ RSH=8.5450E+01 GAMMA=0.5863 NSUB=1.6160E+16
+ NFS=5.0000E+12 VMAX=2.0820E+05 ETA=7.0660E-02
+ KAPPA=1.3960E-01 CGDO=4.0241E-10 CGSO=4.0241E-10
+ CGBO=3.6144E-10 CJ=3.8541E-04 MJ=1.1854
+ CJSW=1.3940E-10 MJSW=0.125195 PB=0.800000

.MODEL pfet PMOS LEVEL=3 PHI=0.600000 TOX=2.1200E-08
+ XJ=0.200000U TPG=-1 VTO=-0.9056 DELTA=1.5200E+00
+ LD=2.2000E-08 KP=2.9352E-05 UO=180.2 THETA=1.2480E-01
+ RSH=1.0470E+02 GAMMA=0.4863 NSUB=1.8900E+16
+ NFS=3.46E+12 VMAX=3.7320E+05 ETA=1.6410E-01
+ KAPPA=9.6940E+00 CGDO=5.3752E-11 CGSO=5.3752E-11
+ CGBO=3.3650E-10 CJ=4.8447E-04 MJ=0.5027
+ CJSW=1.6457E-10 MJSW=0.217168 PB=0.850000
```

Note: Substrate Connection

A MOSFET is in fact a 4-terminal device. These 4 nodes are gate, source, drain and substrate (or sometimes called bulk). Usually, in a circuit diagram, we do not plot the substrate node connection.

It is desired that, for the same MOSFET, its substrate node is connected to its source node. However, in reality this might not be straight forward to implement. Therefore, circuit designers usually connect the substrate nodes of all NMOS to ground, and the substrate nodes of all PMOS to V_{DD}.

In this assignment, please assume the above is true for the substrate connections.

For this question, submit the circuit diagram with nodes numbered, and the corresponding circuit (.CIR) file. Sweep the value of V_{DD} from 0 to 30 V using a step size of 0.1 V, then provide:

1. Plot V_{SG1} and V_{SD1} on the same graph and mark the values at V_{DD} = 20 V
2. Plot V_{GS2} and V_{DS2} on the same graph and mark the values at V_{DD} = 20 V
3. Plot I_{D1} and I_{D2} on the same graph and mark the values at V_{DD} = 20 V

Question 7: MOSFET Amplifier

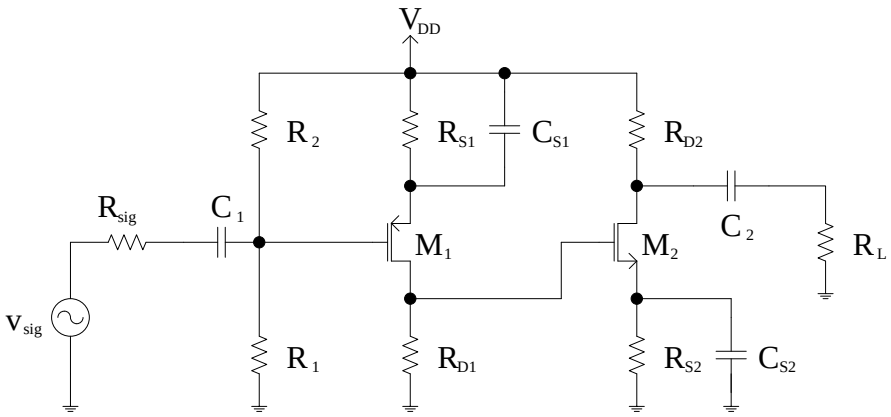

Figure 8: MOSFET Amplifier

Fig. 8 shows a two-stage MOSFET amplifier, which contains the following circuit elements:

1. $R_1 = R_2 = 10\ M\Omega$, $R_{D1} = 2.5\ k\Omega$, $R_{S1} = 1\ k\Omega$, $R_{D2} = 1\ k\Omega$, $R_{S2} = 500\ \Omega$, $R_{sig} = 50\ \Omega$, $R_L = 1\ k\Omega$
2. M_1: L = 20 µm, W = 350 µm
3. M_2: L = 20 µm, W = 100 µm
4. $C_1 = C_2 = C_{S1} = C_{S2} = 100\ \mu F$
5. $V_{DD} = 20\ V$

First, provide a circuit diagram with all nodes numbered. You can use the same transistor model and substrate connection as in Question 6.

Use a sinusoidal signal as v_{sig} with $V_0 = 0$ V, $V_a = 5$ mV, freq = 1 kHz, $t_d = 0$ s, and damp = 0, and run a transient analysis from 0 to 5 ms with a step size of 1 µs. Provide:

1. The circuit (.CIR) file
2. Plot v_{sig} and v_{out} on the same graph and mark the peak values
3. Plot V_{SG1}, V_{SD1}, V_{GS2}, V_{DS2}, I_{D1} and I_{D2} respectively, and mark the peak values

Then use an AC source with magnitude of 5 mV and phase = 0 °, and run an AC frequency response (.AC DEC) from 1 mHz to 1 GHz using 10 points each decade. Provide:

1. The circuit (.CIR) file
2. Plot the overall gain in dB using log scale for frequencies and mark the gain at 10 kHz
3. Mark the 3 dB cutoff gain (and the corresponding frequencies) on the same graph