ECSE-330, Introduction to Electronics (Fall 2015)

SPICE Assignment 2

Due on or before: 11:30 pm, Monday, Dec. 7th, 2015

Submission Guidelines:

1. Due on or before 11:30 pm, Monday, Dec. 7th, 2015
2. Submit one solution per group
3. Submit your report as one PDF file with all relevant plots and information describing your design
4. Describe the process you used to optimize your circuit and include the equations you used. You do not need to include the derivation of any basic equation (e.g. expressions for the gain, output resistance, etc.), but you can include the derivation of non-standard equations you use
5. Write a short conclusion describing the various compromises and how optimizing one aspect of the problem compromises the rest

Important: There is no single answer to this problem. We do not expect you to find the optimum design, but rather to improve on the current design in a systematic way. Full marks will be given even if the design is sub-optimum as long as the process is reasonable and models/equations are correct.

Design of a Cascode Amplifier in SPICE

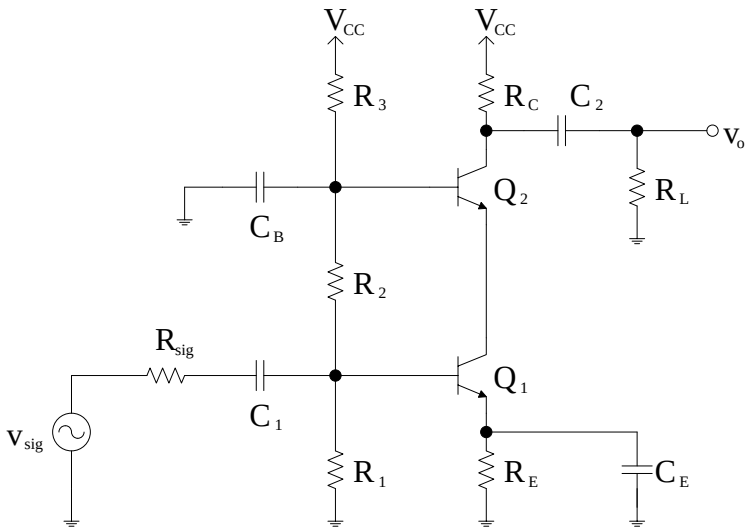

Figure 1: Cascode Amplifier

In the Cascode amplifier shown in Fig. 1:

1. V_{CC} = 15 V
2. $R_{sig} = R_L$ = 1 kΩ
3. In order to minimize the cost of your design, you can use at most one 100 μF capacitor. All other capacitors must be less than 5 μF.

You will have access to the general purpose NPN transistor (model #: MPS2222A) manufactured by ON Semiconductor®. Its SPICE model is:

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*MPS2222A MCE 1/26/96
*Si 625mW  40V 600mA 300MHz pkg:TO-92 1,2,3
.MODEL QMPS2222A NPN (IS=.504F NF=1 BF=339 VAF=113 IKF=.36 ISE=1.63P NE=2
+ BR=4 NR=1 VAR=24 IKR=.54 RE=.173 RB=.692 RC=69.2M XTB=1.5
+ CJE=23.5P VJE=1.1 MJE=.5 CJC=10.6P VJC=.3 MJC=.3 TF=521P TR=272N)
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You will also have access to the following resistors, all rated at ¼ W:

10 Ω, 12 Ω, 15 Ω, 18 Ω, 22 Ω, 27 Ω, 33 Ω, 39 Ω, 47 Ω, 56 Ω, 68 Ω, 82 Ω;

100 Ω, 120 Ω, 150 Ω, 180 Ω, 220 Ω, 270 Ω, 330 Ω, 390 Ω, 470 Ω, 560 Ω, 680 Ω, 820 Ω;

1 kΩ, 1.2 kΩ, 1.5 kΩ, 1.8 kΩ, 2.2 kΩ, 2.7 kΩ, 3.3 kΩ, 3.9 kΩ, 4.7 kΩ, 5.6 kΩ, 6.8 kΩ, 8.2 kΩ;

10 kΩ, 12 kΩ, 15 kΩ, 18 kΩ, 22 kΩ, 27 kΩ, 33 kΩ, 39 kΩ, 47 kΩ, 56 kΩ, 68 kΩ, 82 kΩ;

100 kΩ, 120 kΩ, 150 kΩ, 180 kΩ, 220 kΩ, 270 kΩ, 330 kΩ, 390 kΩ, 470 kΩ, 560 kΩ, 680 kΩ, 820 kΩ, and 1 MΩ

For capacitors, you can use at most one 100 μF capacitor. All other capacitors must be less than 5 μF, and you have access to the following values:

1 μF, 2.2 μF, 3.3 μF, and 4.7 μF

In this assignment, you are asked to design a Cascode amplifier (in this case, the values of R_1, R_2, R_3, R_C, R_E, C_1, C_2, C_B and C_S) in SPICE so that it meets the following minimum design requirements:

- Overall gain G_v (= v_o/v_{sig}) ≥ 25 V/V
- Bandwidth (3-dB frequencies) $f_L \leq 350$Hz, and $f_H \geq 1$ MHz.
- Output voltage swing (peak-to-peak) ≥ 0.5 V
- DC power consumption ≤ 30mW

Meanwhile, your design is bounded by the following design constraints:

- You can only use the available resistance and capacitance values given to you
- To guarantee the bias stability, your design needs to satisfy both of the following conditions (both of these conditions are discussed in details in Section 6.7.1 in Sedra & Smith, 6th Edition, and Section 7.4.2 in the 7th Edition):
    - Currents through R_1, R_2 and R_3 >> base currents of Q_1 and Q_2. For your design, set the bias current in R_1, R_2 and R_3 to be at least $10 \times I_B$.
    - V_{BB} >> V_{BE} for both Q_1 and Q_2. For your design, set $V_{B1} \geq 3$V and $V_{B2} \geq 5$V.
- While considering the output voltage swing, keep in mind that the circuit will become non-linear if v_{be} of Q_1 or Q_2 is greater than $10mV_{pk-pk}$.

In your submission, in addition to your design objectives, please also report on the following values both using hand computation and SPICE simulation:

- R_{in} and R_{out}
- DC voltages at each node
- DC currents through each device (for Q_1 and Q_2, DC current into each terminal).

Design Optimization:

Optimize your design so that the DC power consumption is minimized while still meeting all other design requirements.

Content of Report

1. The final design that meets the minimum design requirements.
2. An explanation of the design process used including equations and derivations (you do not need to derive standard formulas such as gain, input and output resistance).
3. The optimized design that minimizes DC power consumption.
4. An explanation of the process used to optimize the design along with equations and derivations.
5. SPICE simulations and plots that show all design requirements (Gain, bandwidth, input/output impedance, power consumption …).
6. Comparison of results from had computations with results from simulation.
7. Conclusion highlighting the key compromises of the design and providing guidance and insight for future designers trying to design a similar circuit.