Circuit Under Test

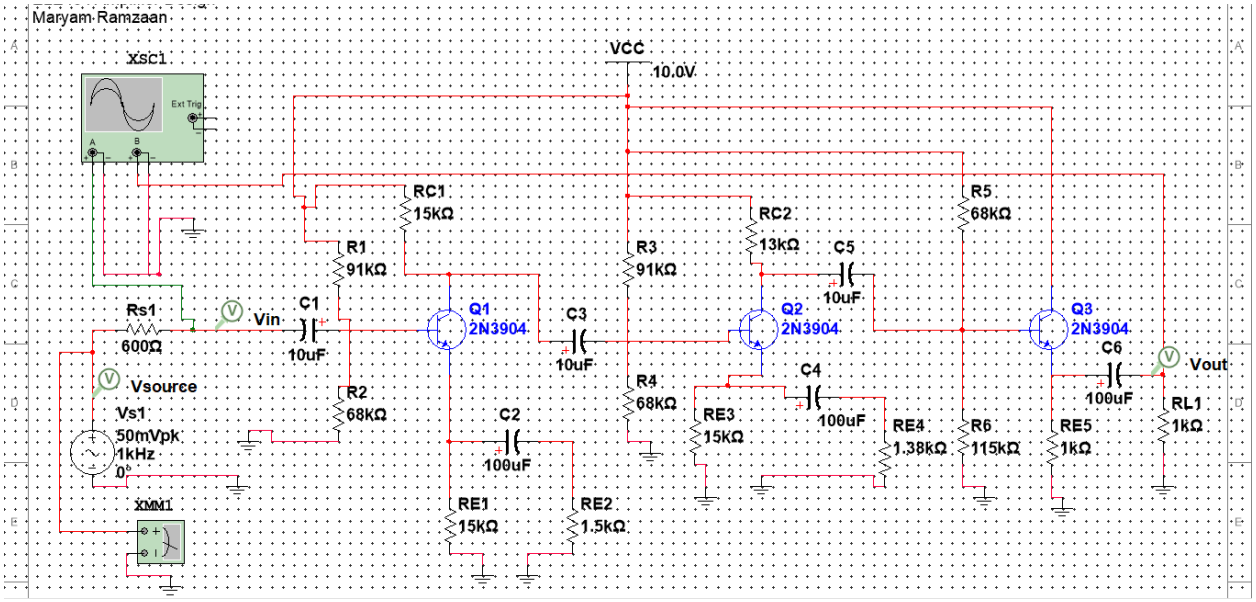

Figure 1: Amplifier circuit simulation created by cascading two CE amplifiers with a CC amplifier

Graphs

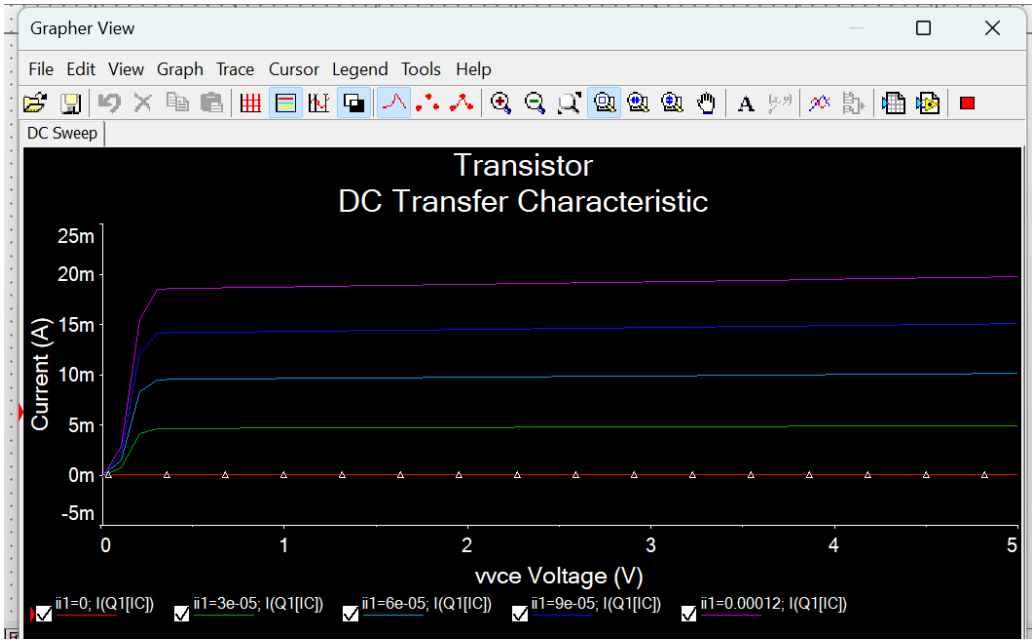

Figure 2: characteristic graph of the 2N3904 BJT

Justifications

Calculation Process

To design an amplifier that meets the stated objectives, it was assumed that a circuit with two common emitter BJTs and a common collector would be suitable. A voltage source of 50m Vpk with a frequency of 1kHz was used to power the circuit, as well as a Vcc value of 10V. Three NPN Bipolar junction transistors were used as well as six capacitors to separate each of the three transistors followed by a load resistor R_L which was removed at certain points of this project to determine whether its presence would create changes among other measurements in the circuit. Furthermore, the chosen load line was 5V for the operation point, and 4.25 for the corresponding CE Voltage for this project although it is not shown and done manually.

As for the calculations, the voltage gain was considered first to fulfill the requirement for $A_{vo} \leq 50$. Since A_{vo}=$A_{vo1} \times A_{vo2} \times A_{vo3}$, and since the third amplifier is a common collector one, its A_{vo}= 1 because voltage gains of the CC amplifier are close to unity, and since the rest of the BJTs were CE, it made sense to assume $A_{vo1} = A_{vo2}$. Two numbers with a product of 50 is about $\sqrt{50} = \pm\ 7.1$. Throughout the calculation, it was recognized that both no-voltage gains needed to be -7.1, and that would yield a non-inverting amplifier as the product would be a positive A_{vo} of $50\frac{V}{V}$. Apart from making calculations simpler, the CC amplifier would not be impacted by the removal and addition of the load resistor, making the circuit stable.

To determine the values of $R_{ES} and\ R_6$, the third amplifier, or stage 3 was considered. Since the values of the resistors could only be those found in the ELE404 lab kit, it was assumed that R_5 had a value of $68k\Omega$. To find R_{E3}, the second stage was considered, and Kirchoffs voltage law and R_{c2} and R_{E4} at the transistor, Q2. Lastly, the capacitor values were calculated for best and worst cases, as well as the quiescent current. All capacitors that were positioned before the BJT, was given the value of $10\ \mu F$, and the capacitors parallel to the R_e in each of the three stages were $100\ \mu F$.