CO HW7

1. Problem 4-1

   Show the block diagram of the hardware (similar to Fig. 4-2a) that implements the following register transfer statement: yT2: R2 <- R1, R1+R2

2. Problem 4-4

What has to be done to the bus system of Fig. 43 to be able to transfer information fromany register to anyother register? Specifically, show the connectionsthat must be included to provide a path fromthe outputsof register C to the inputs of registerA.

Connect the bus to the input of the 4 registers.
Provide load control inputs in the 4 registers.
Provide clock inputs for the 4 register.
To transfer from register C to register A:
- Apply S1 S0 = 10
- Enable the load input of A
- Apply a clock pulse.

3. Problem 4-5

Draw a diagram of a bus system similar to the one shown in Fig. 4-3, but use three-state buffers and a decoder instead of the multiplexers.

4. Problem 4-8

Draw the block diagram for the hardware that implements the following statements:

x + yz: AR <- AR + BR

where ARand BR are two - b i tregisters andx, y, and z are control variables. Include the logic gates for the control function. (Remember that the symbol + designates an OR operation in a control or Boolean function but that it represents an arithmetic plus in a microoperation.)

5. Problem 4-11

Using a 4-bit counter with parallel load as in Fig. 2-11 and a 4-bit adder as in Fig. 4-6, draw a block diagram that shows how to implement the following statements:

x: R1 <- R1 + R2 Add R2 to R1

x'y: R1+R1 +1 Increment R1

where R1 is a counter with parallel load and R2 is a 4-bit register.

6. Problem 4-14

Assumethat the 4-bit arithmetic circuit of Fig. 4-9 is enclosed in one IC package. Show the connectionsamong two such ICs to forman 8-bit arithmetic circuit.

7. Problem 4-16

Derive a combinational circuit that selects and generates any of the 16 logic functions listed in Table 4-5.

8. Problem 4-18

Register A holds the 8-bit binary 11011001. Determine the B operand and the logic microoperation to be performed in order to change the value in A to:

a 01101101

b . 11111101

(a) 1101001

⊕ 1011100

0110101

B = 0110100

A ⊕ B

(b) 1101001

∨ 1111101

1111101

B = 1111101

A ∨ B

9. Problem 4-20

An 8-bit register contains the binary value 10011100. What is the register value after an arithmetic shift right? Starting from theinitial number 10011100, determine the register value after an arithmetic shift left, and state whether there is an overflow.

to right:

11001110

to left:

00111000

overflow

(negative to positive)

10. Problem 4-23

What is wrong with the following register transfer statements?

a. xT: AR <- AR(with hat), AR <- 0

b. yT: R1 <- R2, R1 <- R3

c. zT: PC <-AR, PC <- PC+1

a. can't complement, implement at the same time

b. can't tranfer different values to R_1 at the same time

c. Can't tranfer a value, then increment the original value at the same time

11. Given the 16-bit operand 00001111 10101010, what operation must be performed and what operand must be used

a. to clear all even bit positions to 0? (Assume bit positions are 15 through 0 from left to right.)
b. to set the leftmost 4 bits to 1?
c. to complement the center 8 bits?

a. and with 0101010101010101

b. or with 1111000000000000

c. xor with 0000000011110000

12. A switch-tail ring counter (Johnson counter) uses the complement of the serial output of a right shift register as its serial input.

a. Starting from an initial state of 0000, list the sequence of states after each shift until the register returns to 0000.

b. Beginning in state 00 ... 0. how many states are there in the count sequence of an n-bit switch-tail counter?

13. Two conditional register transfer statements are given (R1 is unchanged if condition fails):

C1 : R1 <- R1 + R2 Add R2 to R1

C1′C2: R1 <- R1 + 1 Increment R1

a. Using a 4-bit counter with parallel load and a 4-bit adder, draw the logic diagram that implements these register transfers.

b. Repeat part (a) using a 4-bit adder plus external gates as needed. Compare with the implementation in part (a).

14. Show the diagram of the hardware that implements the register transfer statement:

C3: R2 <- R1; R1 <- R2

R1
R2