# CS 2614: Computer Organization
# Lab 5

**Spring 2023**

## 2-Bit Adder/Subtractor/Multiplier

| Student ID | Name |
|---|---|
| 113591341 | Kyumin Lee |
| 113597404 | Isaac Stein |

The UNIVERSITY of OKLAHOMA

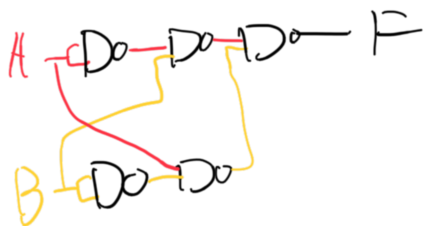
*Gallogly College of Engineering*

School of Computer Science

# Pre-Lab Exercise

1. Draw the circuit diagram for the XOR function (using NAND gates only).

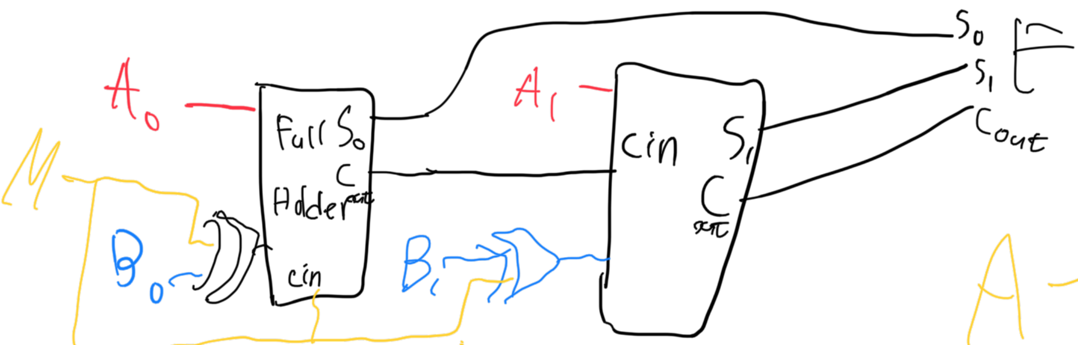
$Y = A'B + AB'$



$((A'B + AB')')'$

$((A'B)' \cdot (AB')')'$

2. Design a 2-bit adder/subtractor circuit [You can use blocks of 1-bit Full Adder in your design].



0 = Sum

1 = Sub

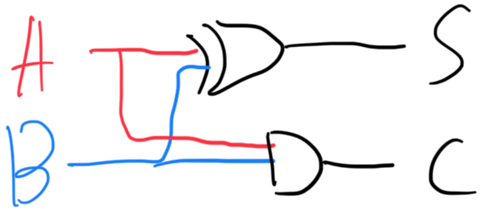
$A - B = A + \bar{B} + 1$

3. Compute the following 2-bit binary multiplication (show all steps):

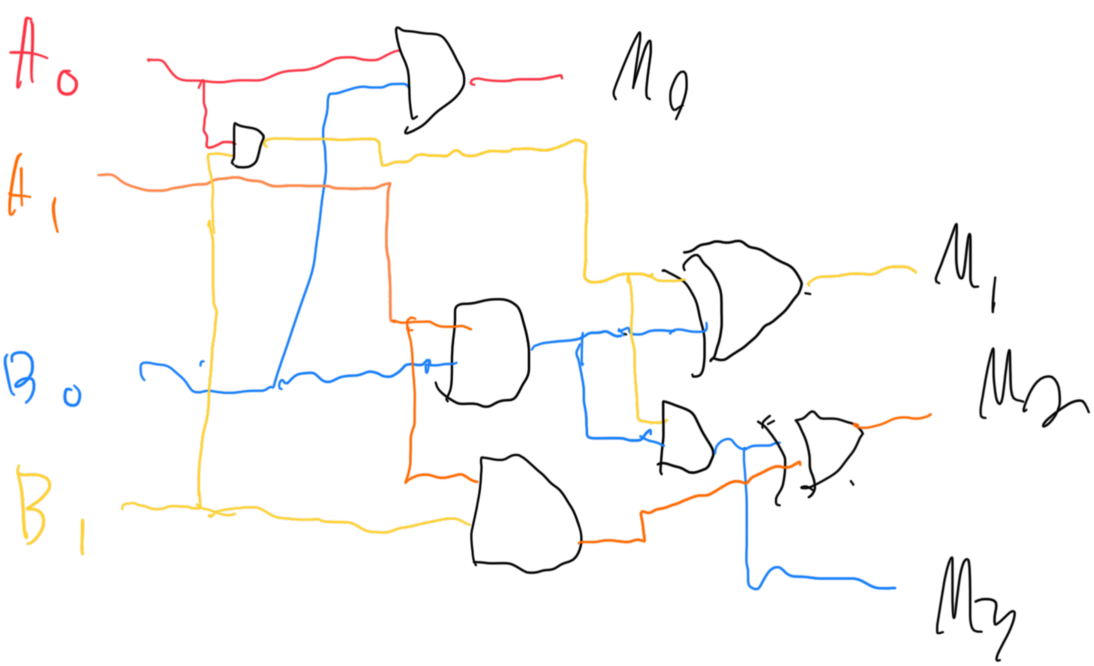
```
    11      3
*   10    * 2
------    ---
    00      6
  110
------
   110
```

4. Draw the circuit diagram and truth table for a half-adder.

| A | B | S | C |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |



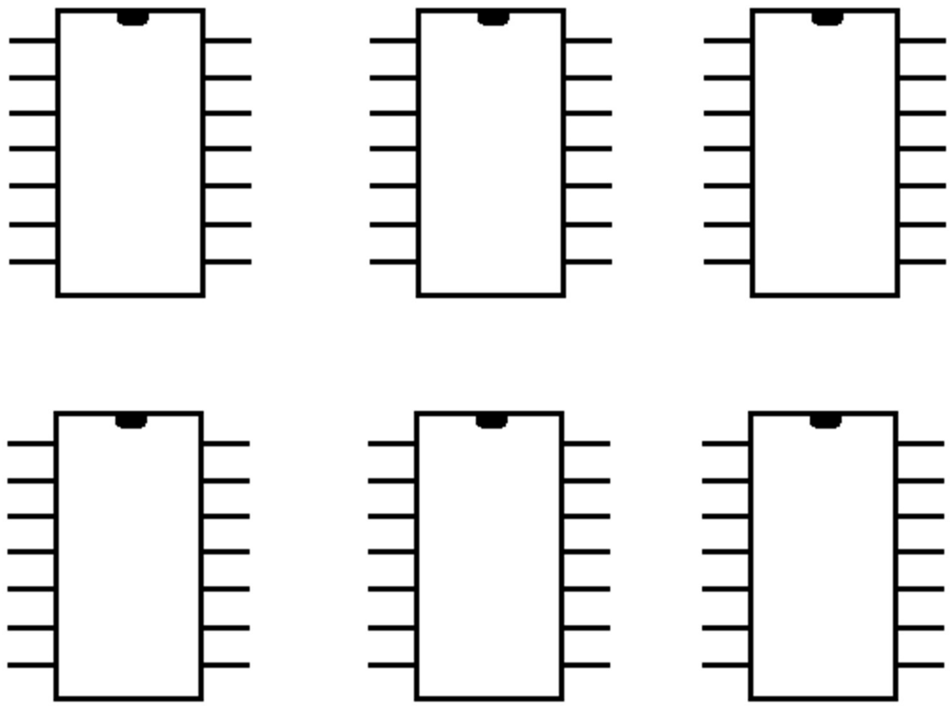

5. Design a 2-bit binary multiplier [Hint: design in Q4 can be useful].




***Remember to upload this to Canvas***

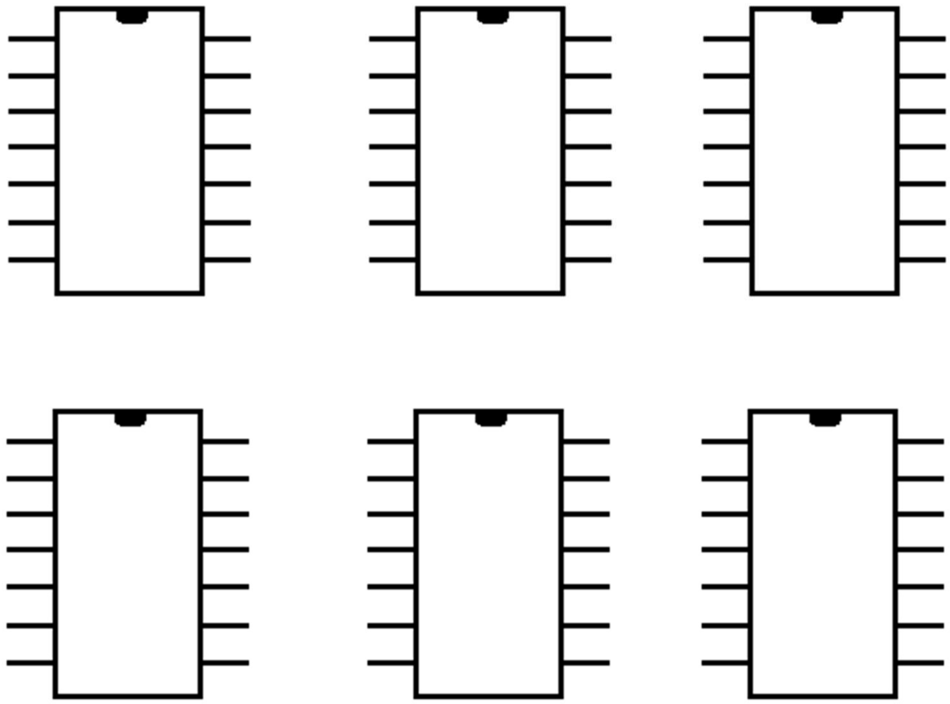
# In-Lab Exercise

6. Draw the circuit from Problem 2 using the chips given below (label the chips and each input/output, **<u>some chips may not be needed</u>**).



7. Implement the circuit of Problem 6 on the breadboard using a SN74F283 (4-bit binary full adder) and NAND gates only [Hint: Use one bit of the 4-bit binary full adder chips].

8. Draw a circuit from Problem 5 using the chips given below (label the chips and each input/output, **some chips may not be needed**)



9. Implement the circuit of Problem 8 on the breadboard.