# Optimized AC/DC Dual Active Bridge Converter using Monolithic SiC Bidirectional FET (BiDFET) for Solar PV Applications

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***Abstract*—Grid interface power conversion systems for commercial, industrial and residential solar power generation are becoming ubiquitous due to the competitive cost of solar energy. The AC/DC dual active bridge (DAB) converter is an upcoming topology in industrial PV energy and energy storage applications, providing bidirectional power transfer and galvanic isolation. In this paper, the properties of a DAB-type converter are leveraged to propose a design optimization process. It can optimize the high-frequency RMS current, size of magnetic elements and zero-voltage-switching (ZVS) region of the converter. The resulting design is compared against that derived from a conventional approach. In addition, an algorithm to compute the harmonic currents at the DC and line frequency AC ports of the system is proposed, and the respective filter designs are presented. The optimized design of the AC/DC DAB converter is implemented using the newly developed, 1200 V, 46 mΩ, four quadrant, SiC-based monolithic bidirectional FETs (BiDFET). Experimental results from the 2.3 kW, 400V/277$V_{RMS}$ hardware prototype are finally presented to verify the design process.**

***Index Terms*—Bidirectional isolated AC-DC conversion, solar energy, PV grid integration, dual active bridge, AC/DC DAB, SiC bidirectional FET, BiDFET, four quadrant power switch.**

## I. Introduction

The declining capital and operational costs of solar power has resulted in its rapid adoption in the commercial and industrial energy generation. The 2020 Annual Technology Baseline data from National Renewable Energy Laboratory (NREL) [1] suggests that with 'moderate' technology outlook, the levelized cost of energy per MWh for commercial, distributed solar in cities like Los Angeles will reduce from the baseline of US$ 70 to US$ 32 in 2030.

A key component in distributed solar installed for commercial-industrial energy generation is the power conversion system to interface with the utility grid at standard nominal voltages. For low voltage systems in North America, these are 208Y/120 V, 240Δ/120 V and 480Y/277 V [2]. Among these, a common single-phase voltage level available for high power loads is a) the 277 V level derived from 3-phase, 4-wire, 480 V system, or b) the 240 V level derived from 240 V-Δ system. The high power loads include lighting devices such as fluorescent and high pressure vapor lamps, heating appliances, unitary air conditioners and heat pumps, electric furnaces, motor compressors and comfort heating.

A mandatory requirement from the article 690 of the NEC [3] is system grounding and fault monitoring on the PV side. In single-phase solar power converter systems, it translates to grounding on its DC as well as its AC port [4]. Therefore, in the US, most modern single-phase grid-connected solar converter topologies comprise of high frequency transformers for galvanic isolation. In this paper, a single phase AC/DC dual active bridge (DAB) converter is considered for supplying solar generated power to the low voltage distribution grid. The topology derived from the popular DC/DC DAB converter [5] was first reported in [6]. It provides galvanic isolation and, if appropriately modulated, soft-switching capability across the operating load range and line cycle voltage.

The AC/DC DAB converter comprises of two full-bridge circuits generating high frequency AC square-wave voltage across a transformer-inductor arrangement. One version of the AC/DC DAB rectifier involves a diode bridge (or synchronous) rectifier as a front-end system, followed by a DAB DC/DC converter [7]. The front-end rectifier folds the bipolar AC grid voltage to a unipolar rectified AC voltage. The topology is evidently not feasible for the inverter operation. The second version of the AC/DC DAB converter that allows rectifier/inverter operation uses four quadrant power semiconductor (4-QPS) switches. These devices can block voltage and carry current in either direction, and may be constructed using commercially available discrete semiconductor devices. Alternatively, reverse-blocking IGBTs may also be utilized as 4-QPS devices.

In this paper, the AC/DC DAB converter is implemented using a 1200 V SiC-based monolithic bidirectional FET (BiDFET) [8], as shown in Fig. 1. The four-terminal 1200 V SiC-BiDFET has a pair of gate and source terminals for each of the constituent FETs. It is fabricated as a single die (Fig. 2a) at the commercial foundry (X-FAB) using an NC State University engineered process [9], [10] and packaged at NC State University [11]. The performance characterization

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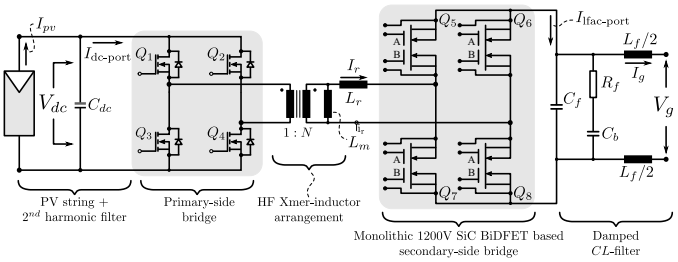



Fig. 1: Schematic of the single phase AC/DC DAB circuit using the monolithic 1200 V SiC bidirectional FETs (BiDFET).

data for the switching and conduction of 1200 V SiC-BiDFET up to 800 V, 20 A is reported in [12]. The monolithic device reduces the semiconductor component count and bond-wire sets, thereby improving the reliability of the grid-connected solar power converter system.

The main contribution of this paper is to establish an optimization procedure to design an AC/DC DAB converter. The advanced modulation schemes developed for the DAB DC/DC converter [13] are also applied to its AC/DC version for optimal operation [14]. However, the reported literature [6], [14], [15] does not encompass all the operating modes of the converter, and therefore, the optimization problem is limited in its scope. In this paper, a method to design the AC/DC DAB converter is proposed, that includes all its modulation strategies and operating modes. The design may be optimized for minimum RMS current, minimum transformer VA rating or other objective function.

Further, the calculation reported in the literature [15] for harmonic current at its AC and DC ports is mode-dependent; it also does not encompass the complete operating range. Therefore, an algorithm based on a singular, explicit model is proposed to compute the harmonic currents at its DC and grid-side AC ports. The proposed model is also used in the design of the respective filters.

The resultant solution of the design optimization procedure may be implemented in either of the two variations of AC/DC DAB converter: a) line frequency rectifier followed by DC/DC DAB converter [7], [14], and b) single-stage converter comprising of four quadrant power semiconductor (4-QPS) devices [6], [15]. In this paper, considering the application of solar power converter system, a SiC-BiDFET based AC/DC DAB converter hardware prototype is developed based on the optimized design. The experimental results at full power, input DC and grid AC voltages of 2.3 kW, 400 V and 277 $V_{RMS}$ are presented. In addition, the total harmonic distortion (THD) in grid-side current at full-load and efficiency of the system throughout the operating load range are also presented.

The paper is organized as follows: section II briefly describes the fabrication, packaging and characterization of NC State University-engineered 1200 V SiC-BiDFET. Section III reviews the basic operation and modulation strategies of the AC/DC DAB converter. It also extends the expressions of switching instant and RMS currents as well as power transfer from the DC/DC DAB converter to its AC/DC version. Section IV formulates the optimization problem including the definition of design space, feasible objective functions and constraints. The design solution derived using proposed strategy is also compared against the conventional strategy in this section. Further, in section V, an algorithm to compute the harmonic currents at the AC and DC ports of the converter and the respective filter design strategies are presented. In section VI, experimental results on a 2.3 kW hardware prototype are also presented to verify the proposed design.

## II. NC State University's 1200 V SiC Bidirectional Field Effect Transistor (BiDFET)

### A. Fabrication

The four terminal monolithic 4H-SiC 1200 V BiDFET, first proposed in [8] and [10], was fabricated at the six-inch commercial foundry, X-FAB, using the NCSU PRECiSE$^{TM}$ process [9]. A 2-D centerline cross-section of the die is shown in Fig. 2a for one of the integrated JBSFETs (MOSFETs with integrated JBS diodes). The fabricated BiDFET die has a large chip area of approximately 1.1 cm$^2$ with 0.45 cm$^2$ of active area for each internal JBSFET. The design includes two gate-pads for each JBSFET. The die demonstrated a low on-state resistance of 46 m$\Omega$, threshold voltage of 1.73 V, transconductance of 17 S, and reverse transfer capacitance of 55 pF. Further details on the fabrication process of the BiDFET are found in [10].

### B. Packaging

The packaging of the 1200 V BiDFET die uses organic laminates such as, in this case, a flex-PCB or substrate made of polyimide material. The package layer stack (Fig. 2b) was designed to provide twelve pin-outs: a pair of gate and Kelvin source connections for each internal JBSFET, and two pins each for the current carrying terminals of the device, as shown in Fig. 2c. The BiDFET bare-die and its terminals were encapsulated in a 24.5 $\times$ 14.5 $\times$ 3.2 mm$^3$ frame. The copper slug, electrically connected to the common-drain of the BiDFET, is attached to transfer the heat generated within the die to the heat sink. Further details on the packaging of the 1200 V SiC-BiDFET are found in [11].

### C. Characterization

The fabricated and packaged 1200 V SiC-BiDFET was characterized for its static and dynamic behavior. The static characterization, conducted using a curve tracer, measured parameters such as on-state resistance, transconductance and breakdown voltage. In addition, dynamic characterization was conducted with a BiDFET phase leg configured for clamped inductive switching test at a DC link voltage of 800 V, on-state current of 20 A, and a gate resistance of 10 $\Omega$. The measured on-state characteristics of the BiDFET device is symmetrical in the first and third quadrant as shown in Fig. 2d. The on-state resistance is 46 m$\Omega$ at 10 A and 20 V gate bias. Further, the loss data during the turn-on and turn-off of the device derived from the clamped inductive switching test are plotted in Fig. 2e. Additional details regarding device characterization are found in [12].

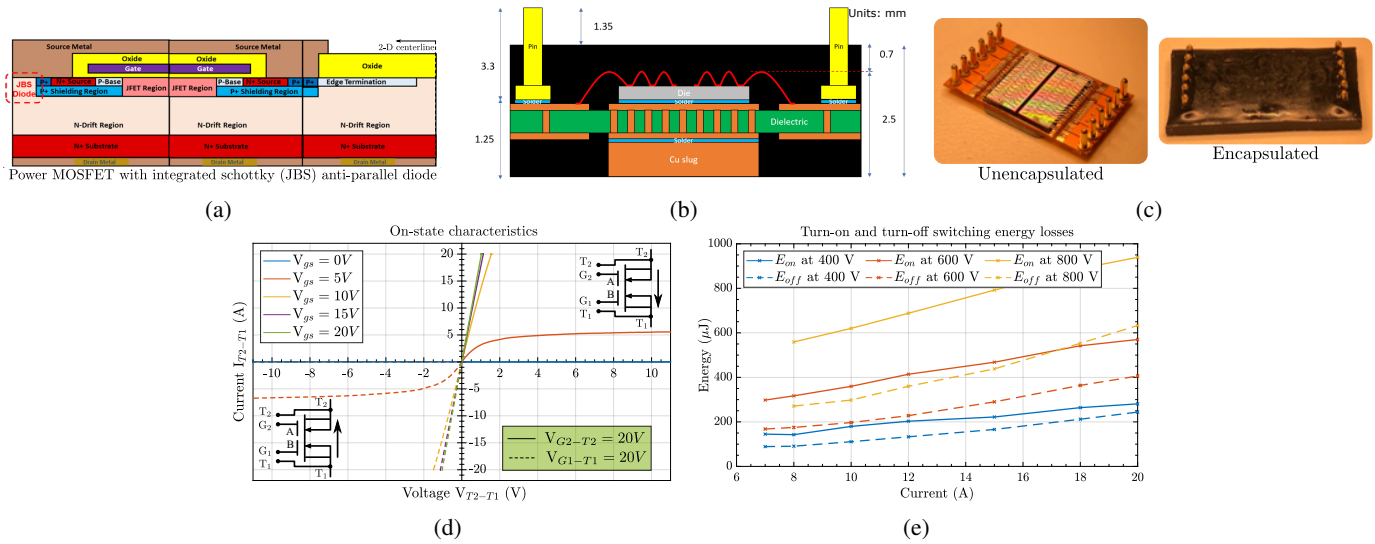



Fig. 2: Monolithic 1200 V SiC bidirectional FET (BiDFET): (a) 2-D center-line cross-section of the die [10], (b) packaging layer stack for the fabricated BiDFET module, (c) un-encapsulated module with the BiDFET die and encapsulated module with 12 pin-outs [11], (d) measured on-state characteristics in the first and third quadrants, and (e) measured turn-on, turn-off losses at different currents and blocking voltages [12].

## III. Basic Operation and Steady-State Model of the AC/DC DAB Converter

The basic operation of the AC/DC DAB converter is similar to that of its DC/DC version. The two full-bridge circuits of the converter generate square or quasi-square wave AC voltages across the transformer-inductor arrangement. Depending on the adopted modulation strategy, the power transfer between the input and output terminals is regulated through the three control variables: the duty-ratios $(d_1, d_2)$ of the high frequency AC voltages and the phase-shift angle $(\phi)$ between them, as shown in Fig. 3. The converter is distinct in its ability to generate bipolar voltage at its grid-side terminals. Depending on the grid-voltage polarity, one constituent FET in the monolithic BiDFET modulates while the second FET conducts throughout the switching period.

### A. Average power over a switching period

The switching frequency of the converter is large compared to the grid frequency. Therefore, the average power over the switching period of the converter is approximately equal to the instantaneous power, $P_{\text{inst}}$, on the AC line cycle. It is derived in (1) through a modeling strategy [13] that uses superposition of multiple circuits. The variables $W, X, Y$ and $Z$ are expressed in (3) as linear combinations of the duty-ratios $(d_1, d_2)$ of the high frequency AC voltages and the phase-shift angle $(\phi)$ between them.

$$P_{\text{inst}} = \frac{N|v_g|V_{dc}}{\omega_s L_r} f(\phi, d_1, d_2) \tag{1}$$

$$f(\phi, d_1, d_2) = \frac{1}{4}\Bigg[ -W_1\left(1 - \frac{|W_1|}{\pi}\right) + X\left(1 - \frac{|X|}{\pi}\right) - Y\left(1 - \frac{|Y|}{\pi}\right) + Z\left(1 - \frac{|Z|}{\pi}\right)\Bigg] \tag{2}$$

$$W_1 = \begin{cases} W, & \text{if } \ 0 \le W < \pi \\ \pi - W, & \text{if } \ \pi \le W \le \frac{3\pi}{2} \end{cases}$$
$$W = \phi + \pi d_1 + \pi d_2 \ ; \ X = \phi + \pi d_1 - \pi d_2$$
$$Y = \phi - \pi d_1 - \pi d_2 \ ; \ Z = \phi - \pi d_1 + \pi d_2 \tag{3}$$

### B. High frequency AC port currents

The principle of superposition may also be used in a different manner [16] to derive the high frequency AC port currents. In Table I, the transformer current at the semiconductor device turn-on instants referred to the grid-side are derived in terms of phase-angles of the switching instants $(A, B, C, D)$, input to output voltage gain $(M)$ and scaling factor $(K)$ for the positive half-cycle. For the negative half-cycle, the sign of currents in Table I is reversed as its modulation is also 180° out-of-phase. The high frequency AC port RMS currents may also be calculated using the algorithm reported in [16].

$$A = \frac{\pi}{2} - \pi d_1; \ B = \frac{\pi}{2} + \pi d_1$$
$$C = \frac{\pi}{2} + \phi - \pi d_2; \ D = \frac{\pi}{2} + \phi + \pi d_2 \tag{4}$$
$$M = \frac{|v_g|}{NV_{dc}}; \ K = \frac{1}{2}\frac{NV_{dc}}{\omega_s L_r}$$

TABLE I: High frequency transformer current at device turn-on instants referred to the AC grid side ($v_g \ge 0$).

| Current | Expressions |
|---|---|
| $I_{Q_1}$ | $+K\Big[M\Big(\pi - \lvert C - A\rvert - \lvert D - \pi - A\rvert\Big) - \lvert B - A\rvert\Big]$ |
| $I_{Q_2}$ | $-K\Big[M\Big(\pi - \lvert D - B\rvert - \lvert C - B + \pi\rvert\Big) - \lvert B - A\rvert\Big]$ |
| $I_{Q_5}$ | $-K\Big[\pi - \lvert C - A\rvert - \lvert C - B + \pi\rvert - M\lvert D - C\rvert\Big]$ |
| $I_{Q_6}$ | $+K\Big[\pi - \lvert D - B\rvert - \lvert D - \pi - A\rvert - M\lvert D - C\rvert\Big]$ |

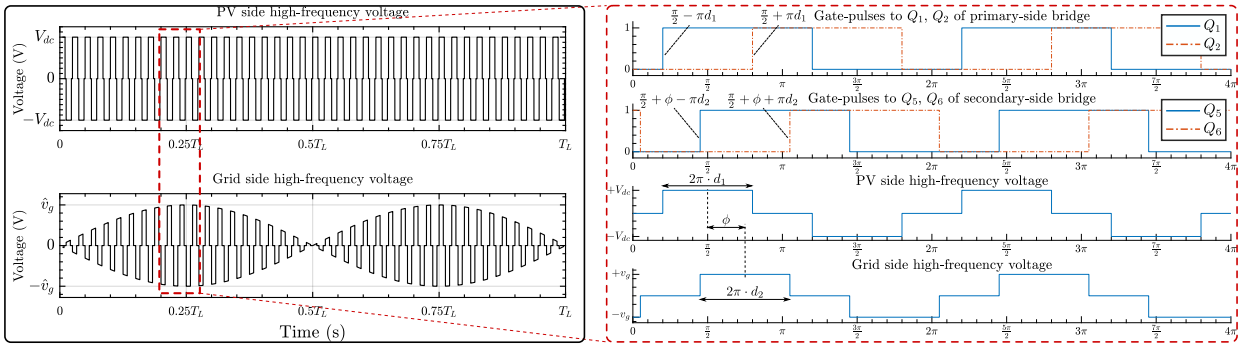



Fig. 3: Representative high frequency voltage waveform of the single-phase AC/DC DAB converter at an operating point on the line frequency cycle. $T_L$ is the period of the AC grid voltage.

## IV. Formulating the Optimization Problem

The single phase AC/DC DAB converter is specified to transfer 2.3 kW of power from a nominal input DC voltage of 400 V to the 277 $V_{RMS}$ grid. In this section, the algorithm to optimize the design of the converter is presented. The design space consists of transformer turns-ratio, $N$, and series inductance, $L_r$. The switching frequency is fixed for ease of understanding, but may be included as a design variable to trade-off the size of passive components with efficiency. It is, however, out of scope of this paper.

### A. Design space and control variable limits

The design limits for the transformer turns-ratio $(N_{lb}, N_{ub})$ are defined by the grid and DC voltages; i.e $N \in [0.01V_{g,pk}/V_{dc}, 10V_{g,pk}/V_{dc}]$. The design limits of the inductor are determined in (5) using specified limits on power transfer, input voltage, grid voltage and control variables $(\phi \in [3.6°, 90°], d_1, d_2 \in [0.01, 0.5])$.

$$\begin{aligned} L_{r,lb} &= \frac{N_{lb}(0.01V_{g,pk})V_{dc}}{\omega_s P_{o,\min}} f(\phi_{\min}, d_{1,\min}, d_{2,\min}) \\ L_{r,ub} &= \frac{N_{ub}V_{g,pk}V_{dc}}{\omega_s (2P_{o,\text{rated}})} f(\phi_{\max}, d_{1,\max}, d_{2,\max}) \end{aligned} \tag{5}$$

$f(\phi, d_1, d_2)$ is expressed in (2). The maximum instantaneous power transfer in the single-phase converter is equal to twice the rated power, $P_{o,\text{rated}}$. The minimum instantaneous power transfer occurs near the zero crossing of the grid voltage; it is fixed at 0.2% of the rated power occurring at 1% of the peak AC voltage. It is ensured that at the design limits, specified instantaneous power transfer is possible at all points on the AC line voltage half-cycle. The limits on transformer turns-ratio $(N)$ and inductor design $(L_r)$ are set, respectively, at $[0.1, 10]$ and $[0.01\ \mu\text{H}, 830\ \mu\text{H}]$.

### B. Setting up the optimization problem

Consider the system specifications described in previous sections, including the limits on design space vector $(\vec{x}_d = [N\ L_r])$ and control variables $(\vec{x} = [\phi\ d_1\ d_2])$. The parameters are fed into the optimization algorithm illustrated through a flow-chart in Fig. 4.

1) Consider a vector $\vec{z}_d$ comprising of elements $y_j$. $y_j$ is the quantity optimized for the $j$-th operating point, where $j = 1, 2, \ldots, n$. It may be the peak current, RMS current, estimated efficiency, transformer VA rating or combined total VA rating (as defined later).
2) For each design point, $[N\ L_r]$, the nested optimization process is followed:
   a) The grid voltage is quarter-wave symmetrical. Therefore, divide the first quarter of the positive half-cycle of grid voltage into $m$ operating points defined by $v_g$ and $P_{\text{inst}}$.
   b) Initialize the optimization with $\vec{x}_i = [\phi_i\ d_{1i}\ d_{2i}]$.
   c) The quantity $p_k$ is optimized for the $k$-th point on the quarter-cycle of the AC voltage by varying a vector, $\vec{x}$, of parameters $[\phi, d_1, d_2]$ subject to constraints defined later.
   d) For the $j$-th operating point, the optimized quantities $p_1, \ldots, p_m$ are collected and are further treated in accordance to their type to derive an overall optimized quantity, $y_j = f(p_1, \ldots, p_m)$.
3) The aforementioned nested process is repeated for all feasible design points to minimize the Euclidean norm, $\|\vec{z}_d\|_2$. The optimal design point is, thus, identified.

### C. Proposed objective functions

*1) **Minimum combined total VA rating (Design 1)**:* The AC/DC DAB converter transfers active power through the high frequency AC link. Therefore, circulating non-useful power is also present on both sides of the high frequency transformer-inductor arrangement. The RMS voltages and currents at the high frequency AC link determine the sizes of the core and winding in this arrangement, respectively. However, the maximum voltage and current may not appear at a concurrent operating point. The total apparent power combined for the two sides of the AC link, therefore, is calculated in (6). Note that $k$ is one of $m$ points on the quarter-wave of the AC line cycle, whereas $j$ is one of $n$ operating points (operating points may mean varying load, line or DC voltage).

$$\begin{aligned} p_k &= I_{\text{RMS},k} \\ y_j &= \left(\max_{k=1}^{m}(NV_{in,j}\sqrt{2d_{1,k}}) + \max_{k=1}^{m}(v_{g,k}\sqrt{2d_{2,k}})\right) \cdot \|\vec{p}_k\|_2 \\ \vec{z}_d &= \max_{j=1}^{n}\left(y_j\right) \end{aligned} \tag{6}$$

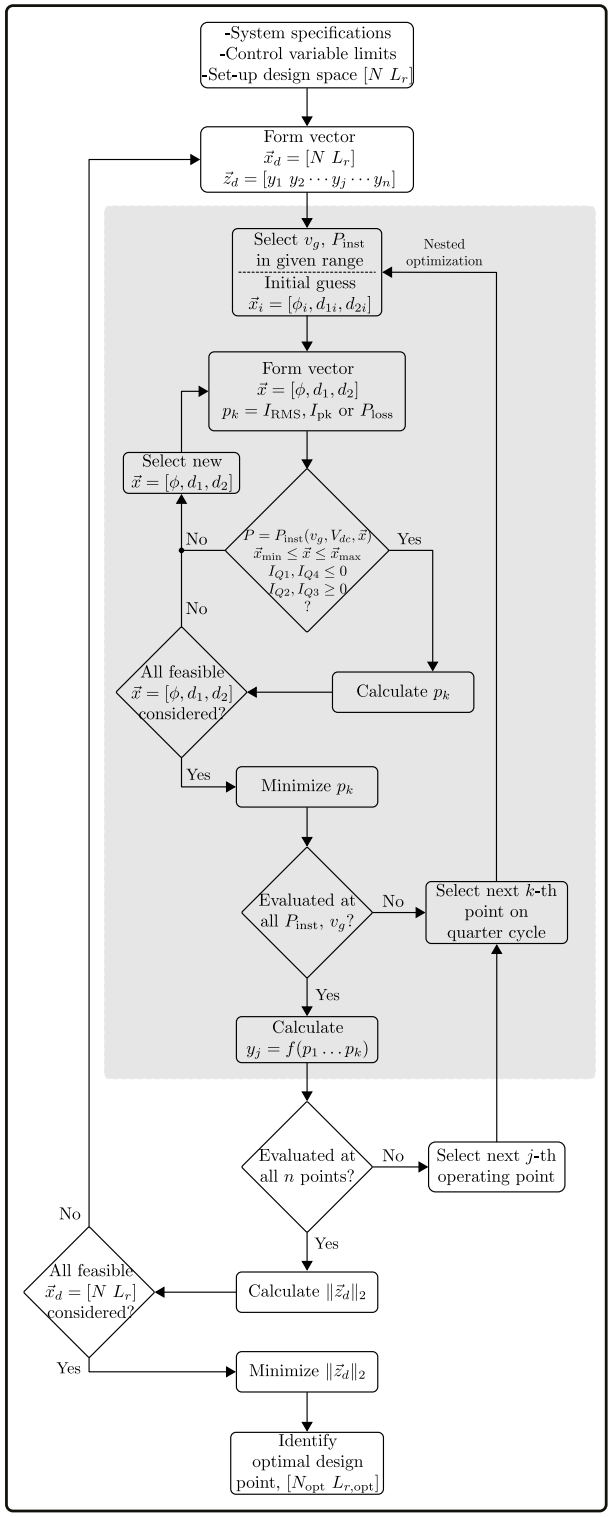



Fig. 4: Flow-chart of the optimization algorithm.

*2) **Minimum RMS current rating (Design 2)**:* The largest proportion of loss in AC/DC DAB converter can be attributed to the conduction and switching losses in the system. If ZVS or near-ZVS is assured through constraints, minimizing the conduction loss can improve efficiency while also reducing the winding size of the high frequency AC link. Therefore, the objective function is defined in (7) to minimize the RMS currents on both sides of the transformer.

$$\begin{aligned} p_k &= I_{\text{RMS},k} \\ y_j &= \sum_{k=1}^{m} \sqrt{p_k^2(1+N^2)} = \|p_1 \ldots p_n\ Np_1 \ldots Np_n\|_2 \\ \vec{z}_d &= [y_1\ y_2\ \ldots\ y_n] \end{aligned} \tag{7}$$

### D. Contraints on the optimization problem

This section lists the constraints not related to the design space ($\vec{x}_d = [N\ L_r]$) described previously. These are related to operating power transfer, limits on control variables and conditions for soft-switched turn-on of semiconductor devices. The variation in DC and grid voltages are inputs to the algorithm as $n$ operating points.

*1) Equality constraint on power transfer:* The constraint ensures that the selected design point vector, $\vec{x}_d$, and control variables' vector, $\vec{x}$, results in a power transfer defined by the $k$-th point on the AC line cycle. It is calculated using (1), (2).

$$P_{\text{inst}}(\vec{x}_d, \vec{x}, V_{dc,k}, v_{g,k}) - P_{\text{inst},k} = 0 \tag{8}$$

*2) Inequality constraints on control variable vector:* The constraint ensures that the control variables remain within the physical boundaries and limits of the control platform. In addition, the average power over switching period at the peak of the AC line cycle is less than the maximum possible power transfer through the converter.

$$\begin{aligned} 3.6^\circ \le \phi &\le 90^\circ \\ 0.01 \le d_1 &\le 0.5 \\ 0.01 \le d_2 &\le 0.5 \\ 2P_{o,\text{rated}} \le \frac{NV_{dc}V_{g,pk}}{\omega_s L_r}&\frac{\pi}{4} \end{aligned} \tag{9}$$

*3) Inequality constraints on switching instant currents:* The ideal constraint ensures that the semiconductor devices are always turning-on at zero voltage. It is determined by the switching instant currents listed in Table I for the positive half-cycle of the grid AC voltage. The constraints may be modified to incorporate the effect of device output capacitance in limiting the soft-switched region of the DAB converter [17].

$$\begin{aligned} I_{Q_1} \le 0\ ;\ I_{Q_2} \ge 0 \\ I_{Q_5} \ge 0\ ;\ I_{Q_6} \le 0 \end{aligned} \tag{10}$$

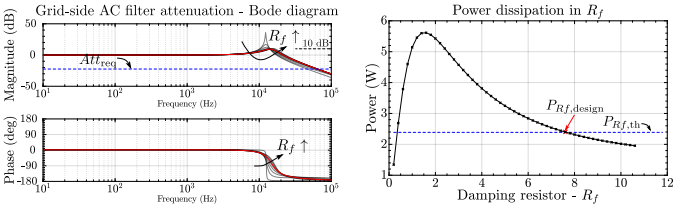
### E. Comparison of results

The parameters and ratings of the two designs shown previously are presented in Table II, along with the conventional designs. The design 1 results in minimum transformer VA rating and combined total VA rating, whereas design 2 results in minimum RMS current. Moreover, the design 2 also results in lower peak current rating of the BiDFET-side bridge. In comparison to the conventional designs, the transformer and the high frequency inductor are up to 14% and 36% smaller, respectively. Moreover, the attenuation required by the DC and AC side filters is 30-50% smaller in case of optimized designs.

TABLE II: Comparison of component ratings designed using proposed methods with the conventionally optimized designs.

| Design strategies | Transformer parameters | | Inductor parameters | | Total combined VA rating (6) | RMS current | | Peak current | | Capacitor currents§ | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Turns-ratio | VA rating | $L_r$ | $L_r I_{pk} I_{RMS}$ | | Prim. | Sec. | Prim. | Sec. | DC-side | Grid-side |
| Design 1 | 400/320 | **3.3 kVA** | 31.5 µH | 8.0 mJ | **7.1 kVA** | 8.3 A | 10.5 A | 19.3 A | 24.3 A | **5.4 A** | 5.5 A |
| Design 2 | 400/354 | 3.5 kVA | 36.2 µH | **6.6 mJ** | 7.4 kVA | 8.7 A | **9.8 A** | 16.5 A | **18.6 A** | 5.8 A | **5.1 A** |
| Design 1† | 400/294 | 3.8 kVA | 54.0 µH | 18.1 mJ | 8.8 kVA | 9.4 A | 12.8 A | 19.2 A | 26.1 A | 7.5 A | 9.8 A |
| Design 1‡ | 400/294 | 3.4 kVA | 54.0 µH | 16.4 mJ | 7.9 kVA | 8.5 A | 11.6 A | 19.2 A | 26.1 A | 6.1 A | 8.1 A |

†Conventional design optimized for minimum combined total VA rating considering single-phase shift (SPS) operation.
‡Conventional design operated with advanced modulation schemes [6], [15] to achieve optimal secondary-side RMS current.
§Grid-side capacitor current calculated assuming 5% THD in grid current.




(a) (b)

Fig. 5: (a) Frequency response plot of the attenuation of the CL-filter and (b) power loss in the damping resistor, $R_f$.

## V. Harmonic current computation algorithm and filter design

### A. Harmonic current computation algorithm

The RMS value of the high frequency current, $i_r$, is derived from the switching instant currents of Table I using an algorithm reported in [16]. Here, the following algorithm computes the RMS current at the line frequency AC and DC ports of the converter and design the respective filters.

- Consider the switching events and semiconductor currents at turn-on instants, $I_{Q_1}, I_{Q_2}, I_{Q_5}$ and $I_{Q_6}$, as expressed in Table I for positive half-cycle of the grid voltage. Note from Fig. 3 that the corresponding high-side device turns-on at $t_{Q_x}$ with current $I_{Q_x}$.

$$t_{Q_x} = \frac{\theta}{2\pi} T_s \ , \quad \forall \ x \in \{1,2,5,6\} \ ; \ \theta \in \{\frac{\pi}{2} \pm \pi d_1, \frac{\pi}{2} + \phi \pm \pi d_2\} \tag{11}$$

- Sort the above four switching 'events' in chronological order (as 'ev$_x$') to find vertices of the piece-wise linear waveform of AC current:

$$\{I_{t_{\text{ev}1}}, I_{t_{\text{ev}2}}, I_{t_{\text{ev}3}}, I_{t_{\text{ev}4}}\} \in \{I_{Q_1}, I_{Q_2}, I_{Q_5}, I_{Q_6}\} \text{ at } \{t_{\text{ev}1}, t_{\text{ev}2}, t_{\text{ev}3}, t_{\text{ev}4}\} \in \{t_{Q_1}, t_{Q_2}, t_{Q_5}, t_{Q_6}\} \tag{12}$$

- For the DC port: compute the RMS value of each $j$-th piece-wise linear element appearing between $t_{Q_1}$ and $t_{Q_2}$ in (13) using the sorted events (12). Similarly, for the grid-side AC port, the RMS value of each $j$-th piece-wise linear element appearing between $t_{Q_5}$ and $t_{Q_6}$ is also computed.

$$I_{\text{RMS},j} = \sqrt{\frac{2}{3}\left(I^2_{t_{\text{ev}(j+1)}} + I^2_{t_{\text{ev}j}} + I_{t_{\text{ev}(j+1)}} I_{t_{\text{ev}j}}\right) \frac{t_{\text{ev}(j+1)} - t_{\text{ev}j}}{T_s}} \tag{13}$$

- Compute the RMS currents at the DC and line frequency AC ports as shown in (14). The RMS value of the non-fundamental component of the currents are shown in (15).

$$\begin{aligned} I_{\text{dc-port,RMS}} &= \left(\sum I^2_{\text{RMS},j}\right)^{1/2} \\ I_{\text{lfac-port,RMS}} &= \left(\sum I^2_{\text{RMS},k}\right)^{1/2} \\ \text{where, } j &= \{j \mid j \in [\text{ev}_j \equiv Q_1, \text{ev}_{j+1} \equiv Q_2)]\} \\ k &= \{j \mid j \in [\text{ev}_j \equiv Q_5, \text{ev}_{j+1} \equiv Q_6)]\} \end{aligned} \tag{14}$$

$$\begin{aligned} I_{\text{dc-port},h,\text{RMS}} &= \sqrt{I^2_{pv} - I^2_{\text{RMS,dc-port}}} \\ I_{\text{lfac-port},h,\text{RMS}} &= \sqrt{I^2_{\text{RMS,lfac-port}} - I^2_{g,\text{RMS}}} \end{aligned} \tag{15}$$

### B. Grid-side filter design

The grid-side filter must attenuate the switching frequency harmonics generated by the AC/DC DAB, and its specification is computed based on the THD requirement of 5%. A first-order $C$-filter consumes unacceptable fundamental frequency reactive power to achieve the required attenuation. Therefore, a second-order $CL$-filter with parallel $R_f$-$C_b$ damping branch is designed on the grid-side port of the monolithic SiC-BiDFET based bridge. Its attenuation transfer function is given in (16).

$$Att_{\text{req}} = \frac{\text{THD}_{\text{req}} \cdot I_{g,\text{RMS}}}{I_{\text{lfac-port},h,\text{RMS}}} \text{ and } \frac{I_g}{I_{\text{lfac-port}}} = \frac{1}{sL_f}\left[sL_f || \frac{1}{sC_{f,\text{eff}}}\right] \text{ where, } C_{f,\text{eff}} = C_f + \frac{C_b}{sC_bR_f + 1} \tag{16}$$

A power factor of 0.999 at the line frequency ($\omega_L$) is assumed and the total capacitance value is constrained by its reactive power consumption. The filter is designed in Fig. 5 for attenuation exceeding $Att_{\text{req}}$ (16) at twice the switching frequency, peak magnitude of 10 dB at the filter resonant frequency and power loss in the damping resistor to be less than 0.1%.

The power loss in the damping resistor, $R_f$, is due to the fundamental frequency component and switching frequency components. Assuming all the high frequency harmonic current through the damping branch is at twice the switching frequency ($2\omega_s$), the current through $R_f$ is expressed as in:

$$I_{R_f} = \frac{I_{\text{lfac-port},h,\text{RMS}}}{C_{f,\text{eff}}|_{2\omega_s}} \frac{C_b}{(j2\omega_s)C_bR_f + 1} + \frac{V_{g,\text{RMS}} \cdot (j\omega_L)C_b}{(j\omega_L)C_bR_f + 1} \tag{17}$$

The power loss with changing $R_f$ is plotted in Fig. 5b using (15), and the filter impedance at $2\omega_s$ and $\omega_L$.

### C. DC-side filter design

At the DC port, the converter current contains second harmonic of the line frequency and the switching frequency harmonics, primarily at $2\omega_s$. The second harmonic component of the line frequency is present in any single phase converter system due to instantaneous power equivalence at its input and output ports, and is directly dependent on the power transfer to or from the grid. Similarly, the even harmonic components of the switching frequency are also present at the DC port and are dependent on the power transfer through the high frequency AC link. The harmonic currents through the DC-side filter capacitance are expressed in (18).

$$\begin{aligned} I_{\text{dc-port},2\omega_L,\text{RMS}} &= \frac{P_{o,\text{rated}}}{\sqrt{2}V_{dc}} \\ I_{\text{dc-port},hf,\text{RMS}} &= \sqrt{I^2_{\text{dc-port},h,\text{RMS}} - I^2_{\text{dc-port},2\omega_L,\text{RMS}}} \end{aligned} \tag{18}$$

The filter capacitance ensures that the total peak-to-peak voltage ripple is within 5% of the nominal DC voltage (19).

$$\Delta V_{dc,\text{pp}} = \sqrt{(\Delta V_{dc,\text{pp},2\omega_L})^2 + (\Delta V_{dc,\text{pp},2\omega_s})^2} \tag{19}$$

The capacitance required to attenuate the respective low and high frequency components are expressed in (20).

$$\begin{aligned} C_{\text{bulk}} &= \frac{2\sqrt{2}\cdot I_{\text{dc-port},2\omega_L,\text{RMS}}}{2\omega_L \cdot \Delta V_{dc,\text{pp},2\omega_L}} \\ C_{\text{hf}} &= \frac{2\sqrt{2}\cdot I_{\text{dc-port},hf,\text{RMS}}}{2\omega_s \cdot \Delta V_{dc,\text{pp},2\omega_s}} \end{aligned} \tag{20}$$

The proportion of high frequency currents through the bulk capacitance is determined by the board layout and parasitic inductance. The overall capacitance requirement, therefore, is also dependent on the current capabilities of the available component selection at the low and high frequencies.

## VI. Hardware Prototype and Experimental Results

### A. Description of the hardware prototype

The design optimization process with minimum combined total VA rating, harmonic current computation algorithms and the filter design results in a hardware prototype system (Fig. 6) with parameters listed in Table III. It utilizes 650 V GaN Systems' semiconductor devices on the DC-side, and NCSU-engineered 1200 V monolithic SiC-BiDFET on the AC-side of the converter. The high frequency AC link comprises of a 3.3 kVA transformer and two series connected 15 µH inductors (Bourns' 1140-150K-RC). The transformer uses a 16 AWG stranded wire wound on a E70 ferrite (3C95) core. Its peak flux density is 150 mT when 400 V full square wave voltage is applied across its primary-side terminals. The estimated core and winding loss at 50 kHz and full load are 11 W and 25 W, respectively. In addition, the net winding resistance of the high frequency inductors at 50 kHz is 0.2 Ω. The DC-side filter capacitor bank comprises of eight 500 V, 0.6 µF TDK Ceralink capacitors and four 500 V, 330 µF KEMET aluminum electrolytic capacitors. On the grid-side, the capacitor bank comprises of 350 $V_{\text{RMS}}$ film capacitors: two 1 µF TDK

TABLE III: System parameters from the design process.

| Parameter | Variable | Value |
|---|---|---|
| Nominal power | $P_{o,\text{rated}}$ | 2300 W |
| Nominal DC voltage | $V_{dc}$ | 400 V |
| Nominal AC voltage | $V_{g,\text{RMS}}$ | 277 V |
| Switching frequency | $f_s$ | 50 kHz |
| HF inductance | $L_r$ | 31.5 µH |
| Transformer size | VA, $1:N$ | 3.3 kVA, 19/15 |
| Grid-side $CL$ filter | $C_f, L_f$ | 2.0 µF, 36 µH |
| Damping branch | $C_b, R_f$ | 2.2 µF, 7.5 Ω |
| DC-side filter | $C_{\text{bulk}}, C_{\text{hf}}$ | 1.3 mH, 4.8 µF |

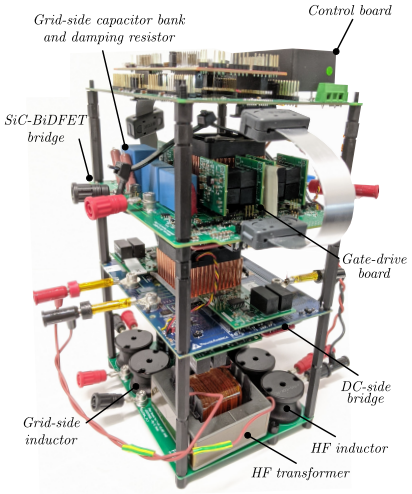


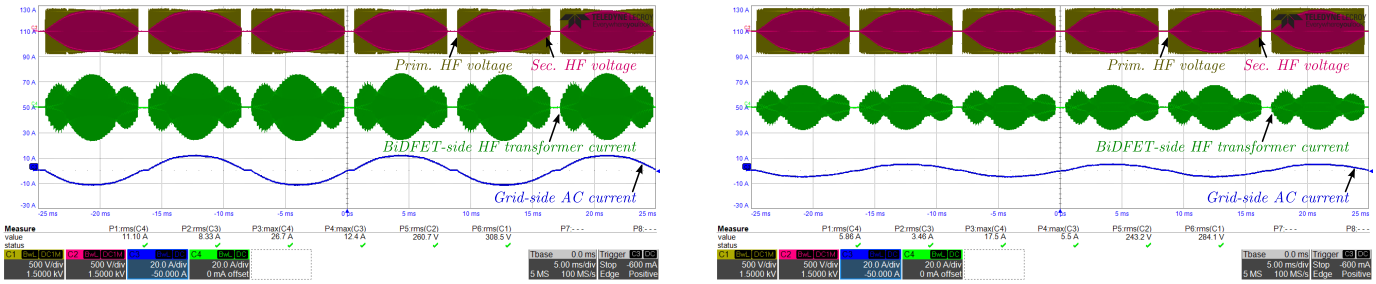

Fig. 6: Hardware prototype of the 2.3 kW, 400 V to 277 $V_{\text{RMS}}$ AC/DC DAB converter based on monolithic SiC-BiDFET.

capacitors for the main filter branch and a 2.2 µF capacitor for the damping branch. The damping resistor is formed by two parallel 15 Ω, 10 W axial resistors. The grid-side inductor comprises of two series connected 18 µH inductors.

### B. Results and discussion

The prototype of the AC/DC DAB converter is tested with a DC power supply connected on the PV or the DC-side with progressively increasing load. The operating waveform of the converter at 100% and 40% load are shown in Fig. 7. In the figure, the high frequency voltages on both sides of the transformer-inductor arrangement are shown along with the secondary-side transformer current and the grid-side AC port current. The transformer RMS and peak current are in agreement with the optimized design shown in Table II. The 'dead-time' near the zero crossing of the AC output current enables safe commutation of the constituent FETs of the BiDFET. Even with the zero crossing distortion, the power factor and the current THD at 100% load, as measured at the converter output by the Hioki Power Analyzer PW6001, are 0.999 and 4.7%, respectively (Fig. 8).

Fig. 9 illustrates the overall input to output port efficiency with operating load ranging from 20% to 100%. In addition, the loss in different components are estimated using the currents predicted through models derived in the previous sections. These include the loss in the transformer core, transformer and high frequency inductor winding, DC side filter




(a) (b)

Fig. 7: Operating waveform of the 2.3 kW AC/DC converter at input DC voltage of 400 V and output voltage of 277 $V_{RMS}$ with (a) 100% load and (b) 40% load.

(a) (b)

Fig. 8: (a) Power factor and (b) current THD at 100% load.

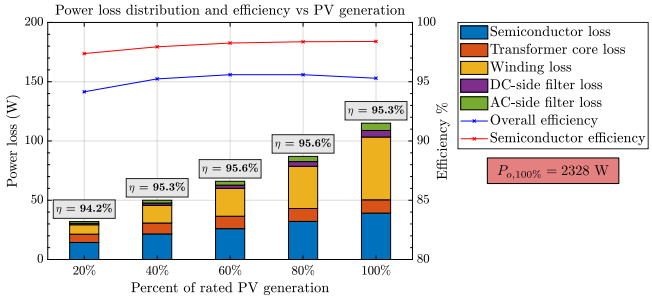



Fig. 9: Overall efficiency, semiconductor efficiency and estimated loss distribution at different rates of PV generation.

capacitor (high and low frequency losses), and AC side filter capacitor. Assuming other loss as negligible, the semiconductor loss and the corresponding efficiency is also estimated. Fig. 9 illustrates the estimated power loss distribution and semiconductor efficiency against the operating load range.

## VII. Conclusion

The paper presents a process to optimize the design of a single-phase AC/DC DAB converter utilized for interfacing a PV-string to the AC grid for commercial, industrial or residential applications. The proposed optimization algorithm leverages the three degrees-of-freedom ($\phi, d_1, d_2$) and optimizes the high-frequency RMS current, size of magnetic elements and the soft-switched region of the converter. Unlike those reported in literature, it incorporates all modulation strategies and operating modes of the AC/DC DAB converter, constrained only by the limits of the controller. It is shown to have clear advantage in terms of transformer, inductor, RMS current and filter ratings when compared to conventional design methods. Further, an algorithm to compute the harmonic ripple currents at the DC and line frequency AC ports is presented. The algorithm aids in the design of the grid-side and DC-side filters which is also presented in the paper. Finally, experimental results on a hardware prototype demonstrate the validity of the design. The current THD, overall efficiency and semiconductor efficiency at full load (2.3 kW) and voltage with 50 kHz switching frequency are 4.7%, 95.3% and 98.4% respectively.

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