Bidirectional Three-phase Current Source Converter based Buck-boost AC/DC System using Bidirectional Switches

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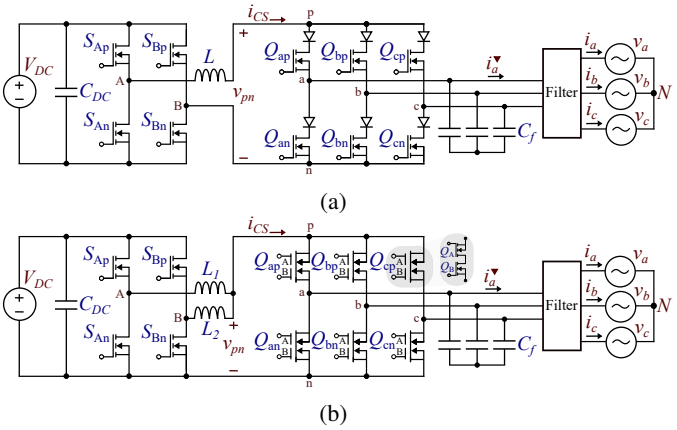
***Abstract*—The 1.2 kV 4H-SiC BiDirectional Field Effect Transistor (BiDFET) is the first monolithic SiC bidirectional switch, which offers a lower voltage drop and semiconductor devices count alternative to the reverse-voltage-blocking (RB) switch used in the current-source converters (CSC). The bidirectional switch based CSC also allows DC-link current reversal for bidirectional power flow and provides multiple system-level benefits in a buck-boost AC/DC system consisting of buck-type DC/DC converter and CSC. This paper discusses the selection of buck converter duty cycle and CSC modulation index for the system's buck-boost operation with a wide variation in DC voltage. CSC modulation schemes categorized based on the number of hard-turn-on transitions per switching cycle are also analyzed along with the three-step and four-step commutation schemes that are essential for the CSC commutation cells. Finally, the different schemes are evaluated and compared through the experimental results of a 10 kW, 480 $V_{RMS,LL}$/ (400 − 800) V AC/DC system.**

***Index Terms*—Bidirectional switches, four-quadrant switches, current source inverter, interleaved buck converter, modulation, commutation, SiC bidirectional FET, BiDFET, CSI, CSC.**

I. Introduction

The advent of wide-bandgap bidirectional switches has made the current-source converter (CSC) an appealing alternative to the voltage-source converter (VSC) [1]–[3]. CSC offers an inherent boost topology, short circuit immunity, lower electromagnetic interference, reduced voltage stress on switches, reduced cable insulation requirements, and a robust DC-link inductor to replace the unreliable DC-link capacitor [4], [5]. Replacing the reverse-voltage-blocking (RB) switch with a lower voltage-drop bidirectional switch reduces the conduction loss in a CSC but increases converter switching loss and gate drive circuitry [6].

In an RB switch based CSC, the MOSFET body-diode does not conduct current in any operating condition; it is the reverse recovery of the series diode that causes additional loss during the hard-turn-on transitions [7]. However, in a bidirectional switch based CSC, the body-diode of one of the bidirectional switch's intrinsic MOSFETs (based on DC-link current polarity) undergoes hard turn-off switching. To reduce the CSC switching loss, MOSFETs can be replaced by MOSFETs with anti-parallel JBS (Junction Barrier Schottky) diodes or single-chip solution, JBSFETs, having monolithically integrated SiC



(a)

(b)

Fig. 1: Three-phase current-source converter (CSC) based bidirectional, buck-boost AC/DC converter: (a) Conventional implementation using reverse-voltage-blocking (RB) switch, and (b) Proposed implementation using monolithic 1.2 kV 4H-SiC BiDirectional FET (BiDFET).

MOSFET and JBS diode [8]. Hence, the SiC BiDirectional FET (BiDFET) device, which is a monolithic SiC four-quadrant switch comprised of two constituent 1.2 kV 4H-SiC JBS-diode-embedded-power MOSFETs (JBSFETs) connected in a common-drain configuration, is perfectly suited for the CSC application [1], [9]. The conventional approach using RB switch and the proposed approach using BiDFET for the implementation of a bidirectional, buck-boost, three-phase AC/DC system are shown in Fig. 1.

The conventional system controls the power flow direction by changing the voltages' polarities on both sides of the DC-link inductor. This is necessary to maintain the same polarity for the DC-link inductor current, which is crucial for the operation of RB switches. However, this approach leads to the under-utilization of the buck converter switches. For positive buck converter output voltage, S_{Ap} and S_{Bn} are modulated, while S_{An} and S_{Bp} are always off, and vice versa for negative output voltage. In contrast, the bidirectional switch based CSC allows changing the DC-link current's polarity, enabling power flow direction reversal while keeping the buck converter output always positive [10]. This capability offers multiple advantages at the system-level. By utilizing the same number

of switches in the DC/DC converter stage, an interleaved buck converter can be implemented, allowing for the sharing of the DC-link current between the two phases and reducing the required current rating of the switches. Furthermore, under certain conditions, the interleaved phases can cancel their output current ripples, resulting in a reduced RMS value of the DC-link current and lowering both the inductance and VA rating of the DC-link inductor. Section II describes the proposed system's operation with a wide variation in DC voltage, different CSC commutation schemes, and different CSC modulation schemes. Section III provides brief overview of the hardware prototype, while section IV presents the hardware results demonstrating the system's performance with different schemes and DC voltage variation.

II. System Operation

A. Buck-boost operation

For a wide DC voltage variation, the AC voltages and power flow are regulated by controlling buck converter duty cycle, d_{buck} and CSC modulation index, m_{CSC}. The interleaved buck converter employs two phases with gate signals having identical duty cycles but a 180° phase shift. This arrangement ensures equal current sharing and minimizes DC-link current to a certain extent, depending on the selected duty cycle. During steady-state, by neglecting all the losses, power balance across CSC can be written as:

$$\begin{aligned} v_{\text{pn,AVG}} \cdot i_{\text{CS,AVG}} &= \sqrt{3} \cdot v_{\text{AC,RMS,LL}} \cdot i_{\text{AC,RMS}} \cdot cos(\phi) \\ \implies d_{\text{buck}} \cdot V_{\text{DC}} \cdot i_{\text{CS,AVG}} &= \sqrt{3} \cdot v_{\text{AC,RMS,LL}} . \frac{i_{\text{AC,PEAK}} \cdot cos(\phi)}{\sqrt{2}} \\ \implies M = \frac{v_{\text{AC,RMS,LL}}}{V_{\text{DC}}} &= \sqrt{\frac{2}{3}} \frac{d_{\text{buck}}}{m_{\text{CSC}} \cdot cos(\phi)}, \end{aligned} \tag{1}$$

where, $d_{\text{buck}} = \frac{v_{\text{pn,AVG}}}{V_{\text{DC}}}$, $m_{\text{CSC}} = \frac{i_{\text{AC,PEAK}}}{i_{\text{CS,AVG}}}$, M is system voltage gain, and ϕ is AC current phase angle w.r.t AC phase voltage. $i_{\text{CS,AVG}}$ and $v_{\text{pn,AVG}}$ denote the average values of the DC-link current and the voltage across the CSC terminals over the switching period. Lastly, $v_{\text{AC,RMS,LL}}$ and $i_{\text{AC,RMS}}$ represent the RMS values of the line-to-line AC voltage and AC current over the AC fundamental cycle.

The same M values can be realized using different combinations of d_{buck} and m_{CSC}. At $d_{\text{buck}} = 1$, buck converter switches incur only the conduction loss. Also, $m_{\text{CSC}} = 1$ results in the minimum DC-link current required to generate particular reference AC currents because the zero state duration (during which no power is transferred) is minimized. Lower DC-link current results in lower conduction and switching losses in the CSC switches. At $d_{\text{buck}} = m_{\text{CSC}} = 1$,

$$V_{\text{DC,boundary1}} = \sqrt{\frac{3}{2}} \cdot v_{\text{AC,RMS,LL}} \cdot cos(\phi) \tag{2}$$

Therefore, for system operation with a wide DC voltage range, at $V_{\text{DC}} < V_{\text{DC, boundary1}}$ (boost region), $d_{\text{buck}} = 1$ and $m_{\text{CSC}} < 1$ combination, and at $V_{\text{DC}} > V_{\text{DC, boundary1}}$ (buck region), $d_{\text{buck}} < 1$ and $m_{\text{CSC}} = 1$ combination can be used to achieve required AC voltages. With this strategy and system operation at a particular AC voltage and power, it can be deduced from (1) that $i_{\text{CS,AVG}}$ decreases with an increase in DC voltage in the boost region and remains constant in the buck region. Alternatively, the buck converter can be regulated to keep the DC-link current constant across the entire V_{DC} range, with AC voltages controlled solely by the CSC modulation index. However, this approach may lead to decreased system power-density and efficiency.

B. Commutation schemes

Buck converter consists of two one-pole, two-throw commutation cells, S_{Ap} and S_{An} form the first, and S_{Bp} and S_{Bn} form the second. These current-bidirectional commutation cells require dead-time during commutation to prevent short-circuit across the DC voltage source. This dead-time-based two-step commutation scheme ensures the short-circuit protection for fixed voltage-source polarity, independent of current polarity.

CSC consists of two one-pole, three-throw commutation cells, Q_{ap}, Q_{bp} and Q_{cp} form the upper commutation cell, and Q_{an}, Q_{bn} and Q_{cn} form the lower commutation cell. To prevent short-circuit across the AC terminals and open-circuit of DC-link inductor, CSC bidirectional commutation cells employ four-step or three-step commutation scheme based on whether switching-node current, voltage-edge, or both polarities are known [7]. Based on the CSC switching state, different line-to-line AC voltages ($\pm v_{\text{ab}}$, $\pm v_{\text{bc}}$ and $\pm v_{\text{ca}}$) are applied across the p and n terminals. Fig. 2 shows upper commutation cell commutation process and v_{pn} during the current commutation from Q_{bp} to Q_{cp}. It can be observed that the Q_{cp} turn-on transition is hard or soft, depending on the relative magnitudes of the phase voltages and irrespective of commutation scheme type. A similar operation can be shown for the lower commutation cell and it can be generalized that

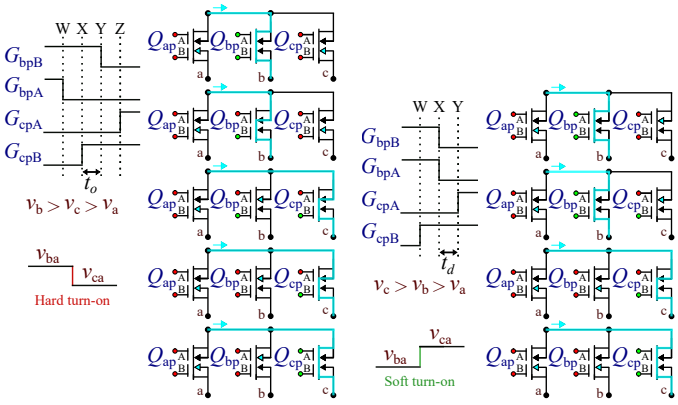


Fig. 2: Current commutating from phase b to phase c in the CSC upper commutation cell (with Q_{an} conducting in lower commutation cell and positive DC-link current): (a) four-step commutation process for v_{pn} negative voltage-edge from v_{ba} to v_{ca} and (b) three-step commutation process for v_{pn} positive voltage-edge from v_{ba} to v_{ca}. Blue line denotes the current flow path, and blue body-diodes are the reverse-biased diodes.

CSC switches undergo soft or hard turn-on based on whether v_{pn} has a positive or negative edge, respectively, for positive DC-link current and vice versa for negative DC-link current.

C. CSC modulation schemes

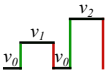
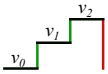
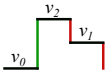
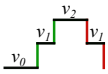
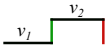
Based on the constraints imposed by the commutation schemes, only two of the six CSC switches conduct at any time instant, one from the upper commutation cell and the other from the lower commutation cell. Therefore, nine switching states, including three zero states (both switches selected from the same phase leg) and six active states (switches selected from different phase legs) are possible. Active states result in power transfer, while no power is transferred during the zero states. The switching states can be represented by stationary current vectors in a typical CSC space vector diagram and the dwell times (T_1, T_2 and T_0) corresponding to neighboring state vectors (active: $\vec{i_1}$, $\vec{i_2}$, and zero: $\vec{i_0}$) can be calculated to synthesize a rotating reference current vector in each of the six 60° sectors [11]. In sector I ($-\pi/6 \leq \theta < \pi/6$), dwell times can be calculated as,

$$\begin{aligned} T_1 &= m_{\text{CSC}} \cdot \frac{T_s}{2} \cdot (cos(\theta) - \sqrt{3} \cdot sin(\theta)) \\ T_2 &= m_{\text{CSC}} \cdot \frac{T_s}{2} \cdot (cos(\theta) + \sqrt{3} \cdot sin(\theta)) \\ T_0 &= 1 - T_1 - T_2, \text{ where, } T_s \text{ is the switching period.} \end{aligned} \tag{3}$$

Similar calculations can be done for other sectors. For unity power-factor (upf) operation, the line-to-line AC voltage vectors align with the current state vectors. If v_1 represents the line-to-line voltage with the highest absolute magnitude and v_2 represents the second-highest voltage at any time, the line-to-line voltages associated with neighboring vectors within any sector correspond to either v_1 or v_2. Both v_1 and v_2 have a common phase with the highest absolute voltage magnitude throughout the sector, while the other two phases have a magnitude crossover at the sector middle ($\theta = 0°$ for sector I). Phase with the highest voltage remains on for the entire sector, while we switch highest and second-highest line-to-line voltage vectors along with zero state to track the reference current vector. Thus, v_1, v_2 and zero state are applied across the p and n terminals and the resulting v_{pn} wave-shape can be analyzed to determine the number of soft and hard turn-on transitions per switching cycle, as discussed in II-B.

Based on the placement of v_1, v_2 and zero state during each switching cycle, multiple modulation schemes with different number of soft and hard turn-on transitions can be realized, as shown in Table I. Mod. 1 and Mod. 4 with four transitions are expected to have lower efficiency than Mod. 2 and Mod. 3 with three transitions per switching cycle. Mod. 1 is studied in this paper as it can be extended to seven-switch CSC modulation reported in [12], while Mod. 4 is not accounted for due to a high number of transitions. Mod. 3 has a higher number of hard-turn-on transitions than Mod. 2, but switches' voltage and current stresses during these transitions are lower for Mod. 3. The CSC efficiency ratio with these two schemes changes based on the switches' switching loss variation with voltage and current. A theoretical switching loss estimation procedure similar to the one proposed in [13] can be followed to calculate CSC efficiency variation with different modulation schemes, but has not been included in this paper for brevity and will be reported in a subsequent paper. With Mod.2, only one switch (from the upper or lower commutation cell) need to be switched at the sector change, while with Mod. 3, two switches (one in the upper and other in the lower commutation cell) need to be switched at the same time. In order to avoid short-circuit or open-circuit conditions during commutation times of the simultaneously transitioning switches, Mod. 3 can be changed to Mod. 2 just before the sector change time-instant and flipped back to Mod. 3 at the sector change.

TABLE I: CSC modulation types.

Modulation	v_{pn}	Turn-on type
Mod. 1		2 Soft 2 Hard
Mod. 2		2 Soft 1 Hard
Mod. 3		1 Soft 2 Hard
Mod. 4		2 Soft 2 Hard
Mod. 5		1 Soft 1 Hard

At some operating points, CSC switching losses can be reduced further by employing a zero state free modulation scheme [14]–[16]. By setting $T_0 = 0$ in (3), we get $i_{\text{CS,AVG}} = i_{\text{AC,PEAK}} \cdot cos(\theta)$, which corresponds to a 6-pulse wave-shape per AC fundamental cycle, with its magnitude equal to the phase current having the highest absolute magnitude at any time. Therefore, zero state can be avoided with a varying DC-link current, and the resulting modulation is denominated as "Mod. 5" in this paper. With this scheme, CSC switches have only one hard turn-on transition per switching cycle, as shown in Table I. To achieve a constant M with a varying DC-link current, d_{buck} needs a multiplication factor of $cos(\theta)$ and can be expressed as $d_{\text{buck}} = d_{\text{buck,PEAK}} \cdot cos(\theta)$. Using (1),

$$M = \sqrt{\frac{2}{3}} \cdot \frac{d_{\text{buck,PEAK}}}{cos(\phi)} \tag{4}$$

For $0 < d_{\text{buck}} \leq 1$, $cos(\frac{\pi}{6}) < d_{\text{buck,PEAK}} \leq (1 - cos(\frac{\pi}{6}))$, and hence,

$$\begin{aligned} &\frac{1}{\sqrt{2}} \cdot \frac{1}{cos(\phi)} < M \leq \sqrt{\frac{2}{3}} \cdot (1 - \frac{\sqrt{3}}{2}) \cdot \frac{1}{cos(\phi)}, \\ \implies &V_{\text{DC,boundary2}} < V_{\text{DC}} \leq V_{\text{DC,boundary3}}, \end{aligned} \tag{5}$$

where,

$$\begin{aligned} V_{\text{DC,boundary2}} &= \sqrt{2} \cdot v_{\text{AC,RMS,LL}} \cdot cos(\phi), \text{ and} \\ V_{\text{DC,boundary3}} &= \frac{\sqrt{\frac{3}{2}}}{(1 - \frac{\sqrt{3}}{2})} \cdot v_{\text{AC,RMS,LL}} \cdot cos(\phi) \end{aligned} \tag{6}$$

For a given AC voltage, three operating regions can be defined for the system operation with a variation in DC voltage. "Boost Region" for $V_{DC} \leq V_{DC,boundary1}$, "Buck Region 1" for $V_{DC,boundary1} < V_{DC} \leq V_{DC,boundary2}$ and $V_{DC} > V_{DC,boundary3}$, and "Buck Region 2" for $V_{DC,boundary2} < V_{DC} \leq V_{DC,boundary3}$. Mod. 5 is only applicable in the Buck Region 2.

III. Hardware Design

A hardware prototype of the proposed buck-boost AC/DC system (Fig. 3a) has been developed for the system parameters listed in Table II. To implement the bidirectional switches in CSC, two 1.2 kV, 16 mΩ MOSFETs (Wolfspeed C3M0016120K) have been utilized in a common-drain configuration. This switch configuration exihibits similar conduction and switching losses to Gen-2 BiDFET but does not have anti-parallel JBS diodes [7]. The interleaved buck converter is implemented by utilizing two of the three phase-legs in the same PCBA as the CSC, resulting in an equivalent on-resistance of 32 mΩ for both the buck and CSC switches. For each phase of the buck converter, two series-connected 110 μH ferrite core inductors are used. Additionally, the two-stage three-phase AC filter schematic is depicted in Fig. 3b. This paper's scope is limited to testing the system's performance for unidirectional power flow from the DC source to a three-phase Y-connected resistive load connected at the AC terminals.

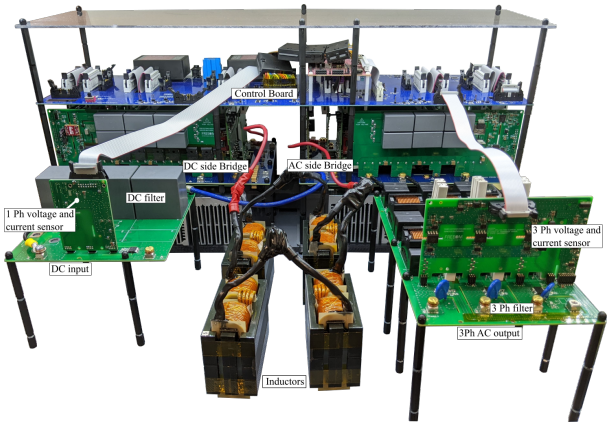
IV. Experimental Results

A. Variation with modulation and commutation schemes

Two system performance indices, including overall system efficiency and AC currents THD are evaluated with different commutation and modulation schemes at $V_{DC} = 550$ V and 480 $V_{RMS,\,LL}$, 10 kW output, as illustrated in Fig. 4. Using (1) and (6), $V_{DC,boundary1} = 587.9$ V, $V_{DC,boundary2} = 678.8$ V, and $V_{DC,boundary3} = 4388$ V for upf operation. At 550 V DC voltage, the system operates in boost region with $d_{buck} = 1$ and $m_{CSC} \approx 0.94$, as calculated using (1). Mod. 2 and Mod. 3 have higher efficiency than Mod. 4 due to a lower number of CSC transitions per switching cycle. Mod. 3 has been found to have the highest efficiency, despite having a higher number of hard turn-on transitions than Mod. 2 due to switching loss

TABLE II: System parameters.

Parameter	Variable	Value
Nominal power	$P_{o,rated}$	10 kW
Nominal AC voltage	v_{xy}	480 $V_{RMS,\,LL}$
DC voltage	V_{DC}	400 - 800 V
DC filter capacitor	C_{DC}	150 μF
AC fundamental frequency	f_L	60 Hz
Buck converter inductors	L_1, L_2	2 x 110 μH
AC filter capacitors	C_f	2 μF
AC filter inductors	L_f	10 μH
AC filter damping resistors	R_f	6 Ω
Switches	S, Q	C3M0016120K
Switching frequency	f_s	100 kHz
Switches gate resistance	R_G	10 Ω
Switches gate voltage	V_{GS}	15/ -4 V
Overlap and dead time	t_o, t_d	300 ns



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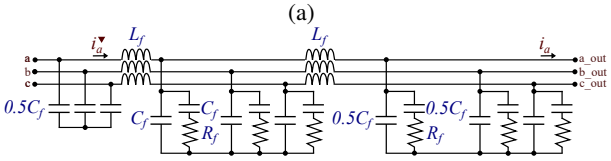


(b)

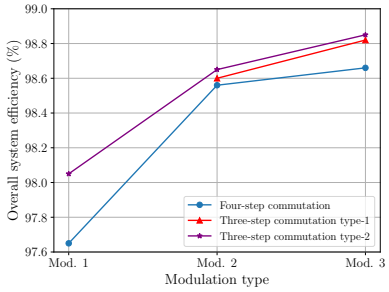
Fig. 3: (a) Hardware prototype of the 10 kW, 400 - 800 V_{DC} to 480 $V_{RMS,\,LL}$ CSC based three-phase AC/DC converter, and (b) Three-phase AC filter schematic.

variation with voltage and current. As shown in Fig. 4c, when Mod. 3 modulation scheme is adopted, it is changed to Mod. 2 for four switching cycles before the sector change time-instant and flipped back to Mod. 3 at the sector change.

Three-step commutation scheme has higher efficiency than the current polarity-based four-step commutation scheme due to a lower body-diode conduction time. At CSC transitions involving transition to or from zero state, the sensed v_{pn} edge polarity value is reliable for upf operation because only the line-to-line voltages having absolute highest (v_1) and second-highest (v_2) values are chosen for the CSC modulation in each sector. However, the phases corresponding to v_1 and v_2 interchange near the sector middle ($\theta = 0°$ for sector I), with exact time instant depending on the power-factor angle. Hence, when switching between v_1 and v_2, the sensed v_{pn} edge polarity value is less reliable. To address this challenge, two methods have been evaluated for switches' commutation during each switching cycle. Both methods employ three-step commutation for the transitions involving zero-state. For other transitions, the first method (three-step commutation type-1) employs four-step commutation and the second method (three-step commutation type-2) employs the three-step commutation at all times except a 10° window near each sector middle. The four-step commutation is utilized during this window. The window placement can be changed based on the power-factor angle and the window degree-span can be changed by accounting for the voltage sensors' accuracy, voltage ripple and any impedance between the CSC switching nodes and the points at which voltage sensors are placed.

B. Variation with DC voltage

The measured system performance indices at 480 $V_{RMS,\,LL}$, 10 kW output for different DC voltages are illustrated in Fig. 5,



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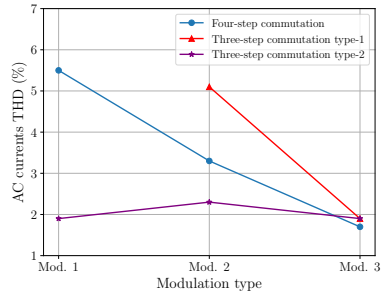

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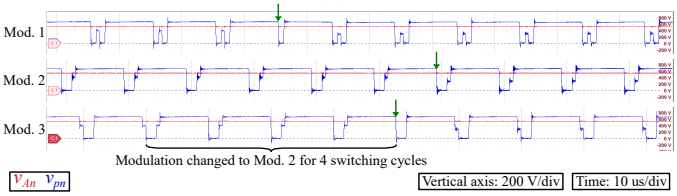
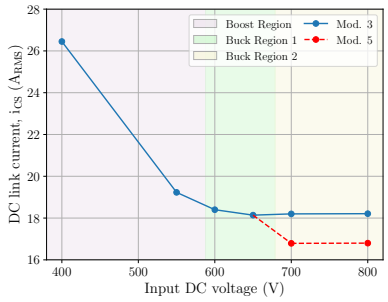


(c)

Fig. 4: Measured (a) Overall system efficiency and (b) Output AC current THD with different modulation types at 10 kW, 480 $V_{RMS,\,LL}$ output and 550 V input DC voltage. (c) Measured v_{pn} near the sector change (indicated by green arrow) for three modulation types.

and the operating waveforms are shown in Fig. 6. Three-step commutation type-2, along with Mod. 3 modulation scheme, is employed at all the operating points. The sudden reduction in the system's efficiency at V_{DC} = 600 V can be attributed primarily to the buck converter switching loss because the system operating region changes from the boost region at V_{DC} = 550 V to the Buck Region 1 at V_{DC} = 600 V.

At $V_{DC} > 678.8$ V (Buck Region 2), the Mod. 5 modulation scheme, involving 6-pulse shaping of the DC-link current to eliminate zero states in the CSC modulation, can be used to improve the system efficiency further, as shown by red dotted lines in Fig. 5. The efficiency improvement results from the reduction in both DC-link current RMS value and the number of CSC switching transitions. The DC-link current reduces as the zero states during which no power transfer happens are eliminated. AC currents THD also improves with Mod. 5, primarily due to a lower number of CSC switching transitions. Each switching transition has a minimum pulse-width depending on the employed commutation scheme, and hence the actual dwell times deviate from the ideally calculated values and lead to AC waveforms distortion.



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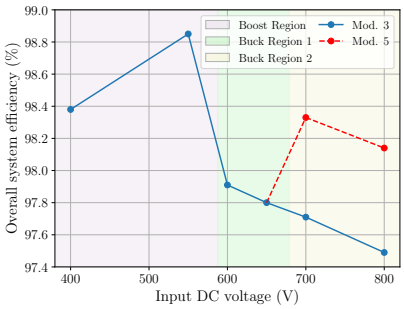

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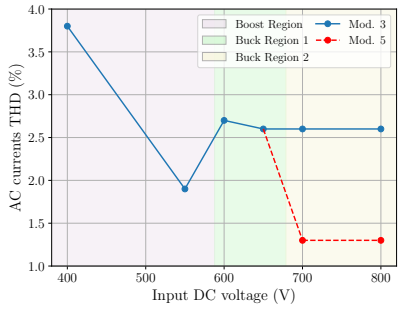

(c)

Fig. 5: Measured (a) DC-link current, (b) Overall system efficiency, and (c) AC currents THD at 10 kW, 480 $V_{RMS,\,LL}$ output and different input DC voltages.

V. Conclusion

The paper proposes and demonstrates a 10 kW buck-boost AC/DC system, consisting of an interleaved buck converter and bidirectional switches based current-source converter, for 400 − 800 V DC to 480 $V_{RMS,\,LL}$ applications like EV motor drives and PV inverters. This converter can also be used for bidirectional power flow.

A strategy for the selection of buck converter duty cycle and CSC modulation index values is devised based on the calculated boundary conditions of the system's operation in the buck or boost region. Also, based on the experimental study of variation in system efficiency with different modulation and commutation schemes, a modulation scheme having one soft and two hard turn-on switching transitions (called "Mod. 3" in this paper) has been chosen along with the three-step commutation scheme for achieving highest CSC stage efficiency. The system efficiency varies from 98.85 % peak to 97.49 % lowest if the same Mod. 3 modulation scheme is

used for the entire input voltage range.

An alternative modulation scheme applicable only for $V_{DC} > 678.8$ V at 480 $V_{RMS,\,LL}$ output and requiring no zero states in the CSC modulation (called "Mod. 5" in this paper) is found to improve the system efficiency by ≈ 0.6 %. With Mod. 3 used for $V_{DC} \leq 678.8$ V and Mod. 5 otherwise, 480 $V_{RMS,\,LL}$, 10 kW output and 100 kHz switching frequency, the variation in system efficiency and AC currents THD are measured as 98.85 % to 98.14 % and 3.8 % to 1.3 %, respectively. The AC currents THD can be enhanced by compensating the dwell times according to the commutation scheme and the system efficiency can be improved by reducing the switching frequency, switches' gate resistances and commutation time.

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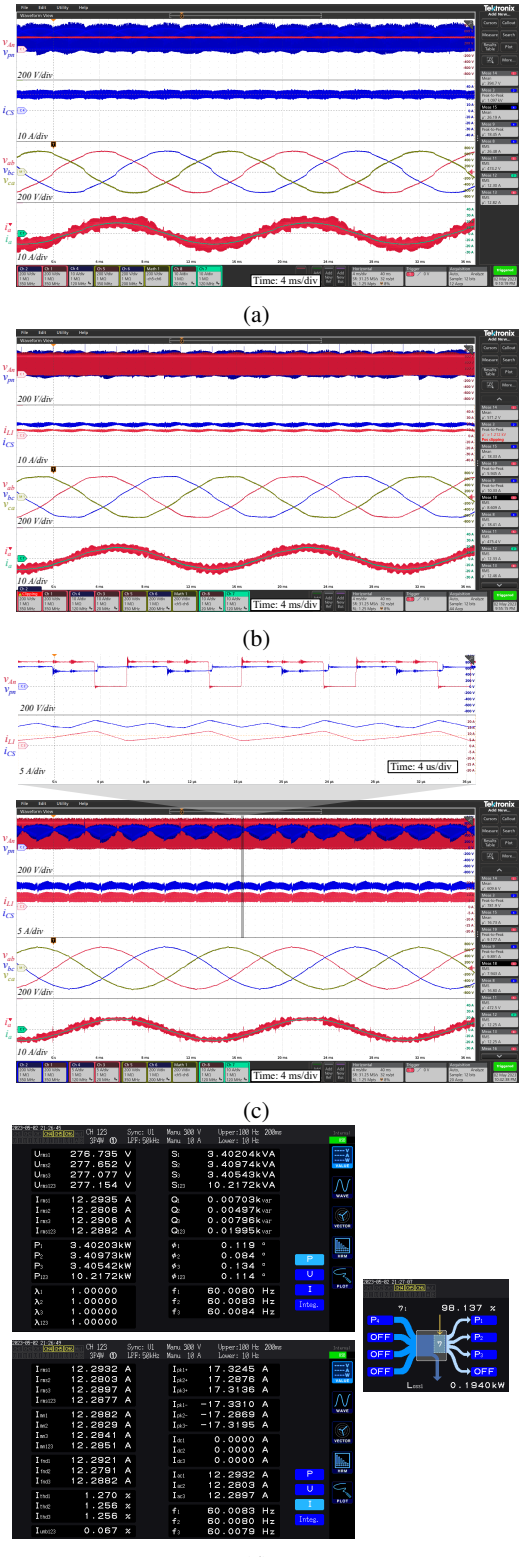

Fig. 6: Operating waveforms of the buck-boost AC/DC system at 480 $V_{RMS,\,LL}$, 10 kW output, and input DC voltage of (a) 400 V (Mod. 3), (b) 600 V (Mod. 3) and (c) 800 V (Mod. 5). (d) depicts power, AC voltages, AC currents, AC currents THD, and overall system efficiency measured using Hioki Power Analyzer PW6001 at 800 V DC voltage.