The BiDFET Device and its Impact on Converters

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INTRODUCTION

The matrix converter topology for direct ac-to-ac conversion offers elimination of the bulky and unreliable D.C. link capacitors used in the popular Voltage-Source Inverter (VSI) with a front-end rectifier. The resulting more compact and higher efficiency implementation is a desirable solution for a wide variety of applications, such as photovoltaic energy generation, motor drives, and energy storage systems.

Comparison of fabricated 1.2 kV 20 A BiDFET with previous bidirectional switch implementations

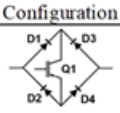
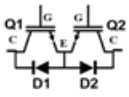
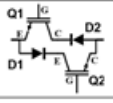
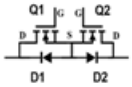
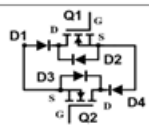
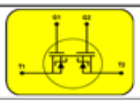
Switch Configuration	Description	Number of components	On-State Voltage Drop (V)	Switching Loss
	Diode Bridge + Asymmetric IGBT Neft & Schauder, IEEE Trans. Ind. Appl., vol. 28, pp. 546-551, 1992	5	8.6 [2 diodes + 1 IGBT]	High
	Asymmetric IGBTs + Freewheeling diodes Moghe et al., ECCE, pp. 3848-3855, 2012	4	5.8 [1 diode + 1 IGBT]	High
	Back-to-back symmetric IGBTs Takei et al., ISPSD, pp. 413-416, 2001	2	2.2 [1 symmetric IGBT]	Very High
	SiC Power MOSFETs + JBS diodes Safari et al., IEEE Trans. Power Electron., vol. 29, no. 5, pp. 2584-2596, 2014	4	3.1 [1 diode + 1 MOSFET]	Low
	Back-to-back SiC Power MOSFETs + antiparallel and series JBS diodes Ahmed et al., IEEE Trans. Power Electron., vol. 32, pp. 1232-1244, 2017	6	3.1 [1 diode + 1 MOSFET]	Low
	Four-terminal SiC Monolithic BiDFET	1	1.0 [1 BiDFET]	Low

Table I

The development of matrix converters has been hampered by the lack of availability of commercial bidirectional power switches with the ability to block high voltages in the first and third quadrants, carry on-state current in both quadrants with low voltage drop, exhibit large forward-biased safe-operating-area (FBSOA), and low switching power losses. Consequently, many implementations have been tried in the past using discrete devices, as listed in Table I. Two implementations utilize commonly available asymmetric blocking IGBTs, while two cases make use of SiC power MOSFETs. They generally have a large parts count (4-6 individual switches) that occupies significant space in the converter where multiple bi-directional switches are required. They also have a high on-state voltage drop that degrades efficiency. One

implementation utilizes symmetric blocking IGBT to achieve a low parts count (2), but its switching losses are unacceptably high.

GEN-1 BIDFET

The silicon carbide (SiC) BiDirectional FET (BiDFET) device was proposed [1] and developed to create a single chip four-terminal bidirectional device with low on-state drop and switching losses for matrix converters. A cross-section of the 4-terminal monolithic SiC BiDFET Gen-1 device is shown in Fig. 1. It contains two adjacent 1.2 kV SiC JBSFETs integrated in a single chip. A JBSFET is a MOSFET structure with an integrated JBS diode to suppress conduction of the body diode in the third quadrant. The drain terminals of JBSFET-1 and JBSFET-2 are internally connected via the common N^+ substrate and back-side metallization. Each JBSFET cell contains a MOSFET portion integrated with a JBS diode. The JBSFETs operate with vertical current flow, like typical high voltage power MOSFETs, ensuring uniform current distribution within the active area. The power MOSFET body diode is deactivated using the integrated JBS diode within each cell to reduce switching losses and avoid the bipolar degradation phenomenon [2]. The two JBSFETs provide high voltage blocking capability, low on-state resistance, excellent FBSOA, and fast switching performance in each quadrant. High voltage blocking capability is achieved in both quadrants when the gates G1 and G2 are shorted to the respective terminals T1 and T2. On-state current flow occurs in both quadrants with low on-state resistance when a gate bias (typically 20 V) is applied to both gates G1 and G2 with respect to terminals T1 and T2. Power switching is performed in the first quadrant by toggling gate bias G1 applied to JBSFET1 with gate G2 held at the on-state gate bias. In the same manner, power switching is performed in the third quadrant by toggling gate bias G2 applied to JBSFET2 with gate G1 held at the on-state gate bias.

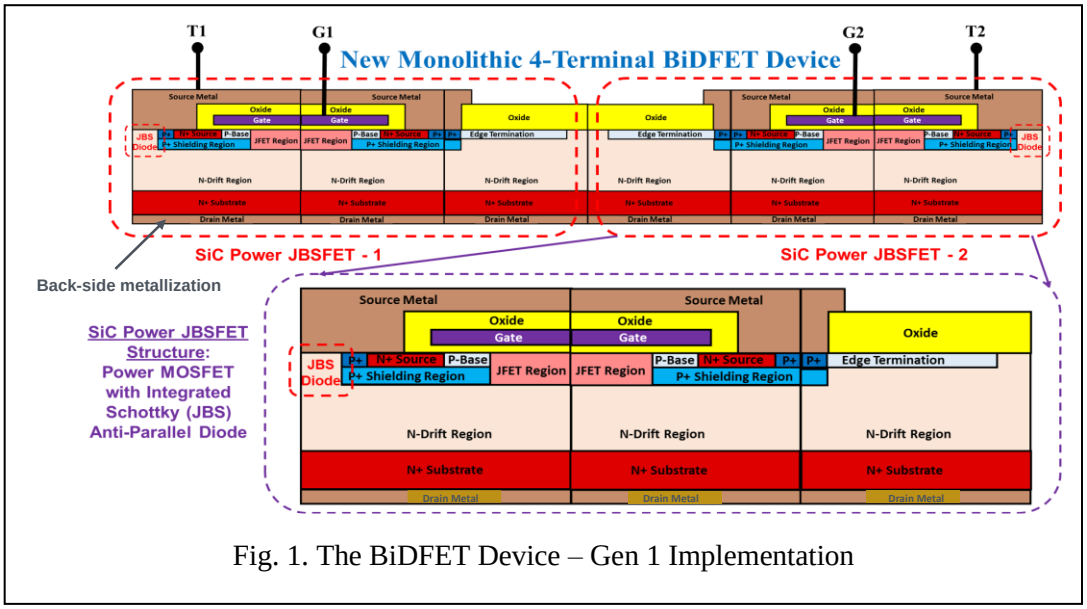


Fig. 1. The BiDFET Device – Gen 1 Implementation

The first generation (Gen-1) BiDFET device was designed using the JBSFET cell cross-section shown in Fig. 2(a). It has a half-cell width of 6.1 µm to accommodate the JBS diode within the MOSFET cell. The accumulation-mode channel was chosen to obtain a mobility of 20 cm^2/V-s with a channel length of 0.5 µm to minimize the channel resistance contribution. The devices were fabricated on n-type epitaxial layers with doping concentration of 8 x 10^{15} cm^{-3} and 10 µm thickness to achieve a blocking voltage above 1400 V using the hybrid-JTE edge termination [8]. An image of the Gen-1 BiDFET chip is shown in Fig. 2(b) with JBSFET1 at the top and JBSFET2 at the bottom. The chip layout contains gate bus bars to distribute the drive voltage with two gate pads per JBSFET for convenient packaging. Since the JBSFET cells have a

specific on-resistance of 11.25 mΩ-cm^2, an active area of 0.45 cm^2 was chosen to achieve a total on-resistance of 50 mΩ for the BiDFET. The Gen-1 BiDFET die size is 1.04 cm x 1.10 cm. The devices were fabricated using the NCSU PRESiCE^{TM} process technology at a commercial foundry X-Fab, TX [9]. The BiDFET process technology is similar to that used for manufacturing SiC power MOSFETs and JBS diodes making these devices commercially viable. After wafer level characterization, the Gen-1 BiDFET dies were mounted in a custom-designed module, as shown in Fig. 2(c), with sufficient wire bonds in the active area to reduce the package resistance to less than 1 mΩ. Fig. 2(d) shows the encapsulated 4-terminal module.

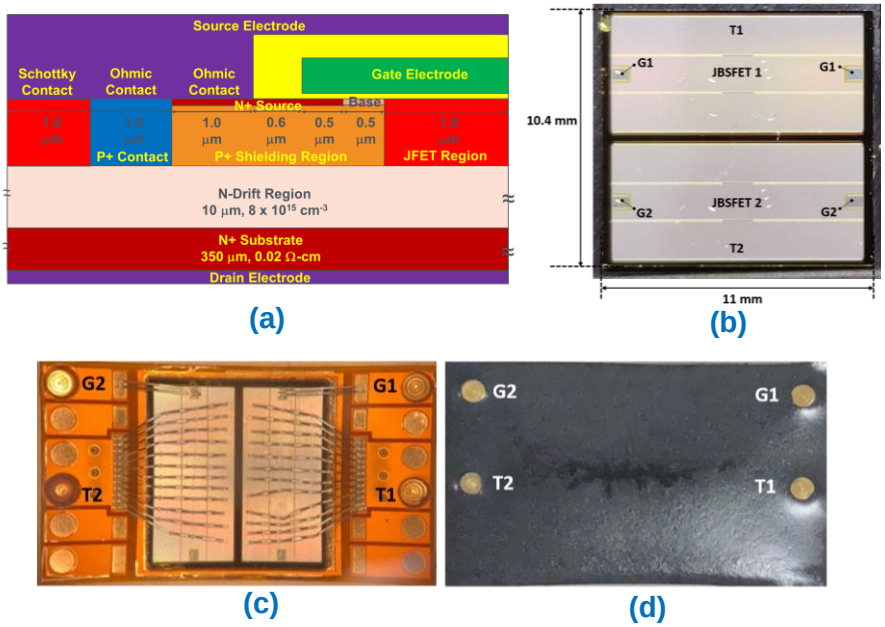


Fig. 2. Gen-1 BiDFET Device Implementation: (a) JBSFET cross-section; (b) BiDFET chip image; (c) Custom designed 4-terminal package; (d) Encapsulated module.

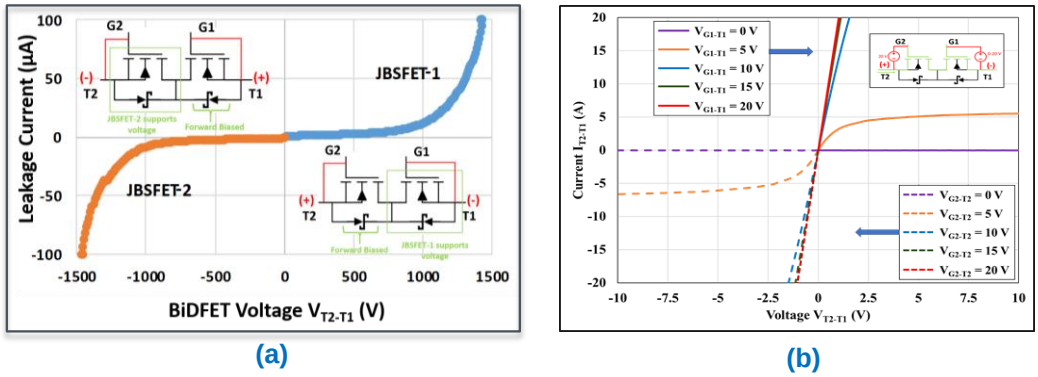
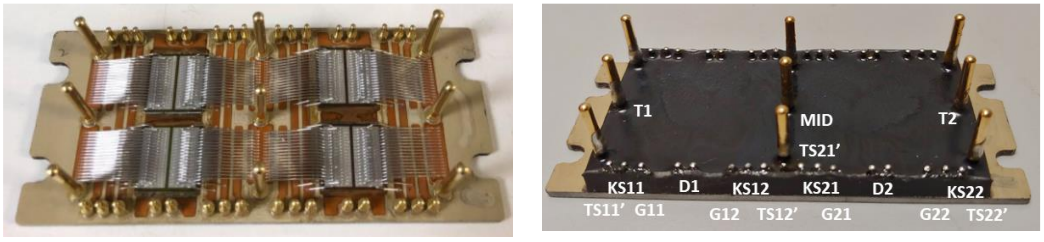


Fig. 3. Gen-1 BiDFET Device: (a) Blocking Characteristics; (b) Output Characteristics.

The measured blocking characteristics for the Gen-1 BiDFET device at 25 °C are shown in Fig. 3(a) [3]. The device can support over 1.4 kV in both the first and third quadrants when the gates G1 and G2 are shorted to the respective terminals T1 and T2 as shown in the inset with the device symbol. JBSFET1 supports the voltage in the first quadrant, while JBSFET2 supports the voltage in the third quadrant. The device exhibits the desired gate voltage controlled output characteristics with saturated drain current at lower gate bias

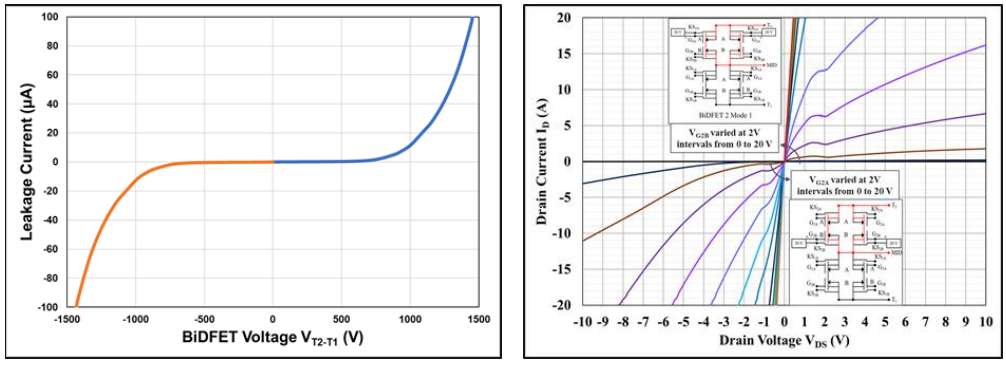
voltages (e.g. 5 V) as shown in Fig. 3(b) at 25 °C. The Gen-1 BiDFET has a total on-resistance of 50 mΩ at a gate bias of 20 V at 25 °C. The device can handle 20 A at a drain bias of 1 V consistent with Table 1. The integrated JBS diodes have a voltage drop of less than 2.5 V to ensure effective bypassing of the MOSFET body diode [2]. The turn-on, turn-off, and total switching losses obtained using double pulse testing of the BiDFET devices [4], performed at a drain supply voltage of 800 V and current of 10 A, were 620, 300, and 920 µJ. The total switching loss was observed to decrease with increasing temperature to 140 °C.



(a) (b)

Fig. 4. Gen-1 BiDFET Paralleled Device Implementation: (a) Internal construction; (b) Encapsulated module.

The BiDFET devices can be paralleled to increase the current handling capability for use in higher power converters. This was demonstrated by building a half-bridge module containing two paralleled BiDFET devices in the upper and lower leg, as shown in Fig. 4(a). The encapsulated module is shown in Fig. 4(b). The measured blocking characteristics for the Gen-1 paralleled BiDFET devices are shown in Fig. 5(a) in both quadrants. The device can support over 1.4 kV in both the first and third quadrants when the gates G1 and G2 are shorted to the respective terminals T1 and T2. The device exhibits the desired gate voltage controlled output characteristics, as shown in Fig. 5(b). It has a total on-resistance of 25 mΩ at a gate bias of 20 V, which is half that of the single Gen-1 BiDFET chip as expected. Double pulse testing of the paralleled BiDFET devices was performed at a drain supply voltage of 800 V and current of 20 A. The extracted turn-on, turn-off, and total switching losses were 1350, 460, and 1810 µJ, which are about twice that of the single Gen-1 BiDFET chip as expected. These results demonstrate that the BiDFET devices can be paralleled to increase the power handling capability.



(a) (b)

Fig. 5. Gen-1 BiDFET Paralleled Devices: (a) Blocking Characteristics; (b) Output Characteristics.

GEN-2 BIDFET

A significant enhancement in the BiDFET die performance has been recently achieved with an innovative new chip design and process technology. The integration of the JBS diode inside the MOSFET cell for the Gen-1 chip design produces a large cell pitch of 6.1 μm with low channel density. In order to simultaneously obtain ohmic contacts to the N^+ and P^+ regions for the MOSFET while achieving a low leakage current Schottky contact to the drift region for the JBS diode, it is necessary to anneal the Nickel contacts at 900 °C [2]. This process produces an N^+ source contact specific resistance of 0.8 mΩ-cm^2. Modelling of the JBSFET on-resistances has shown that the total on-resistance is significantly increased due to the large cell pitch and high source contact resistance [5].

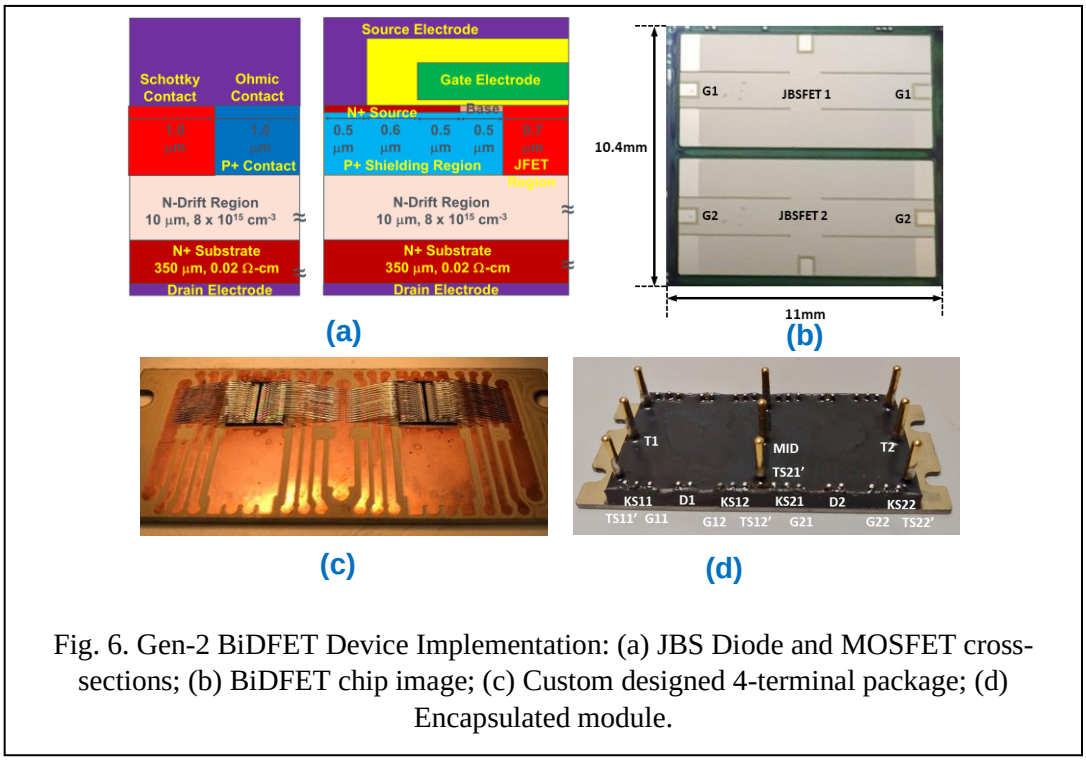


Fig. 6. Gen-2 BiDFET Device Implementation: (a) JBS Diode and MOSFET cross-sections; (b) BiDFET chip image; (c) Custom designed 4-terminal package; (d) Encapsulated module.

A much lower specific on-resistance for the MOSFET cells within the Gen-2 BiDFET device was achieved by separating the JBS diodes from the MOSFET cells and locating them at four corners of the chip. The MOSFET cell size could then be reduced to 2.8 μm, as shown in Fig. 6(a) right side, to achieve 2.2x increase in channel density. The contact to the P^+ region is made orthogonal to the cross-section to make the cell pitch smaller. The Nickel contact to the N^+ source region of the MOSFET was annealed at 1000 °C to reduce the specific contact resistance to 0.05 mΩ-cm^2. The specific on-resistance of the fabricated MOSFET cell with this design and process was measured to be 4.5 mΩ-cm^2, an improvement by a factor of 2.5-times compared with the Gen-1 devices. In order to ensure effective bypassing of the MOSFET body-diode, 10 % of the active area was ascribed to the JBS diodes while keeping the die footprint the same as that of the Gen-1 devices. The Titanium contact to the JBS diodes was separately fabricated to achieve the Schottky contact. JBS diode test elements with an active area of 0.045 cm^2 (the same value as the JBS diodes inside the JBSFETs in the Gen-2 chip) fabricated with the Gen-2 BiDFETs were found to have an on-state voltage drop of less than 2.5 V confirming effective bypassing of the MOSFET body diodes in the BiDFETs. The MOSFET cells in the remaining 90 % of the active area have a calculated on-resistance of 12 mΩ for each JBSFET. Consequently, the new chip architecture and process creates a Gen-2 BiDFET device with an on-resistance of about 25 mΩ, which is half that of the Gen-1 device, *while maintaining the same chip size*. This is a major technological improvement for SiC BiDFETs in terms of reducing the die cost and module size

in half. An image of the Gen-2 BiDFET chip is shown in Fig. 6(b). The regions with the JBS diodes in the four corners of the chip are visible due to a slight difference in the metal texture. The Gen-2 BiDFET chips were packaged in the same half-bridge module designed for the Gen-1 paralleled devices as shown in Fig. 6(c) and occupy half the space. The encapsulated module is shown in Fig. 6(d).

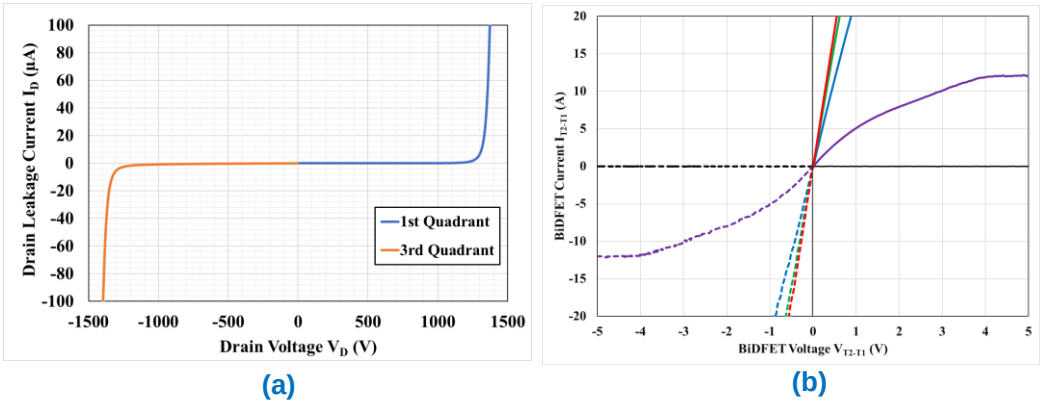


Fig. 7. Gen-2 BiDFET Device: (a) Blocking Characteristics; (b) Output Characteristics.

The measured blocking characteristics for the Gen-2 BiDFET device are shown in Fig. 7(a) in both quadrants. The device can support 1.4 kV in both the first and third quadrants when the gates G1 and G2 are shorted to the respective terminals T1 and T2. This Gen-2 BiDFET has sharper breakdown characteristics than the Gen-1 devices. The device exhibits the desired gate voltage controlled output characteristics with saturated drain current at lower gate bias voltages, as shown in Fig. 7(b). It has a total on-resistance of 27 mΩ at a gate bias of 20 V, which is close to the design value. Double pulse testing of the Gen-2 BiDFET devices was performed at a drain supply voltage of 800 V and current of 20 A. The extracted turn-on, turn-off, and total switching losses were 1120, 250, and 1370 μJ. These values are smaller than those observed for the paralleled Gen-1 BiDFET devices.

Parameter, Units	Gen 1 (2 Chips)	Gen 2 (1 Chip)	Improvement
Chip Area, cm^2	2.28	1.14	2x
$R_{DS,ON}$, mΩ	25	27	-
g_M, S	15	15	-
C_{ISS}, pF	15100	11730	1.3x
C_{OSS}, pF	1050	600	1.75x
C_{RSS}, pF	70	70	-
E_{ON}, μJ	1350	1120	1.2x
E_{OFF}, μJ	460	250	1.8x
E_{TOTAL}, μJ	1810	1370	1.3x

Table II

A comparison between the Gen-1 BiDFET technology with the Gen-2 BiDFET technology is provided in Table II. The improvements in performance are shown in the right-hand column. It can be seen that a BiDFET device on-resistance of 25 mΩ has been achieved with a remarkable 2-times reduction in SiC chip area, which is important for the reduction of chip cost and package size. The capacitances for the single Gen-2 BiDFET chip are smaller than those measured for the paralleled Gen-1 BiDFET devices. In particular, the output capacitance (C_{OSS}) for the Gen-2 BiDFET is 1.75 times smaller, which leads to the reduced switching losses measured for the Gen-2 BiDFET devices.

ADVANCED PACKAGING APPROACH

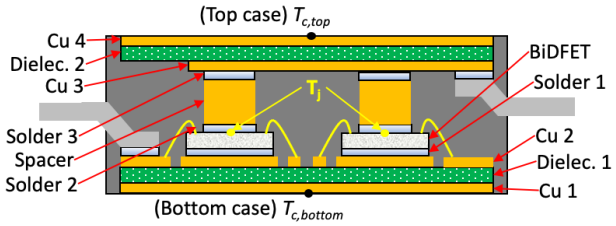
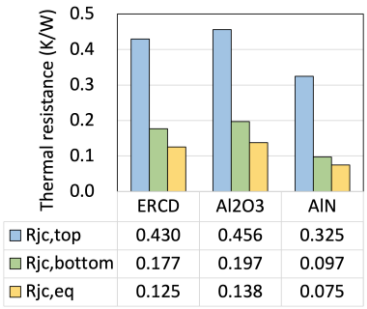


Fig. 8. Two-sided power package to compare ceramic and ERCD dielectric isolated substrates.

The target for this research was a low cost, reliable converter operating in a harsh environment with preferred convective cooling. Since the BiDFET has very low loss, an advanced alternative packaging approach was adopted. An investigation was undertaken to compare the use of ultra-thin epoxy resin composite dielectric (ERCD) as a replacement to traditional DBC that uses plate ceramic. The ERCD material recently introduced by RISHO KOGYO Co. Ltd. is characterized as having 10 W/mK, 40 kV/mm B.V., modulus of 53 GPa, operation at ≤300 °C, and thickness of 120 µm. The material is available as a metalized film, laminate or clad on thick copper to create an insulated metal substrate. Use of an organic approach allows for a metalized substrate, or complete module, to be processed by high-end PCB companies at substantially reduced cost and turnaround time.



	ERCD	Al2O3	AlN
Rjc,top	0.430	0.456	0.325
Rjc,bottom	0.177	0.197	0.097
Rjc,eq	0.125	0.138	0.075

Fig. 9. Thermal resistance of the two-sided package comparing ceramic and DBC.

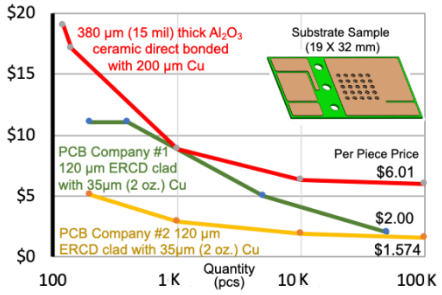


Fig. 10. Comparative pricing of advanced ERCD substrate and Al_2O_3 DBC

To compare ceramic to ERCD, a two-sided module structure, Fig. 8, was designed and simulated in ANSYS as reported in [6]. Two SiC die were mounted and encapsulated to allow heat flow from both surfaces. Spacers were assumed to cover 60% of the die area. For a two-sided structure, four possible combinations of topside and bottom-side dielectrics of ceramic and ERCD were considered, with further consideration of two types of ceramic, Al_2O_3 and AlN. The ceramics were 380 µm thick clad with 127 µm of Cu, and ERCD was 120 µm thick with 100 µm Cu. The thermal conductivities were 24, 170 and 10 W/mK for Al_2O_3, AlN and ERCD respectively. Comparative results for thermal resistance are shown in Fig. 9 and shows that the ERCD $R_{jc,eq}$ is 10% better than Al_2O_3. Though ERCD has lower conductivity, the thinness allows the conductance to be higher. Since cost is of concern and the power dissipation capability with ERCD is well within the project requirements, the more costly AlN and ceramic processing can be avoided. Since cost is of paramount concern, a 19 mm X 32 mm exemplar substrate was provided to three vendors for pricing. The ERCD approach was one third or less than Al_2O_3 DBC, Fig. 10. The ERCD is rated for continuous operation up to 300°C as noted in the paragraph above. Over temperature of the BiDFET would not noticeably affect the cost comparison, and the reliability issues would be dominated by chip attachment in both DBC and ERCD.

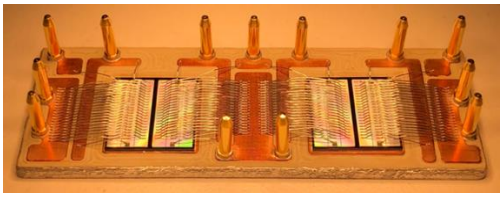


Fig. 11a. Gen-1 BiDFET mounted on ERCD insulated metal substrate [6]

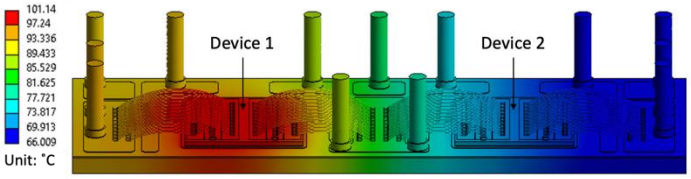


Fig. 11b. Temperature distribution for a Gen-1 BiDFET operating with an I_d = 20A.

The Gen-I BiDFET un-encapsulated single-sided module mounts the die on an ERCD insulated metal substrate (eIMS) as shown in Fig. 11a [6]. The ANSYS thermal analysis, Fig. 11b, shows a 101 °C worst case temperature in a 66 °C environment with conductive cooling with I_D=20A. The Gen-2 has much lower loss, as discussed above, and is well matched to the more cost effective advanced ERCD packaging approach.

IMPACT ON CONVERTERS

A four-quadrant switch enables matrix converter topologies that do not require bulky inductors or electrolytic capacitors for their operation. Yet such converters are not popular commercially, primarily due to a greater number of devices than voltage source converters. The impact of BiDFET invention on the commercial viability of such converters can be understood by accounting BiDFET effect on three of the converter performance metrics: reliability, size, and efficiency.

The reliability of the converter depends on the number of components and the reliability of each component. The BiDFET can replace four-quadrant switch implementations utilizing multiple discrete devices, which leads to not only a lower number of devices per converter but also a lower number of unreliable wire bonds. A monolithic device will obviously require lesser space than discrete devices based four-quadrant switch. The switches' reduced size and simpler packaging facilitate a smaller inductance commutation loop and, consequently, lesser over-voltage for the same di/dt transition or faster di/dt transitions for the same overvoltage. The switching loss of devices typically decreases with faster di/dt transitions.

Furthermore, the BiDFET constituent JBSFETs offer numerous advantages over MOSFETs. JBSFET has lower turn-on loss and almost constant total switching loss over the temperature variation because the JBS diode has a much lower reverse recovery charge than MOSFET's P-i-N body diode. The JBS diode also has almost no variation in stored charge or reverse recovery time with variation in dead-time duration, causing a smaller turn-on current spike and hence allowing faster dv/dt transition, which further decreases the device switching loss.

Depending on the converter modulation scheme, one constituent FET of BiDFET might conduct current for a longer duration or switch more often than the other constituent FET. For example, in a single-phase matrix converter, one constituent FET will remain on for the entire positive A.C. half-cycle while the other is modulated and vice versa during the negative A.C. half-cycle. The temperature cycling of these constituent FETs in a BiDFET will be narrower than discrete devices in a four-quadrant switch implementation. Due to the monolithic nature of BiDFET, the losses in one FET will heat up the other FET as well. This narrower temperature cycle of the device will enhance its reliability further. This phenomenon is expected to provide significant benefits in motor drive applications with lower [e.g. < 10 Hz] output frequency.

Therefore, the BiDFET device has enormous potential for efficient, power-dense, and reliable matrix converters that are fundamentally better than voltage source converters in some applications. The performance of current source converter, T-type voltage source converter, Vienna rectifier, hybrid third-harmonic injection based rectifier, auxiliary resonant commutated pole inverter, and other converters utilizing four-quadrant switches, can also be improved through the use of BiDFET device. The operation of BiDFET die and package has been successfully validated through switching tests at 800 V, 20 A [4], and continuous operation of the single-phase isolated AC/DC converter hardware at 2.3 kW, 400 V_{DC} input, and 277 V_{RMS} output [7].

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REFERENCES

[1] B. J. Baliga, "Monolithically-Integrated AC Switch having JBSFETs therein with Commonly Connected Drain and Cathode Electrodes" *U.S. Patent # 10,804,393*, Issued October 13, 2020.

[2] W. Sung and B. J. Baliga, "Monolithically Integrated 4H-SiC MOSFET and JBS Diode (JBSFET) Using a Single Ohmic/Schottky Process Scheme," *IEEE Electron Device Letters*, Vol. 37, pp.1605-1608, 2016.

[3] K. Han, A. Agarwal, A. Kanale, B.J. Baliga, S. Bhattacharya, T-H Cheng, D. Hopkins, V Amarsinghe, and J. Ransom, "Monolithic 4-Terminal 1.2 kV/20 A 4H-SiC Bi-Directional Field Effect Transistor (BiDFET) with Integrated JBS Diodes", IEEE *Int. Symp. On Power Semiconductor Devices and I.C.s*, pp. 242-245, 2020.

[4] A. Kanale, T-H Cheng, S. S. Shah, K. Han, A. Agarwal, B.J. Baliga, D. Hopkins, and S. Bhattacharya, "Switching Characteristics of a 1.2 kV, 50 mΩ SiC Monolithic Bidirectional Field Effect Transistor (BiDFET) with Integrated JBS Diodes", *IEEE Applied Power Electronics Conf*, pp. 1267-1274, 2021.

[5] A. Agarwal and B.J. Baliga, "Optimization of Linear Cell 4H-SiC Power JBSFETs: Impact of N+ Source Contact Resistance", *Power Electronic Devices and Components*, Volume 2, 2022, 100008, ISSN 2772-3704, https://doi.org/10.1016/j.pedc.2022.100008.

[6] T.-H. Cheng, K. Nishiguchi, Y. Fukawa, B. Jayant Baliga, S. Bhattacharya, and D. C. Hopkins, "Thermal and Reliability Characterization of an Epoxy Resin-Based Double-Sided Cooled Power Module," Journal of Microelectronics and Electronic Packaging, vol. 18, no. 3, pp. 123–136, 2021.

[7] S. S. Shah, R. Narwal, S. Bhattacharya, A. Kanale, T-H Cheng, U. Mehrotra, A. Agarwal, B.J. Baliga, D.C. Hopkins, "Optimized AC/DC Dual Active Bridge Converter using Monolithic SiC Bidirectional FET (BiDFET) for Solar P.V. Applications," 2021 IEEE Energy Conversion Congress and Exposition (ECCE), 2021, pp. 568-575, doi: 10.1109/ECCE47101.2021.9595533.

[8] W. Sung, and B. J. Baliga, "A Near Ideal Edge Termination Technique for 4500V 4H-SiC Devices: The Hybrid Junction Termination Extension," *IEEE Electron Device Letters*, 37(12), pp.1609-1612, 2016, doi: 10.1109/LED.2016.2623423.

[9] B. J. Baliga, "Gen-3 PRESiCE™ Technology for manufacturing SiC Power Devices in a 6-inch Commercial Foundry", *IEEE Journal Electron Device Society*, Special Issue, Vol. 8, pp. 1111-1117, September 2020, doi: 10.1109/JEDS.2020.3014568.