Design Considerations for Developing 1.2 kV 4H-SiC BiDFET-enabled Power Conversion Systems

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***Abstract*—Bidirectional switches are essential for cycloconverter and matrix converter applications to facilitate single-stage AC-AC conversion without intermediate energy storage elements. The 1.2 kV 4H-SiC BiDFET was developed as the first monolithic bidirectional SiC power transistor. This paper describes the design considerations taken into account while creating the BiDFET device and developing custom packages for housing the switch in discrete form for low power applications and in module form for high-power applications. The realized switches are characterized for their on-state and switching performance. The versatility of the BiDFET device is demonstrated by operating a single BiDFET H-bridge in voltage-source-inverter and current-source-inverter topologies only by varying the gate bias on the individual BiDFETs and reversing the input-output connections.**

***Keywords*—Bidirectional, Silicon Carbide, Half-Bridge Module, H-Bridge, BiDFET.**

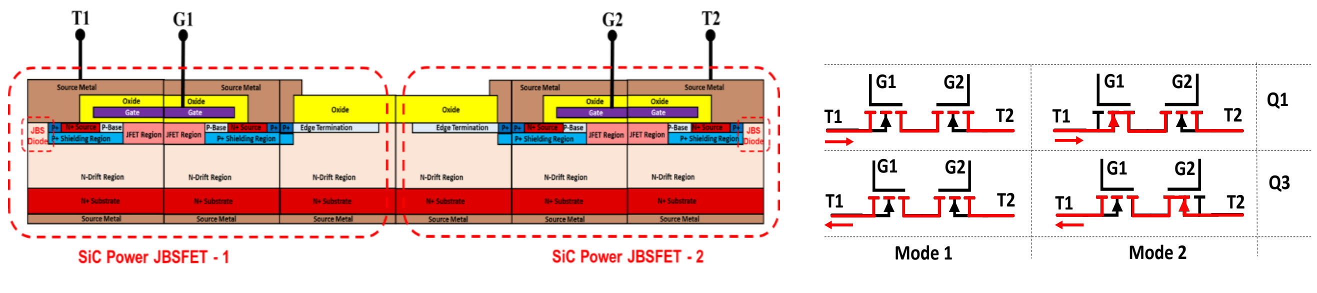
I. Introduction

The proliferation of renewable energy technologies and electric vehicles has created a significant demand for power conversion systems handling bidirectional power flows [1], such as grid connected PV energy resources, electric vehicle charging infrastructure and energy storage systems. Parallely, the development and commercialization of silicon carbide power semiconductor devices has boosted research efforts aimed at realizing bidirectional switches [2]. Traditionally, bidirectional switches have been implemented for matrix converter. Unfortunately, these implementations have required a high device count which would increase system bulk [3] and cost. Additionally, these implementations have exhibited large on-state voltage drop while also having high switching losses.

The 1.2 kV 4H-SiC BiDirectional Field Effect Transistor (BiDFET) [3] has been recently developed as the first SiC-based monolithic bidirectional switch with low forward voltage to enable a compact solution for AC-AC power conversion systems. A cross section of the BiDFET cell structure is shown in Fig. 1, along with its two modes of operation (Mode 1: conduction through both internal MOS channels; Mode 2: conduction through one body diode and one MOS channel). The BiDFET device is realized as a four-terminal switch using two internal power MOSFETs with embedded JBS diodes (JBSFETs) connected in a common-drain configuration. While the BiDFET was developed for AC-AC converter applications, its on-state and switching behavior demonstrate a potential for adoption into conventional voltage-source and current-source inverter applications.

The two gates in the BiDFET can be configured to realize switches for voltage-sourced (VSI), current-sourced (CSI) or matrix converter topologies. It has been shown that the BiDFET has a lower switching loss compared to either of its internal JBSFETs operating independently [4], consequently making it a good option for realizing high frequency voltage-source converters. The presence of two internal channels in the BiDFET enables a reduction in on-state voltage drop, and consequently, conduction losses, compared to reverse-blocking switches, making it an excellent alternative for current-source inverters.

The 1.2 kV 4H-SiC BiDFET has been developed at NCSU as an end-to-end effort, with device design, package development, wafer-level and package-level characterization, switching cell demonstration and implementation in power converter systems [3]-[5]. This paper details the development of the BiDFET as a switch, through the package design and



(a) (b)

Fig. 1. (a) Cross section of the monolithic 1.2 kV 4H-SiC BiDirectional Field Effect Transistor (BiDFET), and (b) Operation Modes with arrows indicating the current flow directions in the first and third quadrants.

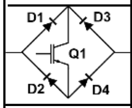
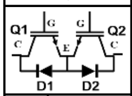
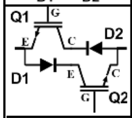
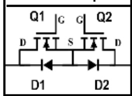
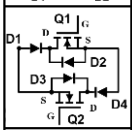
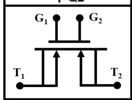
Switch Topology	Switch Description	# of Devices	V_{ON} (V)
	Diode Bridge + Asym. IGBT (**5 dev.**)	*5 Devices*	3.5 V
	Asym. IGBTs + Flyback diodes (**4 dev.**)	*4 Devices*	2.5 V
	Back-to-Back rev. blocking IGBTs (**2 dev.**)	*2 Devices*	2.0 V
	Src.-Conn. SiC MOSFETs + JBS diodes (**4 dev.**)	*4 Devices*	1.25 V
	Bk-to-bk. SiC MOSFETs + series and rev. blocking JBS diodes (**6 dev.**)	*6 Devices*	1.25 V
	***4H-SiC BiDFET***	*1 Device*	0.5 V

Fig. 2. Comparison Chart of bidirectional switch topologies based on device count and on-state voltage drop.

validation process, evolution from discrete to module form, characterization and switching cell realization, and demonstration of operation in converter topologies.

II. Design Considerations

Bidirectional power switches are used in matrix or cycloconverters and multistage inverter circuits to facilitate high-frequency AC-AC converter systems without intermediate energy storage elements such as DC-link capacitors. Conventional Si IGBT- and SiC MOSFET-based switch topologies are shown in Fig. 2. While the IGBT based options use between two and four devices per switch, have voltage drops in excess of 3 V, have high switching losses and a limited operating frequency, the SiC MOSFET based options use between four and six devices per switch and have on-state voltage drops exceeding 1.25 V. The SiC BiDFET is the only monolithic option with a low voltage drop of 0.5 V.

A. BiDFET Chip design considerations

The BiDFET device was fabricated at a commercial 6-inch foundry X-FAB, TX using the NCSU PRESiCE™ process [6]. SiC power MOSFETs are used with antiparallel JBS diodes in order to avoid reverse recovery currents. However, it has been shown that integrating the JBS diode in the SiC MOSFET chip not only reduces the semiconductor area [7], but it also completely suppresses reverse current flow through the P-N body diode [8].

Conventional bidirectional switch implementations with discrete SiC MOSFETs favor a common-source configuration as this option allows a common reference node for the two gate drive circuits [9]. However, it is not feasible to realize this topology in a monolithic form. A common-drain configuration with two MOSFETs placed adjacent to each other on the wafer, on the other hand, not only allows monolithic fabrication, but also enables rapid adoption commercially as the process steps are identical to creating individual MOSFETs. Consequently, the 1.2 kV 4H-SiC BiDFET was designed with two back-to-back JBS-integrated-MOSFETs (JBSFETs) in a common-drain configuration.

The 1.2 kV SiC BiDFET was designed with a chip area of 1 cm². The device was designed to have an on-resistance of 50 mΩ at 10 A and a gate bias of 20 V on both gates. Device on-resistance can be reduced by increasing chip active area. Consequently, the BiDFET die layout was scaled up from a previously fabricated SiC power JBSFET [10][11] to have an active area in excess of 0.45 cm² per JBSFET to keep the on-resistance below 25 mΩ. The designed BiDFET has been shown to achieve a low on-state voltage drop of 0.5 V at a current of 10 A, which is lower than that of conventional topologies by a factor of 2.5x.

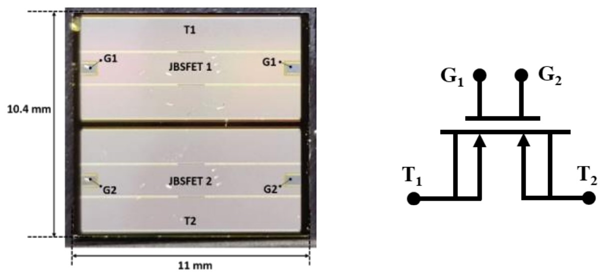
An image of the fabricated BiDFET is shown in Fig. 3(a). The BiDFET chip layout was made symmetric by providing two gate pads within each JBSFET, both having runners upto the center of the chip. The dual-gate-pad design with runners creates two parallel paths for the gate voltage, consequently speeding up the propagation of the applied gate bias throughout the chip.

B. Package Design Considerations

Optimized power semiconductor device packages add minimum resistance and inductance when connecting chip terminals to external pins, while also keeping the weight overhead, switch volume, thermal resistance and cost below a minimum specified value. Consequently, a custom discrete package was designed for the first iteration of 1.2 kV 4H-SiC BiDFET devices at the NCSU PREES laboratory with surface mount pins having Kelvin-connections to terminals T_1 and T_2, and top-side cooling.

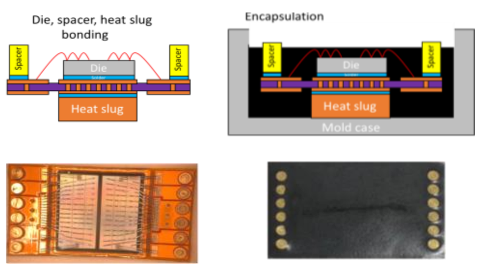
Package materials can be selected by considering the maximum junction temperature expected on the BiDFET switch, described by

$$I_{D,Max} = \sqrt{\frac{T_{J,Max} - T_C}{R_{JC} \times R_{DS,ON}(@T_{J,Max})}} \quad (1)$$



(a) (b)

Fig. 3. (a) Top View of the fabricated 1.2 kV 4H-SiC BIDFET device showing the dual-gate-pad layout, and (b) simplified circuit symbol for the BiDFET.



(a) (b)

Fig. 4. Cross section and the bottom side view of the Custom SMD package for the BiDFET (a) without encapsulation, and (b) with encapsulation.

where $I_{D,Max}$ is the maximum possible current through the switch under normal operating conditions with an ideal heat sink, $T_{J,Max}$ is the maximum rated junction temperature of the switch, T_C is the case temperature, $R_{DS,ON}(@T_{J,Max})$ is the BiDFET on-resistance at max. junction temperature, and R_{JC} is the junction-to-case thermal resistance of the package. For SiC switches, $T_{J,Max}$ is usually 175 °C, while $I_{D,Max}$ and $R_{DS,ON}$ are packaged device specifications.

The custom package used a flex-PCB as substrate to mount the switch as shown in Fig. 4(a). A copper slug was attached to the backside of the die-mounting pad for heat removal, as depicted by the package cross-section in Fig. 4(b). Copper cylinders were provided on either side of the BiDFET, connected by wire-bonds to the pads on the chip. The high-voltage terminals were bonded to the respective JBSFET Source areas using an array of twelve 5-mil stitched-wire bonds to keep resistance overhead below 5% of the BiDFET on-resistance. A Kelvin-source terminal was provided for each gate pad. This assembly was encapsulated in an epoxy-resin potting material to realize a low-weight, 14 mm x 23 mm package.

C. Application Design Considerations

The discrete BiDFET package was characterized for on-state and switching behavior under various operating conditions. Dynamic characterization was conducted to evaluate switching loss at different currents and case temperatures [4]. This data was used to inform the design of a 2.3 kW DC/AC dual active bridge converter, where four BiDFETs would form a single-phase AC-AC cycloconverter [5].

The converter specifications were determined by formulating an optimization problem and comparing two approaches – (1) achieving minimum combined total VA rating, and (2) Minimum RMS current rating of both the primary and secondary sides. The final design resulted in an optimized high-frequency RMS current, magnetics volume and soft-switching region for the switches, and achieved an overall efficiency of 95.3% at full load and a switching frequency of 50 kHz.

D. SiC BiDFET Module Design and Validation

Power conversion system efficiency is intimately influenced by the power handling capability and thermal performance of the switches, which in turn, is determined by the heat removal capabilities of the package and system heat sinks. Furthermore, applications such as onboard charging in electric vehicles require compact hardware assemblies with maximum power density. This necessitates the development of bidirectional power modules.

A custom designed single-side cooled (SSC) half-bridge (HB) module with two BiDFETs in parallel per switch was planned, as shown in Fig. 5. The module was designed with an Epoxy-Resin Composite Dielectric (ERCD) substrate with an inherent Aluminum base plate. This dielectric material has been shown to be more cost-effective and have better thermal performance and stress ruggedness compared to Al2O3 and other Direct-Bond-Copper (DBC) ceramic substrates [12]. The module was designed in a symmetric fashion to enable easy mounting on the converter board. The module was provided with three long 15 mm cylindrical pins for each of the power terminals, and 5 mm pins for the gate, kelvin-source and common-drain terminals. The power terminals are designed to be through-hole mounts, while the signal pins are designed to be surface-mounts. This combination of pins enables excellent mechanical stability, precise alignment and good adherence to the board. Additionally, the aluminum baseplate is provided with notches to mount the module on to a heat sink.

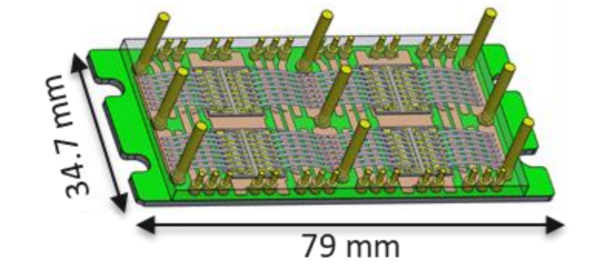


Fig. 5. 3D model top view of the paralleled BiDFET half-bridge module.

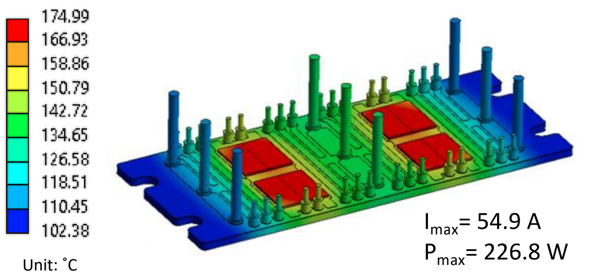
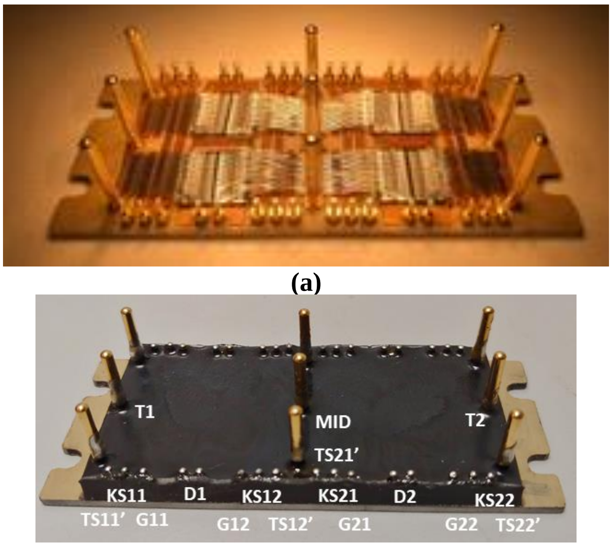


Fig. 6. Simulated heat map of the single side cooled half-bridge paralleled BiDFET module used to estimate maximum device current for a given cooling condition.



(b)
Fig. 7. Top view of the single-side-cooled, paralleled BiDFET half-bridge module (a) before encapsulation, (b) after encapsulation.

The 3D model of the proposed module was simulated using ANSYS to determine the maximum continuous current allowed for a given cooling condition, assuming a maximum semiconductor die temperature of 175 °C. A sample simulated heat map for the HB module is shown in Fig. 6. The designed module was then fabricated at the NCSU PREES laboratory. The top views of the SSC HB BiDFET module with exposed wire bonds, and post encapsulation, are shown in Fig. 7. In order to validate the thermal design of the module, it was heated to a set case temperature and the switch on-resistance and conduction loss were measured at currents varying from 20 to 50 A. The power module thermal validation was conducted by comparing the power loss produced at a set case temperature to the simulated junction temperature for a given power loss.

III. Experimental Results

The 1.2 kV 4H-SiC BiDFET switches encapsulated in the SSC HB module were characterized to determine on-state and switching behavior. Static characterization was performed on a Keysight B1505A Curve Tracer. Measured parameters included on-resistance, threshold voltage, transfer characteristics and switch capacitance.

Dynamic characterization was performed on a custom double-pulse test setup at a DC voltage of 800 V and different currents.

A. Static Characteristics

The BiDFET can be operated in two modes, as shown in Fig. 1(b). The measured bidirectional on-state characteristics of the high-side switch in the SSC HB module in Mode 1 measured across different gate bias voltages are shown in Fig. 8. The measured on-resistance of the high-side switch in the first and third quadrants at a current of 10 A and a gate bias of 20 V is 23 mΩ.

The measured bidirectional on-state characteristics of the high-side switch in the SSC HB module in Mode 2 measured across different gate bias voltages are shown in Fig. 9. The measured on-state voltage drop of the high-side switch in the first and third quadrants at a current of 10 A, and a gate bias of 20 V is 1.5V.

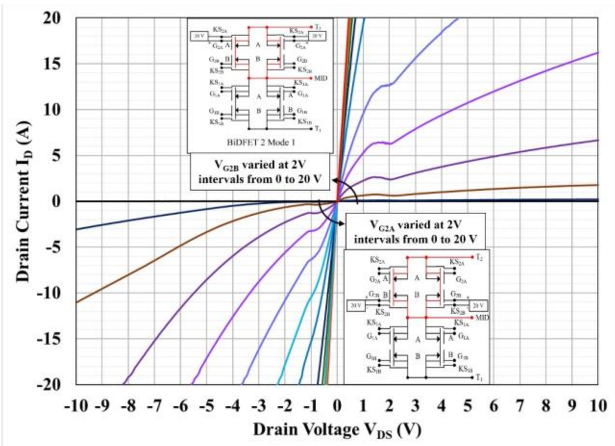


Fig. 8. Measured on-state characteristics of the SSC HB BiDFET module in Mode 1.

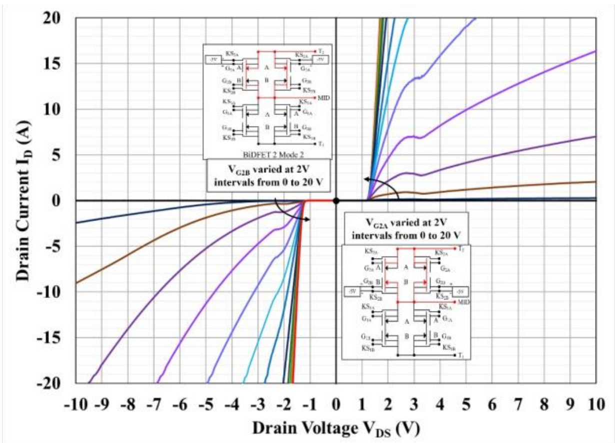


Fig. 9. Measured on-state characteristics of the SSC HB BiDFET module in Mode 2.

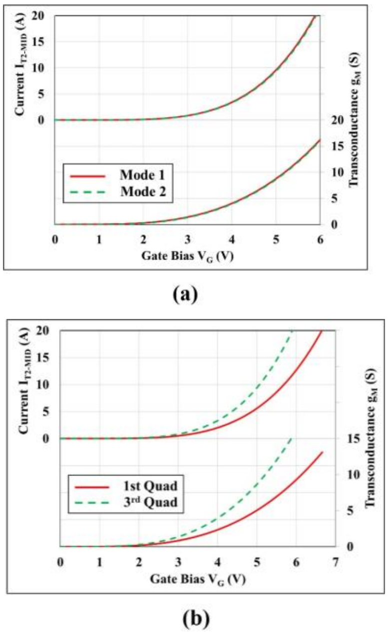


Fig. 10. Measured transfer characteristics for the SSC HB BiDFET module (a) comparing Modes 1 and 2, and (b) comparing 1st and 3rd quadrant behavior in Mode 1.

The BiDFET switches exhibited a threshold voltage of 1.12-1.15 V in first and third quadrant considering a current of 1 mA per BiDFET.

The measured transfer characteristics for the paralleled high-side BiDFETs in the first and third quadrants with a bias of 20 V are shown in Fig. 10. The transfer curves measured for Modes 1 and 2 are plotted in Fig. 10(a) while the transfer curves for the high-side BiDFETs in the first and third quadrants are plotted in Fig. 10(b).

These characteristics demonstrate that the BiDFET SSC HB module has symmetric on-state behavior, and achieves half the resistance per switch as that obtained with discrete packages, as expected.

B. Dynamic Characteristics

The SSC HB BiDFET module was mounted on a 4-layer double-pulse test (DPT) board. The power stage was equipped

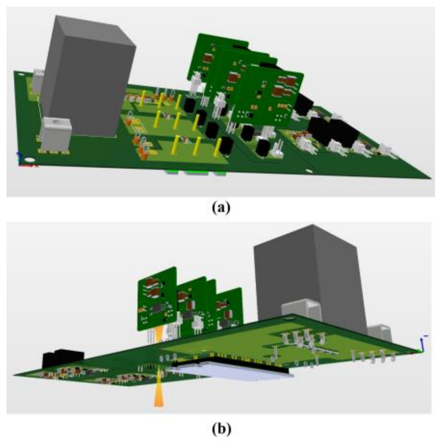


Fig. 11. 3D model of the double pulse test setup designed for dynamic characterization of the SSC HB BiDFET.

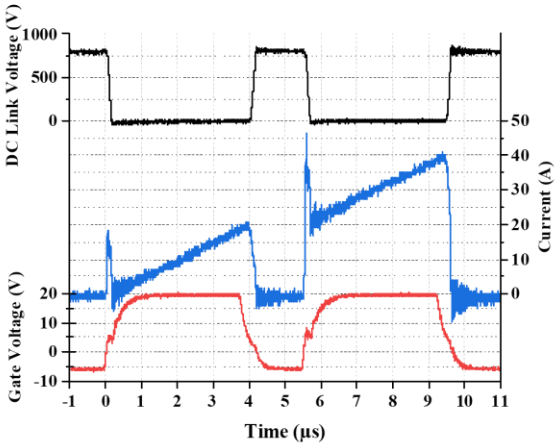


Fig. 12. Measured switching test waveforms for the SSC HB BiDFET at a DC Link voltage of 800 V and a current of 20 A.

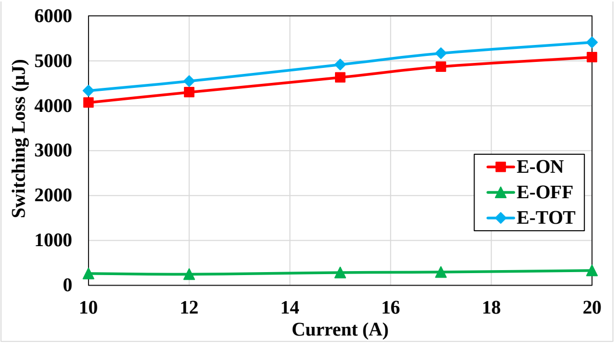


Fig. 13. Measured turn-on, turn-off and total switching loss for the SSC HB BiDFET module at V_{DC} = 800 V and different currents.

with DC link capacitors and decoupling capacitors in close proximity to the module, while the gate drive circuitry was realized on daughter cards. A 3D image of the designed double-pulse test board is shown in Fig. 11. The module is attached at the bottom side of the power stage in order to be mounted on to a heatsink.

Switching tests were conducted at 800 V across a range of currents (10 – 20 A) and module temperatures (25 °C to 125 °C). The gate drive was configured to provide -5/+20 V to the individual BiDFETs. The measured switching waveforms at 800 V and 20 A are shown in Fig. 12. The measured turn-on and turn-off loss values across different currents are shown in Fig. 13. Turn-on losses are dominant as also observed in SiC power MOSFETs.

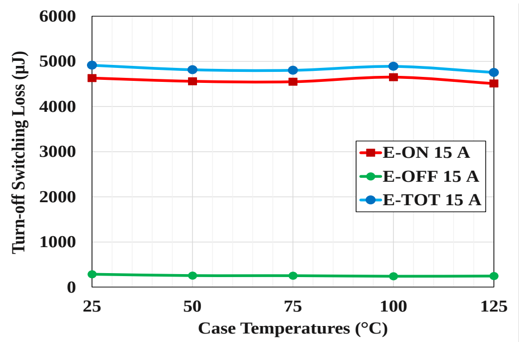


Fig. 14. Measured turn-on, turn-off and total switching loss for the SSC HB BiDFET module at V_{DC} = 800 V and I_D = 15 A across different case temperatures.

The measured turn-on, turn-off and total switching loss values at 800 V, 15 A across different case temperatures is shown in Fig. 14. The total switching loss variation from 25 °C to 125 °C stays within 3%. It has been demonstrated that the switching losses in a SiC JBSFET device do not exhibit much increase (< 5%) across a wide range of case temperatures compared to SiC MOSFETs (~ 44%) with similar cell structures [10]. The measured switching behavior for the SSC HB module agrees with this observation.

C. *Converter Concept Demonstrations*

Two BiDFET half-bridge modules were mounted on double-pulse test boards and connected in parallel to create an H-bridge. Since the BiDFET modules are symmetric, their gate drives can be configured to achieve operation in Mode 1 or Mode 2, as required. This configurability allows the realization of both VSI and CSI topologies with the BiDFET. The BiDFET H-bridge assembly is shown in Fig. 15.

The BiDFET is equipped with two internal MOS channels and two antiparallel JBS diodes. Consequently, selective application of -5 V and +20 V on individual gate-source terminals of the BiDFETs can achieve operation as a voltage-switch (Unidirectional voltage blocking with Bidirectional current conduction), a current-switch (Unidirectional current conduction with Bidirectional voltage blocking) and a matrix switch (four-quadrant operation). The discrete BiDFET devices have been shown to operate in a single-phase matrix converter [5] to achieve AC-AC conversion with good THD on output currents, high efficiency and compact magnetics.

The H-bridge assembly in Fig. 15 was assembled as a concept demonstration to exhibit the versatility of the BiDFET device. The same assembly, with a few modifications, can be operated as a Voltage-source inverter (VSI) or as a current-

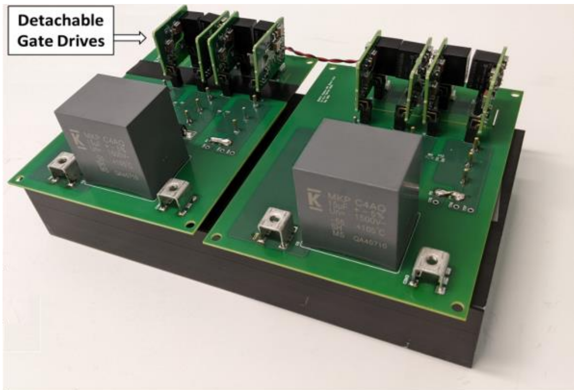


Fig. 15. A H-bridge assembly made using two SSC HB BiDFET modules connected in parallel.

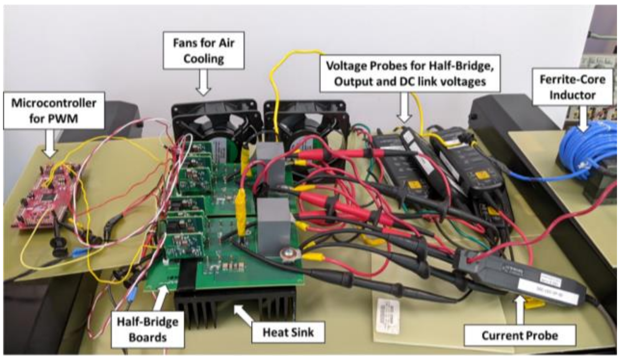


Fig. 16. The BiDFET H-bridge assembly being operated as a Voltage-Source Inverter with an R-L load.

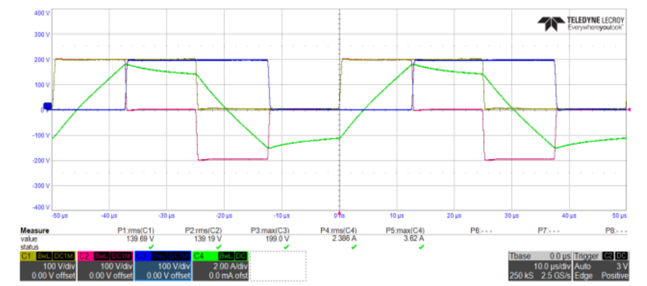


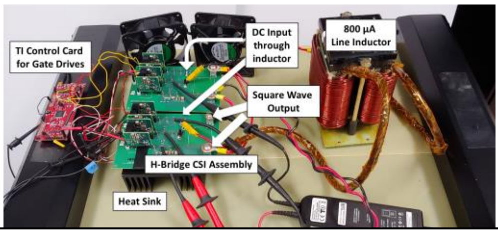
Fig. 17. Measured DC-link voltage, output voltage, and output current waveforms for the SSC BiDFET H-bridge VSI.

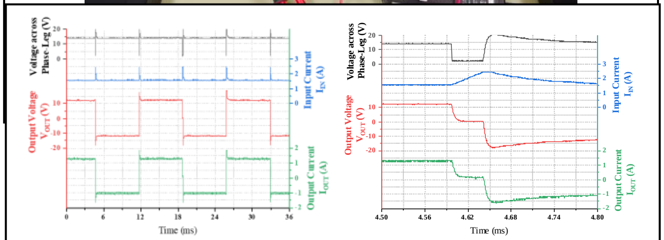
source inverter (CSI). Operating the BiDFETs in Mode 1 realizes a VSI. The VSI topology was realized using the existing DC link capacitors on the DPT boards and a 435 µH inductor and 200 Ω resistor used as an R-L load at the output. The assembled VSI test setup is shown in Fig. 16. Continuous mode operation was achieved at a DC input voltage of 200 V and an output RMS current of 1.8 A at a power level of 335 W. The DPT board is designed with 1 oz. copper per layer and a through-hole to allow switching-test current sensing. The VSI continuous mode currents were kept below 3A to avoid overheating of the board copper and prevent damage to the contact pads.

The measured waveforms showing VSI operation are shown in Fig. 17. The BiDFET devices were switched at a frequency of 20 kHz with a 12.5 µs duty cycle and a 2 µs dead-time between complementary gate signals in each phase leg to avoid short-circuiting a module. The two modules were switched with a 90° phase shift.

Operating the BiDFETs in Mode 2 makes the H-bridge work like a CSI. This topology requires an inductor at the input and a capacitor bank at the output. A preliminary demonstration of the H-bridge was achieved in a CSI topology using an 800 µH inductor and using the existing decoupling capacitors on the DPT board as output filters. The assembled CSI setup is shown in Fig. 18, with its measured waveforms in Fig. 19. The CSI was operated at an RMS current of 1.5 A.

The above results demonstrate that the BiDFET H-bridge can be operated as a VSI or a CSI by changing the operating modes of the BiDFETs.





(a) **(b)**

Fig. 19. (a) Measured DC input voltage, Input current, output voltage and output currents for the BiDFET CSI assembly (b) Zoomed-in view of the switching transient showing the overlap between complementary switches.

IV. Discussion

The 1.2 kV 4H-SiC BiDFET enables the creation of compact power converters with bidirectional power flow handling capability without the need for power storage elements such as DC link capacitors. The BiDFET-enabled DC/AC DAB realizes a single-stage AC-AC conversion, as compared to the conventional AC-DC/DC-AC cascades which operate at reduced power densities. Photovoltaic energy farms can benefit from BiDFET enabled topologies as compact power converter systems can be transported and readily deployed in remote areas. Similarly, electric vehicle onboard chargers stand to benefit greatly from BiDFET-enabled topologies. As renewable energy technology proliferation increases on a global scale, the electric grid must adapt to integrate distributed energy resources without disrupting the existing power distribution networks. This draws attention to local units that produce as well as store energy. Such units need a bidirectional power flow regulator that can supply renewable energy into the grid and intelligently store up energy as an emergency reserve.

The BiDFET module is developed in a compact, symmetric fashion to enable easy deployment in converter systems. The adaptability of the BiDFET device enables similarly designed power stages to be deployed in both VSI and CSI topologies. This could help accelerate the commercialization of BiDFET-enabled converter systems.

V. Conclusions and Future Work

The 1.2 kV 4H-SiC BiDFET has been developed as a monolithic bidirectional power transistor using two back-to-back JBS-integrated MOSFETs in the common-drain configuration. The BiDFET has been shown to produce symmetric blocking and on-state characteristics along with steady switching behavior across a range of case temperatures. Custom-designed discrete BiDFET packages were realized using flex-PCB, characterized for their static and dynamic performance and successfully deployed in an optimized 2.3 kW DC/AC dual active bridge converter. In order to scale up the power handling capability of the BiDFET device, a single-side cooled half-bridge (SSC HB) module was designed with two paralleled BiDFETs per switch. The module was designed to keep die junction temperatures below 175 °C. The FEM simulated design was validated by continuous mode current conduction tests. Subsequently, the module was characterized and deployed in a switching cell with detachable gate drives.

Two switching cells were developed with one SSC HB module per board. The two switching cells were connected in parallel to realize an H-bridge. The SiC BiDFET is equipped with two internal MOS channels and two JBS body diodes. This enables the realization of voltage-switch and current-switch topologies by operating the BiDFET in Mode 1 and Mode 2, respectively. The H-bridge assembly was operated in continuous mode as a VSI and then as a CSI by changing the connections at its input and output terminals.

The evolution of the 1.2 kV SiC BiDFET switch as a discrete package and subsequently as a module demonstrates the availability of a simple power device solution to enable single-stage AC-AC conversion systems without the need for intermediate energy storage elements. Further research towards deploying BiDFETs in power converters could enable large scale commercialization of cycloconverter and matrix converter technologies.

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