**CMPEN 270: Digital Design: Theory and Practice**

**Module 2 Lab: Introduction to the Basys-3 Board**

**Due: 1/23/22**

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**Grading Rubric**

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| **Criteria** | **Grade** |
| Initial grade, based on how well the functional specification is met  Excellent (exceptional achievement) 90-100%  Good (extensive achievement) 80-89%  Satisfactory (acceptable achievement) 72-79%  Poor (minimal achievement) 65 to 71%  Failure (inadequate achievement) 0-64% | / 25 |
| Modification for design documents  Block diagrams  State diagrams  State tables  Other |  |
| Modification for coding style, comments, efficiency  Header comments for files  Other comments (informative but not excessive)  Proper code indenting, alignment, use of whitespace  Code is clean (doesn't have commented out code without a good reason)  Self documenting code (good signal and component names, clear structure, etc.)  General approach (algorithms)  Coding details (operations)  Proper use of components  VHDL matches design documents  Other |  |
| Modification for sections in this report  Design  Verification  Evaluation  Questions  Other |  |
| Bonus (optional challenge, etc.) |  |
| Penalties  No grade until all deliverables are submitted, late submission penalty for anything submitted late  Late submission: (<1 day) -10%, (<1 week) -30%, (<2 weeks) -50%, (>=2 weeks) -99%  Attachments missing, not in order, instructions not followed: -10%  Other |  |
| TOTAL (Max is 100% of total points unless specified otherwise in handout) | / 25 |

**ACKNOWLEDGEMENT**

This work is entirely my own and I did not provide any assistance except as noted.

100% Robert Myers \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_Robert Myers\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**ATTACHMENTS**

The following are attached, in this order:

* Starting Digital Circuit page with completed truth table

**DESIGN**

There was no design for this lab.

**VERIFICATION**

For this Lab, I split the functional specification into two parts, the I/O part that followed the circuit design given, and the Operation part. After filling out the truth table of I/O circuit, I converted this to the .vhd file. I then ran the simulation to verify my logic was correct. Before programming my FPGA board, I had to ensure that the pin was mapped correctly in the constraint file. Here I went cross-referenced the truth table and the results from flipping “A”, “B” and “C”.

For the operation part, I started by mapping all necessary pins in the constraint file. Then I moved over to the .vhd file and added all pins the entity section. I then added these pins under the alias section and assigned appropriate names. After, I converted the logic from the Lab02 handout to the .vhd file using a combination of not, and, or, nor, xor, xnor, and nand. I built 1-2 requirements at a time and tested in the simulation before programming my board as I felt this was faster than synthesizing, implementing, generating bitstream and programming every time I wanted to test. Once I confirmed testing in the simulation, I then programmed the board and tested again on the physical device.

**EVALUATION**

No performance metrics are required for this lab.

**QUESTIONS**

1. How many test cases are needed to test the functional specification for LD5 exhaustively (every possible input combination)? Explain how you got this number.

For each input there is 2 possible values, on or off. There are 5 inputs in total. In test case 1 the truth values would be 0 0 0 0 0, the second would be 0 0 0 0 1 and so on. This would be 25 possible combinations which is 32 unique tests.

1. How many test cases are needed to test the functional specification for LD2 exhaustively (every possible input combination)? Explain how you got this number.

For each input there is 2 possible values, on or off. There are 8 inputs in total. In test case 1 the truth values would be 0 0 0 0 0 0 0 0, the second would be 0 0 0 0 0 0 0 1 and so on. This would be 28 possible unique combinations which is 256 unique tests.

1. What FPGA pin is BTNR (the right pushbutton) wired to? What logic family is the pin?

BTNR is wired to T17. The logic family is LVCMOS33.

1. What FPGA pin is LD7 wired to? What logic family is the pin?

LD7 is wired to V14. The logic family is LVCMOS33.