**CMPEN 270: Digital Design: Theory and Practice**

**Module 13 Lab: Memory**

**Due: 4/17/2022**

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**Grading Rubric**

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| **Criteria** | **Grade** |
| Initial grade, based on how well the functional specification is met  Excellent (exceptional achievement) 90-100%  Good (extensive achievement) 80-89%  Satisfactory (acceptable achievement) 72-79%  Poor (minimal achievement) 65 to 71%  Failure (inadequate achievement) 0-64% | / 35 |
| Modification for design documents  Block diagrams  State diagrams  State tables  Other |  |
| Modification for coding style, comments, efficiency  Header comments for files  Other comments (informative but not excessive)  Proper code indenting, alignment, use of whitespace  Code is clean (doesn't have commented out code without a good reason)  Self documenting code (good signal and component names, clear structure, etc.)  General approach (algorithms)  Coding details (operations)  Proper use of components  VHDL matches design documents  Other |  |
| Modification for sections in this report  Design  Verification  Evaluation  Questions  Other |  |
| Bonus (optional challenge, etc.) |  |
| Penalties  No grade until all deliverables are submitted, late submission penalty for anything submitted late  Late submission: (<1 day) -10%, (<1 week) -30%, (<2 weeks) -50%, (>=2 weeks) -99%  Attachments missing, not in order, instructions not followed: -10%  Other |  |
| TOTAL (Max is 100% of total points unless specified otherwise in handout) | / 35 |

**ACKNOWLEDGEMENT**

This work is entirely my own and I did not provide any assistance except as noted.

100% Robert Myers \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_Robert Myers\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**ATTACHMENTS**

The following are attached, in this order:

* Top Level document with your equality comparator circuit

Be sure to submit all files needed to recreate and test your design (all VHDL files, Tcl test files, and the XDC file). Also be sure to submit your demo video.

**DESIGN**

See attached design worksheet.

**VERIFICATION**

I had a tough time with finding what was controlling the order of anodes illuminating. After studying the schematic for the word component, I still could not find what was causing the illuminated segment to bounce from end-to-end in the initial demo. After taking some time away from the lab, I came back with a fresh set of eyes and realized in the Light Show file there was an address selector for the 7-segment light show. It was smooth sailing from there on.

**EVALUATION**

No performance metrics are required for this lab.

**QUESTIONS**

There are no questions for this lab.