

Speeding up SIFT for Security Applications

Ben Anglin, Stanislav Bobovych, Robert Brandon

December 5, 2012

1 Introduction

The goal of this design project is to propose a method of dramatically boosting the performance of the SIFT algorithm. This enhancement is provided in two forms, the introduction of a new ISA-level instruction and the addition of a specialized coprocessor and cache. Specifically, we will allow the most common and processor-intensive pieces of SIFT to be implemented using these specialized structures, rather than relying on a general purpose processor.

2 Background

2.1 Application

For the purposes of this project, the application space of security video surveillance is to be targeted. Our system is designed to allow a security camera's live stream to be analyzed in near-real time, allowing for rapid feature recognition (facial, object, etc). This implementation assumes a fixed input type from a surveillance camera and a reliable processing backend platform.

This usage scenario serves to provide several parameters for the system design. As the input stream from the camera is reliable, we will use the assumption that new data is always available for processing. Because many security systems rely upon custom hardware, we can design a system using some flexibility in terms of power and space requirements. Finally, because we can assume that every frame captured is to be analyzed, we can design our system to explicitly streamline and accelerate image access and processing.

2.2 SIFT

Simply stated, SIFT (Scale-Invariant Feature Transform) is an image processing algorithm. It is used for image recognition and is noted for its ability to recognize elements of an image even when they are rotated or scaled in unusual ways. A full treatment of the algorithm is best left to other papers, but a look at it's core will show what our architecture will impact.

A key part of the SIFT algorithm is scale space construction. This process begins by scaling the image n times (usually shrinking the image). At each scale, a Gaussian blur is applied to the image, generating a new image. This blurring is repeated m times per scale. A set of blurred images at a given scale is known as an octave. In total then, the Gaussian blur is applied to every pixel in $n \times m$ images (every image in every octave). After profiling an implementation of SIFT we decided that this part of the algorithm was a good candidate for speedup.

3 Methodology

3.1 Profiling SIFT

Add this section

3.2 Ahmdal's law

Add this section Why are we speeding up convolution? 30% of computation, blah blah

4 Results

4.1 High level design

The heart of our system is a Convolution Module(CM). This module is dedicated to performing convolution on input images. It uses a dedicated cache, as well as a new instruction that allows the compiler to take advantage of a massively parallel, specialized convolution pipeline to speed up the convolution process.

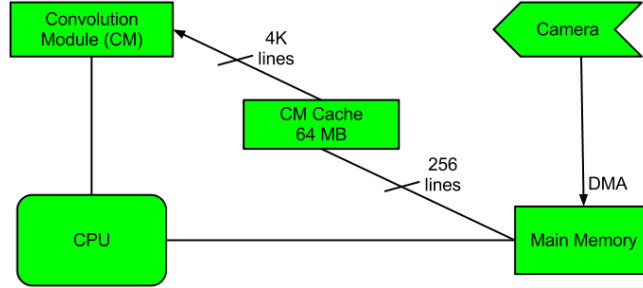


Figure 1

As input, the system uses a grayscale image stream of a camera at a fixed 512 x 512 pixel resolution at any standard frame rate (24, 30, 60 FPS). The camera feed is given DMA access to a fixed region of main memory. This will allow our dedicated cache to easily prefetch images as they arrive. On every hit, the CM cache will prefetch the next set of image data. This ensures a constant flow of data into the CM and ideally eliminates stall cycles caused by cache misses.

During execution of the SIFT algorithm, our new ISA-level instruction will call the Convolution Module (CM) to begin convolving the image stream. Our implementation uses a fixed-size Gaussian kernel to speed up processing. The design we developed allows the CM to deal exclusively with the CM Cache at very high speed. Every cache hit will result in the next image being loaded into the CM module. Once there, every row in the image is convolved in parallel, granting us a massive speedup as discussed later.

4.2 Cache design

4.2.1 Organization

Organization The goal of the special convolution cache is to constantly feed the Convolution Module (CM) with data. We are not concerned with monetary cost or the transistor count of this hardware. We want the CM to execute a single row pass of convolution per call of the CONV instruction. Since our source images are 512x512, we need to give the CM module a cache line that is 512 words, with each word being 8 bits. To accomplish this, the interface to the cash from the CM has to be a 512 word wide bus. To reduce

the hit time on the cache, we will use a direct mapped cache. The cache will use virtual addresses to once again keep hit time as low as possible. To avoid capacity misses, we need to use a cache that is at least big enough to keep an entire working set for an image in the cache. To avoid cold start misses, the cache will prefetch data from memory over a dedicated 8 word bus.

Since our application creates 3 octaves with 3 levels per octave per image, the total amount of memory used by one image will be $32 \times 512 \times 512$ or 64 MB. This stems from the fact that we convolve an image across the rows, store that result, and then convolve the output of the row wise computation and store its output in the original image. This saves us a 512×512 chunk of memory per convolution.

Storing the convolution set of a single image in the cache is not enough because we want to keep the CM unit busy convolving images that are coming from the camera. Since a single image working set takes up so many resources, we can only store a few working sets in cache. Without simulation, it is impossible to figure out the optimal number. We choose to store only four working sets, making the total size of the cache 512 MB. This will enable us to do convolutions and other computations on one image while we prefetch the next images to be convolved.

Possibly add a pretty picture of cache here

For the convolution results to be usable by the rest of the algorithm, the convolution cache has to be accessible by the regular CPU. To simplify the design, the convolution data's virtual addresses will be fixed. When the application code needs to access the convolution data to do calculations, a normal memory access will occur through a load instruction. Our convolution cache will be connected to the same bus as the level 1 cache and will service the load instructions that use the special virtual address range reserved for convolution data. This necessitates that our cache can handle two read requests in the same cycle and that supporting this does not affect hit time. We assume that the level 1 cache can ignore requests for this special address range and that this does not affect hit time on the level 1 cache.

4.2.2 Performance

With this cache organization, we expect the following performance. Due to prefetching and large capacity, we will have a hit rate from the CM close to 100%. We assume that our system would be turned on once and expected to operate indefinitely, so initially the miss rate would be really high but quickly converge as the system operates. The hit rate from the CPU should also be close to 100% for the same reasons. Thus, a single convolution can be performed in $(3 \times 512) \times 2$ CPU cycles. (Load + execute + store) Since a

single image requires 16 convolutions, the total number of cycles to process an image would be 49152. Since our interface to main memory is 8 words wide, it will take $64 \times 512 = 32768$ cycles to prefetch the next image to be convolved. This is less than the time it takes to convolve an image. We assume that while one image is being convolved and another is being fetched from memory, the application can work on the intermediate results and that there is never a stall in the Convolution Module. This is why we chose to store four working sets in the cache instead of just one or two.

5 Conclusion

Overall this design should provide a significant improvement in image throughput for a security system. This leaves the majority of the general purpose processing in the system available for more advanced functions, such as facial and object recognition. This design achieves the goals we set out to attain in this project.