Week of 3/23/20 (CP1)

Ricky Machado:

For this week, I did a large chunk of the datapath and control for the cpu. This was different compared to the last checkpoint as I included four monolithic registers to hold all the necessary data in between states. This was pretty difficult as I had to make all of these modules from scratch. Luckily, we had a pretty detailed datapath beforehand so making the actual cpu datapath wasn't too difficult. The control however took me a while to figure out since it required a wildy more complicated fsm, but I ended up using 5 fsms for each stage and an overarching fsm to tell the pipeline when every stage is done.

Robbie Ernst: For this week, I expanded off of the datapath and control Ricky wrote. Mostly just connecting to the magic memory, and running the control signals through the pipeline. I instantiated the design in the testbench, and connected all of the signals. I figured out the magic memory ports and hooked them up in the design. I then worked together with Ricky to debug the design after we believed we had it all together. I then defined a halt condition, as we ran into our design timing out. For next week, I plan on helping write the code for the L1 caches and the arbiter. As well as, working on getting the testbench working with the shadow memory.

Filip Cakulev: For this week, i spent time researching and designing split L1 caches and hooked up to arbiters talking to L2 caches. I was not able to connect to fastx because nj suk so my partners had to frontload the coding but it seems to be fine now so i don't think it'll be a problem. For next week, I plan on flushing the cache design bugs and helping my partners understand it as I had the most luck with cache on mp2. Since the design is pretty sound and detailed for the majority of the design I will focus on hooking up the arbiter to physical memory or possibly even try to implement L2 Cache