Design of a 4-Bit Up-Counter

FSM in VHDL – Nexys 4 DDR Implementation

Tanner Roberson

Project Requirements

- 4-bit up-counter with synchronous active-low reset
- Count through sequence: 0 → n^0 → (n+1) → (2n^2+2) → (3n^3+3) → …
- Behavioral VHDL modeling in AMD Vivado
- No adders or multipliers used
- Test with VHDL test bench and waveform verification
- FPGA Implementation on Nexys 4 DDR:
  SW0: Clock
  SW2–SW1: Input n (2 bits)
  CPU Reset: Reset
  LD3–LD0: Output

Learning Objectives

- Develop a finite state machine (FSM) using VHDL
- Create a state diagram
- Create an excitation table

General Approach

1. Write case statements for each n value (1, 2, 3)
2. Implement state transitions with if statements
3. Add synchronous active-low reset
4. Develop test bench for all states and inputs
5. Verify with captured waveforms
6. Implement design on FPGA

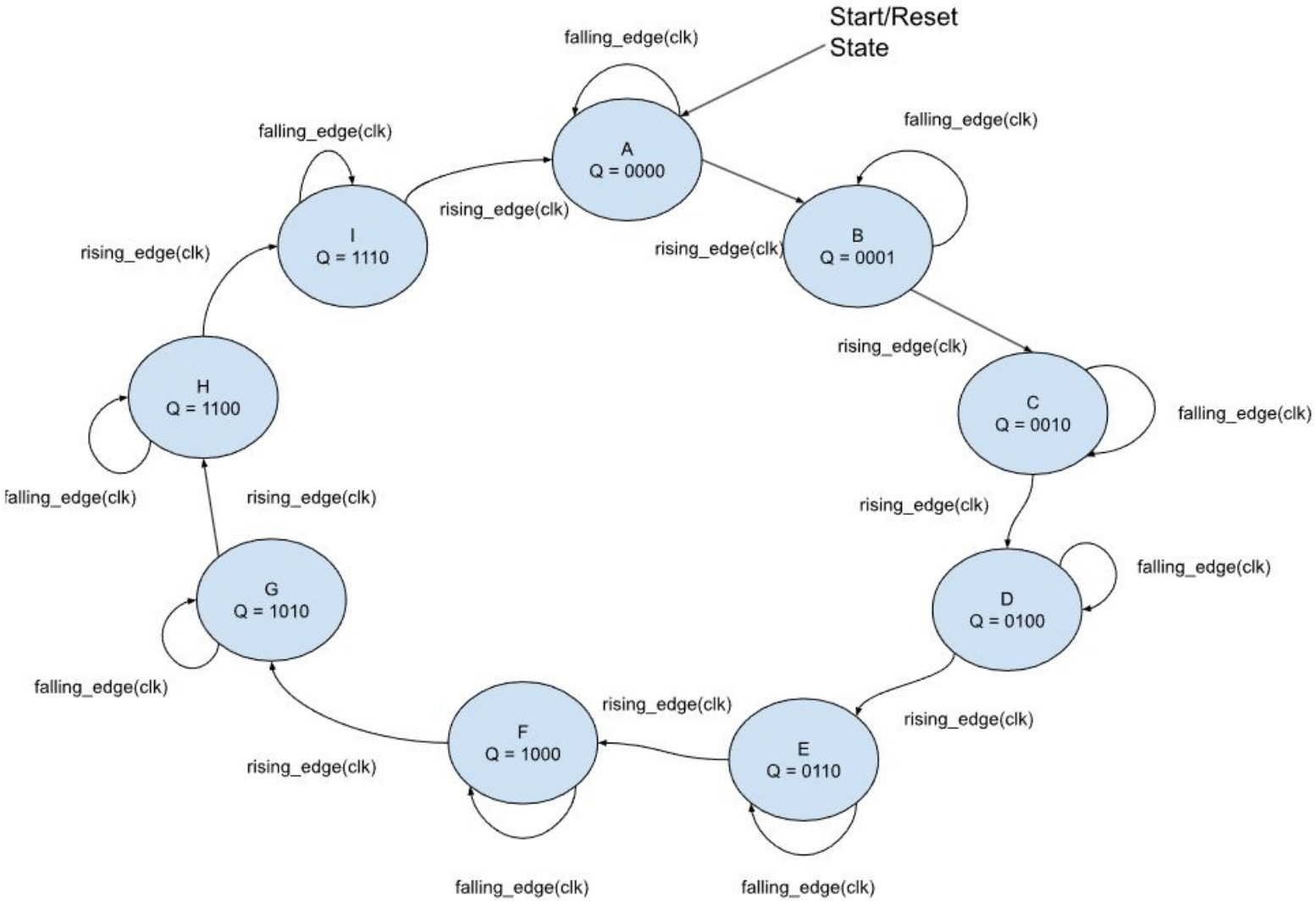
FSM Design Details

- Case statement for each n value
- State transitions based on n and clock input
- Synchronous reset to 0000
- Test bench demonstrates valid sequences and reset

Example State Table (n=01)

	n = 01	
Current State (q3q2q1q0)	Clock Input	Next State (Q3Q2Q1Q0)
0000	1 0	0001 0000
0001	1 0	0010 0000
0010	1 0	0100 0000
0100	1 0	0110 0000
0110	1 0	1000 0000
1000	1 0	1010 0000
1010	1 0	1100 0000
1100	1 0	1110 0000
1110	1 0	0000 0000

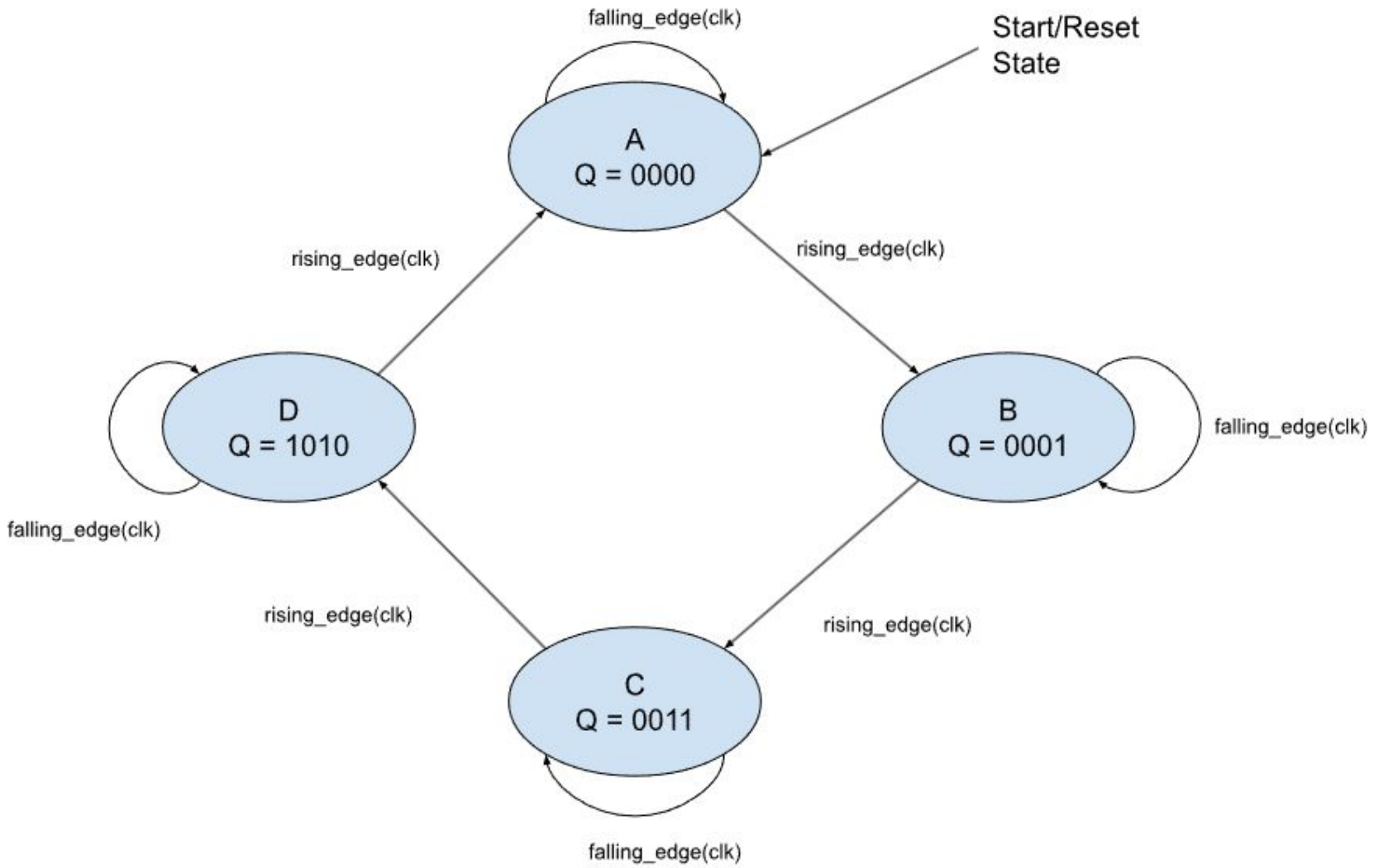
Example State Diagram(n=01)



Example State Table (n=10)

	n = 10	
Current State (q3q2q1q0)	Clock Input	Next State (Q3Q2Q1Q0)
0000	1 0	0001 0000
0001	1 0	0011 0000
0011	1 0	1010 0000
1010	1 0	0000 0000

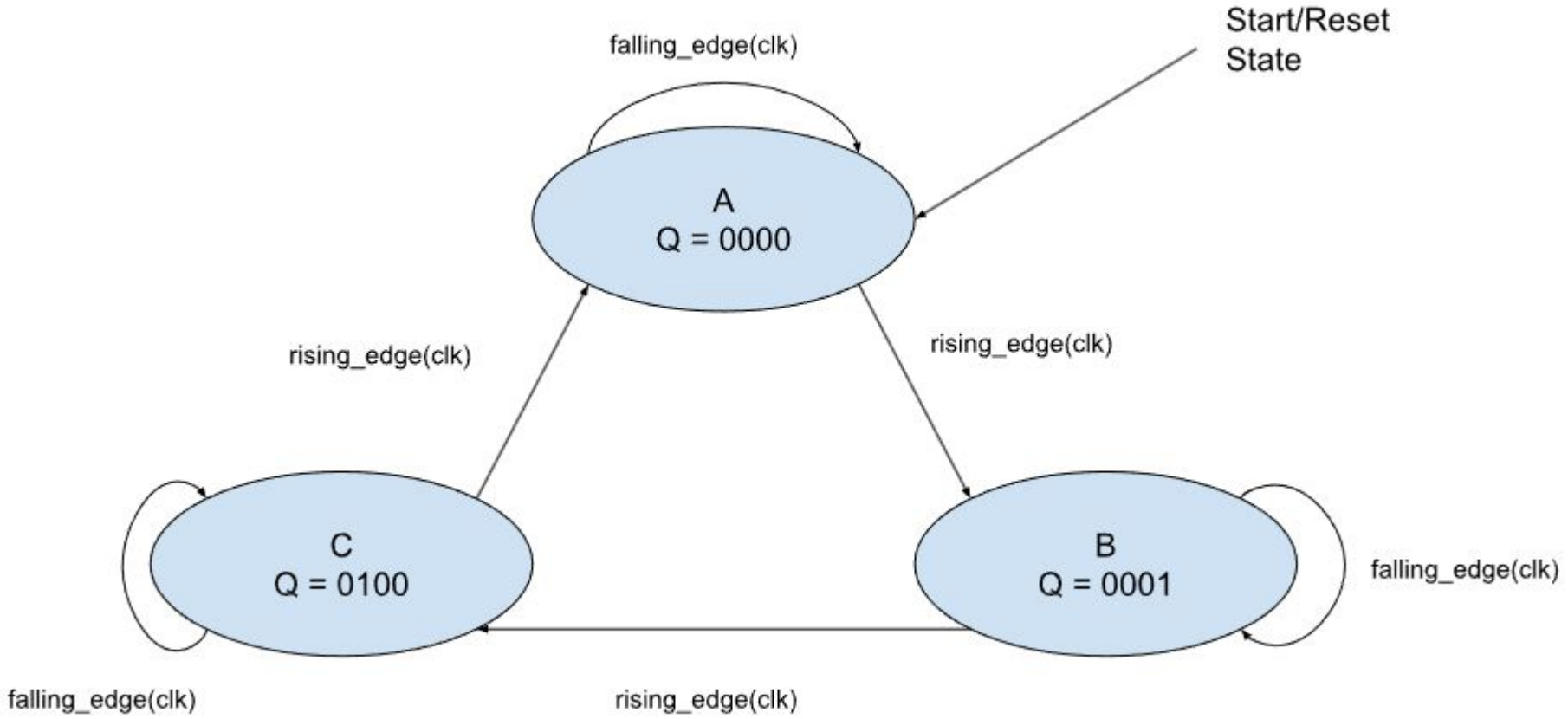
Example State Diagram (n=10)



Example State Table (n=11)

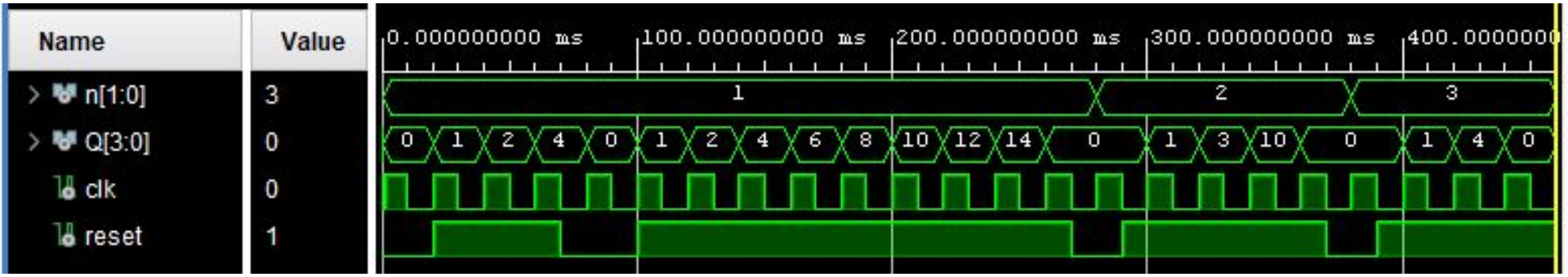
	n = 11	
Current State (q3q2q1q0)	Clock Input	Next State (Q3Q2Q1Q0)
0000	1 0	0001 0000
0001	1 0	0100 0000
0100	1 0	0000 0000

Example State Diagram (n=11)



Simulation Results

- Verified for n=01, n=10, n=11
- Outputs followed specified sequence
- Reset returned counter to 0000



FPGA Implementation

- Nexys 4 DDR connections:
- SW0: Clock
- SW2–SW1: Input n
- CPU Reset: Reset
- LD3–LD0: Output

Observations & Challenges

- Clock must be managed carefully in test bench
- Reset must be synchronized with clock
- Behavioral modeling ensured flexibility

Summary & Takeaways

- Designed 4-bit up-counter FSM in VHDL
- Verified functionality with simulation waveforms
- Implemented successfully on Nexys 4 DDR FPGA
- Learned FSM design, excitation tables, and reset handling