UNIVERSITY OF TORONTO
FACULTY OF APPLIED SCIENCE AND ENGINEERING

ECE253F – Digital and Computer Systems
Midterm Examination

October 26, 2017 9:30am - 11:00am
Duration: 90 minutes

Examiner: J. Anderson

Exam Type D: Examiner specified aids: One single sheet of letter size paper (8.5 x 11 inch), both sides may be used.

Calculator Type 4: No calculators or other electronic devices are allowed.

All questions are to be answered on the examination paper. There is one extra page at the end and you may use the back of a page. If you use more than the given space, please direct the marker to the appropriate page and indicate clearly on that page which question(s) you are answering there. It is your responsibility to make sure the marker can find your solution.

The number of marks for each question are indicated.

The examination has **18 pages**, including this one.

Last Name: _____ First Name: _____

Student Number: _____ UTORID: _____

Lab day (circle one): Tuesday Thursday

MARKS

1	2	3	4	5	6	7	8	9	10	Total
/6	/6	/8	/10	/6	/6	/6	/6	/10	/6	/70

Question 1 [6 Marks]

Assuming that all numbers given below are unsigned integers, fill in the following table with the appropriate number conversions:

11-bit binary	decimal	hexadecimal
11001001010		
	1020	
		7F7

Question 2 [6 Marks]

In Lab 1, you used the 7400-series chips to build logic circuits. Consider the following 7400-series chip and associated connectivity.

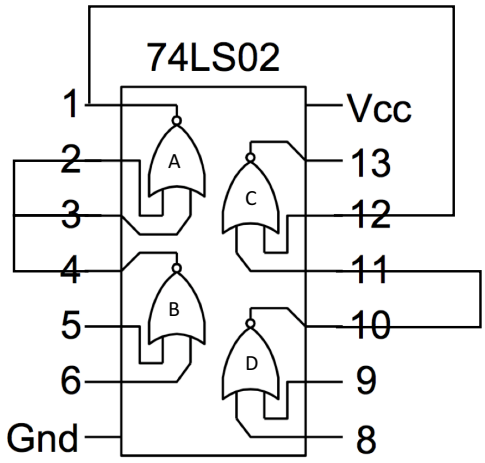


Fig 1. Chip schematic

Inputs applied				Observed outputs			
PIN # 5	6	8	9	1	4	10	13
0	0	0	0	1	1	1	0
0	0	0	1	1	1	0	0
0	0	1	0	1	1	0	0
0	0	1	1	1	1	0	0
0	1	0	0	0	0	1	0
0	1	0	1	0	0	0	1
0	1	1	0	0	0	0	1
0	1	1	1	0	0	0	1
1	0	0	0	0	0	1	0
1	0	0	1	0	0	0	1
1	0	1	0	0	0	0	1
1	0	1	1	0	0	0	1
1	1	0	0	0	0	1	0
1	1	0	1	0	0	0	1
1	1	1	0	0	0	0	1
1	1	1	1	0	0	0	1

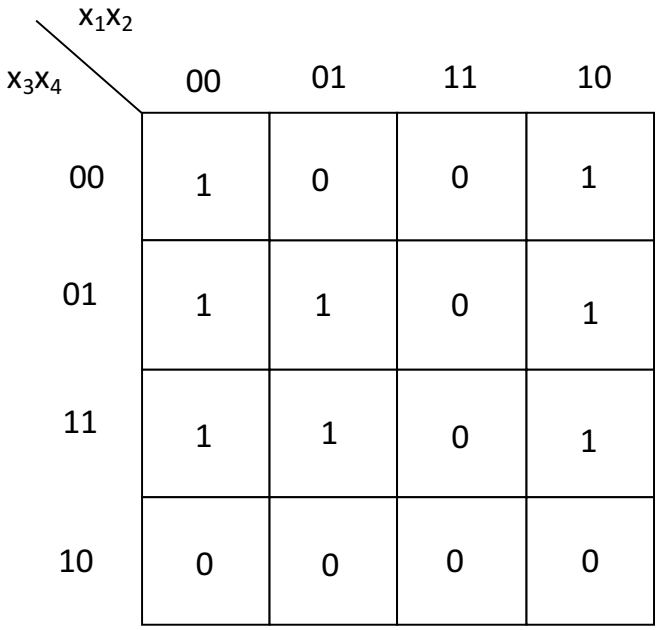
Fig 2. Test inputs and outputs with defective gate(s)

a) [4 marks] Using the schematic in Figure 1, derive the intended circuit and show the logic function in sum-of-products (SOP) form. For logic signal names, use the pin number; for example, signal x_5 is attached to pin 5. Your function should express x_{13} as a function of x_5, x_6, x_8, x_9. You do not need to minimize the function.

b) [2 marks] Figure 2 shows applied inputs and observed outputs on pins of the chip. There is a problem with the chip – it is defective. Determine which gate(s) A, B, C, D are not working properly and state why.

Question 3 [8 Marks]

Consider the following Karnaugh map for a 4-input logic function f:



a) [3 marks] Write the function f in a minimized sum-of-products (SOP) form:

b) [3 marks] List the prime implicants of the function f:

c) [2 marks] List the essential prime implicants of the function f:

Question 4 [10 Marks]

a) [4 marks] Use Boolean algebra to minimize the following function into sum-of-products (SOP) form: $f = (x + \overline{y} + z)(\overline{x} + y + \overline{z})$. Show your work for full marks.

b) [1 mark] Report the $cost$ of the minimum SOP form, where cost is defined to the number of gates plus the number of gate inputs. You may assume that variables are freely available in true/complemented form (i.e. inversion incurs no cost).

Question 4 continued ...

c) [5 marks] Use Boolean algebra to prove the following equality: $\overline{x_1}x_2 + x_1x_3 + x_1x_4 = \overline{x_1}x_2\overline{x_3}\,\overline{x_4} + x_1(\overline{\overline{x_3}\,\overline{x_4}}) + x_1\overline{x_2}\,\overline{x_3}x_4 + x_1\overline{x_2}x_3\overline{x_4} + \overline{x_1}x_2\overline{x_3}x_4 + \overline{x_1}x_2x_3\overline{x_4} + \overline{x_1}x_2x_3x_4 + x_1\overline{x_2}\,\overline{x_3}x_4$

Question 5 [6 Marks]

You are to design a 4-bit *pop-count* circuit. The circuit has 4 inputs, X_3, X_2, X_1, X_0 and three outputs Z_2, Z_1, Z_0. The circuit counts the number of inputs that are logic-1, and outputs this count, in binary. For example, if the input were $X_3X_2X_1X_0 = 0110$, then the output, $Z_2Z_1Z_0 = 010$, since two of the input bits are logic-1.

a) [3 marks] Write the truth table for the pop-count circuit.

Question 5 continued ...

b) [3 marks] Show an implementation of the circuit using a single full adder (FA) and additional logic gates. Draw the circuit schematic. The full adder (FA) can be shown as a block with three inputs (x, y, c_{in}) and two outputs (s, c_{out}), as depicted in the lectures. Ensure you label the FA input and outputs.

Question 6 [6 Marks]

Consider the following circuit described in the Verilog hardware description language (HDL):

```
module foo(D,Q,Qn,resetn,clock);
       input [1:0] D;
       input resetn, clock;
       output reg [1:0] Q;
       output [1:0] Qn;

       assign Qn = ~Q;

       always@(posedge clock, negedge resetn)
       begin
                if (resetn == 1'b0)
                begin
                        Q <= 2'b00;
                end
                else
                begin
                        Q <= D;
                end
       end
endmodule
```

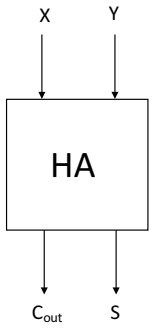
a) [2 marks] Show a circuit schematic for the Verilog specification using D flip-flops.

Question 6 continued ...
b) [4 marks] Simulation is an important part of digital circuit design. Draw waveforms for inputs D, $clock$, and $resetn$ that you would use to simulate and test the circuit. Also, draw the expected output waveforms for Q and Qn given your input stimulus. Be sure your input waveforms test all relevant aspects of the circuit's behaviour.

Question 7 [6 Marks]

A half-adder (HA) is a circuit that adds two binary inputs, X and Y. The HA has two outputs, S and C_{out} representing the sum and carry bit, respectively. The HA truth table and circuit symbol are as follows:

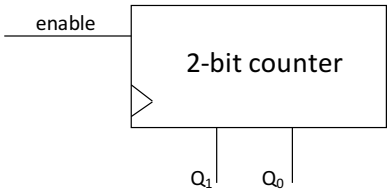
X	Y	Cout	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0



You are to design a two-bit ripple-carry adder using only HAs and a minimum number of additional logic gates. The two-bit ripple-carry adder computes the sum of two 2-bit binary numbers, x_1x_0 and y_1y_0, producing a 3-bit output z_2, z_1, z_0. Draw the circuit schematic. Hint: first think about how to create a full adder (FA) using HAs and additional gates.

Question 8 [6 Marks]

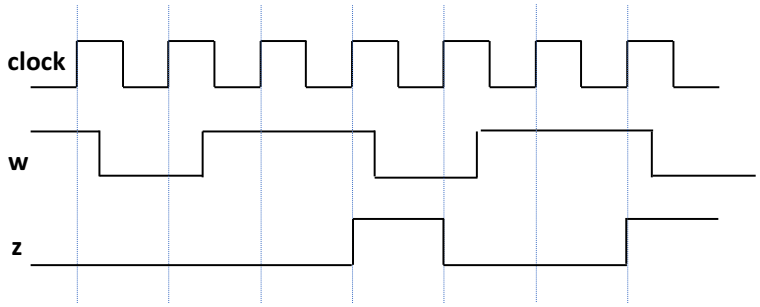
You are to design a circuit with two inputs, $clock$, and S, and one output Z. $clock$ is a 4 Hz periodic input signal. The circuit works as follows: If $S = 0$, output Z should be asserted (logic-1) for every 2^{nd} period of $clock$ (i.e. twice per second), and zero otherwise. If $S = 1$, output Z should be asserted (logic-1) for every 4^{th} period of $clock$ (i.e. once per second), and zero otherwise. You may use any number of 2-bit counters with enable (symbol below). You may use any number of logic gates or multiplexers.



Draw a circuit schematic:

Question 9 [10 Marks]

In this question, you will design a Moore-type FSM sequence recognizer with an input w and an output z. The output z should be 1 when the pattern 1011 appears on input w across four successive clock cycles. Otherwise output z is 0. Overlapping patterns are allowed. Here is an example of the desired behaviour:



a) [4 marks] Draw the state diagram.

b) [6 marks] Using a three-bit state encoding, derive the logic equations for the next-state logic and output logic (for z). Use Karnaugh maps to minimize the logic functions. Following the convention in the textbook, use y_2, y_1, y_0 as signal names to represent the current state; use Y_2, Y_1, Y_0 as signal names to represent the next state. Show your work (show the state table and state-code assignment).

Question 9 continued . . .

Question 10 [6 Marks]

Design a three-bit counter having outputs Q_2, Q_1, Q_0 and one input s. The counter works as follows: When $s = 0$, the counter counts in increments of 1. When $s = 1$, the counter counts in increments of 3. Your counter must use *exactly* three T flip-flops. You may also use any logic gates and 2-to-1 multiplexers in your design. Draw the circuit schematic.
Counting sequence when $s = 0$:

Q2	Q1	Q0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1
0	0	0
...		

Counting sequence when $s = 1$:

Q2	Q1	Q0
0	0	0
0	1	1
1	1	0
0	0	1
1	0	0
1	1	1
0	1	0
1	0	1
0	0	0
...		

Question 10 continued . . .

Question 11 [1 Marks]

BONUS: Name the type of memory chip used in the fictional Star Trek universe of the 24th century.

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