ANALOGUE ELECTRONICS

D. K. Hamilton

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ABOUT THE COURSE

Background

This course will build on the material covered for Prelims electronics and, more strongly, on the third year "Electronic circuits and instrumentation" course both of which will be useful revision. Familiarity with the material on electronic circuits in the course for Paper B3 will be useful, too.

As we look at each topic to be covered we will very briefly revise the background from these courses and then use it as a foundation for new material.

Topics to be covered

We shall look at the following topics, broadly in this order:-

Background to analogue electronics and electronic design
Basic bipolar and field effect transistor circuits - building blocks for integrated circuits
High frequency behaviour of transistors
Operational amplifiers - characteristics and limitations
Anatomy of an actual operational amplifier
Gain, frequency response and stability
Current feedback amplifiers
Noise - both irreducible circuit noise and interference
Bootstrapping

LEARNING OUTCOMES

What you should know:

1. The characteristics of bipolar and field effect transistors.
2. Small signal equivalent circuits for bipolar and field effect transistors.
3. Common transistor circuit configurations.
4. The effects of internal capacitances on the high frequency behaviour of transistors.
5. High frequency equivalent circuits for transistors.
6. The use of ideal operational amplifiers in standard circuit configurations.
7. The limitations of actual (ie non-ideal) operational amplifiers.
8. How to analyse the internal circuit of an actual operational amplifier.
9. The relationship between open- and closed-loop gain, frequency response and stability of an operational amplifier.
10. The circuit topology of current-feedback operational amplifiers.
11. The reasons why current feedback amplifiers have a fundamentally wider bandwidth which is only weakly dependent on closed-loop gain.
12. The origin of the different types of noise in electronic circuits.
13. The noise models for bipolar and field effect transistors.
14. The noise model for an operational amplifier.
15. Noise figure as a measure of the performance of an amplifier.
16. Analysis of noise in a frequency-dependent circuit.
17. The technique of bootstrapping used to increase gain to raise input impedance.
18. Bootstrapping used to cancel capacitance.

What you should be able to do:

1. Model and analyse transistor amplifier circuits, recognising basic configurations such as differential pairs, Darlington pairs, complementary emitter followers, and current mirrors.

2. Design transistor amplifiers using the basic configurations as building blocks.
3. Understand how to overcome the effects of transistor capacitances in designing wide bandwidth amplifiers.
4. Use operational amplifiers in standard configurations, assuming ideal behaviour.
5. Understand the effects on these circuits of the various aspects of non-ideal behaviour of operational amplifiers.
6. Design circuits to avoid the effects of operational amplifier imperfections.
7. Appreciate the internal circuitry of an operational amplifier in terms of the basic transistor circuit configurations.
8. Calculate the principal parameters of an operational amplifier from the internal circuit.
9. Understand and use the detailed data sheet for an operational amplifier.
10. Analyse the stability of a given operational amplifier circuit using frequency response plots.
11. Be able to suggest ways to improve the stability of a particular operational amplifier feedback configuration.
12. Appreciate the differences in circuit topology between current feedback and conventional operational amplifiers.
13. Be able to explain the independence of closed-loop bandwidth and closed loop gain with a current feedback amplifier.
14. Design wide bandwidth amplifiers using current feedback amplifiers.
15. Derive the noise model of a bipolar transistor.
16. Analyse the noise performance of transistor and operational amplifier circuits.
17. Design an amplifier optimised for low noise with a given source impedance.
18. Use bootstrapping to raise the input impedance of an amplifier.
19. Use bootstrapping to cancel lead capacitance of a transducer or sensor.

REFERENCES

Horowitz, P. and Hill, W, "The Art of Electronics", 2nd edition, Cambridge 1994

(Probably the best book on the subject, and very practically orientated - certainly it is readable!)

Linsley Hood, J., "The Art of Linear Electronics", Butterworth Heinemann, 1993

(Also quite practical. Chapter 1 has a comprehensive list of circuit symbols, and chapter 2 is an excellent survey of components.)

Franco, S., "Design with Operational Amplifiers and Analog Integrated Circuits", 3rd edition, McGraw Hill, 2002

Clayton, G. B. and Newby, B. W. G., "Operational Amplifiers", 3rd. edition, Newnes, 1992.

Clayton, G. B., "Linear Integrated Circuit Applications", Macmillan, 1975.

"Electronics World" (monthly magazine)

Manufacturers' information and suppliers' catalogues

Manufacturers' data books, data sheets and application information provide much information about how a particular device is intended to be used. In the case of integrated circuits, the full internal circuit is often given (it can be quite a challenge to fathom out just how an i.c. *does* work), as well as a number of suggested applications. Together these can give much insight into the possibilities and limitations of the chip. Later on we will look in detail at the full manufacturer' s data for a particular operational amplifier, to see what information is there.

ANALOGUE ELECTRONICS

It is not correct (despite appearances!) to think that all electronics has become digital. Obviously, an increasing amount of signal processing is done by computer techniques these days, but the fact remains that quantities which need to be either detected or measured in the real world are continuous and not fundamentally digital in nature. Sensors and transducers usually give an output in analogue form which needs some form of processing before being digitized.

Examples might be:-

optical detectors (photodiodes, photoconductors),
pressure sensors (including microphones),
radio frequency receivers (signal from an aerial),
position sensors.
tape heads
temperature sensors
strain gauges

In all these cases, the transducer output will pass into an amplifier and the sensitivity, or resolution, of the measuring system will depend on the smallest signal which can be detected. This is directly dependent on the amount of electrical noise added by the amplifier. The speed of the system will depend on the bandwidth of the amplifier. Therefore we need to be able to understand how to design amplifiers to optimise these parameters for a particular transducer. Optical detectors are used for digital signals in fibre optic communications, with bit rates well over 1 GB/s; designing low-noise receiver amplifiers for such speeds is really an analogue problem.

AIMS OF ELECTRONIC DESIGN

A design will be required to carry out certain specified functions, and it is the job of the electronic designer to fulfil these requirements within certain guidelines. For example:-

1. Minimum cost.
2. Adequate performance, i.e. within the specification, but not exceeding it unnecessarily.
3. Good reliability and thermal stability.
4. Minimum number of power supplies.
5. Low power dissipation.
6. Minimum size and weight.
7 Minimum setting up needed - preset adjustments take people and time (and hence money).
8. Serviceability - easy to repair if it does go wrong.

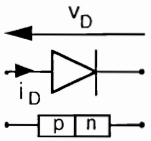
Obviously, these requirements are interdependent with trade-offs between them. For example cost depends on complexity and thermal stability is enhanced if the power dissipation is minimized. On the other hand, the need for minimal setting up may lead to slightly more complexity, but the cost of extra components would almost certainly be less than the saving in people and time.

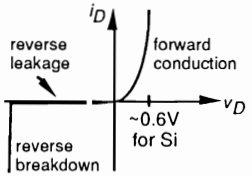
Usually, a system will be split into a number of sub-systems, each one being designed separately (as we did with the systems in the electronic engineering coursework module).

ACTIVE DEVICES

SEMICONDUCTOR DIODES

Semiconductor diodes used in electronic circuits are usually silicon p-n junctions. Germanium diodes are available, too, but are used only when their lower forward voltage (0.2 - 0.3V rather than 0.6 - 0.7V for silicon) is an advantage.





Signal diodes

Signal diodes are small diodes intended for low current (< 100mA or so) applications. The behaviour of such diodes follows quite well the diode equation:-

$$i_D = i_0\left(\exp\left(\frac{ev_D}{kT}\right) - 1\right)$$ which at room temperature (~20°C) can be written

$$i_D = i_0\left(\exp\left(\frac{v_D}{25mV}\right) - 1\right)$$ or, for $v_D >> 25mV$, $i_D \approx i_0 \exp\left(\frac{v_D}{25mV}\right)$

The approximation makes calculations much easier with insignificant loss in accuracy.

For calculating d.c. conditions in circuits, it is often sufficient to take the voltage across a diode to be constant at 0.6 - 0.7V for silicon, and 0.2 - 0.3V for germanium.

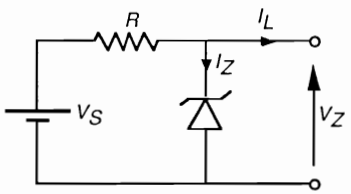
Rectifier diodes

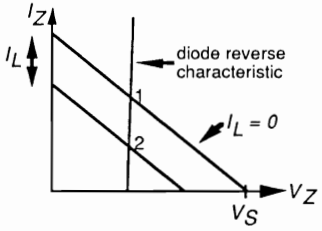
This includes high current (>100mA) diodes intended for use in power supplies, where they would be producing d.c. at currents up to hundreds of amps. At high currents such a diode (although still a p-n junction) appears not to follow the diode equation mainly due to the resistance of the bulk semiconductor on each side of the junction.

A useful rule of thumb for design is to take the forward voltage as between 1V and 1.5V for currents up to a few tens of amps. Manufacturers often specify this voltage for various currents.

Zener (voltage reference) diodes

Zener diodes exploit the reverse breakdown of the p-n junction, and are doped to make breakdown occur at a certain voltage. They are available in an E24 series of voltages from 2.4V up to 75V in several power ratings. The series resistor is chosen to set the current through the diode, I_Z which should usually be similar in magnitude to the current being supplied to the load I_L.



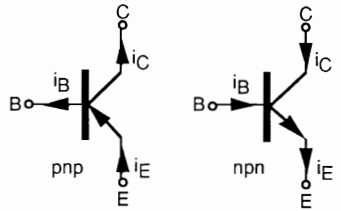


$V_Z = V_S - (I_Z + I_L)R$

For $I_L = 0$, this gives the upper load line, and the diode operates at point 1.

As I_L increases, the load line moves down to an operating point such as 2, with smaller diode current. V_z is then slightly smaller because the diode characteristic is not perfectly vertical.

BIPOLAR TRANSISTORS



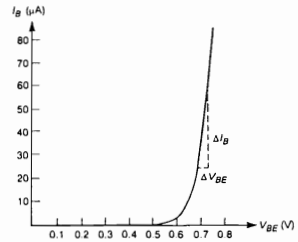
$i_E = i_B + i_C$

$i_C = \beta\, i_B$

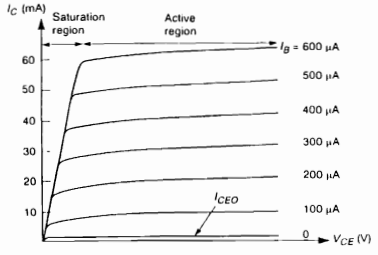
$i_C = \alpha\, i_E = \frac{\beta}{1+\beta}\, i_E$

Usually, $\beta >> 1$ ($\approx$100), so $\alpha \approx 1$

If we specify just two of the terminal currents, and two of the voltages between the terminals, the third current and the third voltage are defined. (This must be true, by Kirchoff's laws, for any three terminal device). The exact relation between the transistor terminal voltages and currents can be presented in the form of curves:-



Input characteristic of a bipolar transistor in the common-emitter configuration.

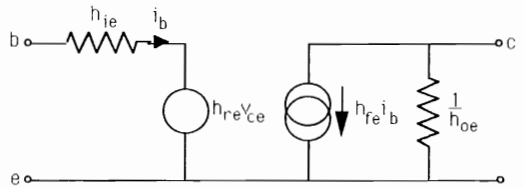


Common-emitter output characteristic.

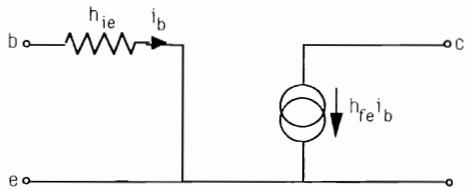
Base-emitter voltage and base current are related by the Ebers-Moll equation,

$$i_B = i_0\left(\exp\frac{ev_{BE}}{kT} - 1\right) \approx i_0 \exp\frac{v_{BE}}{25mV}$$ at room temperature.

For small signals at not-too-high frequencies, the h-parameter (h for hybrid) incremental model is used:-



The parameters h_{re} (nearly always) and h_{oe} (almost nearly always) are negligibly small, which means that the incremental equivalent circuit simplifies to:-



$h_{fe} = \frac{i_c}{i_b} = \frac{\partial i_C}{\partial i_B}$

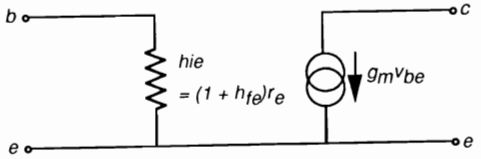
$h_{ie} = \frac{v_{be}}{i_b} = \frac{\partial v_{BE}}{\partial i_B}$

Using the the simplified Ebers-Moll equation, $h_{ie} = \frac{25mV}{I_B}$.

It is possible to express i_c in terms of v_{be}, via the mutual conductance, g_m. The current generator is now $g_m v_{be}$ rather than $h_{fe} i_b$.

$$g_m = \frac{i_c}{v_{be}} = \frac{\partial i_C}{\partial v_{BE}} = \frac{\partial i_C}{\partial i_B} \cdot \frac{\partial i_B}{\partial v_{BE}} = \frac{h_{fe}}{h_{ie}} = \frac{\mathbf{I_C}}{\mathbf{25mV}}$$

This leads to the following equivalent circuit, which can be useful when a stage is voltage driven. The circuit is beginning to resemble the "hybrid π" model, which is used at high frequencies. Here h_{ie} is expressed in terms of r_e, the output resistance at the emitter terminal.



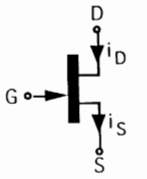
$$r_e = h_{ie}/(1 + h_{fe}) = \frac{\mathbf{25mV}}{\mathbf{I_E}}$$

So, as $I_E \approx I_C$, $\mathbf{r_e \approx \frac{1}{g_m}}$.

Both g_m and r_e depend on collector current, g_m being proportional to it, and r_e inversely proportional. At 1mA collector current, g_m is 40mS (mA/V) and r_e is 25Ω. Knowing these, it is obviously easy to get the values at any other current.

The only difference between **npn and pnp transistors** is the direction the d.c. flows. V_{BE} is about +0.65V in a npn and about -0.65V in a pnp transistor. The incremental models are exactly the same.

FIELD EFFECT TRANSISTORS

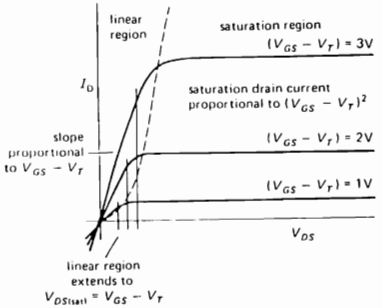


In the saturation region, FETs obey a square law,

$i_D = I_{DSS}\left(1 - \frac{v_{GS}}{V_p}\right)^2$ V_p is the pinch-off voltage (< 0).

$i_D = i_S$ as i_G is usually negligibly small (≈ 1pA or less)

Capacitance from G to S and from G to D will cause i_G to increase at high frequencies.



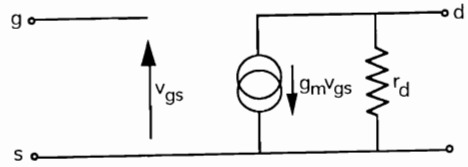
In the linear region,

$$i_D = \frac{2I_{DSS}}{V_P^{\,2}}\left[(v_{GS} - V_P)v_{DS} - \frac{v_{DS}^{\,2}}{2}\right]$$

The diagram on the left shows typical FET characteristics - here the pinch-off voltage is denoted by V_T.

As amplifiers, FETs are normally biassed in the saturation region. An incremental model can be derived:-

Incremental model for the junction f.e.t.



$$g_m = \frac{i_d}{v_{gs}} = \frac{\partial i_D}{\partial v_{GS}}$$

$$= -2\frac{I_{DSS}}{V_p}\left(1 - \frac{v_{GS}}{V_p}\right) \quad (V_p < 0)$$

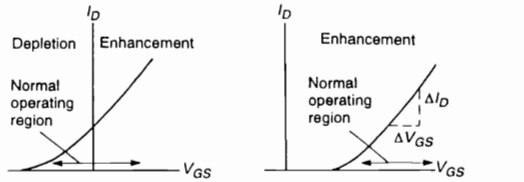
$$r_d = \frac{v_{ds}}{i_d} = \frac{\partial v_{DS}}{i_D}$$ - usually big.

MOSFETS

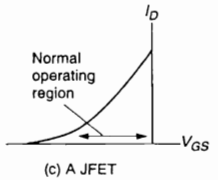
MOSFETS (Metal Oxide Field Effect Transistors) are similar to JFETS in that the current flowing through the channel is controlled by the electric field set up by the gate electrode. In a MOSFET, the gate is insulated from the channel by a thin layer of insulator (SiO_2) rather than a reverse-biassed p-n junction as in a JFET.

MOSFETS can be depletion mode or enhancement mode, or somewhere in between. For n-channel devices, where drain is positive with respect to source (similar to an npn transistor), in an depletion mode device I_D is almost maximum when V_{GS} is zero and decreases as V goes negative. An enhancement mode device has I_D zero for V_{GS} zero, and increasing as V_{GS} increases past the turn-on voltage.

The following curves compare FET characteristics.



(a) An *n*-channel DE MOSFET (b) An *n*-channel enhancement MOSFET



(c) A JFET

Transfer characteristics of *n*-channel FETs.

FETs as switches

Most electronic switches are based on field effect transistors, which have the advantage that they can be designed to have a low 'on' resistance (channel fully conducting) and a very high 'off' resistance (channel depleted).

Single JFETS or MOSFETS can be used as simple switches, the switch terminals being the source and drain, and the control voltage being applied to the gate. The gate-source voltage is what controls the transistor, and will clearly depend on the signal voltage on the source. So the voltage range needed on the gate to control the switching action will be affected by the signal. For simple applications, this problem can often be overcome, but for a generally useful switch, is a serious drawback.

Analogue switch i.c.s solve the problem by having a complex combination of many MOSFETS to make switches which can cope with a wide range of signal voltages, usually extending from one power supply rail to the other, and which have a well defined switching threshold independent of signal voltage. Such devices are the DG500 series.

SINGLE STAGE AMPLIFIERS

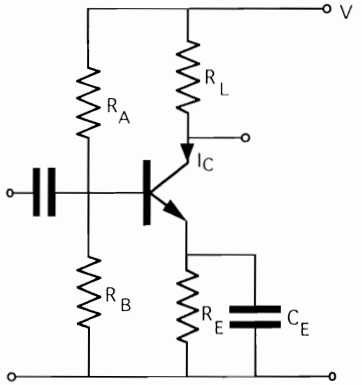
BIASSING

You will remember that because transistors are non-linear devices, passing current only in one direction, they need to be biassed to a suitable operating point (standing values of I_C or I_D) in order to form amplifiers for small a.c. signals. The small signals then add to these currents, varying them to either side of their quiescent values.

We need to design bias circuits which will set the collector current (for bipolars) or drain current (for F.E.T.s) to a well-defined value, which is independent of transistor parameters which vary widely between different samples of the same transistor type. For example the d.c. current gain, β, for a typical small-signal transistor might be specified in the manufacturer's data to be anywhere in the range 50-200 (type BC182L). The pinch-off voltage for a F.E.T., which is a key parameter in the relationship between I_D and V_G, similarly might vary between -1V and -4V (type 2N5434). Clearly, if we want to be able to mass produce circuits, we need to be able to use transistors with parameters anywhere in these ranges and be confident that the circuit will work correctly.

Bipolar transistors

A single stage amplifier is usually biassed using the three resistors, R_A, R_B, and R_E :-



Let $\alpha = \dfrac{R_B}{R_A + R_B}$, $R_S = \dfrac{R_A R_B}{R_A + R_B}$

$$\alpha V - R_S \frac{I_C}{\beta} = V_{BE} + I_C R_E$$

So $I_C = \dfrac{\alpha V - V_{BE}}{R_E + \dfrac{R_S}{\beta}} \approx \dfrac{\alpha V - V_{BE}}{R_E}$ if $\beta R_E >> R_S$

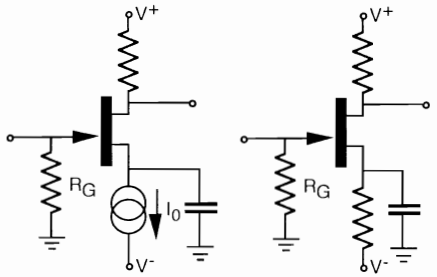
which sets the operating point independently of β.

Remember the low frequency break points which are due to C_E.

A similar circuit can be used with a fet to give I_D substantially independent of I_{DSS} and V_P.

Using a current source

Another way of setting the quiescent current in an amplifier stage is to use a current source. For example, the left-hand diagram shows how a f.e.t. stage might be biassed.



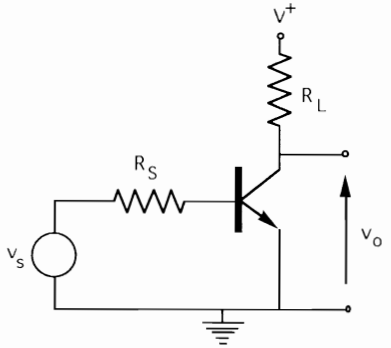
Here the current source sets the drain current at I_0 and as the gate is returned to 0 volts through R_G, the source becomes negative to set V_{GS} to the appropriate value for this drain current. The capacitor is necessary to ground the source to a.c.

V might typically be –15 or so volts, which is significantly larger than V_{GS} (which would be a volt or two). In this case, a resistor could be used as an approximation to a current source as in the right-hand diagram – the voltage across the resistor is dominated by V.

TRANSISTOR AMPLIFIER CIRCUITS

You should seen many of these circuits before, in more or less detail, but we will quickly summarize them all for completeness and look at some aspects in more depth than before. For clarity and simplicity, they will usually be shown without the biassing components.

1a) Common emitter



Typical values might be I_C = 1 mA, h_{fe} = 200, giving h_{ie} = 5kΩ
Say R_L = 10kΩ, R_S = 1kΩ

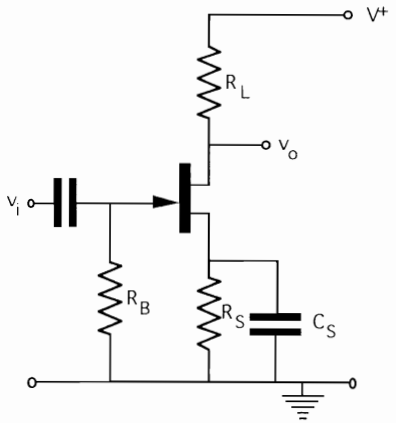
Voltage gain = $-\dfrac{h_{fe}R_L}{R_S + h_{ie}} = -333$

Current gain = h_{fe} = 200

Input resistance = h_{ie}, Output resistance = R_L

As both voltage and current gains are high, this configuration gives the highest power gain compared with common base and common collector.

1b) Common source



Voltage gain = $-g_m R_L$

Input resistance = R_B

Output resistance = R_L

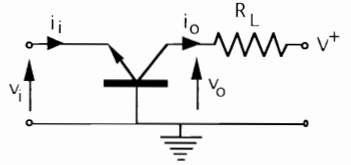
The amplifier has low frequency break points due to C_S at

$$\omega = \frac{1}{C_S R_S} \text{ and } \frac{1}{C_S\left(R_S \,||\, \dfrac{1}{g_m}\right)},$$

and one due to the input capacitor, C_{in} at

$$\omega = \frac{1}{C_{in} R_B}$$

2a) Common base



Current gain = $\alpha \approx 1$, Voltage gain = $-\dfrac{h_{fe}R_L}{h_{ie}}$

(333 with the values above)

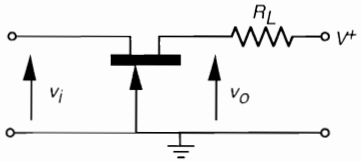
Input resistance = $\dfrac{h_{ie}}{1 + h_{fe}} \approx r_e$, therefore low

(25Ω with the values above)

Output resistance = R_L (5kΩ with values above)

The common-base circuit avoids problems due to the base-collector capacitance of the transistor and is used in high-frequency amplifiers – we shall look at it again later.

2b) Common gate

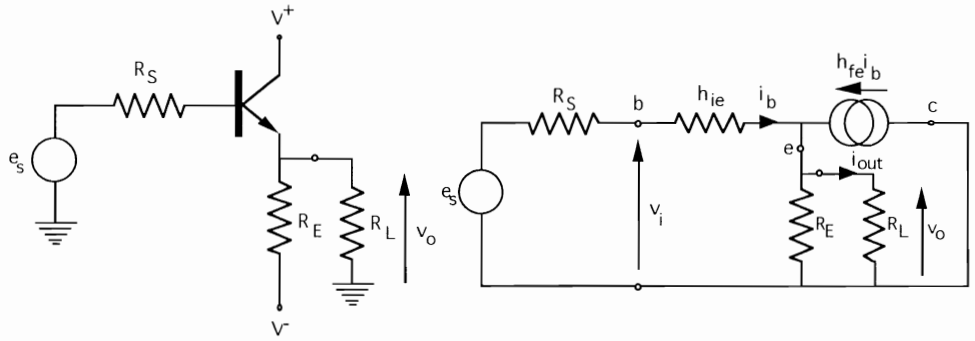


Current gain = 1, voltage gain = $g_m R_L$

Input resistance = $1/g_m$. Output resistance = R_L

The common-gate amplifier has similar topology to the common-base stage, and again avoids problems caused by transistor capacitance – this time the drain-gate capacitance.

3) Common collector (emitter follower)



The equivalent circuit gives

$$v_o = \left(\frac{(1+h_{fe})R_E}{h_{ie}+(1+h_{fe})R_E}\right)v_i - \left(\frac{(R_S+h_{ie})R_E}{(R_S+h_{ie})+R_E(1+h_{fe})}\right) i_{out}$$

where the term in the first large bracket gives the open-circuit gain and the second large bracket is equal to the output impedance. (This is a useful way of calculating gain and output impedance of a circuit at the same time - get the output voltage in terms of input voltage and output current. Otherwise calculate output impedance as the ratio of open-circuit voltage to short-circuit current).

If we divide the top and bottom of the output impedance expression by $(1 + h_{fe})$ it becomes

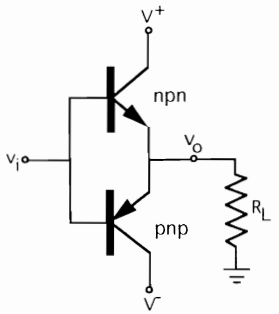
$$R_{out} = \frac{\frac{(R_S+h_{ie})}{(1+h_{fe})}R_E}{\frac{(R_S+h_{ie})}{(1+h_{fe})}+R_E}$$ which is seen to be the parallel combination of R_E and $\frac{R_S+h_{ie}}{1+h_{fe}}$, the output resistance of the transistor, which, if $R_S << h_{ie}$, becomes $\frac{h_{ie}}{(1+h_{fe})}$ or $\frac{1}{g_m}$.

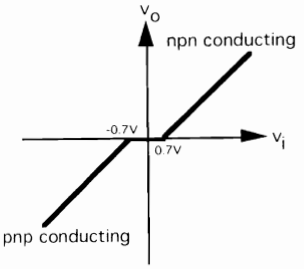
The input resistance $= \frac{v_i}{i_b} = h_{ie} + (h_{fe}+1)(R_E \parallel R_L)$

The emitter follower has a high input impedance and a low output impedance, and is used as a buffer to boost current from a voltage source. Its current gain is $(h_{fe} + 1)$, and its voltage gain approximately unity. If the circuit is directly coupled, there is a d.c. shift of 0.7V from input to output due to V_{BE}.

For large signals the voltage swing is limited. For positive going outputs current is supplied to the load through the transistor but for negative going signals current has to flow to the negative supply via R_E, and voltage drop across R_E due to the current limits the negative-going voltage excursion. The complementary emitter follower gets over this limitation.

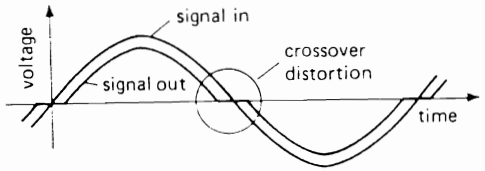
4) The complementary emitter follower

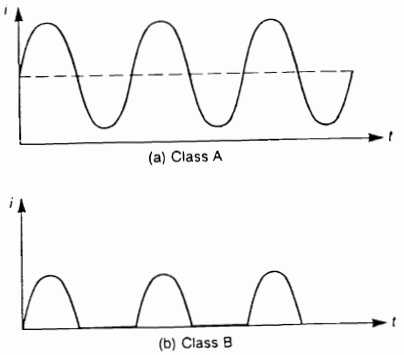




Here two complementary transistors (an npn and a pnp with similar characteristics, usually specified as a 'complementary pair' by the manufacturers) are connected as emitter followers so that the circuit is entirely symmetrical for positive and negative signals. For a positive output, current is supplied to the load via the npn transistor, and for negative-going signals current flows from the load to the negative supply through the pnp transistor. So only one transistor conducts at a time, and for zero input voltage neither conducts. This type of circuit is called 'Class B'.

As the input voltage increases in either direction from zero, the appropriate transistor cannot begin to conduct until v_i reaches 0.7 volts (V_{BE} has to be overcome, and the emitter voltage is zero because R_L goes to the zero volts line). The transfer characteristic therefore has a 'dead band' around zero volts , which gives rise to discontinuities in waveforms as they cross zero. The result is 'crossover distortion'.

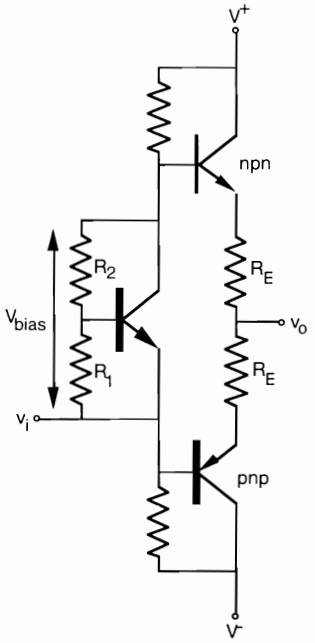




The diagram on the right shows device currents for Classes A and B. In Class A the dotted line is the quiescent current, and the current varies to each side of it. In Class B, the current in one transistor is shown; the other transistor carries the other half cycle.

Crossover distortion can be overcome by applying some bias to the stage in the form of a voltage of around 1.4 volts between the transistor bases, ideally so that both transistors are just on the point of turning on. In practice, the bias is increased a bit beyond this point so that a small quiescent

current flows through both transistors. A common way of doing this is to use a third transistor connected as a 'V_{BE} multiplier' as shown.



The collector-emitter voltage of the extra transistor is given by

$$V_{CE} = \frac{R_1 + R_2}{R_1} V_{BE}$$

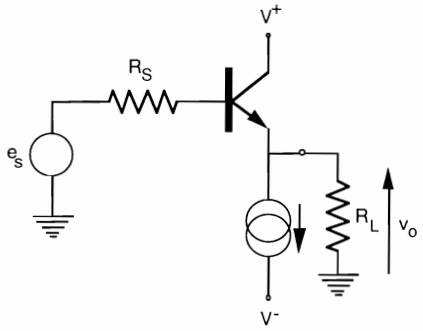
So if $R_1 = R_2$, the voltage between the bases is about 1.4 volts. In practice one of R_1 and R_2 might be made variable so that the quiescent current could be set precisely.

If the bias voltage is not needed to be precise, the bias transistor, R_1 and R_2 could be replaced by two diodes in series to provide about 1.4 volts.

The resistors R_E are included to give more stability to the quiescent current. They provide negative feedback - as the current increases, the voltage across them also increases which tends to reduce the V_{BE}s. To minimize power loss and restriction of voltage swing they should obviously be kept small. Typically they might be from a fraction of an ohm to a few ohms depending on the current the stage is to deliver.

This circuit is widely used in power amplifiers, for example for driving actuators and motors at moderate powers in control systems. It has been used for twenty years or more to form the basis of many audio power amplifiers, with refinements to improve its linearity and minimize crossover distortion. Even a small amount of crossover distortion is audible and can sound unpleasant because it contains high order harmonics.

5) Emitter follower with constant current source

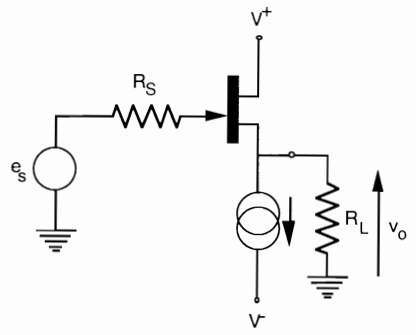


An improvement to the simple emitter follower which allows the circuit to sink current without the output voltage restriction is to replace R_E with a constant current source which, ideally, sinks the same current whatever the voltage across it. With a practical current source, this is true as long as there is a volt or two across it so the load voltage can go almost to the negative rail.

Performance is better than the simple emitter follower, but the circuit is still asymmetrical. The negative current can be no greater than that supplied by the current source (the maximum negative current flows in the load when the transistor is cut off) whereas the positive current, supplied by the transistor, is, in principle, unlimited. When the load current is positive the current in the transistor is the load current plus the current into the current source. However there is no discontinuity as the signal crosses zero volts, and therefore no crossover distortion. This is a 'Class A' circuit.

6 Common drain (source follower)

Here the source follower has a current generator connected to the source but a resistor could be used, as we have just seen for the emitter follower. It is easy to show, using the incremental model, that, with the current generator,



$$\text{open-circuit gain} = 1,$$

$$\text{output resistance} = \frac{1}{g_m},$$

and with resistor R replacing the current generator,

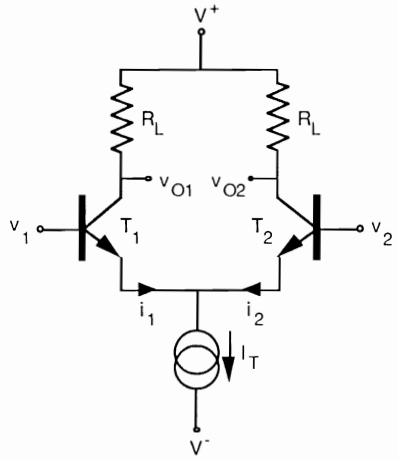
$$\text{open-circuit gain} = \frac{g_m R}{1 + g_m R},$$

$$\text{output resistance} = \frac{1}{g_m} \| R.$$

As g_m of FETs is typically considerably less than g_m in a bipolar transistors (≈ 5mS, compared with a bipolar's 40mS for 1mA collector current), the output resistance of a source follower is generally not as low as that of an emitter follower.

7) Long-tailed pair

The long-tailed pair is a basic differential amplifier and forms the basis of the input stage of virtually every integrated circuit operational amplifier. It can be made with either bipolar or field effect transistors.



We have a differential input voltage $\Delta v = v_1 - v_2$ and $\Delta v = v_{BE1} - v_{BE2}$.

From the Ebers-Moll equation the emitter currents of T_1 and T_2 are, respectively

$$i_1 = I_0 \exp \frac{v_{BE1}}{V_T}, \quad i_2 = I_0 \exp \frac{v_{BE2}}{V_T}$$

where the transistors are assumed to be identical.

Dividing these two currents gives

$$\frac{i_1}{i_2} = \exp \frac{(v_{BE1} - v_{BE2})}{V_T} = \exp \frac{\Delta v}{V_T},$$

and because of the constant current source in the tail

$i_1 + i_2 = I_T$.

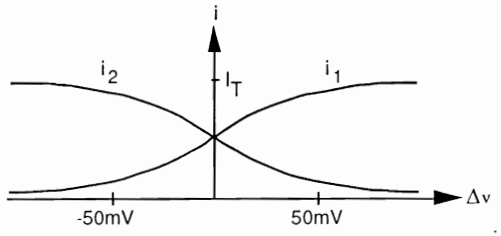
Solving the last two equations for i_1 and i_2 leads to

$$i_1 = \frac{I_T}{1 - \exp \frac{\Delta v}{V_T}} \text{ and } \quad i_2 = \frac{I_T}{1 + \exp \frac{\Delta v}{V_T}}$$

or

$$i_1 = \frac{I_T}{2}\left(1 + \tanh \frac{\Delta v}{2V_T}\right) \text{and} \quad i_2 = \frac{I_T}{2}\left(1 - \tanh \frac{\Delta v}{2V_T}\right)$$

So the variation of i_1 and i_2 with Δv looks like:-

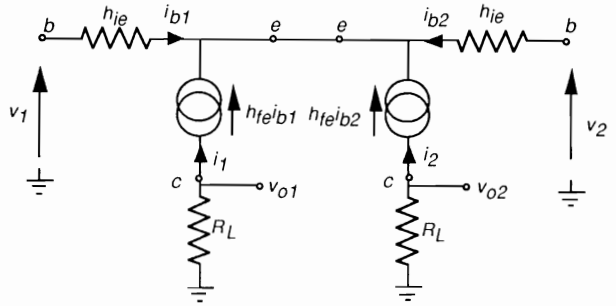


Here we have solved the circuit exactly, starting from the Ebers-Moll equations, and as we would expect, the solution is non-linear. The curves are approximately linear for small signals ($\Delta v \approx 0$), so distortion would be low here, but would increase as the input voltage became larger.

For small signals the gain from Δv to i_1 (strictly we should say 'transfer conductance' as it is the ratio of a current to a voltage) will be $\frac{\partial i_1}{\partial \Delta v}$ evaluated at $\Delta v = 0$ which is $\frac{I_T}{4V_T}$ or $\frac{I_T}{100mV}$.

Similarly, the small signal gain from Δv to i_2 is $-\frac{I_T}{100mV}$.

We will now look at the incremental equivalent circuit and show that, as we might expect, it predicts the same value for small-signal gain.



Summing currents at the emitter node gives $i_{b1} = -i_{b2}$.

Summing voltages round the outside loop and using the above, $v_1 - v_2 = 2h_{ie} i_{b1}$

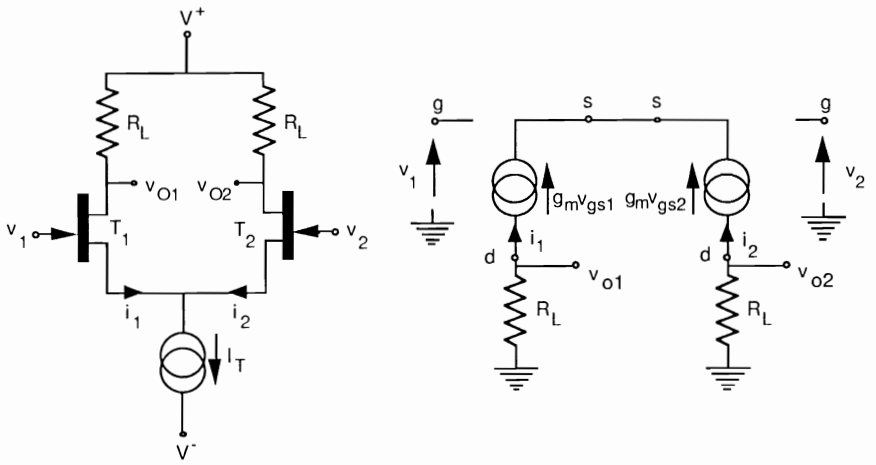
Now, $i_1 = h_{fe} i_{b1} = h_{fe} \frac{(v_1 - v_2)}{2h_{ie}}$, so the incremental gain is

$$\frac{i_1}{(v_1 - v_2)} = \frac{h_{fe}}{2h_{ie}} = \frac{g_m}{2} = \frac{1}{2}\frac{I_C}{25mV} = \frac{\frac{I_C}{2}}{50mV} = \frac{I_T}{100mV} \text{ as before!}$$

The differential voltage gain is then

$$\frac{(v_{o1} - v_{o2})}{(v_1 - v_2)} = \frac{I_T}{50mV} R_L \text{ or } \frac{h_{fe}}{h_{ie}} R_L \text{ or } g_m R_L.$$

Long-tailed pairs are also made with field-effect transistors particularly where their high input impedance is needed:-



Here, from the incremental model, $v_{o1} = -\frac{g_m}{2}(v_1 - v_2)R_L$, $v_{o2} = \frac{g_m}{2}(v_1 - v_2)R_L$

Close matching is harder to achieve with FETs.

In general, pairs of transistors in integrated circuits or multiple transistor arrays (e.g. the CA3046) are closely matched, as the transistors are made at the same time by the same process

Common-mode rejection

In analysing differential pairs, we have assumed a perfect current source in the tail, and with matched transistors, the gain has come out to be purely differential, with zero common-mode gain, i.e. the CMRR is infinite. Remember we could write

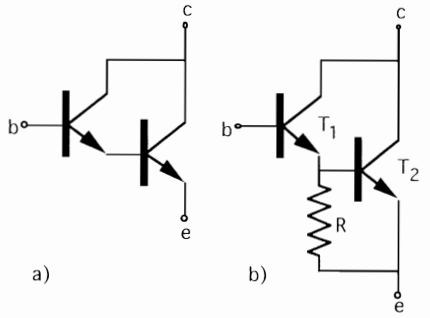
$$v_0 = Av_1 - Bv_2 = C(v_1 + v_2) + D(v_1 - v_2), \qquad C = \text{common-mode gain} = \frac{1}{2}(A - B)$$

$$D = \text{differential mode gain} = \frac{1}{2}(A + B)$$

So if $A = B$, $C = 0$ and common mode signals are totally rejected.

If the current source is replaced by a resistor, (which is equivalent to the current source having a finite output resistance) A and B are no longer the same and so the common-mode gain C becomes non-zero, with the result that the CMRR becomes finite. It is not difficult to analyse the circuit for this case and to derive a value for the CMRR – one of the questions on the examples sheet asks you to do this.

8) Darlington pair



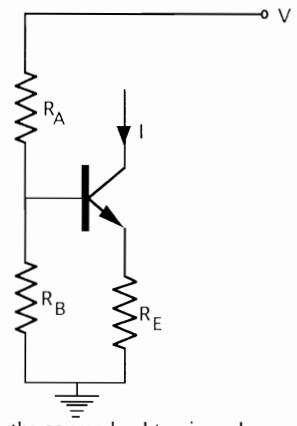
Two transistors connected together as in a) behave like a single transistor with β (and h_{fe}) equal to the product of the values for the individual transistors. Obviously the base-emitter voltage is twice that for a single transistor (around 1.4V).

The resistor R (diagram b)) is often included to speed up the turn-off of T_2. Without it, if T_1 turns off its emitter becomes an open circuit and there is nowhere for charge stored on T_2 base to go. The resistor allows this charge to flow to T_2's emitter.

Darlington pairs can be made from pairs of separate transistors, but can also be bought ready-made - often called Darlington transistors. The circuit is useful in high current situations, where T_2 would be a power transistor and T_1 a smaller device. It is also used in the input stages of amplifiers where a high input impedance is needed (here the transistors would probably be the same). Examples of these applications might be respectively the complementary emitter follower and the long-tailed pair in both of which the single transistors could be replaced by the Darlington circuit.

CURRENT SOURCES (and sinks)

1) Simple current sources



A current source can be made using a single bipolar transistor. The circuit shown is identical to the arrangement we have already seen for biassing a single amplifier stage, and so the current is given by

$$I = \frac{\left(\frac{R_B}{R_A + R_B}\right)V - V_{BE}}{R_E}.$$

A disadvantage of this circuit is that correct operation of the transistor requires that the collector voltage does not go more negative than the base, limiting the voltage range of the circuit)

We also saw that a JFET can be used as a current source, either with gate and source tied together, when the current is I_{DSS}, or with a resistor in the source lead to give a lower current.

FETs as simple current sources

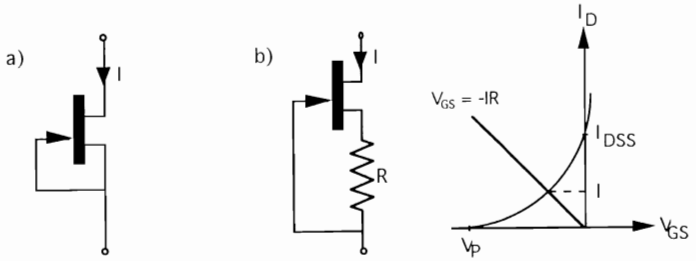
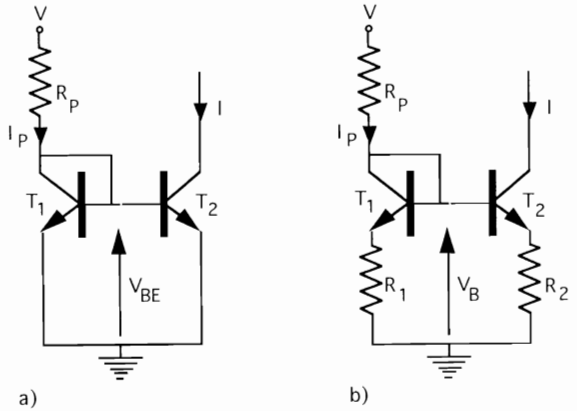


Diagram a) shows a single JFET with the gate connected to the source, so $V_{GS} = 0$, and as long as V_{DS} is large enough for the transistor to be in the pinch-off region, $I = I_{DSS}$.

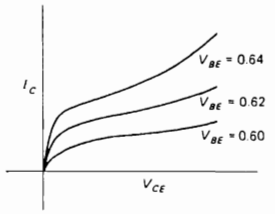
In diagram b) a resistor R has been included in the source lead, so $V_{GS} = -IR$, and the operating point is given by the intersection of this line with the transistor characteristic, as in the graph (again assuming pinch-off). R could be made variable to give a controlled current source.

2) Current mirrors



Current mirrors make use of the fact that identical transistors, with the same base-emitter voltage, will have the same collector current. Diagram a) shows the basic current mirror circuit, which is 'programmed' by setting the collector current of T_1 to I_P ($= \frac{(V - V_{BE})}{R_P}$). V_{BE} for T_1 is then caused to be the appropriate value for that transistor at the temperature of the circuit. The bases and emitters of T_1 and T_2 are connected together, so T_2 is forced to have the same value of V_{BE} as T_1. Because T_1 and T_2 are identical, I, the collector current of T_2, is the same as that of T_1 which, neglecting base currents, is I_P. So we have 'mirrored' the current I_P.

A disadvantage of simple current sources is that the output current varies slightly with changes in output voltage - the output resistance is not infinite. This is due to the so-called Early effect in the transistors.



At a given collector current there will be a slight variation in V_{BE} with collector voltage, so the plot of I_C against V_{CE} at fixed V_{BE} will not in fact be flat., unlike idealized transistor characteristics. The current might vary by 20% or 30% over the full output voltage range.

A possible solution is the circuit b), where resistors are included in series with the emitters. The resistors should be large enough to drop a few hundred millivolts. To analyse this start from the Ebers-Moll equation for each transistor:-

$$I_P = I_O \exp \frac{V_{BE1}}{V_T}, \qquad I = I_O \exp \frac{V_{BE2}}{V_T}.$$

Dividing these two, $\frac{I_P}{I} = \exp \frac{V_{BE1} - V_{BE2}}{V_T}$, which gives $V_{BE1} - V_{BE2} = V_T \ln \frac{I_P}{I}$.

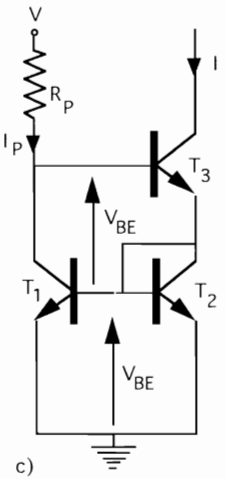
The base voltages are equal, so $V_{BE1} + I_P R_1 = V_{BE2} + IR_2$.

This gives $I = \frac{1}{R_2}(I_P R_1 + V_{BE1} - V_{BE2}) = \frac{1}{R_2}\left(I_P R_1 + V_T \ln \frac{I_P}{I}\right)$.

So if $I_P R_1 >> V_T \ln \frac{I_P}{I}$, $\boldsymbol{I = I_P \frac{R_1}{R_2}}$ and any difference in the V_{BE}s becomes insignificant.

Obviously, if $R_1 = R_2$, I is equal to I_P, but any ratio of currents can be produced by setting the resistors appropriately.

3) Wilson current mirror

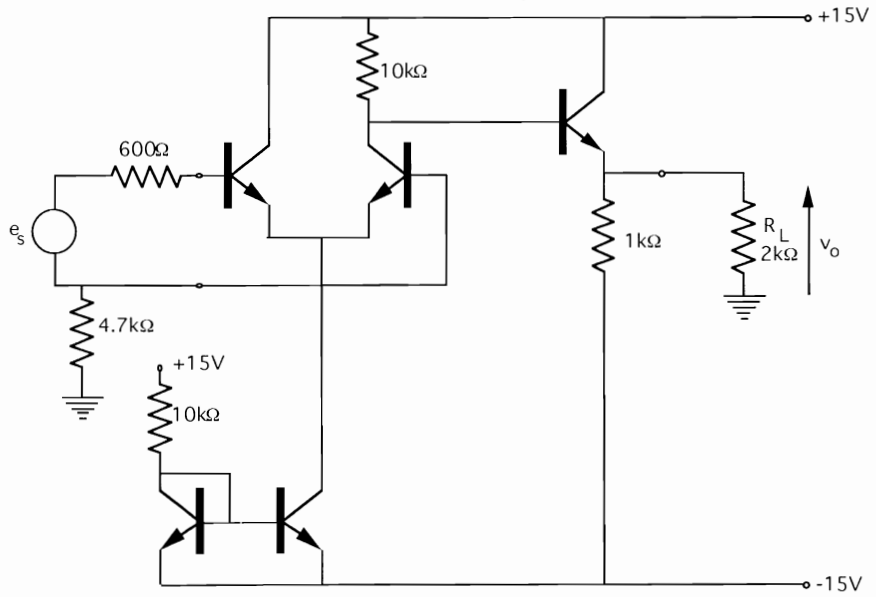


An even better arrangement, the Wilson current mirror, is shown here. T_1 and T_2 are in the usual mirror arrangement, and T_3 keeps the collector of T_1 fixed at $2V_{BE}$ above 0V, so its V_{CE} is constant and the Early effect is removed. Both T_1 and T_2 now have fixed collector-emitter voltages. T_2 sources the output current, which passes through T_3, whose base current is assumed to be negligible and therefore has negligible effect on the output current.

All these circuits have been shown in the form of current sinks referred to 0V at their negative ends (they could equally well have been referred to the negative supply) - the load would be connected between them and the positive supply rail. Obviously they could turned upside down, and the transistors replaced with pnp types, to form current sources referred to either 0V or the positive rail.

CASCADED AMPLIFIER STAGES

To calculate the overall gain of cascaded stages, it is easiest to represent each stage in terms of its input impedance, open-circuit gain and output impedance. As an example, consider a balanced source feeding a two-stage amplifier consisting of a long-tailed pair with an emitter follower on its output, and connected to a load R_L. The transistors have h_{fe} = 200.



The current mirror sets the tail current at 2.94mA, so I_E = 1.47mA,in each transistor, making g_m = 1.47 x 40 = 58.8mA/V and $h_{ie} = \frac{25}{1.47}$ x 200 Ω = 3.40kΩ

Gain from differential input to single ended output = $\frac{g_m}{2}$ x R_L = 29.4 x 10 = **294**

Input resistance = $2h_{ie}$ = **6.80kΩ**, Output resistance = R_L = **10kΩ**

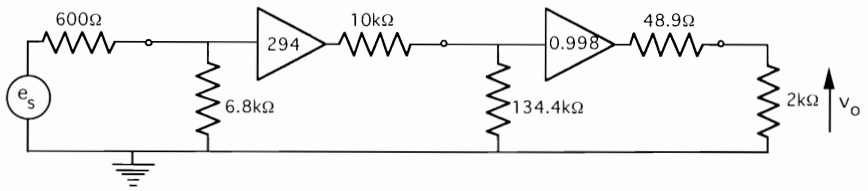
V_B for the emitter follower = 15 - 1.47 x 10 = +0.3V, so V_E is this less V_{BE} = 0.3 - 0.6 = -0.3V.

I_E in the emitter follower is $\frac{14.7V}{1k\Omega} - \frac{0.3V}{2k\Omega}$ = 14.6mA, so $h_{ie} = \frac{25}{14.55}$ x 200Ω = 344Ω

Gain = $\frac{(1+h_{fe})R_E}{h_{ie}+(1+h_{fe})R_E} = \frac{201 \text{ x } 1}{0.344 + 201 \text{ x } 1}$ = **0.998**

Input resistance = 0.344 + 201(1 ‖ 2) = **134.4 kΩ**

Output resistance = 1 ‖ $\frac{10 + 0.344}{201}$ kΩ = **48.9Ω**



The overall gain is then a simple product:-

$$\frac{v_o}{e_s} = \frac{6.8}{6.8+0.6} \text{ x } 294 \text{ x } \frac{134.4}{134.4+10} \text{ x } 0.998 \text{ x } \frac{2}{2+0.049} = \mathbf{245.}$$

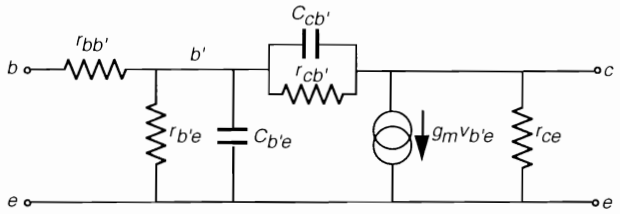
HIGH-FREQUENCY BEHAVIOUR OF BIPOLAR TRANSISTORS

The hybrid-π model

The h-parameter equivalent circuit models well the behaviour of a bipolar transistor at frequencies low enough for the effect of the internal capacitances of the transistor to be negligible. These capacitances, associated with the p-n junctions of the transistor, (the base-emitter junction which is forward biased, and the base-collector junction which is reverse biased) have to be taken into account at frequencies above approximately a few hundred kHz: the actual frequency will depend on the particular transistor. The so-called hybrid-π model includes these capacitances, and is useful for calculating their effects. This equivalent circuit is still a hybrid model, so it has some similarity to the h-parameter circuit.

The base-emitter junction is forward biased, with minority carriers injected into the base from the more heavily doped emitter region. These carriers diffuse across the base region, taking a finite time to do so and as a result the base-emitter junction has a capacitance, C_{dif} (the diffusion capacitance), which is proportional to emitter current. Added to this is the depletion layer capacitance which is usually negligible in comparison. The base-collector junction, being reverse-biased, has just its depletion layer capacitance, which will vary with reverse voltage according to the doping profile. For an abrupt junction the depletion layer capacitance is inversely proportional to the square root of reverse voltage, and for a linearly graded junction it is inversely proportional to the cube root of reverse voltage.

The diagram below shows the full hybrid-π equivalent circuit.



The resistor $r_{bb'}$ is the base spreading resistance (the resistance due to the base contact and the bulk semiconductor between the contact and the actual junction) and the terminal labelled b' is effectively the base side of the base-emitter junction. Its value is usually a few tens to a few hundreds of ohms, depending on the transistor. Often, to simplify analysis, $r_{bb'}$ is made zero; this is reasonable as long as the impedance of the source is significantly greater than $r_{bb'}$.

The resistor $r_{b'e}$ is $\frac{v_{b'e}}{i_b}$ (incremental quantities) and is the input resistance of the actual junction which, from the Ebers Moll equation, is given by

$$r_{b'e} = \frac{25mV}{I_B} = \beta\frac{25mV}{I_C} \approx h_{fe}\frac{25mV}{I_C} \text{ where we have taken } \frac{kT}{e} = 25\text{mV}.$$

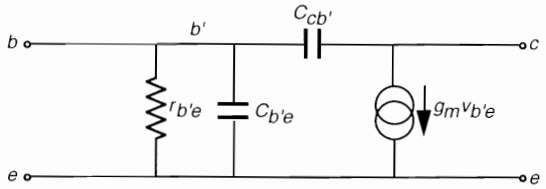
This, of course, is the same expression as we had previously for h_{ie} (defined as $\frac{v_{be}}{i_b}$) when we were not bothering about $r_{bb'}$. Now, we have carefully separated the base spreading resistance from the actual base-emitter junction incremental resistance.

The capacitance in parallel with $r_{b'e}$, $C_{b'e}$ is the diffusion capacitance of the forward biased base-emitter junction, (proportional to I_E) and $C_{b'c}$ represents the base-collector capacitance.

The value of the collector current generator is g_m (the transconductance, equal to $\frac{I_c}{25mV}$) times $v_{b'e}$, the voltage between the *internal* base terminal b' and the emitter. Notice that this model is

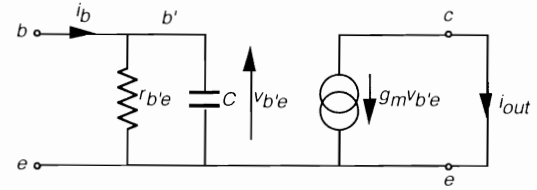
voltage controlled in contrast to the h-parameter model where the collector current generator is proportional to the base *current*.

We remember that the full h-parameter circuit is usually simplified by taking both h_{re}, which represents the effect of v_{ce} on v_{be}, and the output conductance h_{oe}, to be negligibly small. Hence we might deduce that in the hybrid-π circuit the equivalent components at low frequencies, $r_{b'c}$ and r_{ce}, may be replaced by open circuits. These approximations along with putting $r_{bb'} = 0$ lead to the simplified circuit :-



Short-circuit current gain with hybrid-π model

The short circuit current gain is defined as the ratio of incremental collector current to base current, with the collector voltage held constant, that is, with the incremental collector voltage set to zero. In the h-parameter model it is, of course just h_{fe}. The following circuit shows the hybrid-π model with the collector shorted to a.c.

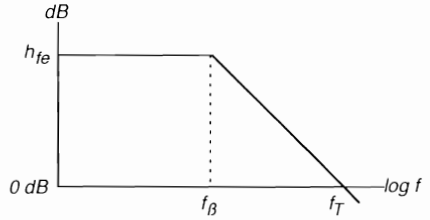


The capacitance C is the sum of $C_{b'e}$ and $C_{cb'}$. In this circuit,

$$v_{b'e} = i_b \frac{r_{be}}{1 + j\omega C r_{b'e}} \text{ and so}$$

$$i_{out} = -g_m v_{b'e} = \frac{-g_m r_{b'e}}{1 + j\omega C r_{b'e}} = \frac{-h_{fe}}{1 + j\frac{\omega}{\omega_\beta}} \text{ where } \omega_\beta = \frac{1}{C r_{be}} \text{ or } f_\beta = \frac{1}{2\pi C r_{b'e}}$$

The current gain is h_{fe} at low frequencies with a high frequency break point at ω_β :-



The current gain falls to 0 dB at a frequency f_T, which is equal to h_{fe} times f_β, so $\boldsymbol{f_T = \frac{1}{2\pi}\frac{h_{fe}}{C r_{b'e}}}$.

Remembering $r_{b'e} = h_{fe}\dfrac{25mV}{I_C}$, we get $f_T = \dfrac{1}{2\pi}\dfrac{I_C}{25mV}\dfrac{1}{C} = \dfrac{1}{2\pi}\dfrac{g_m}{C}$, again taking $\dfrac{kT}{e} = 25\text{mV}$.

Manufacturers' data sheets for transistors usually specify f_T and $C_{cb'}$ at a particular collector current and V_{CE}. This gives sufficient information for $C_{b'e}$ to be deduced at this value of current. The specified value of $C_{cb'}$ will usually include the capacitance due to the package.

As an example, consider a transistor which has the following specification:-

$$f_T = 300\text{MHz},\quad C_{cb'} = 1.6\text{pF},\quad h_{fe} = 120$$

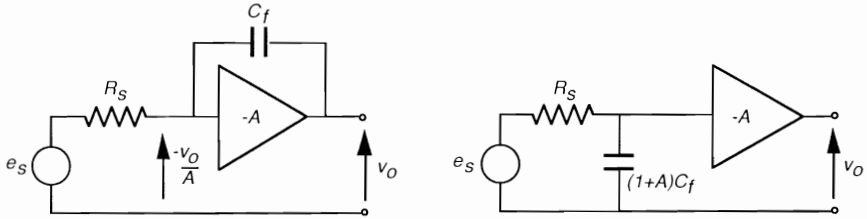
measured at I_C = 1mA and V_{CE} = 10V and at a transistor junction temperature of 25°C

We can calculate $r_{b'e} = h_{fe}\dfrac{kT}{eI_C}$ which, with the given values of h_{fe}, I_C and T, comes to **3110Ω**.

The expression $f_T = \dfrac{1}{2\pi}\dfrac{I_C}{25mV}\dfrac{1}{C}$ gives C = 20.6pF. $C = C_{b'e} + C_{cb'}$ so $C_{b'e}$ = 20.6 -1.6 = **19pF.**

The Miller effect

This is a general theorem which will help us analyse the behaviour of a common-emitter amplifier at high frequencies. The left-hand diagram shows a generalized inverting amplifier of gain A, with capacitance C_f from output back to input. Specifically, this might be a common-emitter stage (input to the base, output from the collector), where C_f represents the base-collector capacitance of the transistor.



The circuit is straightforward to analyse - sum currents at the input node:-

$$\frac{e_s - \frac{v_o}{A}}{R_s} + j\omega C_f\left(v_o - \frac{v_o}{A}\right) = 0 \quad \text{which simplifies to}$$

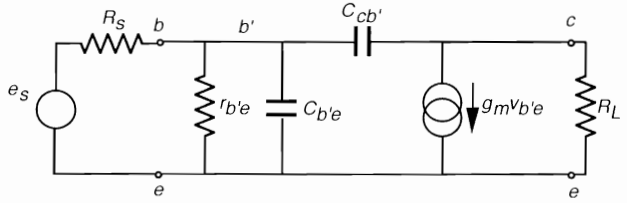
$$v_O = \frac{-A}{1 + j\omega C_f(1+A)R_s}$$

This has a break point at a frequency set by the product of R_S and a capacitance of $(1 + A)C_f$. The response is exactly the same as that of the second diagram where the feedback capacitance has been replaced by a capacitor of $(1 + A)$ times its value connected from the input to ground.

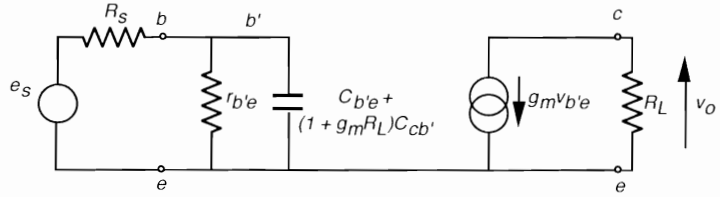
The standard operational amplifier integrator is of course the limiting case of this as $A \to \infty$.

High frequency response of a common emitter amplifier with a resistive load

The equivalent circuit of a single common-emitter stage is in the diagram below. The load resistor is R_L. A full analysis gives a quite complicated transfer function (try it if you want), but the dominant response can be derived more simply using Miller's theorem.



The transistor can be treated as an amplifier of voltage gain $-g_mR_L$, which is the gain A in the discussion of the Miller effect above. According to the Miller theorem, the collector-base capacitance $C_{cb'}$ is replaced by a capacitor of $C = (1 + g_mR_L)C_{cb'}$ connected from b' to emitter, as shown in the following circuit.



It is easy to show that the transfer function is now given by

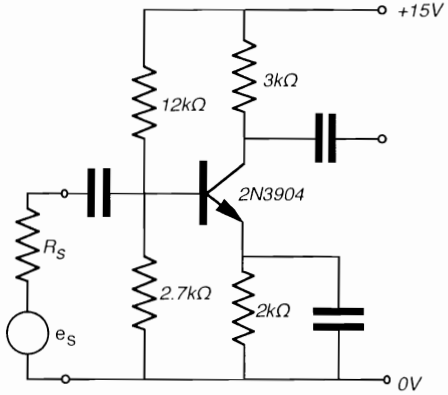
$$\frac{v_O}{e_S} = -g_mR_L\,\frac{r_{b'e}}{R_s + r_{bb'}}\,\frac{1}{1 + j\omega\left(C_{b'c} + (1 + g_mR_L)C_{cb'}\right)(r_{b'e} \parallel R_s)}.$$

The high frequency break point is at

$$\omega = \frac{1}{\left(C_{b'e} + (1 + g_mR_L)C_{cb'}\right)(r_{b'e} \parallel R_s)}$$

It is quite reasonable to assume that for a reasonable value of collector current (and hence g_m), $(1 + g_mR_L) \gg 1$, with the result that the effect of $C_{cb'}$ will dominate the base-emitter capacitance. We also see that the break point depends on the source resistance - the lower this is, the higher the break point frequency. A voltage-driven amplifier has a bigger bandwidth than a current-driven one.

An example will help to show what happens, and confirm that in such a circuit it is usually $C_{cb'}$ which determines the high frequency response. Consider a single stage amplifier using the 2N3904 transistor whose parameters we analysed previously, and fed from a source with resistance 10kΩ.



The biassing components set I_C at 1mA, and V_{CE} at 10V so we know $r_{b'e}$ = 3110Ω, $C_{cb'}$ = 1.6 pF and $C_{b'e}$ = 19.6 pF as before.

At I_C = 1 mA, g_m is 40 mA/V.

The two factors in the expression above for the high frequency break point are now:-

$C_{cb'} + (1 + g_mR_L)C_{cb'}$ = 19 + 121 x 1.6
= 212.6 pF

and $r_{b'e} \parallel R_s$ = 3110Ω ‖ 10kΩ = 2.37kΩ.

so the break-point frequency is

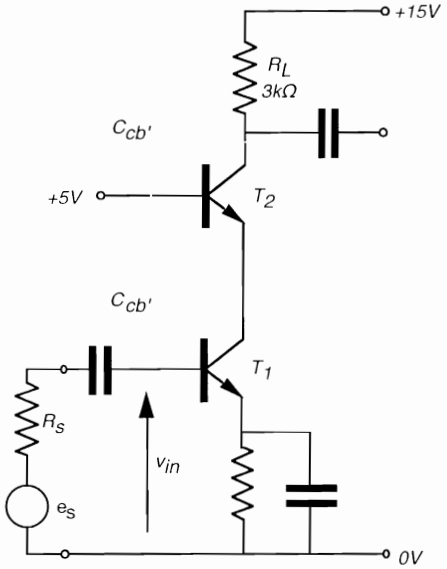
$$\frac{1}{2\pi}\,\frac{1}{212.6\text{pF} \times 2.39\text{k}\Omega}\ \text{Hz} = \textbf{316 kHz}.$$

If the resistance $r_{bb'}$ had been included, it would simply have added to R_s in these calculations and would therefore have to be included in the model if R_s was small.

We see from the calculation that the dominant term in the total capacitance is that due to $C_{cb'}$, multiplied by the Miller effect. This is the result of a large voltage swing at the transistor collector. If the collector fed into a low impedance (that is, the following stage was current driven), the voltage swing there would be small, and the Miller effect should be removed. The next circuit achieves this

The cascode circuit

This is a commonly used two transistor high-frequency amplifier circuit - you may remember it from first year design, build and test. For clarity it is shown here without biasing components.



The input goes to the base of the bottom transistor T_1, as it did to the single transistor before. The collector of T_1, however, connects to the emitter of a second transistor T_2, whose base is held at a constant voltage – T_2 is a common-base stage.

The input voltage causes the collector current of T_1 to change as

$i_c = g_m v_{in}$ (incremental values again)

and this current goes into T_2 emitter and flows through to its collector. The output voltage $-g_m R_L v_{in}$ appears across R_L.

T_2's base-emitter voltage must also change by v_{in} to give the change in collector current - as its base voltage is held fixed, its emitter voltage, and hence the collector voltage of T_1, changes by $-v_{in}$. The voltage across $C_{cb'}$ of T_1 is therefore just $2v_{in}$ - we have the Miller effect with $A = 1$. So $C_{cb'}$ here is multiplied by just 2, rather than the whole gain of the amplifier.

As the base of T_2 is fixed in voltage (grounded for signals), $C_{cb'}$ appears in parallel with R_L, with a negligible effect on high frequency response (remember $C_{cb'}$ is typically a few pF.

So this is a circuit which gets round the effect of $C_{cb'}$ in limiting the high frequency response. A full analysis takes a few lines of calculation, but brings out the results we have reached simply - high frequency break points at $\frac{1}{2\pi}\frac{1}{C_{cb'}R_L}$ and $\frac{1}{2\pi}\frac{1}{2C_{cb'}(R_s \parallel R_{b'e})}$.

Long-tailed pair

The long-tailed pair can also be used to avoid the Miller effect on $C_{cb'}$, if a single-ended input is fed to the base of one transistor whose collector is grounded to a.c. and the output is developed across an impedance in the collector circuit of the other transistor.

Radio-frequency amplifiers

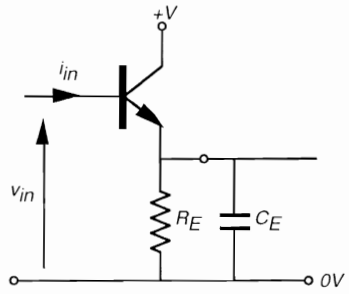
A radio frequency amplifier, for example an intermediate frequency amplifier stage in a superheterodyne receiver, might have a parallel resonant circuit as the collector load in order to give

a bandpass response. If such a stage was made with a single transistor, current would be fed back from collector to base via $C_{cb'}$ the same way that we have seen. However, because of the resonant collector load, the feedback would now be positive at some frequency, leading to oscillation. The cascode circuit again gets round this – in fact the circuit was first used (with thermionic valves) in r.f. amplifiers.

Emitter follower with a capacitive load

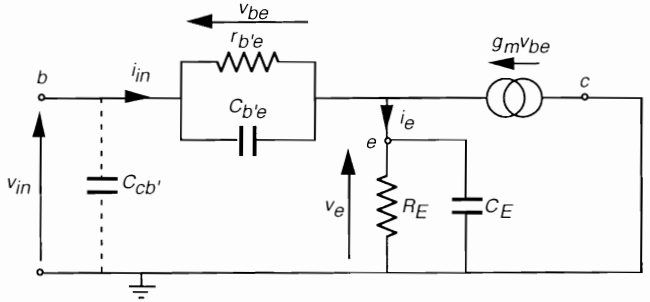
As we saw earlier, the emitter follower is usually thought of as a robust buffer circuit used to isolate a source with a relatively high output impedance from a load. It normally works without problems, but sometimes, if a small capacitance is connected to the emitter follower output, the circuit will surprisingly begin to oscillate at a high frequency. We shall see that it is the base-emitter capacitance, $C_{b'e}$, that is responsible for this, and that under certain conditions the input impedance of the emitter follower can behave oddly.

You may remember, in the first year DBT, if you made a radio with a cascode radio frequency amplifier, you had an emitter follower following the resonant circuit, buffering the output of the r.f. amplifier. All was well as long as you connected the oscilloscope to the emitter follower via a times 10 probe (which adds only a few pF of capacitance to the emitter follower output) but if a times 1 probe was used, with over 100 pF capacitance, often the circuit burst into violent oscillation.



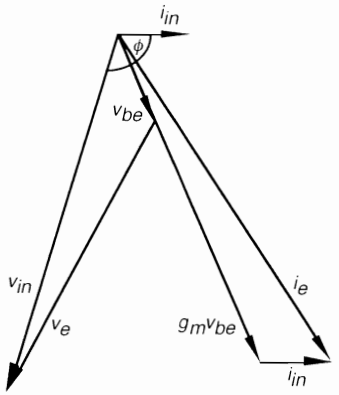
The diagram shows an emitter follower, biassing components being omitted for clarity, with emitter resistor R_E, and with a capacitance C_E connected to the output. The small-signal input voltage and current are v_{in} and i_{in} respectively.

The incremental model for the circuit, using the simplified hybrid-π transistor model, is:-



We see that as the collector is grounded for small signals, the collector-base capacitance, $C_{cb'}$, now appears across the input. We are going to calculate the input admittance of the circuit, which we can think of as the admittance of $C_{cb'}$ (which is purely imaginary) plus the admittance of the circuit to the right of it, v_{in}/i_{in}. This makes the calculaton easier.

A straightforward way of seeing what is happening before we do the calaulation is to construct a phasor diagram for the voltages and currents in the equivalent circuit. Starting with i_{in} as reference, v_{be}, the voltage across the $r_{b'e}$, $C_{b'e}$ combination will be lagging and as the transconductance, g_m, is real, the current $g_m v_{b'e}$ will have the same angle. The emitter current i_e



is the sum of this and i_{in}, and the emitter voltage v_e, due to i_e flowing through R_E and C_E in parallel will lag with respect to i_e. The input voltage v_{in} is then the sum of $v_{b'e}$ and v_e.

The diagram shows that v_{in} lags with respect to i_{in} by an angle ϕ, which is clearly more than 90°, giving v_{in} a negative real part. This means that the input impedance, v_{in}/i_{in}, and the input admittance, i_{in}/v_{in} will both also have negative real parts. Thinking in terms of admittances, it is obvious that when the input admittance of the whole circuit is calculated by adding in the imaginary admittance of $C_{cb'}$, the negative real part is unchanged.

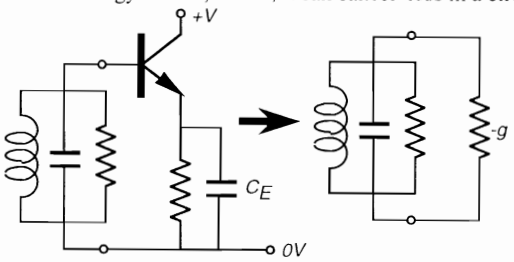
Analysis of the equivalent circuit is quite easy (if a bit tedious) and shows Y_{in} to be:-

$$Y_{in} = \frac{i_{in}}{v_{in}} = \frac{1}{r_{b'e} + R_E\left(1 + g_m r_{b'e}\right)} \; \frac{\left(1 + j\omega C_{b'e} r_{b'e}\right)\left(1 + j\omega C_E R_E\right)}{1 + j\omega\left(C_{b'e} + C_E\right)\dfrac{r_{b'e}}{\left(1 + g_m r_{b'e}\right)} \,||\, R_E}$$

This expression is of the form $Y_{in} = Y_0 \dfrac{\left(1 + j\dfrac{\omega}{\omega_1}\right)\left(1 + j\dfrac{\omega}{\omega_2}\right)}{\left(1 + j\dfrac{\omega}{\omega_3}\right)}$,

with phase $arg\left(Y_{in}\right) = tan^{-1}\left(\dfrac{\omega}{\omega_1}\right) + tan^{-1}\left(\dfrac{\omega}{\omega_2}\right) - tan^{-1}\left(\dfrac{\omega}{\omega_3}\right)$.

If ω_3 is significantly greater than ω_1 and ω_2, (this is very likely – using the transistor parameters from page 27, and taking R_E as 5 kΩ and C_E as 100pF gives $\omega_1/2\pi$ = 2.61MHz, $\omega_2/2\pi$ = 318 kHz and $\omega_3/2\pi$ =53 MHz), there will be a range of frequencies where $arg(Y_{in})$ is greater than 90°, making the real part of Y_{in} negative – in this case above about 900 kHz. This is what we saw from the phasor diagram. The negative real part of the input admittance tells us that the input can act as an energy source, that is, it can cancel loss in a circuit connected to it.



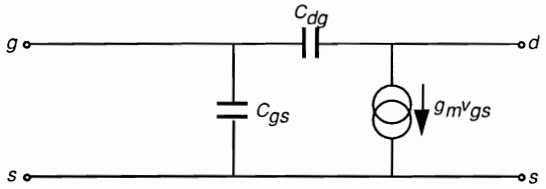
If a resonant circuit is connected to the input, and the negative input conductance is greater than the equivalent parallel conductance in the resonant circuit, the circuit will act as an oscillator. Sometimes just stray inductance and capacitance in the circuitry connected to the base are sufficient to provide the resonance, and the circuit will then oscillate at a very high frequency.

The article 'Negative Resistance Oscillator', by I. Hickman (Electronics World 106 p. 977, December 2000) describes some experiments in making very high frequency oscillators (~100 MHz) with this circuit. Unfortunately the article incorrectly refers to phasor diagrams as vector diagrams! Another article discussing emitter follower buffers with capacitive loads is 'Flat, Wideband Buffers' by D. de Lange (Electronics World 109 p. 19, October 2003).

Field effect transistors

The high frequency performance of field effect transistors is limited in the same way by internal capacitances between drain and gate, C_{dg}, and between gate and source, C_{gs}. The Miller effect applies to the drain-gate capacitance in the same way as for bipolar transistors.

The equivalent circuit for a field effect transistor at high frequencies can be drawn:-



If bipolars are replaced with field effect transistors in the circuits we have considered, the behaviour of the circuits is qualitatively very similar. Analysis of the fet circuits tends to be somewhat less tedious, though, because of the simpler equivalent circuit (the resistor $r_{b'e}$ has become an open-circuit).