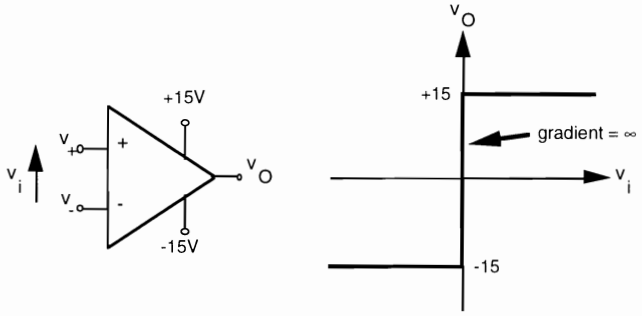
OPERATIONAL AMPLFIERS

THE IDEAL OPERATIONAL AMPLIFIER



All the operational amplifier calculations you have done up to now have assumed the amplifier to be ideal with the following characteristics:-

1) Infinite differential gain, i.e. $v_{OUT} = A\ v_{IN} = A(v^+ - v^-)$ with $A \to \infty$. This leads to the assumption $v^+ = v^-$. The idealised transfer characteristic is as shown.

2) Zero common mode gain, i.e. $v_{OUT} = 0(v^+ + v^-)$.

3) Infinite input impedance, i.e. no current flows into either input.

4) Zero output impedance, i.e. the output voltage is independent of any load connected to the output terminal.

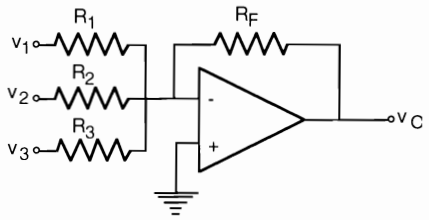
5) Infinite bandwidth. Zero phase shift at all frequencies.

6) Zero offset voltage - zero input gives zero output (c.f. 1))

7) Amplifier is noiseless

We can go a long way towards designing op-amp circuits using this ideal model, but circuit performance is ultimately limited by one or more of these idealisations breaking down. We will next look at a number of standard operational amplifier circuits, most of which you will have seen before, and which can all be analysed using the ideal amplifier assumptions.

1) Inverting amplifier and adder

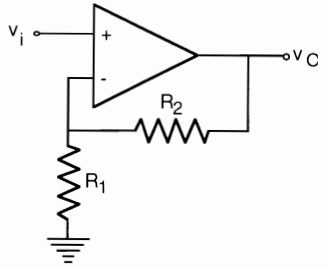


$$v_O = -R_F\left(\frac{v_1}{R_1} + \frac{v_2}{R_2} + \frac{v_3}{R_3}\right)$$

With just one input this forms a simple inverting amplifier.

Input impedance is equal to R_1 at the v_1 input (similarly for the other imputs) and can be low if the stage has a high gain - for example for a gain of 1000, R_F might be 1MΩ and R_1 therefore 1kΩ. This might draw too much current from a previous stage, and a better arrangement might be to use a non-inverting circuit, followed, if necessary, by an inverter.

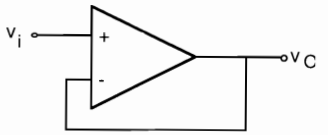
2) Non-inverting amplifier



$$v_O = \left(1 + \frac{R_2}{R_1}\right) v_i$$

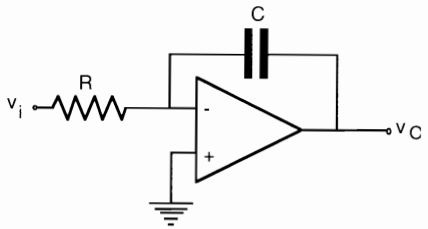
The input here goes directly into the non-inverting op. amp input, so the input impedance is high and does not depend on the gain determining resistors.

3) Unity gain buffer



This is a special case of the non-inverting amplifier with $R_2 = 0$ and $R_1 = \infty$. It has unity gain and very high input impedance.

4) Integrator

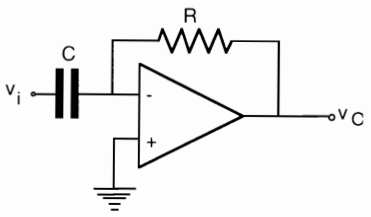


$$v_O = -\frac{1}{CR}\int v_i\, dt$$

or, in the frequency domain,

$$\frac{V_o}{V_i} = -\frac{1}{j\omega CR}$$

5) Differentiator



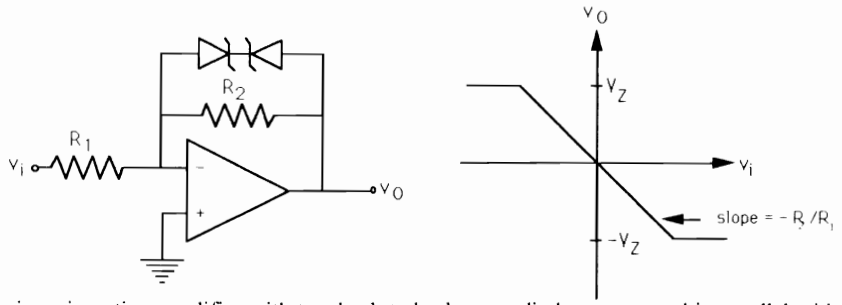
$$v_O = -CR\frac{dv_i}{dt},$$

or, in the frequency domain,

$$\frac{V_o}{V_i} = -j\omega CR$$

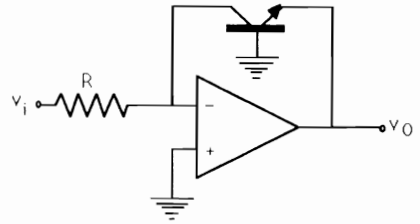
greatly, and, as we shall see when we look at stability, the circuit is likely to be unstable. Both problems can be solved by including a small capacitor in parallel with the resistor or a small resistor in series with the capacitor, both of which cause the gain to level off at high frequencies.

6) Limiting amplifier



This is an inverting amplifier with two back-to back zener diodes connected in parallel with the feedback resistor. The diodes will not conduct until the voltage across them reaches V_Z in either polarity. Because one diode is forward biassed, and the other is conducting in the reverse direction V_Z is (zener voltage + 0.7V). As the inverting input of the op.amp is always at 0V the diodes conduct when the output reaches $\pm V_Z$ and prevent it exceeding this voltage.

7) Log and antilog amplifiers

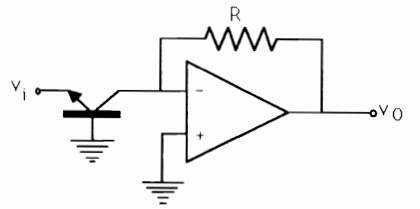


For the transistor, $i_C = I_0 \exp \frac{ev_{BE}}{kT}$

Also, $i_C = \frac{v_i}{R}$ and $v_O = -v_{BE}$

$$v_O = -\frac{kT}{e} \ln \frac{v_i}{I_0 R}$$

The circuit only works for positive input voltages, and gives a negative output - a pnp transistor would give opposite polarities.



Similarly to the previous circuit,

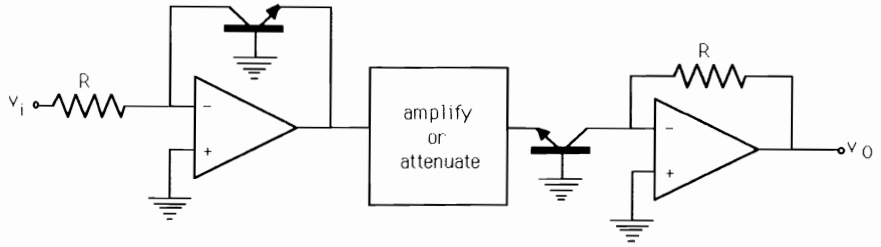
$$v_O = I_0 R \exp \frac{ev_{BE}}{kT} = I_0 R \exp \frac{e(-v_i)}{kT}$$

i.e. an antilog function.

This circuit only works for negative input voltages, giving a positive output. Again, using a pnp transistor would give opposite polarities.

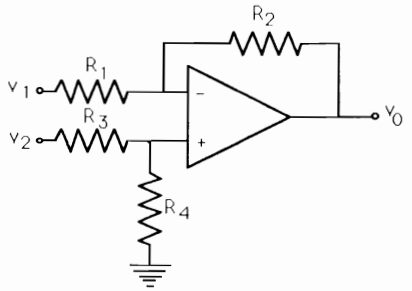
Log and antilog circuits can obviously be used in combination for multiplication - take logs of two signals, add them then take antilog.

It is also possible to make an amplifier with a variable power law, $v_O = (v_i)^n$:-



Here, the first part of the circuit gives an output $-\frac{kT}{e} \ln \frac{v_i}{I_0 R}$, which is then amplified (for n > 1) or attenuated (for n < 1). Obviously, for reliable performance of such a circuit, the two transistors should be a matched pair, and should be at the same temperature. Integrated circuits carrying out this function are available (the attenuation or amplification is done externally).

7) Differential input amplifiers



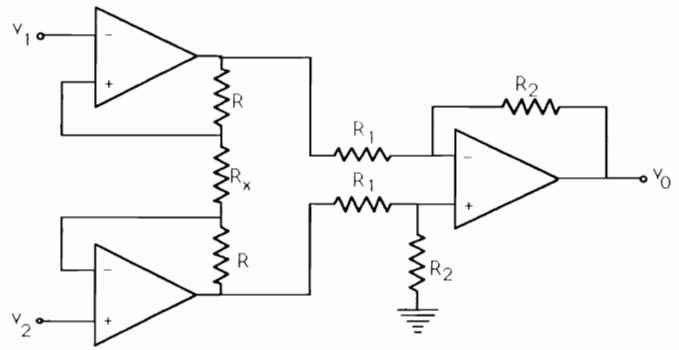
This is the simplest differential amplifier, and relies on accurate resistor matching $\left(\frac{R_2}{R_1} = \frac{R_4}{R_3}\right)$ for good common mode rejection.

In this case, $v_O = \frac{R_2}{R_1}(v_2 - v_1)$,

i.e. common mode gain is zero and CMRR is infinite. However, this is severely degraded by even a very small error in resistor matching. A possible solution is to make one of the resistors variable by a small amount, and then adjust it to give best common mode rejection. However the circuit still has the problem that the output resistance of the sources adds to R_1 and R_2 which can also upset the matching. The input resistance is not very high, either.

The instrumentation amplifier overcomes these problems. The second stage is identical to the one we have just seen, but the first has a differential mode gain of $\left(1 + \frac{2R}{R_x}\right)$ (easily shown) and a common mode gain of 1 (put $v_1 = v_2$ to calculate it). So the CMRR of this stage is equal to the differential gain, and the CMRR of the whole amplifier is the CMRR of the second stage multiplied by this factor. A further advantage is that the inputs go straight into op. amp inputs, making the input impedance high.

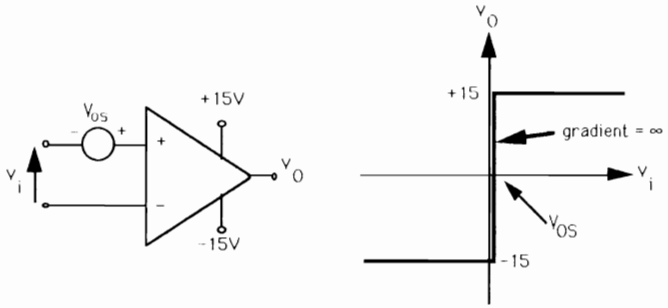
Instrumentation amplifiers are made integrated in a single package, with terminals to connect R_X externally to set the gain:-



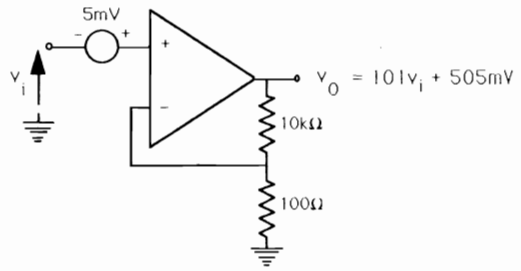
REAL OPERATIONAL AMPLIFIERS

1) Input offset voltage

Because of mismatching between components on the two sides of the input differential pair amplifier, the amplifier will not give zero output for zero input voltage. The input offset voltage is the input voltage which does give zero output. It can be represented as a voltage source in series with the input of an ideal operational amplifier.

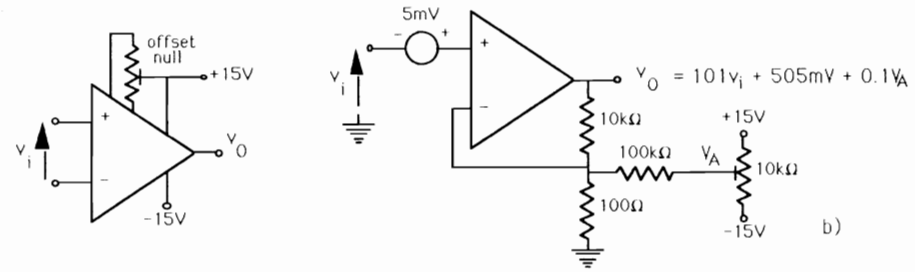


For general purpose op. amps V_{OS} can be up to 10mV. Special, laser trimmed amplifiers can have V_{OS} as low as 10 μV, but, of course cost more. If the amplifier is used in a circuit with d.c. gain, V_{OS} appears, added to the signal and amplified, at the output. For example, imagine a x101 non-inverting amplifier made with an op.amp which has an offset of 5mV.



The offset voltage has been amplified to more than 0.5V at the output.

Most op. amps have provision for an 'offset nulling' adjustment, with an arrangement something like in the diagram, to eliminate the offset voltage by slightly altering the balance between the currents in the two sides of the input differential amplifier (diagram a)).

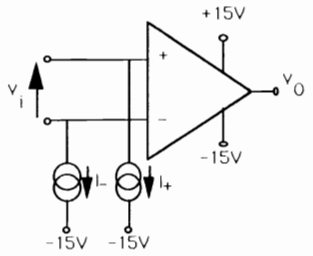


However, a drawback of using this adjustment can increase the temperature coefficient of V_{OS}, and thus make it more sensitive to temperature changes. If the offset has to be nulled, and the worsened temperature coefficient due to this method is unacceptable, a better way of doing it is to add in an adjustable external voltage. One possible way of doing this is shown in diagram b), where adjusting the potentiometer effectively adds about ±15mV at the input. The 100kΩ resistor is high enough to have a negligible effect on the gain - as far as the signal is concerned it, plus the Thevenin resistance seen at the slider of the potentiometer, appears in parallel with the 100Ω resistor, making around 0.1% difference.

A better way (but more expensive) of eliminating the effect of offset voltage and the need for an adjustment is to use one of the very low offset op. amps.

2) Input bias current, input offset current

The inputs of an operational amplifier are usually the two sides of a long-tailed pair, the bases if the pair are bipolar transistors, or the gates in the case of field effect transistors. These will take a d.c.input current, either base current or gate current, and this is called the input bias current. It can be modelled by two current sinks I_+ and I_-, on the non-inverting and inverting inputs respectively, of the ideal amplifier.



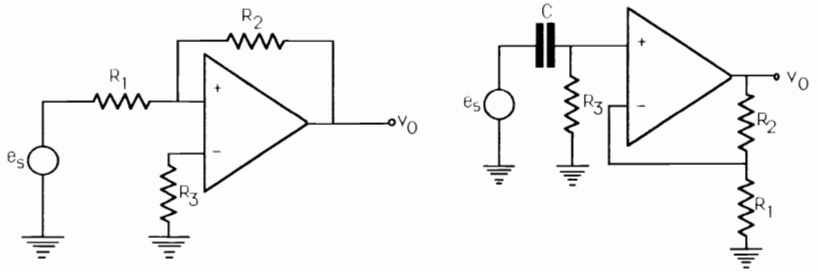
Bias current $I_B = \frac{I_+ + I_-}{2}$, and offset current $I_{OS} = I_+ - I_-$.

So $I_+ = I_B + \frac{1}{2} I_{OS}$, $I_- = I_B + \frac{1}{2} I_{OS}$.

FET input stages have very low I_B and I_{OS} - typically a few pA. Bipolars have higher values (they need base current), for example in the 741 (rather outdated now) $I_B \approx 500nA$, $I_{OS} \approx 200nA$.

These currents flow through the resistance of the circuitry connected to each input, and the resulting voltage drops appear as voltages at the two amplifier inputs. Assuming $I_+ = I_-$ (so $I_{OS} = 0$), these voltages will be equal, and so will cancel, if the resistances 'seen' by the two inputs are the same. This might be an appropriate design rule for bipolar op. amps to minimise errors due to the bias currents - obviously, though, I_{OS} will not be zero, and there will still be some offset voltage caused by this. So we should modify the design rule, to make the resistances seen by the inputs not only equal, but small enough so that the voltage due to the offset current is negligibly small.

As examples, consider respectively inverting and non-inverting amplifiers, the non-inverting amplifier being a.c. coupled:-

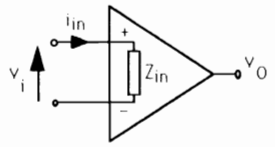


In the inverting amplifier, the resistance seen by the inverting input is $R_1 \parallel R_2$, and R_3, equal to this, should be included in series with the non-inverting input. If the source were coupled to this amplifier through a capacitor, then the inverting input would see just R_2, which would be the value for R_3. In the non-inverting amplifier, the condition is again $R_3 = R_1 \parallel R_2$. Of course, here, a resistor is necessary in the R_3 position in any case to provide a path for I_+.

With FET op. amps, because of their minute bias currents , it is seldom necessary to take these precautions unless the circuit resistances are extremely high (>> 1MΩ), and, in the inverting amplifier, R_3 could be left out.

Some modern high performance bipolar op. amps have extra circuitry to provide the bias current internally.

3) Input impedance



The input impedance of a real op.amp is not actually infinite, so a current $i_{in} = \frac{v_i}{Z_{in}}$ will flow as a result of v_i. Z_{in} will usually be a resistance (perhaps around 1MΩfor a bipolar amplifier, and 100-1000MΩ for one with a FET input stage) and a capacitance (usually a few pF) in parallel. The current which flows into the input impedance is completely separate from the bias current.

4) Frequency response

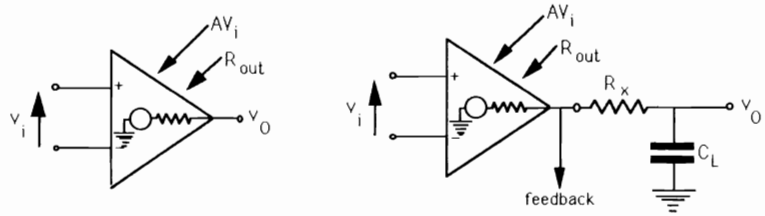
For all op. amps, the actual gain is far from the ideal of being very large at all frequencies. The high frequency response of any complex amplifier is going to be limited by the effects of capacitances associated with the individual transistors and stray circuit capacitances. Because the op. amp operates with feedback, it is necessary, for stability, to limit further the gain at high

frequencies by deliberately introducing a pole (the so-called 'dominant pole') into the amplifier response at quite a low frequency (around 100Hz in general purpose amplifiers). We will look at this in detail later.

5) Slew rate

The slew rate is the maximum rate, in volts per second (volts per microsecond in practice) at which the output of the amplifier can change. It is usually set by the current available internally to charge and discharge the capacitor which sets the dominant pole in the open-loop frequency response. The slew rate is a large signal parameter, and should not to be confused with the frequency response, which is measured with output amplitude kept low enough that the slew rate limit is not reached. As the slew rate is approached the maximum undistorted amplitude the amplifier can deliver depends on the frequency - the higher the frequency the smaller the amplitude. If the rate of change of the signal is too large, the output degenerates into a triangular wave with gradients equal to the slew rate.

6) Output current, output impedance



Unlike the ideal op. amp which has zero output impedance, real amplifiers have output resistance of a few ohms or tens of ohms - the output stage might be some kind of complementary emitter follower, probably with emitter resistors.

If the amplifier feeds a capacitive load C_L, this and R_{out} put a pole into the feedback loop at $\omega_p = \frac{1}{R_{out}C_L}$, which can threaten stability:-

$$v_O = \frac{1}{1 + j\omega C_L R_{out}} Av_{in} \quad \text{so as } \omega \rightarrow \infty, \text{ phase shift} \rightarrow -90°$$

A useful trick in this case is to connect the load through a small (10Ω - 100Ω) resistor, R_x. Without R_x, the response falls at -20dB/decade above ω_p, with phase shift approaching -90°, but with R_x, the response (to the point where the feedback is connected) has a downward step, with phase lag which returns to 0° at high frequencies:-

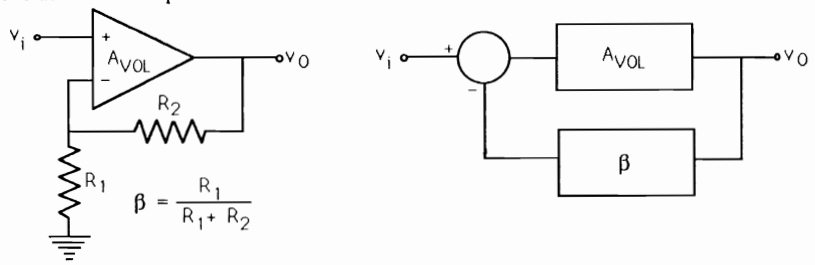
$$v_{feedback} = \frac{1 + j\omega C_L R_x}{1 + j\omega C_L (R_x + R_{out})} Av_{in} \quad \text{- phase returns to 0° as } \omega \rightarrow \infty$$

The output stage cannot deliver unlimited current to a load - indeed current limiting circuitry is built in to prevent excessive power dissipation in the output transistors. The data sheet will specify the maximum positive and negative current the amplifier can deliver, and this will, of course, put limits on the load that may be connected to it.

FREQUENCY RESPONSE AND STABILITY

From control theory, we know that frequency response and stability of a feedback system are inextricably linked. Operational amplifier circuits are feedback systems - it is their closed-loop behaviour that we set with the feedback components. In designing an amplifier it is necessary to be able to predict its frequency response, and to be sure that the system will be stable. It can be all too easy to make a 1MHz oscillator when a well behaved amplifier was intended.

Consider a basic amplifier circuit with feedback:-



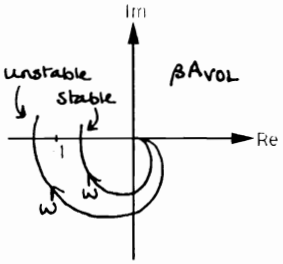
A_{VOL} = amplifier open-loop gain (now no longer assumed infinite)

β = feedback factor (this can be complex)

Obviously, the closed-loop gain $A_{VCL} = \frac{A_{VOL}}{1 + \beta A_{VOL}} \approx \frac{1}{\beta}$ for $\beta A_{VOL} >> 1$.

As in a control system it is the loop gain, βA_{VOL}, which determines stability, and the Nyquist criterion predicts that the system will oscillate if

$1 + \beta A_{VOL} = 0$, that is $|\beta A_{VOL}| = 1$ and $\arg(\beta A_{VOL}) = -180°$.



Remember that for stability the Nyquist criterion requires that

$|\beta A_{VOL}| < 1$ when $\arg(\beta A_{VOL}) = -180°$

or

$\arg(\beta A_{VOL}) > -180°$ when $|\beta A_{VOL}| = 1$

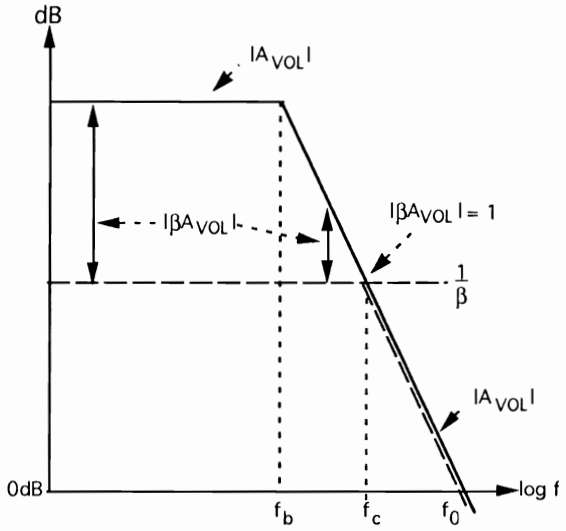
The **phase margin** $\phi_m = \arg(\beta A_{VOL}) - (-180°)$ at the frequency where $|\beta A_{VOL}| = 1$, and for stability, $\phi_m > 0$. A phase margin of $\approx 90°$ will give a slightly overdamped step response, and as ϕ_m decreases, the damping decreases and the response becomes progressively more oscillatory.

Now, we know $A_{VCL} = \frac{A_{VOL}}{1 + \beta A_{VOL}}$ gives the closed loop gain, and we can get its asymptotes on a Bode diagram by looking at the two limiting cases:-

$\beta A_{VOL} >> 1$ when $A_{VCL} \rightarrow \frac{1}{\beta}$

$\beta A_{VOL} << 1$ when $A_{VCL} \rightarrow A_{VOL}$

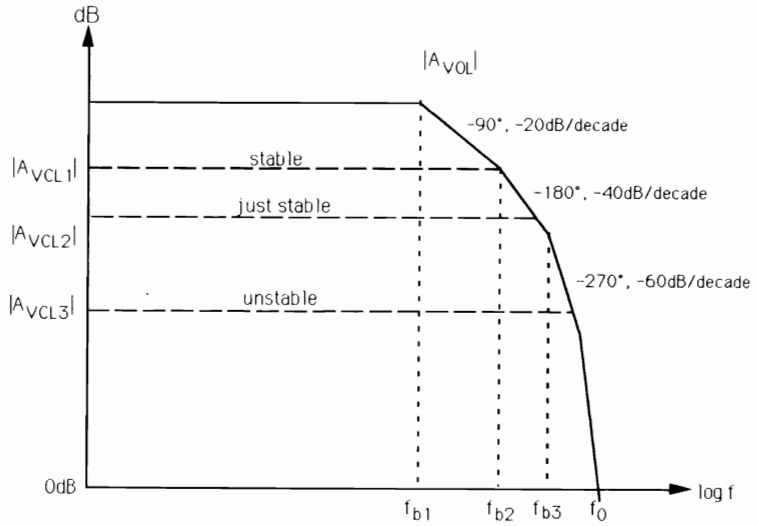
These are plotted as the coarse dotted lines on the Bode diagram here, which is for an ideal amplifier with just one high frequency break point at frequency f_b.



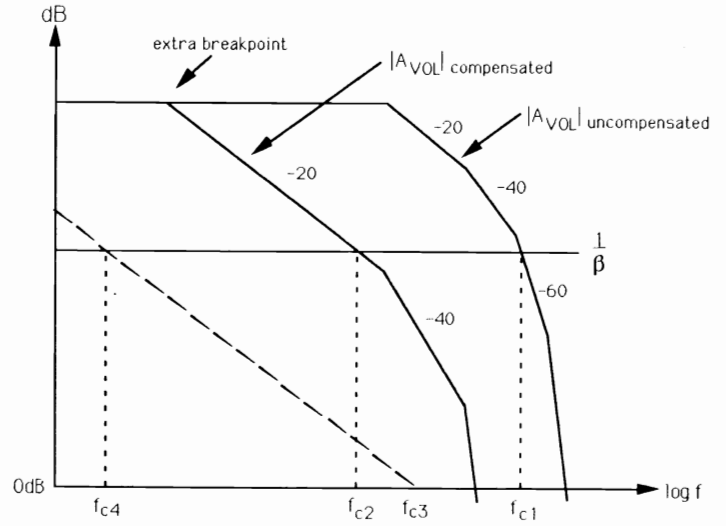
To predict the stability, we are interested in the behaviour of βA_{VOL} (the loop gain), and Nyquist requires that **when $|\beta A_{VOL}| = 1$, $\arg(\beta A_{VOL}) > -180°$.** In the Bode plot, $|\beta A_{VOL}|$ is the distance between $|A_{VOL}|$ and $\frac{1}{\beta}$, shown by the double-arrowed lines.

For frequency responses of the type we are likely to encounter with most amplifier circuits (minimum phase responses), there is a definite relationship between amplitude and phase responses. A +20dB/decade slope in the amplitude response always corresponds to 90° phase lead, and a -20dB/decade slope corresponds to 90° phase lag. So the phase margin can be estimated from the difference in slopes of $|A_{VOL}|$ and $\frac{1}{\beta}$ at their intersection (which must be where $|\beta A_{VOL}| = 1$). In the diagram this is 20dB/decade, (and would be for all values of β), so the phase margin is always 90° and this amplifier would be stable for all closed-loop gains. The closed-loop bandwidth $f_c = \beta f_0 = \frac{f_0}{A_{VCL}}$ where f_0 is the frequency where $|A_{VOL}| = 1$, the unity gain frequency of the amplifier.

Actual operational amplifiers can have three or more breakpoints (due to capacitances - mainly in transistors - in different parts of the circuit) before $|A_{VOL}|$ reaches 0dB and the closed-loop amplifier becomes more unstable as A_{VCL} is reduced (i.e. β increased). The following Bode diagram is for such an amplifier, and shows that the range of closed-loop gains at which it could be used would be quite limited. In practice, satisfactory transient response would be obtained only for gains greater than $\approx A_{VCL1}$.



The problem is solved by dominant pole compensation. A capacitor is added in the op. amp - usually from collector to base of the second stage transistor (the 10pF capacitor in the LF351 which we will be looking at soon), to introduce an extra breakpoint at a much lower frequency than the ones already there.

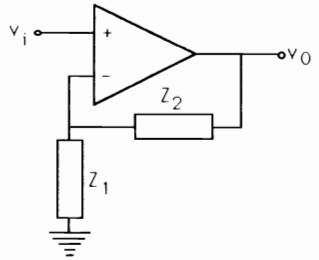


We can see in the Bode plot that the closed loop gain can now be lower than it was before. The $\frac{1}{\beta}$ line shown intersects the compensated open loop gain at -20dB/decade, but intersects the

uncompensated line at -60dB/decade where it would without doubt have been unstable. The amplifier still could not be used at unity gain - in order for this to be possible the dominant pole would have to be at a lower frequency as shown by the dotted line. In this unity gain case the closed loop bandwidth would be f_{c3}.

The penalty paid for stability is reduced closed-loop bandwidth, which is f_{c2} (compensated) compared with f_{c1} (uncompensated). The closed-loop bandwidth with the uncompensated amplifier is an academic point, though, as an unstable amplifier is not much use! If the dominant pole was at the frequency to allow unity gain operation, and the amplifier used at the gain A_{VCL}, the closed loop bandwidth would be reduced to f_{c4} - smaller than with the less severe compensation.

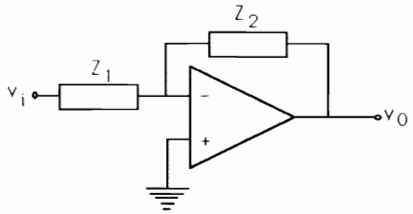
Non-inverting and inverting configurations

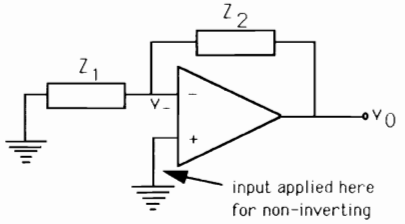


The preceding analysis was done for the non-inverting amplifier configuration, where the closed-loop response (for $\beta A_{VOL} >> 1$) was $\frac{1}{\beta}$.

Here, $\beta = \frac{v_-}{v_O} = \frac{Z_1}{Z_1 + Z_2}$ (put $v_i = 0$)

$$\left(\frac{v_O}{v_i}\right)_{noninverting} = \frac{Z_1 + Z_2}{Z_1} = \frac{1}{\beta}$$





In the inverting arrangement, the circuit topology is identical, with just the point at which the input is applied changed: the non-inverting input of the amplifier is now earthed, and the input is applied between the bottom of Z_1 and earth. Because the circuit is the same, β ($= \frac{Z_1}{Z_1 + Z_2}$) is the same. We now see that, for the inverting arrangement,

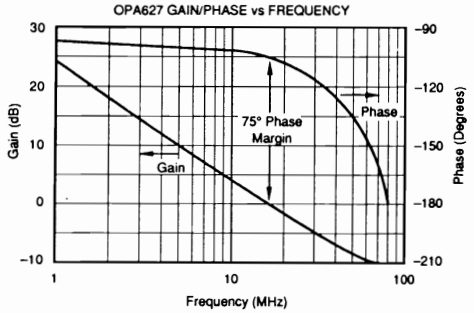
$$\left(\frac{v_O}{v_i}\right)_{inverting} = -\frac{Z_2}{Z_1} = 1 - \left(\frac{v_O}{v_i}\right)_{noninverting} = \mathbf{1 - \frac{1}{\beta}}$$

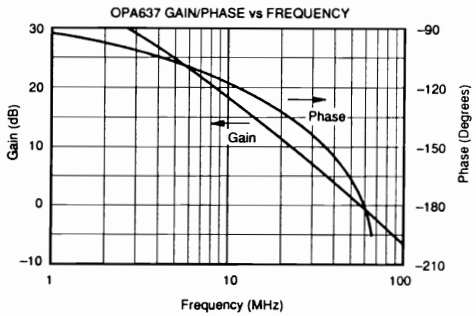
Commercially available operational amplifiers

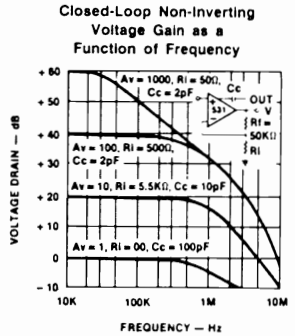
General purpose op. amps such as the LF351 and the older 741 have internal compensation for use down to unity gain. The LF351 has $f_0 = 4MHz$. Clearly this means that at higher closed-loop gains the bandwidth is less than it could be if the compensation were changed, but this is the penalty we pay for convenience - having one cheap op. amp which is as versatile as possible.

Other types are compensated so that they will operate stably only down to a certain closed-loop gain greater than 1, meaning that for a given gain the bandwidth is greater than it would have been

with unity gain compensation. These are described as 'decompensated'. Examples of a pair of otherwise similar op. amps differing in only in their compensation are the OPA627 (unity gain compensated, f_0 = 16MHz) and the OPA637 (minimum closed-loop gain = 5, f_0 = 60MHz). There are many other similar families. The open-loop responses of the OPA627 and OPA637 are compared here.



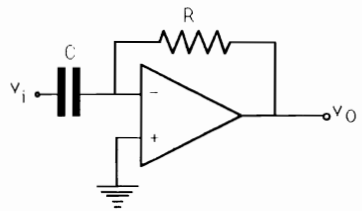


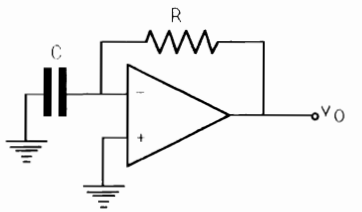


There are some op. amps where the compensation is provided by external capacitors and resistors (e.g. the NE531). This is the most flexible arrangement, but at the expense of complexity and the need for extra components. The plot here, taken from the data sheet for the NE531, shows the closed-loop response for different closed -loop gains, with a different value of compensation capacitor for each gain. Notice how the high frequency asymptotes are different for the different capacitors.

In general, op. amps are made so that they are as versatile as possible and can be used off the shelf in as many applications as possible. If an amplifier is being designed specifically for a particular application with a particular closed-loop transfer function, though, then the compensation would be optimised for that to achieve the best possible performance.

Stability of the differentiator circuit

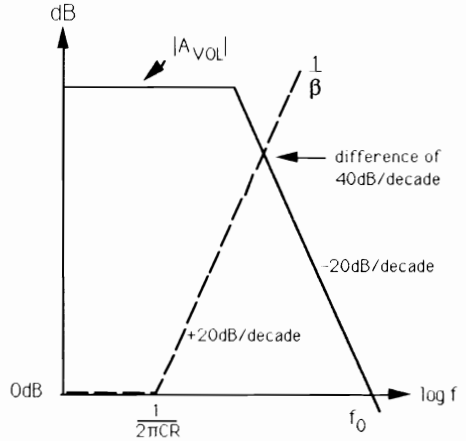




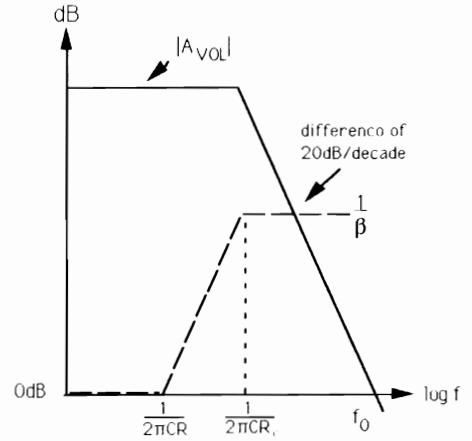
We are now in a position to see why the op. amp differentiator is intrinsically unstable. To investigate its stability, put $v_i = 0$, by shorting the input (right-hand diagram) and calculate β:-

$$\beta = \frac{v_-}{v_O} = \frac{1}{1+j\omega CR} \quad \text{so} \quad \frac{1}{\beta} = 1 + j\omega CR$$

This is plotted in the Bode diagram along with the amplifier open-loop response which, for clarity, has been assumed to have just a single breakpoint followed by a -20dB/decade rolloff. It is clear that the where the two lines intersect the difference in their slopes is -40dB/decade, so the phase, at loop gain unity will be approaching -180°. At best the closed-loop response will be very underdamped, and the effect of higher frequency lags (which will certainly be there in a real amplifier) will be to increase the phase lag and make it unstable.

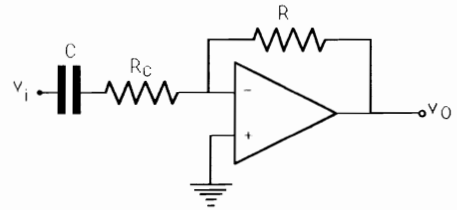


Uncompensated differentiator



Compensated differentiator

If a resistor R_c is put in series with the capacitor,



$$\beta = \frac{v_-}{v_O} = \frac{1 + j\omega CR_c}{1 + j\omega C(R + R_c)} \quad \text{so} \quad \frac{1}{\beta} = \frac{1 + j\omega C(R + R_c)}{1 + j\omega CR_c}$$

and this is plotted on the right-hand Bode diagram. As long as the frequency $\frac{1}{2\pi CR_c}$ is low enough, the asymptotes intersect with a slope difference of 20dB/decade, and the system is stable. If we knew f_0, we could estimate the value of R_c for a particular phase margin. It is easy to show that a similar result is achieved by putting a capacitor C_c in parallel with the resistor R.

The closed -loop response with compensation is

$$\frac{v_O}{v_i} = -\frac{j\omega CR}{1 + j\omega CR_c} \quad \text{compared with} \quad \frac{v_O}{v_i} = -j\omega CR \quad \text{for the ideal differentiator.}$$

So now the circuit operates as a differentiator only for frequencies less than $\omega = \frac{1}{CR_c}$.

TYPE LF351 OPERATIONAL AMPLIFIER

The LF351 is a general purpose operational amplifier with FET input. It has come to replace the older 741 generation of op. amps - it has a wider bandwidth, and the FET input gives it a higher input impedance. By looking at the information provided on the manufacturer's data sheet we will analyse as much of the circuit as we can.

The simplified circuit diagram gives the basic structure of the circuit. A differential pair of JFETs, with a current mirror load feeds a common emitter amplifier stage, with a capacitor from collector to base to introduce a dominant pole into the frequency response. This stage has a constant current load and is then connected to a complementary emitter follower output stage.

LF351

National Semiconductor

LF351 Wide Bandwidth JFET Input Operational Amplifier

General Description

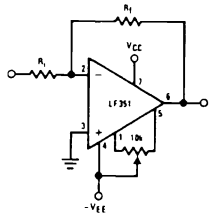
The LF351 is a low cost high speed JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF351 is pin compatible with the standard LM741 and uses the same offset voltage adjustment circuitry. This feature allows designers to immediately upgrade the overall performance of existing LM741 designs.

The LF351 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift, but for applications where these requirements are critical, the LF356 is recommended. If maximum supply current is important, however, the LF351 is the better choice.

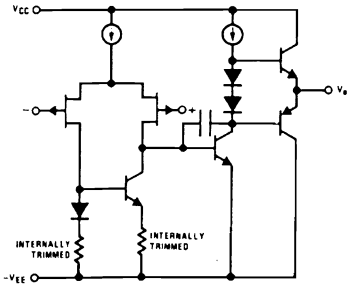
Features

■ Internally trimmed offset voltage	10 mV
■ Low input bias current	50 pA
■ Low input noise voltage	25 nV/√Hz
■ Low input noise current	0.01 pA/√Hz
■ Wide gain bandwidth	4 MHz
■ High slew rate	13 V/μs
■ Low supply current	1.8 mA
■ High input impedance	$10^{12}\Omega$
■ Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20$ Vp-p, BW = 20 Hz–20 kHz	<0.02%
■ Low 1/f noise corner	50 Hz
■ Fast settling time to 0.01%	2 μs

Typical Connection

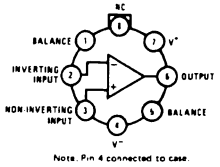


Simplified Schematic



Connection Diagrams (Top Views)

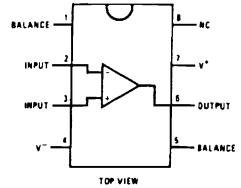
Metal Can Package



Note: Pin 4 connected to case.

Order Number LF351H
See NS Package Number H08C

Dual-In-Line Package

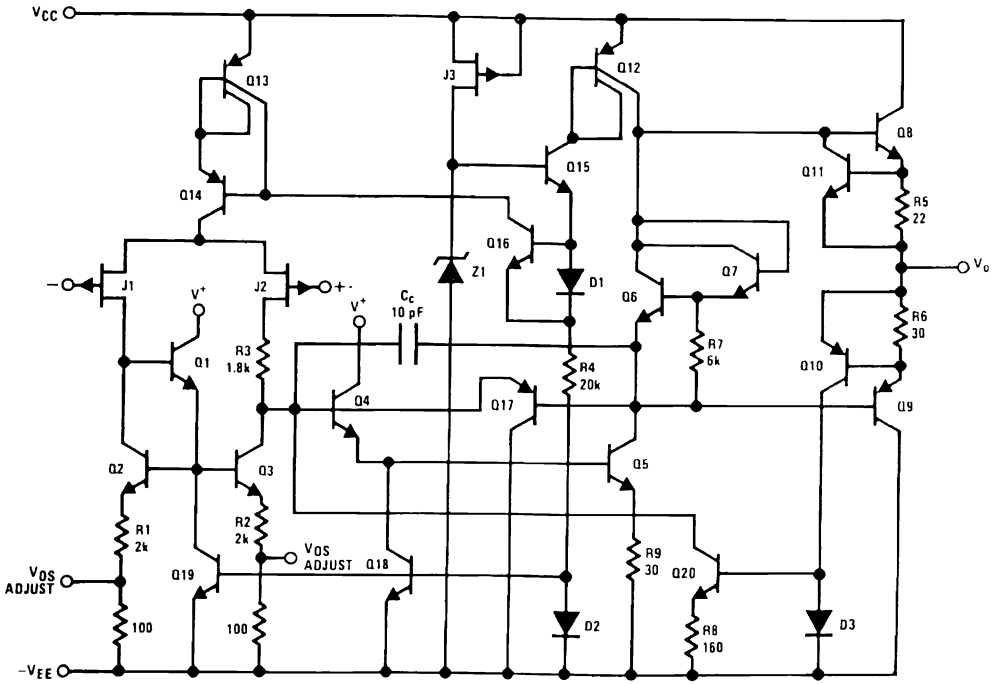


TL/H/5648-1

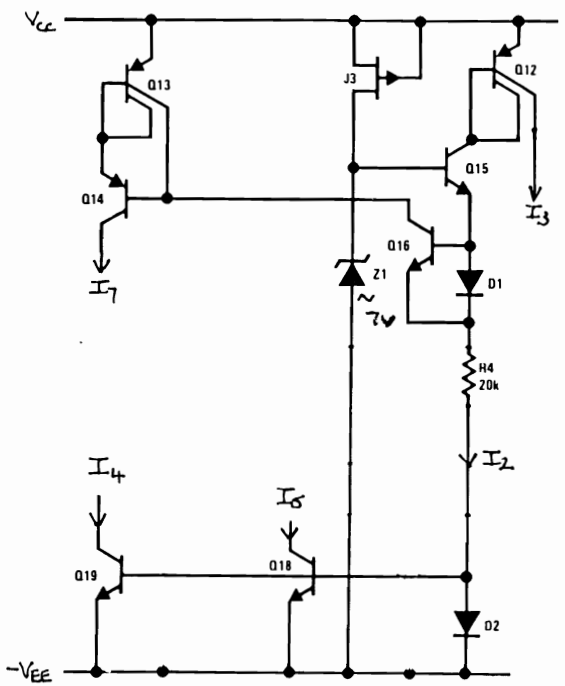
Order Number LF351M or LF351N
See NS Package Number M08A or N08E

We shall now look at the detailed circuit diagram and separate the various functional blocks of the circuit.

Detailed Schematic



1. Current sources to provide bias



J_3 is a p-channel FET connected as a current source providing a constant current I_1, which feeds the zener diode Z_1. If the zener diode is about 7V, this sets Q_{15} base 7V above V_{EE} and Q_{15} emitter about 6.4V above V_{EE}. If D_1 and D_2 each drop 0.6V, 2.6V is left across R_4, making I_2 about 260µA. I_2 is independent of V_{CC} - V_{EE}, the total supply voltage, which may be anything between 8V and 36V. As I_2 forms the reference current for current mirrors supplying the various parts of the circuit this ensures that the device operating currents (and hence the performance of the op.amp - e.g. its gain) are independent of supply voltage.

The different current mirrors work from I_2 as follows:-

D_2 and Q_{19} mirrors I_2 to give constant I_4

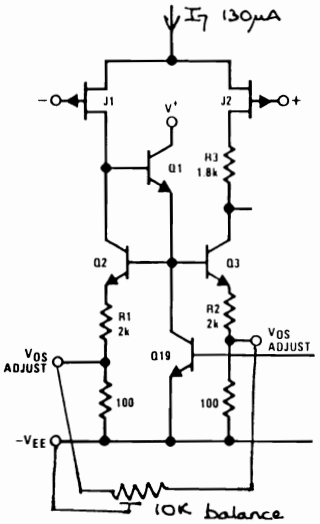
D_2 and Q_{18} mirrors I_2 to give constant I_5

D_1 and Q_{16} form a current mirror, each carrying half of I_2, so I_6 = 130µA and the current in Q_{15} and Q_{12} is also 130µA.

Q_{12} mirrors this 130µA to give constant I_3

Q_{13} and Q14 form a Wilson current mirror controlled by I_6 to give I_7 = 130µA. A Wilson mirror is probably used here to ensure good CMRR in the input stage

2. Input stage



J_1 and J_2 are p-channel JFETs, and form a long-tailed pair, with tail current $I_7 \approx$ 130µA. The drain current in each transistor will thus be only ≈ 65µA, so that g_m will be low, perhaps around 250µS (g_m in a JFET gets less as I_D is reduced - check this from the square-law expression).

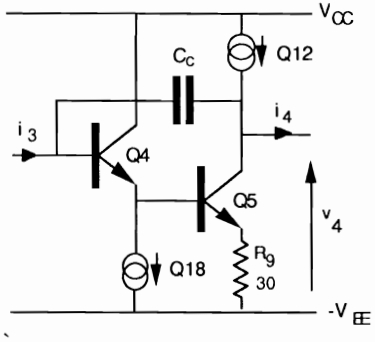
Q_2, Q_3 and Q_1 form a current mirror load that reflects the drain current of J_1 at Q_3 collector. If a differential input $v_{in} = (v_+ - v_-)$ is applied, then

$$i_2 = \frac{g_m}{2} v_{in}, \quad i_1 = -\frac{g_m}{2} v_{in}$$

The current i_1 is reflected at the collector of Q_3, so the output current $i_3 = i_2 - i_1 = g_m v_{in}$. The current mirror doubles the gain over that with a simple load.

The 10kΩ balance potentiometer varies the emitter resistors of Q_2 and Q_3 by a small amount, varying the balance of the currents in J_1 and J_2. This is to correct input offset voltage due to transistor mismatch.

3. Second stage

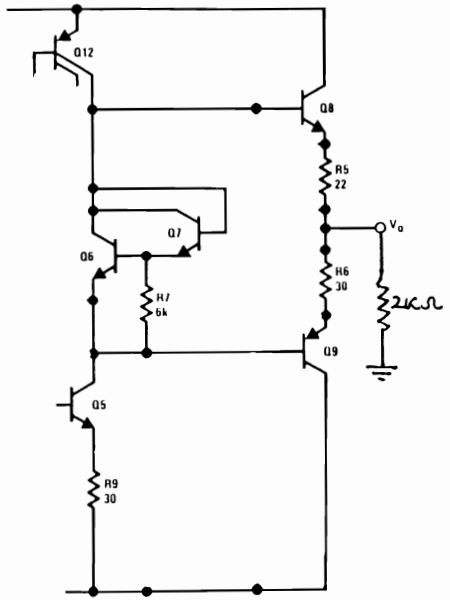


Q_4 and Q_5 form a high current gain pair, similar to a Darlington pair. The current source Q_{12} is a high impedance load for Q_5.

Because of the high current gain, the input resistance at the base of Q_4 will be very high, so at all but the lowest frequencies, there will be an easier path for i_3 through C_c, and the voltage (incremental) at Q_5 collector will be $v_4 = -\frac{i_3}{j\omega C_c}$.

At low frequencies and d.c., the reactance of C_c is high so i_3 flows into Q_4 base and then $i_4 = -h_{fe4}h_{fe5}\, i_3$. The voltage output v_4 will be given by i_4 flowing into the input resistance of the following stage.

4. Output stage



Q_8 and Q_9 form a complementary emitter follower pair, working in class AB with Q_6 and Q_7 providing bias to overcome crossover distortion - the voltage between Q_8 and Q_9 bases will be about 1.2 -1.3V. The 22Ω and 30Ω resistors are to stabilise the quiescent current in Q_8 and Q_9 and also form part of the protection circuitry.

The voltage gain of this stage is unity. Assume h_{fe} for the transistors is 100. Then, with a 2kΩ load (the condition given in the data sheet), the input resistance will be approximately h_{fe} x 2kΩ = 200kΩ. h_{ie} is negligible in comparison.

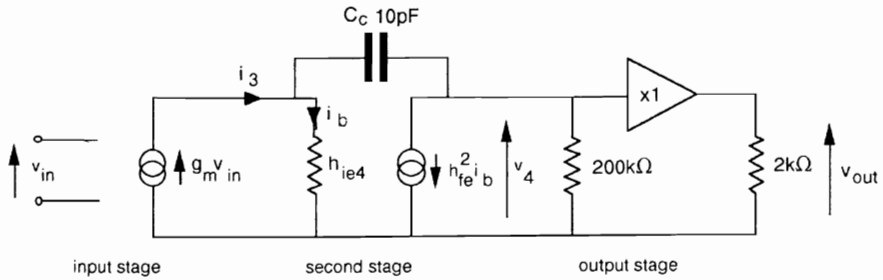
5. Protection

Positive output current limiting is provided by R_5 and Q_{11}. (See the detailed circuit diagram). If the voltage across R_5 exceeds 0.6V, corresponding to an output current of $\frac{0.6V}{22\Omega} \approx$ 27mA, Q_{11} turns on and takes the base current away from Q_8.

Negative output current limiting is slightly more complicated. An output current of ≈ -20mA develops a voltage of 0.6V across R_6 which turns on Q_{10}. The current in Q_{10} is mirrored by D_3 and Q_{20} and this starves Q_4 of base current. Q_{17} also takes the base current of Q_4 if V(Q_4 base) - V(Q_5 collector) > 0.6V under overload which might arise if the common-mode input limit is exceeded.

The data sheet gives the current limits as 20mA and 18mA respectively

Open-loop gain



As $\omega \to 0$, $\frac{v_4}{i_3} = -h_{fc}^2 \times 200k\Omega = -2 \times 10^9\ \Omega$ (taking $h_{fc} = 100$)

So $v_{out} = g_m v_{in} \times -2 \times 10^9$ giving $\frac{v_{out}}{v_{in}} = 250 \times 10^{-6} \times 2 \times 10^9 = 5 \times 10^5$ (114dB)

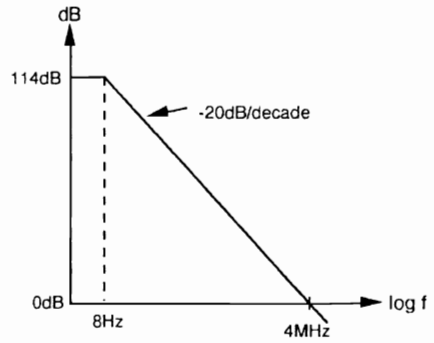
The data sheet gives the d.c. gain as typically 10^5.

As $\omega \to \infty$, $\frac{v_4}{i_3} = -\frac{1}{j\omega C_c}$

So $v_{out} = g_m v_{in} \times -\frac{1}{j\omega C_c}$ giving $\frac{v_{out}}{v_{in}} = -\frac{g_m}{j\omega C_c} = -\frac{2.5 \times 10^7}{j\omega}$ i.e. $\left|\frac{v_{out}}{v_{in}}\right| = \frac{2.5 \times 10^7}{\omega}$

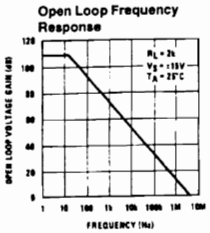
We see from this that the unity gain frequency is $\omega_{()} = 2.5 \times 10^7$rad/s, or $f_0 = 3.98$MHz - it is given in the data sheet as 4MHz!

Plotting these two asymptotes on a Bode diagram,



Thus the dominant pole is at about 8Hz, and the gain decreases continuously above this frequency. As the amplifier is be unity gain stable, we would not expect to see any higher frequency poles below about 4MHz.

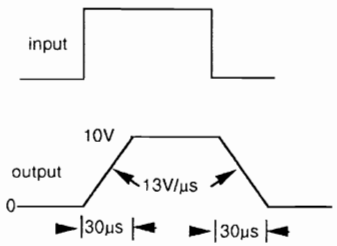
From the data sheet:-



Slew rate

The slew rate is limited by the current available to charge the capacitor C_c. The voltage at the left hand end of C_c is almost constant at about 1.2V above V_{EE}, and the voltage at its other end is is equal to the output voltage. This means that $\frac{dv_{out}}{dt} = \frac{dVC_c}{dt}$. So $C_c \frac{dv_{out}}{dt}$ is equal to the current in C_c. The current into C_c comes from the input stage (i_3 in the diagram of the second stage) and cannot exceed I_T, which is 130μA. So

$$\left(\frac{dv_{out}}{dt}\right)_{max} = \pm\frac{I_T}{C_c} = \pm\frac{130\mu A}{10pF} = \pm 13V/\mu s \quad \text{as in the data sheet.}$$



A rectangular pulse would be distorted like this by slew-rate limiting.

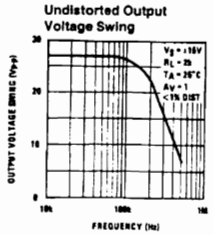
When the amplifier slew rate limits, the output is no longer in the control of the input, and the feedback loop is temporarily broken.

Slew rate limiting determines the power bandwidth which is the highest frequency sine wave at which the amplifier can deliver its maximum voltage output swing. For a sine wave output signal $v_{out} = V_p \sin\omega t$ and $\frac{dv_{out}}{dt} = \omega V_p \cos\omega t$ - this has a maximum value ωV_p at the sine wave's zero crossing point. For no slew rate distortion, $\omega V_p \le \left(\frac{dv_{out}}{dt}\right)_{max}$ or $2\pi f V_p \le \left(\frac{dv_{out}}{dt}\right)_{max}$.

Given that the maximum output voltage swing the LF351 can deliver (with power supplies of ±15V) is ±13.5V, the highest frequency for no slew rate distortion will be

$$f_{max} = \frac{\left(\frac{dv_{out}}{dt}\right)_{max}}{2\pi V_p} = \frac{1}{2\pi}\frac{13V/\mu s}{13.5V} = 153kHz$$

This is in good agreement with the plot on the data sheet which suggests a full power bandwidth of a little over 100kHz.



At 1MHz the maximum undistorted output is down to 2V peak.

The whole manufacturer's data sheet for the LF351 is reproduced on the following pages.

National Semiconductor

LF351 Wide Bandwidth JFET Input Operational Amplifier

General Description

The LF351 is a low cost high speed JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF351 is pin compatible with the standard LM741 and uses the same offset voltage adjustment circuitry. This feature allows designers to immediately upgrade the overall performance of existing LM741 designs.

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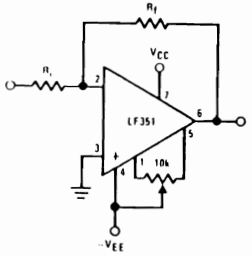
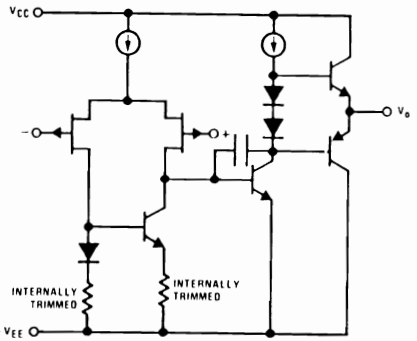
Features

- Internally trimmed offset voltage — 10 mV
- Low input bias current — 50 pA
- Low input noise voltage — 25 nV/$\sqrt{Hz}$
- Low input noise current — 0.01 pA/$\sqrt{Hz}$
- Wide gain bandwidth — 4 MHz
- High slew rate — 13 V/μs
- Low supply current — 1.8 mA
- High input impedance — $10^{12}\Omega$
- Low total harmonic distortion A_V = 10, R_L = 10k, V_O = 20 Vp-p, BW = 20 Hz–20 kHz — ≤0.02%
- Low 1/f noise corner — 50 Hz
- Fast settling time to 0.01% — 2 μs

Typical Connection

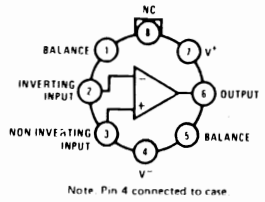


Simplified Schematic



Connection Diagrams (Top Views)

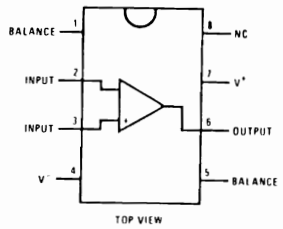
Metal Can Package



Note: Pin 4 connected to case.

Order Number LF351H
See NS Package Number H08C

Dual-In-Line Package



TL/H/5648-1

Order Number LF351M or LF351N
See NS Package Number M08A or N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	± 18V
Power Dissipation (Notes 1 and 6)	670 mW
Operating Temperature Range	0°C to + 70°C
$T_{j(MAX)}$	115°C
Differential Input Voltage	± 30V
Input Voltage Range (Note 2)	± 15V
Output Short Circuit Duration	Continuous
Storage Temperature Range	65°C to + 150°C
Lead Temp. (Soldering, 10 sec.)	
Metal Can	300°C
DIP	260°C

	H Package	N Package	M Package
θ_{jA}	164°C/W (Still Air) 66°C/W (400 LF/min Air Flow)	120°C/W	TBD
θ_{jC}	21°C/W		

Soldering Information
- Dual-In-Line Package
  - Soldering (10 sec.) — 260°C
- Small Outline Package
  - Vapor Phase (60 sec.) — 215°C
  - Infrared (15 sec.) — 220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating to be determined.

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	LF351 Min	LF351 Typ	LF351 Max	Units
V_{OS}	Input Offset Voltage	R_S = 10 kΩ, T_A = 25°C Over Temperature		5	10 13	mV mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S = 10 kΩ		10		μV/°C
I_{OS}	Input Offset Current	T_j = 25°C, (Notes 3, 4) $T_j \leq$ 70°C		25	100 4	pA nA
I_B	Input Bias Current	T_j = 25°C, (Notes 3, 4) $T_j \leq$ 70°C		50	200 8	pA nA
R_{IN}	Input Resistance	T_j = 25°C		10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S = ± 15V, T_A = 25°C V_O = ± 10V, R_L = 2 kΩ Over Temperature	25 15	100		V/mV V/mV
V_O	Output Voltage Swing	V_S = ± 15V, R_L = 10 kΩ	± 12	± 13.5		V
V_{CM}	Input Common-Mode Voltage Range	V_S = ± 15V	± 11	+ 15 − 12		V V
CMRR	Common-Mode Rejection Ratio	$R_S \leq$ 10 kΩ	70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 5)	70	100		dB
I_S	Supply Current			1.8	3.4	mA

AC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	LF351			Units
			Min	Typ	Max	
SR	Slew Rate	$V_S = \pm 15V$, $T_A = 25°C$		13		V/μs
GBW	Gain Bandwidth Product	$V_S = +15V$, $T_A = 25°C$		4		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, $f = 1000$ Hz		25		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$T_j = 25°C$, $f = 1000$ Hz		0.01		$pA/\sqrt{Hz}$

Note 1: For operating at elevated temperature, the device must be derated based on the thermal resistance, θ_{jA}.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: These specifications apply for $V_S = \pm 15V$ and $0°C \leq T_A \leq +70°C$. V_{OS}, I_B and I_{OS} are measured at $V_{CM} = 0$.

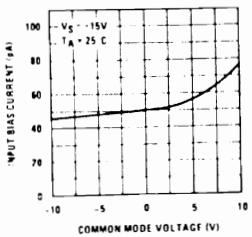
Note 4: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to the limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 5: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. From $\pm 15V$ to $\pm 5V$.

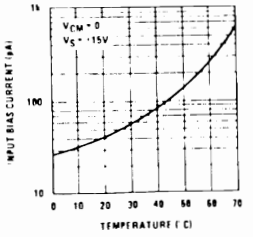
Note 6: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

Typical Performance Characteristics

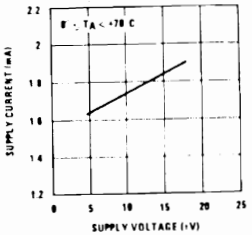
Input Bias Current



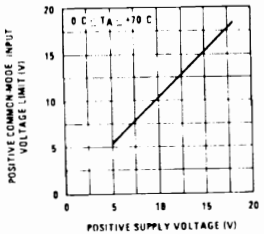
Input Bias Current



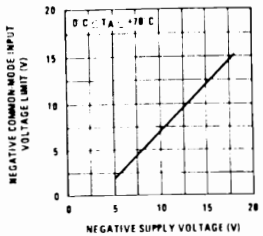
Supply Current



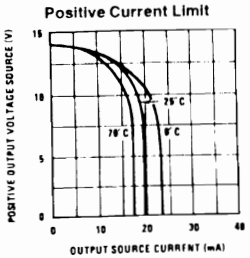
Positive Common-Mode Input Voltage Limit



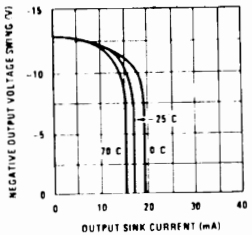
Negative Common-Mode Input Voltage Limit



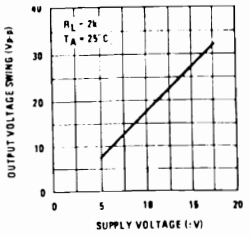
Positive Current Limit



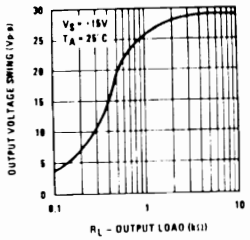
Negative Current Limit



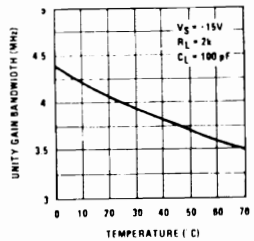
Voltage Swing



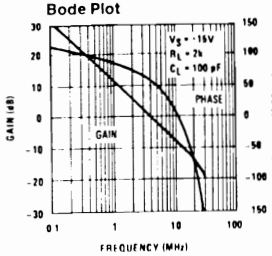
Output Voltage Swing



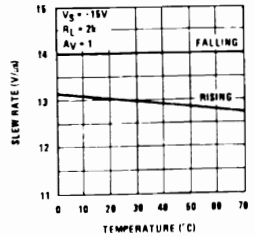
Gain Bandwidth



Bode Plot



Slew Rate



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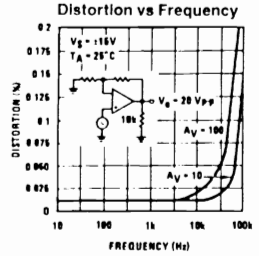
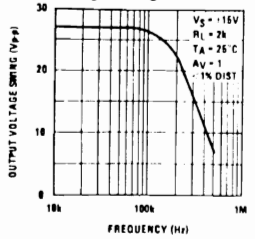
Typical Performance Characteristics (Continued)

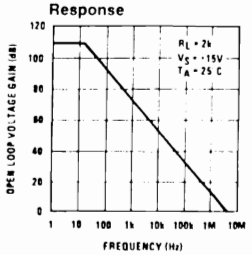
Distortion vs Frequency



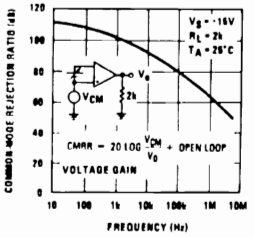
Undistorted Output Voltage Swing



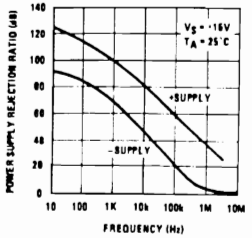
Open Loop Frequency Response



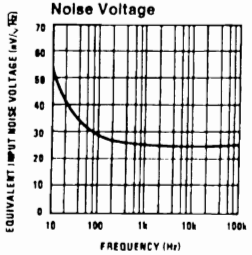
Common-Mode Rejection Ratio



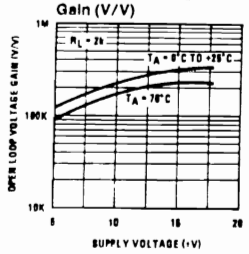
Power Supply Rejection Ratio



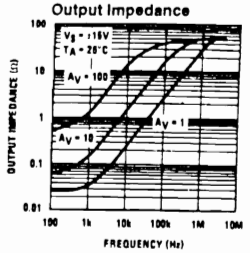
Equivalent Input Noise Voltage



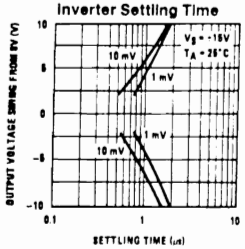
Open Loop Voltage Gain (V/V)



Output Impedance



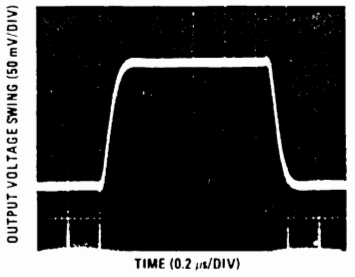
Inverter Settling Time



TL/H/5648–3

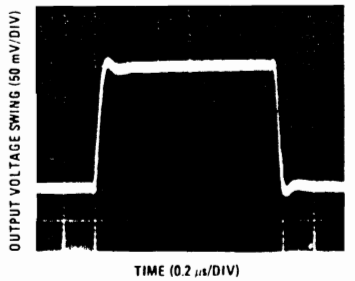
Pulse Response

Small Signal Inverting



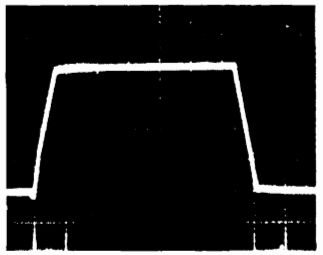
TL/H/5648–4

Small Signal Non-Inverting



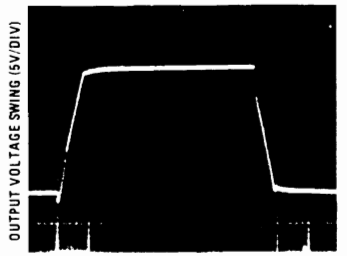
TL/H/5648–5

Large Signal Inverting



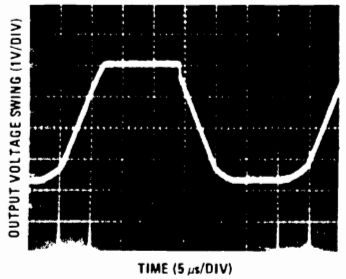
TL/H/5648–6

Large Signal Non-Inverting



TL/H/5648–7

Current Limit (R_L = 100Ω)



TL/H/5648–8

Application Hints

The LF351 is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II™). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output.

Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the

Application Hints (Continued)

common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 4V of the negative supply, an increase in input offset voltage may occur.

The LF351 is biased by a zener reference which allows normal circuit operation on ±4V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

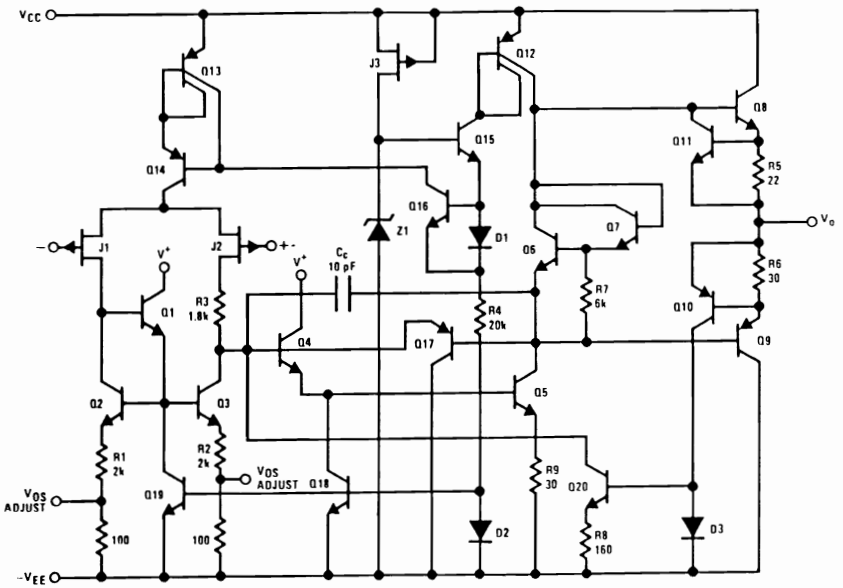
The LF351 will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

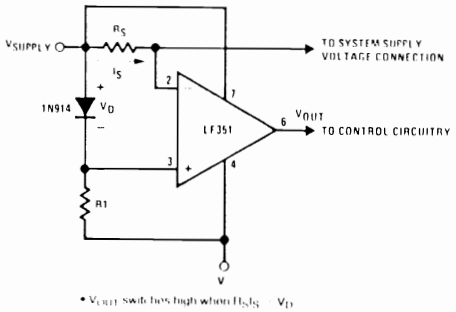
Detailed Schematic



TL/H/5648-9

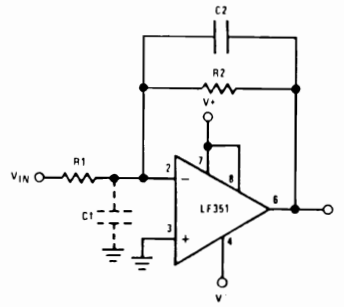
Typical Applications

Supply Current Indicator/Limiter



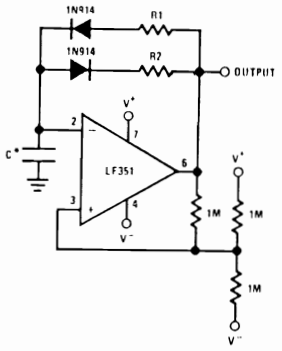
• V_{OUT} switches high when $I_S R_S \geq V_D$

Hi-Z_{IN} Inverting Amplifier



Parasitic input capacitance C1 ≈ (3 pF for LF351 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate, add C2 such that R2C2 ≈ R1C1.

Ultra-Low (or High) Duty Cycle Pulse Generator



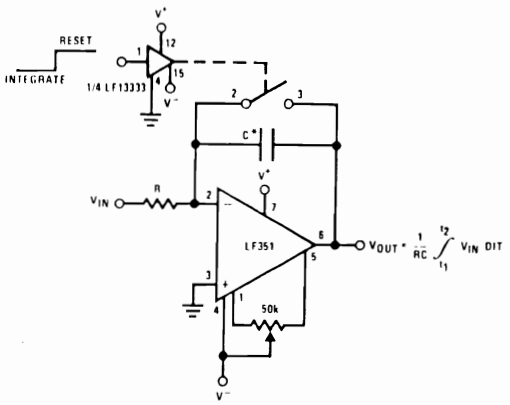
• $f_{OUTPUT\ HIGH} \approx \frac{1}{R1C\ ln\frac{4.8 - 2V_S}{4.8 - V_S}}$

• $f_{OUTPUT\ LOW} \approx \frac{1}{R2C\ ln\frac{2V_S - 7.8}{V_S - 7.8}}$

where $V_S = V^+ + |V^-|$

*low leakage capacitor

Long Time Integrator



TL/H/5648-10

*Low leakage capacitor

• 50k pot used for less sensitive V_{OS} adjust

CURRENT FEEDBACK OPERATIONAL AMPLIFIERS

A fundamental limitation of the conventional operational amplifier

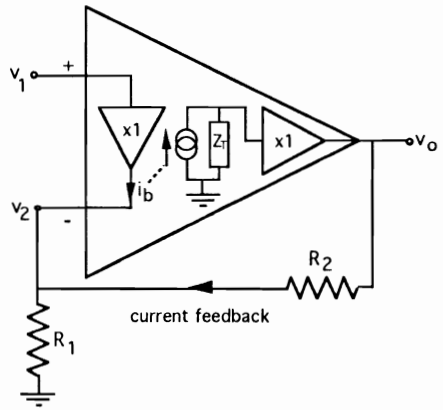
Conventional operational amplifiers are essentially high gain voltage amplifiers with negative feedback defining the closed loop gain, and to a first order approximation the closed loop bandwidth is inversely proportional to the closed loop gain (the gain-bandwidth concept which we have seen in the previous section). We saw that this was an inevitable consequence of the dominant pole compensation which was necessary for stability.

The need for such compensation arises directly from the fact that in a high gain differential voltage amplifier there are large internal voltage swings within the device, usually at high impedance nodes such as transistor collectors. Collector-base capacitance in such transistors gives local frequency-dependent feedback, which tends to reduce gain, with an associated phase lag, as frequency increases. In a multi-stage amplifier this happens in each stage, giving a number of poles in the open loop response. The slew rate is also limited by the current available to charge and discharge the compensation capacitor.

Current mode operational amplifiers were first proposed as a solution to this limitation in the early 1980s, but the idea was slow to catch on, and devices were not being widely manufactured until later in the decade.

Principle of the current mode amplifier

If the pin connections of a typical current mode amplifier are compared with those of a standard op-amp, the two appear very similar. Even circuits using the two kinds of amplifier look similar. Don't be misled - the two are actually very different in their construction and mode of operation.



The diagram shows the essential features of a current mode amplifier with external resistors connected to make a non-inverting amplifier. It comprises three sections. The first is a unity gain voltage buffer whose high impedance input is connected as the non-inverting input, and whose output forms the 'inverting input'. The current flowing through the buffer's output terminal is sensed by a current mirror (the second stage) whose output feeds into an impedance Z_T (which will usually be a resistor with some stray capacitance in parallel) and the resulting voltage appears, via a unity gain buffer (the third stage), at the output terminal. The philosophy of the design is that current is sensed in the input buffer, and the amplification takes place by the current mirror having

a large transfer ratio, and Z_T being large. There are no internal nodes with large voltage swings on them where collector-base capacitance would be important.

Comparison between current mode amplifiers and conventional operational amplifiers

In the circuit of the previous section the output voltage v_o is given by

$$v_o = Z_T\, i_b.$$

Summing currents at the inverting input, where the voltage v_2 is forced by the buffer between the inputs to be equal to the input voltage v_1 gives

$$\frac{v_o - v_1}{R_2} - \frac{v_1}{R_1} + i_b = 0$$

and if these two expressions are combined we get

$$\frac{v_o - v_1}{R_2} - \frac{v_1}{R_1} + \frac{v_o}{Z_T} = 0,$$

leading to

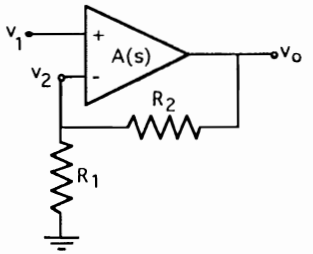
$$\frac{v_o}{v_1} = \frac{R_1 + R_2}{R_1} \cdot \frac{Z_T}{R_2 + Z_T}.$$

Remembering that Z_T is complex and a function of frequency and should so be written $Z_T(s)$, then

$$\frac{v_o}{v_1} = \mathbf{G} \cdot \frac{\mathbf{Z_T(s)}}{\mathbf{R_2 + Z_T(s)}} \quad \text{where} \quad G = \frac{R_1 + R_2}{R_1}, \text{ the desired gain.}$$

and if $R_2 \ll Z_T$, $\frac{v_o}{v_1} = G$ which is the same result as for an ideal conventional operational amplifier.

Now recall the results for a conventional op-amp with a frequency dependent open loop gain A(s).



As we saw before,

$$\frac{v_o}{v_1} = \frac{A(s)}{1 + \frac{R_1}{R_1 + R_2} A(s)} = \frac{A(s)}{1 + \frac{A(s)}{G}}$$

$$= \mathbf{G} \cdot \frac{\mathbf{A(s)}}{\mathbf{G + A(s)}}$$

and when $A(s) \gg G$, $\frac{v_o}{v_1} = G$ as we know.

Both bold expressions for closed loop gain are of the form G multiplied by a frequency dependent term which arises from the open loop gain. Looking at their denominators (whose roots are the closed-loop poles), we see an important difference. In the case of the conventional op-amp, G appears in the denominator, meaning that if G is changed, the closed loop poles are also changed, - the bandwidth unavoidably depends on the closed loop gain. In contrast, in the case of the current mode amplifier, only R_2 appears in the denominator - so if R_2 is kept the same, the frequency response remains the same whatever the value of R_1. Therefore, varying the value of R_1 changes only the gain and does not affect the bandwidth.

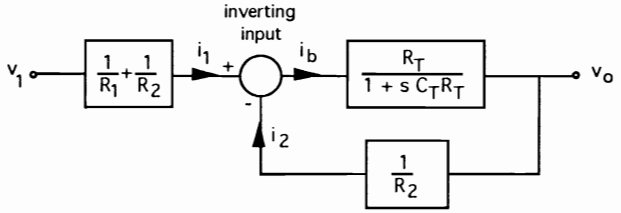
The model we have used for the current mode amplifier is admittedly rather simplified and idealized and we shall refine it soon, but it has served to show the basic differences from a conventional operational amplifier. The key points to have emerged so far are

1) Because of the different internal circuit topology, where gain is achieved by current rather than voltage amplification, the effect of device capacitances is minimized, with the result that the amplifier has a wider open loop bandwidth.

2) Because a difference between currents is taken at the 'inverting input', with the difference current forming the input to the amplifier, the voltage at this point is constant and equal to the input voltage ($v_2 = v_1$) and so R_1 has no effect on the feedback current flowing through R_2. This current is just $\frac{v_o - v_1}{R_2}$. Therefore R_1 plays no part in the feedback loop.

   In contrast, in a conventional op-amp circuit the voltage at the inverting input depends on the ratio of R_1 and R_2 and so changing either resistor affects the loop gain.

The second point can be seen very clearly if the current mode amplifier circuit is redrawn in the form of a conventional feedback system:-



$$i_1 = v_1\left(\frac{1}{R_1} + \frac{1}{R_2}\right)$$

$$i_2 = \frac{v_2}{R_2}$$

Z_T has been represented as a resistor R_T in and a capacitor C_T in parallel and forms the forward path of the feedback loop, with current feedback via R_2. The feedback current i_2 is subtracted from the input current i_1 at the 'inverting input' node. It is easy to see that R_1 is outside the feedback loop, and merely affects the ratio of i_1 to v_1 and hence the overall gain.

Analysis of this circuit gives for the voltage gain

$$\frac{v_o}{v_1} = \frac{R_1 + R_2}{R_1} \cdot \frac{R_T}{R_T + R_2} \cdot \frac{1}{1 + sC_T\frac{R_TR_2}{R_T + R_2}}$$

which of course is the same as would be obtained if the expression for Z_T were substituted in the equation in bold type in the previous section. If we take $R_T \gg R_2$, we get the interesting result

$$\frac{v_o}{v_1} = \frac{R_1 + R_2}{R_1} \cdot \frac{1}{1 + sC_T R_2}$$

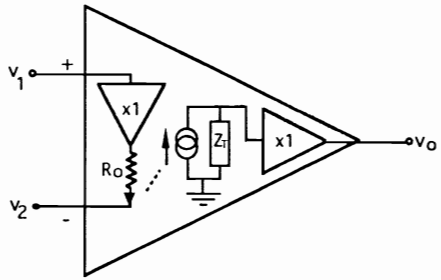
The bandwidth is fixed just by the internal capacitance and R_2.

This then is an important difference in circuit behaviour between current mode amplifiers and conventional operational amplifiers. The feedback resistor controls frequency response, and in practice there is usually a recommended value of R_2. The gain can then be set with R_1.

Effect of follower output resistance

The model of the amplifier can be further refined by taking into account the output resistance of the unity gain buffer between the inputs. We are used to assuming that unity gain buffers have a negligibly low output resistance when they are made with op-amps. In current-mode circuits, to get

a wide bandwidth and avoid slew rate limitation, a simple complementary emitter follower is usually employed. The output resistance may well be a few tens of ohms (the manufacturers, Analog Devices quote 60Ω for the OP-160) and this needs to be included in the amplifier model, as in the following diagram



When this is substituted for the simpler model in the non-inverting amplifier circuit which we analysed previously, the expression for the voltage gain becomes

$$\frac{v_o}{v_i} = \frac{R_1 + R_2}{R_1} \frac{1}{1 + \frac{1}{R_T}\left(R_o\frac{R_1 + R_2}{R_1} + R_2\right) + s\left(R_2 + \frac{R_1 + R_2}{R_1}R_o\right)C_T}$$

which, if $R_T \gg R_o$ and $R_T \gg R_2$ (quite realistic assumptions), reduces to

$$\frac{v_o}{v_i} = \frac{R_1 + R_2}{R_1} \frac{1}{1 + s\left(R_2 + \frac{R_1 + R_2}{R_1}R_o\right)C_T}$$

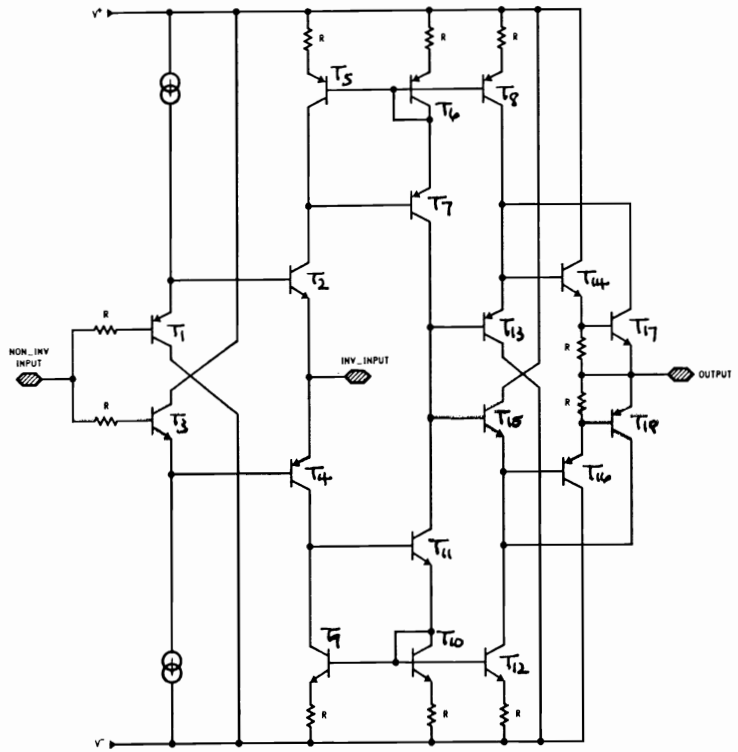
Comparing this with the expression in the previous section, we see that, in the time constant multiplying s, R_2 has been replaced by $R_2 + \frac{R_1 + R_2}{R_1}R_o$ which is $R_2 + GR_o$, G being the closed loop gain. Check the derivation of these expressions for yourself.

For small values of G, when $GR_o \ll R_2$, the result reduces, as we would expect, to that of the previous section, where R_o was taken as zero. As G becomes larger, the second term in the bracket becomes significant, and the bandwidth does begin to reduce and is no longer independent of G. In reality, as we shall see when we look at data for an actual amplifier, for moderate closed loop gains, the falloff in bandwidth with gain is still very much less than with a conventional op-amp.

The frequency response is also modified by unavoidable stray capacitance from the 'inverting input' node to ground which effectively shunts R_1, putting a zero in the closed loop response and causing the response to rise at high frequencies. This can sometimes be put to profitable use - see the frequency response plots of an actual amplifier.

The internal circuit of a current mode amplifier

The diagram is taken from the manufacturer's data sheet for the National Semiconductors LM6181 and is a simplified version of the circuit of the device. The LM6181 is described as a '100 MHz current feedback operational amplifier'. The three sections of the circuit are labelled.



The input stage is a unity gain emitter follower arrangement, with T_2 and T_4 forming a class AB (it looks like a class B, but the details have probably been omitted) output stage to the 'inverting input'. For positive-going signals T_2 is fed from the non-inverting input via T_1; the diode drops in the base-emitter junctions of these transistors cancel, giving approximately zero d.c. offset between input and output. Similarly for negative-going signals T_4 is fed from the input via T_3, with base-emitter drops in T_3, and T_4 cancelling.

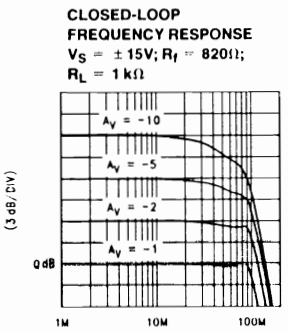
Current flowing through the 'inverting input' is sensed by either the top current mirror (T_5, T_6, T_7 and T_8) or the bottom current mirror (T_9, T_{10}, T_{11} and T_{12}). When current flows out of the 'inverting input' it is supplied through T_2 and T_5, with T_8 mirroring it to drive base current into T_{14} the top output emitter follower. At the same time, the increased current in T_7 drives T_{15} which reduces the drive to T_{16}, the bottom output emitter follower. This 'push-pull' action gives an increased output slew rate. When current flows into the 'inverting input' the lower half of the transimpedance stage works in a similar (but opposite) way to turn T_{16} on and turn T_{15} off .

The transimpedance is formed by the output of the current mirror feeding into the input impedance of the output stage. As this stage comprises emitter followers, its input impedance is a multiple of the load connected to the output terminal, with the result that transimpedance is affected by the load. Amplifier characteristics in the data sheets are usually given for a specified load, therefore. Also the current mirror may possibly have a magnification, achieved by forming it with transistors of different areas.

Some data for a typical current mode amplifier

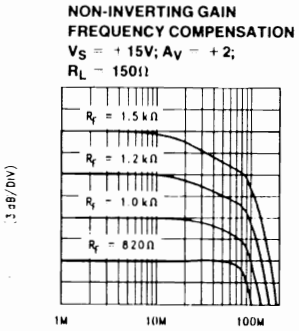
This is all taken from the data sheet for the National Semiconductors LM6181

FREQUENCY RESPONSE FOR DIFFERENT GAINS WITH THE SAME VALUE OF R_2



Responses are plotted for a range of gains from 1 to 10 inverting (the usual inverting circuit, with the input in series with the bottom of R_1 and the non-inverting input grounded). The value of R_2 is that recommended as optimum by the manufacturer. The response does vary, but very much less than it would with a conventional op-amp. At a gain of -1 the -3dB point is at 100 MHz, and when the gain has been increased to -10 (by changing R_1), the -3dB point has reduced to about 55 MHz. The bandwidth has reduced by a factor of less than 2 - with a conventional voltage feedback op-amp it would have reduced by a factor of 10.

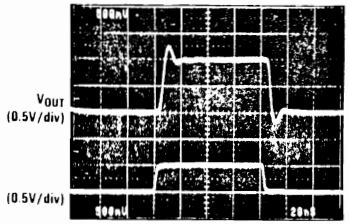
FREQUENCY RESPONSE WITH DIFFERENT VALUES OF R_2



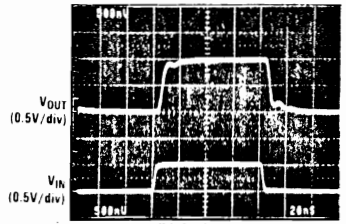
Here we see the response for a non-inverting gain of 2 for a range of values of R_2, from the optimum value of 820Ω up to 1.5kΩ. The bandwidth reduces as R_2 is increased. The effect of reducing R_2 below 820Ω is not shown - in fact it would lead to a response which peaked at the high frequency end before rolling off. This could be exploited to extend the bandwidth at higher gains - it could significantly reduce the droop in the above plot for a gain of 10, for example. See the third step response below.

STEP RESPONSE WITH DIFFERENT VALUES OF R_2

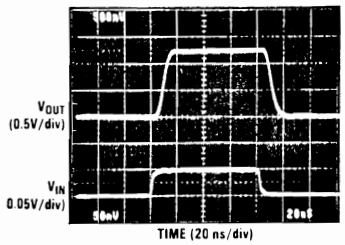
The first two plots are for a gain of 2, with R_2 820Ω and 1640Ω respectively. The reduction in overshoot and increased rise time show the reduced bandwidth. The third plot (overleaf) is for a gain of 25, with R_2 reduced to 500Ω. The rise time is only slightly less than that for the lower gain.



Rf 820Ω



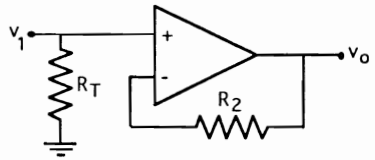
Rf = 1640Ω



Reducing R_f for Large
Closed Loop Gains, R_f = 500Ω

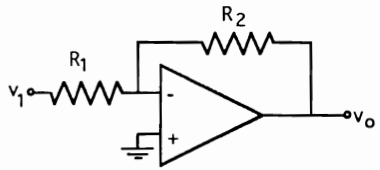
Other circuits using current mode amplifiers

UNITY GAIN FOLLOWER



Because the amplifier needs a feedback current proportional to its output voltage, the resistor R_2 must be used even for a unity gain buffer (with a conventional op-amp, the output is tied directly to the inverting input). The resistor R_T defines the input resistance which might, for example, need to terminate a 50Ω or 75Ω line in a wide bandwidth system

INVERTING AMPLIFIER



A current mode amplifier will operate as an inverting amplifier in the same circuit arrangement as a conventional op-amp. The voltage gain is

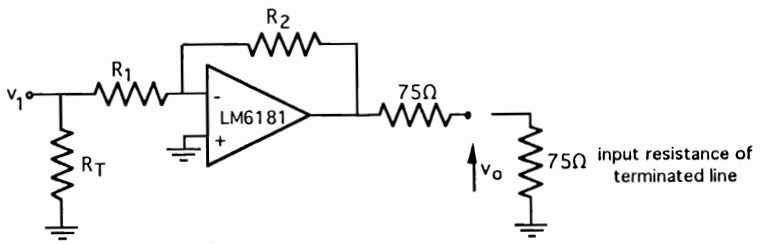
$$\frac{v_o}{v_1} = -\frac{R_2}{R_1}$$

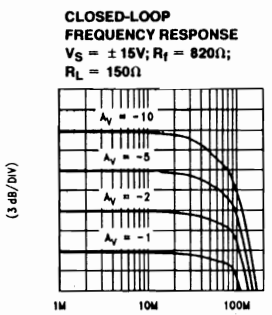
and the input resistance is R_1. Check these for yourself using the amplifier model. As in all the other configurations R_2 controls the bandwidth.

A DESIGN EXAMPLE - INVERTING VIDEO AMPLIFIER

As part of a high definition tv system an inverting amplifier is required with a voltage gain of 5 to be inserted in a matched 75Ω system. Its -3dB bandwidth must be at least 30 MHz.

The amplifier has to match the 75Ω line at input and output. At the output, therefore it must have a 75Ω resistor in series to define the output resistance and this forms a potential divider with the 75Ω input resistance of the line. So for an overall gain of -5 the amplifier needs a gain of -10, which means that in the circuit $R_2 = 10R_1$.





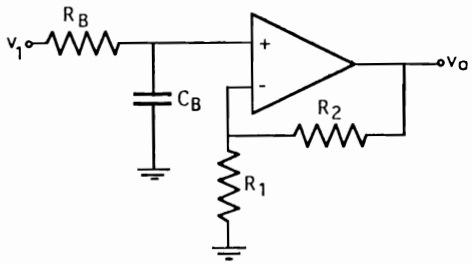
The amplifier sees a load resistance of 150Ω, and frequency response plots for this value when R_2 = 820Ω are reproduced on the left from the LM6181 data sheet. Notice the difference from those in the previous section which were for a load of 1kΩ. With this value of R_2 the response is about 1 dB down at 30 MHz, which meets the specification. For a gain of -10, therefore R_1 needs to be 82Ω. The input resistance of the basic inverting circuit would be equal to R_1, 82Ω. To terminate the input cable, 75Ω is needed, and R_T is included to reduce the input resistance to this value. R_T and 82Ω in parallel have to equal 75Ω, so R_T must be 879Ω. The nearest preferred value is 910Ω, giving an input resistance of 75.22Ω which would be accurate enough in practice.

Capacitive feedback

With conventional op-amps a high frequency rolloff can be introduced by putting a capacitor in parallel with the feedback resistor R_2. Integrators are made by replacing R_2 with a capacitor. With current feedback amplifiers the decreasing reactance of the capacitor with increasing frequency means that the feedback current goes on increasing (in theory indefinitely) as frequency rises, with a corresponding increase in loop gain. The loop gain is therefore likely to be greater than unity when loop phase lag (defined by the transimpedance lag plus additional high frequency lags due to spurious capacitances) reaches -180°, with resulting oscillation. So neither circuit is possible.

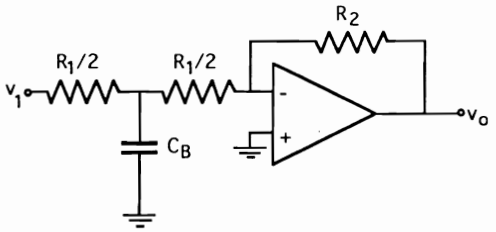
TO LIMIT BANDWIDTH

If bandwidth is to be limited, this is most easily done by passing the signal through a separate R-C circuit at the input or output of the stage. For example, with the filter at the input, typical circuits for inverting and non-inverting amplifiers respectively might be



$$\frac{v_o}{v_1} = \frac{R_1 + R_2}{R_1} \frac{1}{1 + s\,C_B R_B}$$

(non-inverting)



$$\frac{v_o}{v_1} = -\frac{R_2}{R_1}\frac{1}{1 + s\frac{C_B R_1}{4}}$$

(inverting)

TO MAKE AN INTEGRATOR

It is possible to make an integrator with a current mode amplifier using the trick of putting an extra resistor in series with the inverting input, to stop the feedback increasing at high frequencies. This technique is described in the data sheet for the Analog Devices OP-160 current mode amplifier which is reproduced here. We can see that over a reasonable frequency range the circuit behaves quite well as an integrator, and a square wave input gives the expected ramp output. Try deriving the transfer function for this circuit, and see if it agrees with the Bode plots given by the manufacturers.

OP-160

USING CURRENT FEEDBACK OP AMPS IN INTEGRATOR APPLICATIONS

The small-signal model of a current feedback op amp shown earlier in Figure 3 assumes a non-varying value of feedback impedance. A non-varying feedback impedance ensures that the bandwidth of the amplifier does not extend beyond its 180° phase shift point and create unwanted oscillations. In integrator circuits, the feedback element is a capacitor whose impedance does vary with frequency. By definition then, integrator applications using current feedback amplifiers should be unstable. However, a simple trick, shown in Figure 22, enables high-speed, wide bandwidth current feedback op amps to be used in integrator applications.

Resistor R_F is placed between an artificial sum node and the inverting input of the amplifier. This resistor maintains a minimum value of feedback impedance over all frequencies. At high signal frequencies, the integrator capacitor, C_1, is a short circuit; the feedback impedance is equal to R_F only and the amplifier has maximum bandwidth. At low frequencies, C_1 adds to the overall feedback impedance. This lowers the amplifier's bandwidth but not enough to affect the integrator's performance.

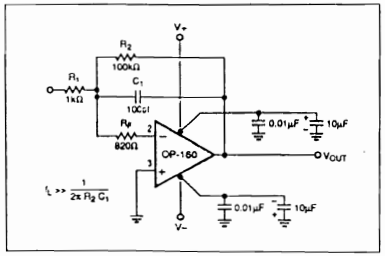


FIGURE 22: *An Integrator Using a Current Feedback Op Amp*

Figure 23 shows the gain and phase performance of the integrator. The integrator has the desired one-pole response for signal frequencies

$f_C >> 1/(2\pi R_2 C_1) = 16kHz$.

A more strenuous test of integrator performance is the pulse response. Ideally, this should be a linear ramp. The current feedback integrator's pulse response is exhibited in Figure 24. The response closely approximates the ideal linear ramp.

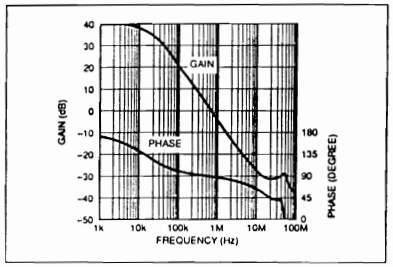


FIGURE 23: *Gain and phase response of the integrator shows a one-pole response.*

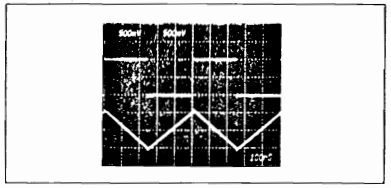


FIGURE 24: *Pulse response of the current feedback integrator. f = 2MHz.*

NOISE

IRREDUCIBLE ELECTRICAL NOISE

The noise with which we are concerned in this course is fundamental noise arising from the physical nature of electrical conduction mechanisms - it is due to the nature of the physical processes involved in conduction, and is therefore irreducible. Electrical noise is always present, and we shall see some ways of analysing its effect, and of minimizing it in certain situations. It is usually the limiting factor in determining whether a channel can convey information correctly and, ultimately, what is the weakest signal that can be detected in a particular system.

Noise is a random variation in current or voltage (or other signal), randomness implying a lack of repeatability. An oscilloscope trace of a noise signal, drawn in a few microseconds, may not be repeated in a lifetime. Consequently, statistics must be used to characterize a noise signal. Because the noise signal is the result of a vast number of independently varying contributions, it is described by Gaussian statistics. (See Connor, chapter 2). A noise signal is random, with zero d.c.mean, and so it is characterized in terms of a mean square voltage or current, equal to σ^2 in the probability density function.

Three types of noise are important, thermal noise, shot noise and flicker noise.

Thermal noise (Johnson noise)

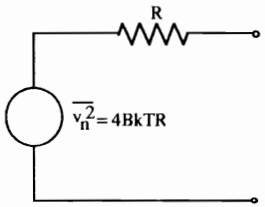
In a conductor, the electrons which act as current carriers, are in thermal equilibrium with their surroundings, and are in random motion with energy which depends on the temperature of the conductor. Thermal noise is due to the currents (and hence voltages in a resistor) set up as a result of this random motion. The energies, and hence the velocities, of the electrons increase with temperature, and therefore the noise voltage or current increases with temperature; at absolute zero there is no motion, and the thermal noise should decrease to zero.

It was proved by Nyquist (Connor, appendix I) that the thermal noise generated in a resistor of resistance R has a mean square open circuit voltage given by:-

$$\bar{v_n^2} = 4BkTR$$

where B = bandwidth,
k = Boltzmann's constant,
T = temperature (K).

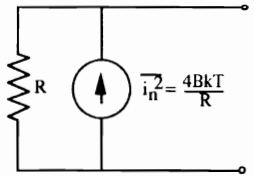
So a Thevenin equivalent circuit for a resistor, including thermal noise, has a noise voltage generator in series with the resistor:-



This can be transformed into a Norton equivalent circuit in the usual way: the Norton current is equal to the short-circuit current of the Thevenin circuit, remembering that in noise calculations we are dealing with mean square quantities. Hence,

$$\bar{i_n^2} = \frac{\bar{v_n^2}}{R^2} = \frac{4BkTR}{R^2} = \frac{4BkT}{R}$$

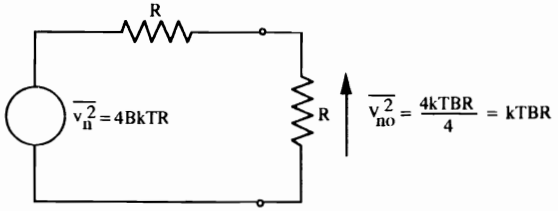
and the Norton equivalent becomes:-



Every resistance in a circuit is a source of thermal noise and should be represented by whichever of these equivalent circuits makes analysis of the circuit easier.

Thermal noise is 'white noise': its power spectral density is uniform with frequency. In other words, the noise power passing through a band-pass filter of constant bandwidth B will be the same whatever the centre frequency of the filter. The noise power from a source of white noise measured between 1 and 2 MHz will be equal to noise from the same source measured between 10 and 11 MHz or between 50 and 51 MHz. This is true up to very high frequencies (of the order of 10^{12} Hz) when quantum effects become significant, and when the time scale becomes comparable with the mean time between scattering collisions in the conductor.

The maximum amount of power is extracted from a source when it is connected to a matched load, which for a source with a resistive output impedance is a resistor equal to that output resistance. Consider the noise power delivered from a resistor R at temperature T into an equal resistor:-



The mean square noise voltage across the second resistor, v_{no}^2, is one quarter of the open-circuit mean square noise voltage produced by the first:-

$$\bar{v_{no}^2} = kTBR$$

and the noise power in the second resistor is $\frac{\bar{v_{no}^2}}{R}$, which is equal to kTB watts. This is the maximum noise power which can be extracted from the first resistor and is called the available noise power. It is important in calculating the noise performance of systems whose components are matched at their inputs and outputs.

Shot noise

This is noise produced in active devices where the current flowing through the device is the summation of a large number of individual current pulses due to electrons crossing the device. This is a random process, and the noise arises because of fluctuations in the number of electrons with time. Shot noise occurs in a situation where the electrons are not in thermal equilibrium with their surroundings. Devices which exhibit shot noise are thermionic valves, where the fluctuation is in the number of electrons emitted from the cathode, and semiconductor junctions (p-n diodes and bipolar transistors) where the number of electrons (and holes crossing the potential barrier of the junction is fluctuating.

Shot noise is, like thermal noise, white noise, so its dependence on bandwidth is similar, but it is independent of temperature. As one might expect, it depends on the average current I_{dc} flowing through the device. It is usually modelled by a current source, with mean square value

$$\bar{i_n^2} = 2eI_{dc}B$$

It is worth noting that despite being active devices, field effect transistors exhibit thermal noise, not shot noise. The current through the channel of a field effect transistor does not cross a p-n junction, but just flows through bulk semiconductor where the carriers are in thermal equilibrium.

Flicker noise

Flicker noise is another source of noise occurring in active devices. It is sometimes called 1/f noise, as its power density is approximately proportional to frequency at low frequencies. It is associated with surface imperfections in semiconductor devices, and the frequency below which it becomes significant varies for different devices, being usually in the range of 1 Hz to 1 kHz. In communications systems, which operate at frequencies very much higher than this, it is not usually a problem, but might be significant in low frequency instrumentation electronics, where the signals are dc or a few Hz. It is minimized by using devices selected (at a price!) by the semiconductor manufacturer for low noise performance.

SIGNAL TO NOISE RATIO

The amount of noise associated with a particular signal in a communications system is quantified in terms of signal to noise ratio, defined as:-

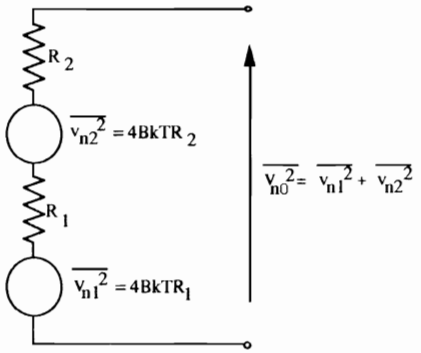
$$\text{signal to noise ratio} = \frac{\text{signal power}}{\text{noise power}},$$

and often expressed in dB. A useful rule of thumb is that a signal is undetectable is the signal to noise ratio falls to unity (0 dB), although sophisticated techniques (matched filters), beyond the scope of this course, exist which can retrieve specially coded signals from noise where the signal to noise ratio is an order of magnitude or two below unity.

COMBINATION OF NOISE FROM SEVERAL SOURCES

Noise signals from different sources are uncorrelated (independent), and therefore are summed by adding their average powers or mean square values, not by adding the rms values of voltage or current sources.

As an example, consider two resistors in series. Each is modelled with a voltage source in series representing its thermal noise:-



The mean square noise voltage across the two resistors is

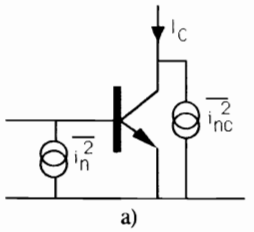
$$\overline{v_{no}^2} = \overline{v_{n1}^2} + \overline{v_{n2}^2} = 4BkT(R_1 + R_2),$$

and the r.m.s. noise voltage is hence

$$\sqrt{\overline{v_{no}^2}} = \sqrt{4BkT(R_1 + R_2)}.$$

NOISE IN TRANSISTORS

Bipolar transistors



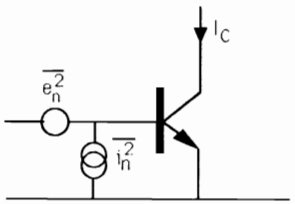
a)

In a bipolar transistor both base current and collector current flow across p-n junctions, and there is shot noise associated with each The noise generated can be represented by two uncorrelated noise current generators as in diagram a), where

$$i_{nb}^2 = 2eI_BB$$

$$i_{nc}^2 = 2eI_CB$$

It is convenient to have all noise sources in any amplifier represented in a way that refers them to the input. To this end, i_{nc}^2 is transformed into a voltage source e_n^2 in series with the base, adding to v_{BE} (diagram b)).



b)

The ratio between incremental collector current and base-emitter voltage is g_m, so

$$e_n^2 = \frac{i_{nc}^2}{g_m^2} = \frac{2eI_CB}{g_m^2}$$

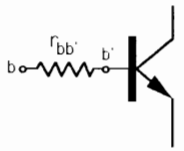
$$= 2eI_CB\left(\frac{kT}{e}\right)^2\frac{1}{I_C^2} = 2\left(\frac{kT}{e}\right)^2\frac{eB}{I_C}$$

also,

$$i_n^2 = 2eI_BB = \frac{2eI_CB}{\beta}$$

So we see that as I_C increases, e_n^2 decreases and i_n^2 increases.

An additional source of noise is the 'base spreading resistance", $r_{bb'}$ which is the resistance between the base terminal and the active base region of the device - it is effectively in series with the base connection.



It arises mainly from the bulk semiconductor between the base contact and the active region, and typically has a value of a few tens of ohms. Its thermal noise (mean square voltage $4BkTr_{bb'}$) adds to e_n^2, making

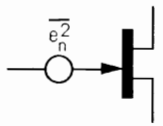
$$e_n^2 = 2\left(\frac{kT}{e}\right)^2\frac{eB}{I_C} + 4BkTr_{bb'}$$

It is only significant when I_C is large, making the first term small. We shall discuss this later when we shall see that it can limit the noise performance of an amplifier with a very low impedance source.

Field effect transistors

The current in a field effect transistor flows just through the bulk semiconductor of the channel, and not through any p-n junctions. the carriers are in thermal equilibrium, so the only noise generated is thermal. There is no significant gate current ($I_G \approx 10^{-12}$A), so shot noise from this is

almost always negligible. The thermal noise is represented as a voltage source in series with the gate:-



$$e_n^2 = \frac{2}{3}\frac{4BkT}{g_m} \qquad i_n^2 = 0$$

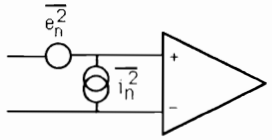
Therefore transistors with higher values of g_m have lower noise - noise voltage densities as low as $1nV/\sqrt{Hz}$ are possible.

Noise densities

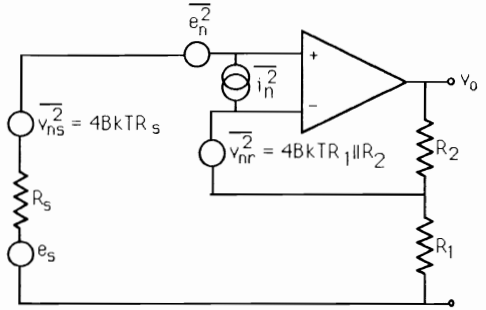
Thermal noise and shot noise are 'white noise' - they have a power spectral density which is the same at all frequencies. The larger is the bandwidth B, the more noise power in proportion. It is customary to express noise voltages and currents as measured in unit bandwidth, so noise voltage would be V^2 per Hz, or V_{rms} per $\sqrt{Hz}$. Similarly noise current would be A^2 per Hz or A_{rms} per $\sqrt{Hz}$. We will see that amplifier manufacturers commonly use the 'per $\sqrt{Hz}$' notation.

NOISE IN AMPLIFIERS

Operational amplifiers usually have their noise specified in the form of equivalent voltage and current sources at the input.



The voltage noise will always add straight into the amplifier input voltage, but the contribution from the current noise source will depend on the impedance seen by the input terminals due to the components connected to them - the noise current flows through this resistance and develops a voltage across it. Consider a non-inverting amplifier fed from a source with resistance R_s:-



The sources of noise in the circuit are the two amplifier sources, the resistance R_s (part of the signal source) and the feedback resistors R_1 and R_2. These are all shown in the diagram - let us now calculate the total mean square noise output voltage from the stage, which is easily done using superposition, taking one source at a time and adding up the m.s. output voltages (remember the sources are uncorrelated). This gives

$$v_{no}^2 = \left(\frac{R_1 + R_2}{R_1}\right)^2 \left[4BkTR_s + e_n^2 + i_n^2(R_s + R_1 \| R_2)^2 + 4BkT(R_1 \| R_2)\right]$$

where the terms are respectively source noise, amplifier voltage noise, amplifier current noise and noise from the feedback resistors R_1 and R_2. (The Thevenin equivalent of v_o, R_1 and R_2 has a resistance $R_1 \| R_2$.

Inspection shows that if R_1 and R_2 are chosen so that $R_1 \| R_2 << R_s$, the fourth term vanishes and the third term simplifies giving

$$v_{no}^2 = \left(\frac{R_1 + R_2}{R_1}\right)^2 \left[4BkTR_s + e_n^2 + i_n^2R_s^2\right]$$

This indicates that for the amplifier noise contribution to be small,

$$e_n^2 + i_n^2R_s^2 << 4BkTR_s$$

For small values of R_s (low impedance sources), e_n^2 becomes more important and should be minimised, and as R_s becomes larger, i_n^2 gets more important. In a bipolar transistor e_n^2 and i_n^2 vary in inverse proportion to each other as the collector current is changed, so a bipolar input stage, with high I_C, will be best for low impedance sources. As source impedance gets larger, I_C needs to be reduced, to reduce i_n^2. For very large source impedances a field effect transistor, with negligible current noise, will be best.

Noise figure

For the source, the m.s. noise voltage $v_{nin}^2 = 4BkTR_s$

Now noise figure $F = \dfrac{\left(\frac{signal}{noise}\right)_{in}}{\left(\frac{signal}{noise}\right)_{out}} = \dfrac{v_{no}^2}{Gv_{nin}^2} = 1 + \dfrac{1}{4BkT}\left(\dfrac{e_n^2}{R_s} + i_n^2R_s\right)$ (G= gain)

which has a minimum when $R_s = (R_s)_{optimum} = \dfrac{\sqrt{e_n^2}}{\sqrt{i_n^2}}$

Therefore a given amplifier has an optimum value of R_s for which it gives a minimum noise figure.

Optimum collector current for a bipolar transistor

Taking the expression for $(R_s)_{optimum}$ and putting in the expressions for e_n^2 and i_n^2 for a bipolar transistor (neglecting thermal noise from $r_{bb'}$) gives, at collector current I_C

$$(R_s)_{optimum} = \sqrt{2\left(\frac{kT}{e}\right)^2 \frac{eB}{I_C} \frac{1}{2eI_CB}} = \sqrt{\left(\frac{kT}{e}\right)^2 \frac{1}{I_CI_B}} = \frac{kT}{e}\frac{\sqrt{\beta}}{I_C} = \frac{25mV\sqrt{\beta}}{I_C}$$

Conversely, for a particular source resistance R_s,

$$(I_C)_{optimum} = \frac{25mV\sqrt{\beta}}{R_s}$$

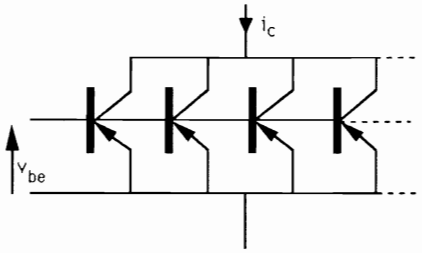
This is the collector current which minimises the noise figure for source resistance R_s.

Very low source resistances

As I_C is increased, current noise increases and voltage noise decreases, and, as we have seen, the transistor is optimised for a lower source resistance. However, we have so far neglected $r_{bb'}$ which adds its noise to e_n^2. If $r_{bb'}$ is of comparable size to R_s, obviously its contribution must be significant and will form a lower limit to the total e_n^2 as I_C is increased. So, in practice, we cannot go on noise matching to lower and lower resistance sources just by increasing I_C indefinitely.

Transistors intended for low-noise front ends with a low source impedance are constructed to have a very low $r_{bb'}$ to keep its noise contribution low. Examples are the LM394 npn differential pair ($r_{bb'} = 30\Omega$) and the 2SD786 ($r_{bb'} = 4\Omega$).

A trick to reduce the effective value of $r_{bb'}$ is to connect a number of such transistors in parallel.



This arrangement is equivalent to a single transistor with effective collector current i_c which is the sum of the collector currents of the individual transistors. If the mutual conductance of one transistor is g_m, then for a signal v_s applied between base and emitter, the collector current is

$$i_{cs} = ng_m v_s$$

giving an effective mutual conductance ng_m. The gain of the stage has been increased by a factor n over that of a single transistor.

Each transistor has a mean square noise voltage in series with its base of e_n^2, so the total mean square noise current in the collector circuit is $i_n^2 = ng_m^2 e_n^2$ and the r.m.s. noise current here is

$$\sqrt{i_n^2} = \sqrt{n}\, g_m \sqrt{e_n^2}$$

We will assume that the source resistance is so low that the amplifier current noise makes a negligible contribution to noise at the input.

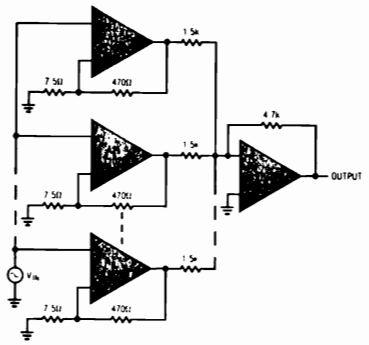
The signal to noise ratio in the collector current is now

$$\frac{i_{cs}}{\sqrt{i_n^2}} = \frac{ng_m v_s}{\sqrt{n}\, g_m \sqrt{e_n^2}} = \sqrt{n}\,\frac{v_s}{\sqrt{e_n^2}}$$

and we see from the final expression that it has been improved by a factor $\sqrt{n}$ over what would be achieved by a single transistor. If e_n^2 was due mostly to thermal noise from $r_{bb'}$,we could say that $r_{bb'}$ has effectively been reduced by a factor $\sqrt{n}$. The reason is, of course, that the signal currents from the separate transistors are correlated and add coherently, whereas the noise currents are from uncorrelated sources and add incoherently.

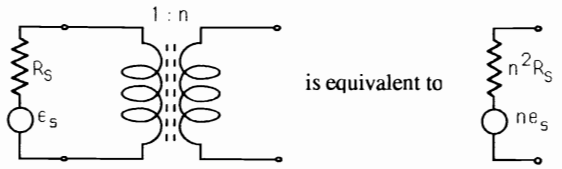
The same method can be used with operational amplifiers - the diagram here is taken from the data sheet for the LT1028 ultra-low noise amplifier.

Paralleling Amplifiers to Reduce Voltage Noise



1 ASSUME VOLTAGE NOISE OF LT1028 AND 7.5Ω SOURCE RESISTOR = 0.9nV/√Hz
2 GAIN WITH n LT1028's IN PARALLEL = n × 200
3 OUTPUT NOISE = √n × 200 × 0.9nV/√Hz
4 INPUT REFERRED NOISE = $\frac{\text{OUTPUT NOISE}}{n \times 200} = \frac{0.9}{\sqrt{n}}$ nV/√Hz
5 NOISE CURRENT AT INPUT INCREASES √n TIMES
6 IF n = 5 GAIN = 1000 BANDWIDTH = 1MHz RMS NOISE DC TO 1MHz = $\frac{2nV}{\sqrt{5}} = 0.9\mu V$

Another method of dealing with low source impedances with a.c. signals is to use a step-up transformer, which reproduces the source with a higher voltage and at a higher impedance level.

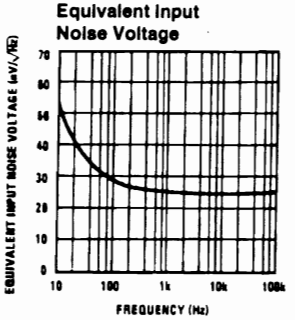


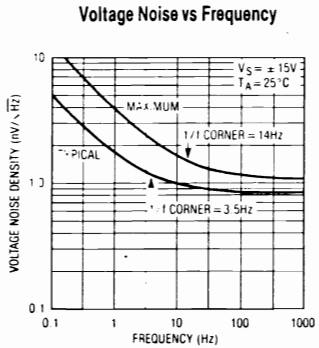
This can then be used with an amplifier which is optimised for a higher source resistance.

FLICKER NOISE IN AMPLIFIERS

So far we have assumed that the spectral density of noise was uniform with frequency, which is usually true above the so-called 1/f corner frequency. The spectral density of flicker (1/f) noise increases as frequency decreases, and the 1/f corner frequency is where flicker noise begins to dominate shot and thermal noise.

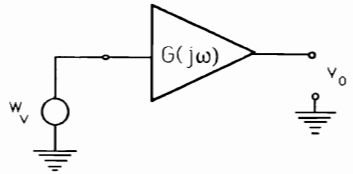
Manufacturer's data for transistors and op.amps contains plots of noise density against frequency which show clearly this effect. It obviously must be taken into account if signals below the corner frequency are to be amplified as the noise figure at such frequencies will be worse than that calculated, as we did earlier, with uniform spectral density. The following curves for voltage noise density are taken from the data sheets for the LF351 (on the left) and for the LT1028 (on the right) an ultra-low noise op.amp. They have the same general shape, but the 1/f corner frequency is significantly lower for the lower noise (and more expensive) device.





NOISE IN FREQUENCY-DEPENDENT CIRCUITS

If noise from a source with uniform spectral density passes through an amplifier whose gain varies with frequency, then obviously, different frequency components of the noise are amplified different amounts. This will clearly affect the total noise at the output in a given bandwidth.



Imagine a voltage noise source, spectral density w_v V^2/Hz, feeding an amplifier with a transfer function G(jω). In a narrow range of frequency dω at a frequency ω, the mean square noise output voltage will be

$$dv_{no}^2 = |G(j\omega)|^2 \frac{w_v}{2\pi} d\omega \quad V^2$$

In a bandwidth B, therefore, the total mean square noise output will be

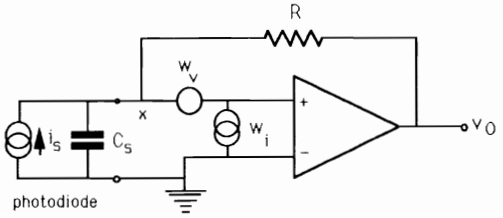
$$v_{no}^2 = \int_0^{2\pi B} |G(j\omega)|^2 \frac{w_v}{2\pi}\, d\omega.$$

These calculations can appear slightly untidy because noise densities and bandwidths are conventionally expressed in terms of Hz, whereas we usually write transfer functions using radian frequency. So you have to think where to put in the factors of 2π.

Photodiode amplifier

Now let us consider a real noise problem concerned with optical detection.. Photodiodes are widely used as optical detectors because of their sensitivity, linearity and relative cheapness. A photodiode is basically a pn junction diode in which electron-hole pairs are created in the depletion region by incident light in direct proportion to incident power (number of photons). These carriers are swept out of the depletion region by the built-in field, and form a reverse current in the diode.

A photodiode can be modelled very closely as a current generator in parallel with a capacitance (the usual reverse-biassed diode capacitance). To get a voltage output, a photodiode can be connected to an operational amplifier 'transfer resistance' circuit - a current to voltage converter.



The current source and capacitance represent the photodiode, and the operational amplifier is drawn including its equivalent noise sources at the input. Otherwise, it is taken, for simplicity, as ideal (for the moment at least). The output due to the signal is easily seen to be $-Ri_s$.

Consider the amplifier noise sources. They are expressed in terms of spectral density, w_v V^2/Hz and w_i A^2/Hz respectively. It is easiest to use superposition and to take them one at a time to get their contributions to the output voltage. Removing i_s and shorting w_v gives, due to the amplifier current noise in a bandwidth $d\omega$,

$$dv_{no1}^2 = \frac{w_i}{2\pi} R^2\, d\omega$$

Now remove i_s and i_n^2 and get the output due to the amplifier voltage noise. The voltage at the non-inverting input is zero, so the voltage at x, in bandwidth $d\omega$ at frequency ω, is

$$dv_x^2 = \frac{w_v}{2\pi} d\omega = dv_{no2}^2 \left| \frac{1}{1 + j\omega C_s R} \right|^2 = dv_{no2}^2 \frac{1}{1 + \omega^2 C_s^2 R^2}$$

$$\text{giving} \quad dv_{no2}^2 = \frac{w_v}{2\pi} (1 + \omega^2 C_s^2 R^2)\, d\omega$$

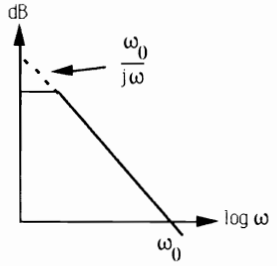
The combined noise output is $dv_{no}^2 = dv_{no1}^2 + dv_{no2}^2 = \left[\frac{w_v}{2\pi} R^2 + \frac{w_v}{2\pi} (1 + \omega^2 C_s^2 R^2) \right] d\omega$

and the total noise in a bandwidth from d.c. to B Hz is

$$v_{no}^2 = \int_0^{2\pi B} dv_{no}^2\, d\omega = w_i R^2 B + w_v \left[B + \frac{(2\pi)^2 B^3 C_s^2 R^2}{3} \right]$$

The final expression gives the total mean square noise voltage in bandwidth B. The first term, due to the current noise is simple and proportional to B, because this is amplified independently of frequency. The voltage noise is amplified with a gain which increases with frequency, and this has led to the second term whose dominant part is proportional to B^3. As we would expect with w_v amplified with a gain rising with frequency, the total noise increases dramatically as the bandwidth is increased.

In this analysis we neglected the frequency response of the operational amplifier which we have seen is usually characterised by a dominant pole and as a result we have derived closed-loop responses for both the signal and the noise which appear to have no upper frequency limit, which is obviously not correct. Instead of taking the open-loop gain of the op. amp to be infinite, a good approximation is to write it



$$A_{VOL}(j\omega) = -\frac{\omega_0}{j\omega}$$

where ω_0 is the unity gain frequency. This is plotted in the Bode diagram as the dotted line, and is seen to depart from the actual op. amp response only at very low frequencies, where the gain is very high anyway. So negligible error is introduced by the approximation.

If the circuit is now analysed fully using this expression for open-loop gain, the transfer functions for the signal and the noise are the same as before, except that they are multiplied by a second-order low-pass function $\frac{1}{1 + 2\zeta \frac{j\omega}{\omega_n} - \left(\frac{\omega}{\omega_n}\right)^2}$ with $\omega_n = \sqrt{\frac{\omega_0}{C_s R}}$.

You should recognise the topology of this circuit as being identical to that of the differentiator, so the loop transfer function will be the same, and this second order transfer function comes out very underdamped. As with the differentiator, a small capacitor in parallel with R needs to be included, chosen to make ζ say, 0.7. Then the response will be 3dB below its low frequency value at ω_n and ω_n can be taken as the bandwidth of the system.

Analysing this circuit to get these results is a bit messy, but is worth a try!

SOME OPERATIONAL AMPLIFIER NOISE SPECIFICATIONS

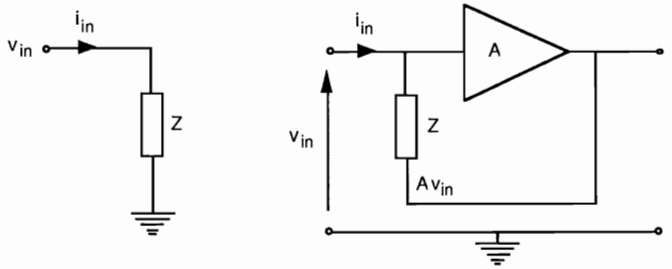
Type	Bipolar or FET	$\sqrt{e_n^2}$ (nV/$\sqrt{Hz}$)	$\sqrt{i_n^2}$ (pA/$\sqrt{Hz}$)	Comments
LF351	FET	25	0.01	general purpose
LF356	FET	13	0.01	lower noise
NE5534	Bipolar	4	0.6	low noise
OP-27	Bipolar	2.7	0.4	very low noise
LT1028	Bipolar	0.85	1	ultra low noise

ROOM TEMPERATURE THERMAL NOISE

Resistance	Open-circuit voltage noise	Short-circuit current noise
10Ω	0.41nV/$\sqrt{Hz}$	41pA/$\sqrt{Hz}$
100Ω	1.3nV/$\sqrt{Hz}$	13pA/$\sqrt{Hz}$
1kΩ	4.1nV/$\sqrt{Hz}$	4.1pA/$\sqrt{Hz}$
10kΩ	13nV/$\sqrt{Hz}$	1.3pA/$\sqrt{Hz}$
100kΩ	41nV/$\sqrt{Hz}$	410fA/$\sqrt{Hz}$
1MΩ	130nV/$\sqrt{Hz}$	130fA/$\sqrt{Hz}$

BOOTSTRAPPING

Bootstrapping is a technique for increasing the apparent impedance of a component in a circuit, and implies that the circuit is being "hauled up by its own bootstraps". Imagine an impedance Z with one end connected to signal earth. When a voltage v_{in} is connected to it a current $i_{in} = \frac{v_{in}}{Z}$ flows from the source. Now , if the lower end of Z is disconnected from earth and connected instead to the output of a unity gain buffer whose input is connected to v_{in} , the voltage across the impedance is made zero, and so i_{in} also goes to zero. For a voltage v_{in}, current i_{in} is zero - the impedance appears to be infinite.

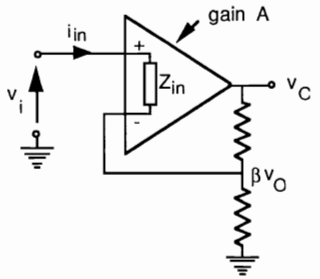


In practice the gain of a so-called unity gain buffer will be slightly less than unity. If its gain is A (see the diagram) and less than unity, then the voltage across Z is $v_{in}(1 - A)$. This makes the input current

$$i_{in} = \frac{v_{in}(1 - A)}{Z}, \quad \text{and the input impedance of the circuit is} \quad \frac{v_{in}}{i_{in}} = \frac{Z}{(1 - A)} .$$

If A were 0.99 (reasonable for an op. amp follower), the input impedance would become 100Z.

Input impedance of operational amplifier non-inverting amplifier



A good example of bootstrapping is the non-inverting operational amplifier configuration, shown here with the non-infinite op. amp input impedance included. The input current is

$$i_{in} = \frac{v_{in} - \beta v_O}{Z_{in}}$$

and the output voltage is

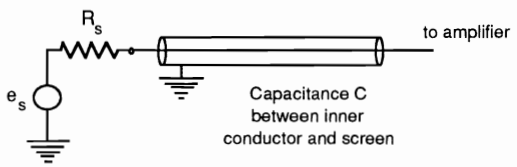
$$v_O = \frac{A}{1 + A\beta} .$$

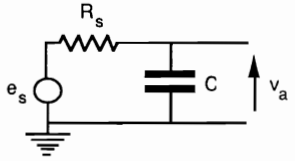
Combining these equations,

$$i_{in} = \frac{v_{in}\left(1 - \frac{A\beta}{1 + A\beta}\right)}{Z_{in}} \quad \text{and so the input impedance of the buffer is} \quad \frac{v_{in}}{i_{in}} = (1 + A\beta)\, Z_{in} .$$

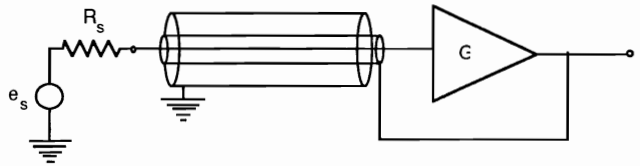
The effect of the feedback has been to multiply the op.amp input impedance by the factor 1 + Aβ, because the bottom end of Z_{in} is at voltage βv_O.

Capacitance of a screened lead



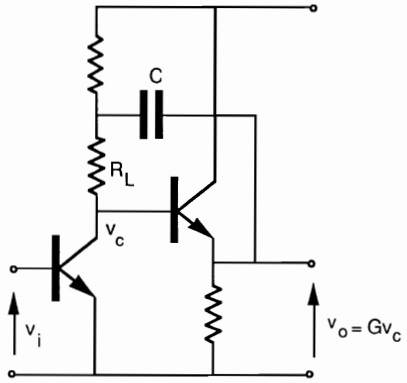


A screened cable might be used to connect a very small signal from a transducer to an amplifier to avoid interfering signals being picked up by the lead, due to capacitive coupling. Screened cable has a significant capacitance between inner and outer (typically 60-100pF per metre) and this can form a low-pass filter with the source resistance. The diagram above illustrates this. The response here has a high frequency break point at $\omega = \frac{1}{CR_s}$.



Here the signal has been fed to a buffer amplifier (gain G, again just less than 1) and the screen around the signal conductor is connected to the amplifier output. In the same way as our first example, the impedance of the capacitance has been increased by $(1 - G)^{-1}$. In other words the effective value of the capacitance has been reduced by this factor and the new high frequency break point is $\omega = \frac{1}{(1 - G)CR_s}$. This has also been increased by the same factor. The outer screen, connected to earth is there as a precaution.

Bootstrapping a load resistor



Bootstrapping can be used to increase the gain of an amplifier stage, too. Here a common emitter stage is followed by an emitter follower. The top of the load resistor of the first stage is capacitively coupled to the emitter follower output.

Without the bootstrap capacitor, the gain of the first stage would be (for a load resistor R_L) equal to g_mR_L. With bootstrapping, if the gain of the emitter follower is G (G just < 1), the voltage across R_L is $v_c(1 - G)$.

The collector current (incremental) is g_mv_i, , so $g_mv_iR_L = v_c(1 - G)$, or

$$v_c = g_mv_i\frac{R_L}{1 - G}) \quad \text{and} \quad \frac{v_o}{v_i} = G\frac{g_mR_L}{1 - G}.$$

The gain of the stage has ben increased by the factor (1 - G). This has ben achieved by increasing the effective value of the resistor R_L, so the impedance level at the collector of the first transistor has also been increased. Any capacitance at this point (stray wiring capacitance, C_{cb} in the emitter follower) appears in parallel with this and gives a high frequency breakpoint. Because R_L has been multiplied, the breakpoint is at a correspondingly lower frequency. So the gain may be higher, but the bandwidth has been reduced. Yet again we don't get something for nothing!