Enriching Design Intent for Optimal OPC and RET

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ABSTRACT

In typical rule- or model-based optical proximity correction (OPC) the goal is to align the silicon layout edges as closely as possible to the corresponding edges in the design layout. OPC precision requirements are approaching 1nm or less at the 0.1μm process node. While state-of-the-art OPC tools are capable of operating at this accuracy, such tight requirements increase computational cycle time, output file size, and photomask fabrication cost.

Accuracy requirements on different features in the design may vary widely, and regions that do not need the highest accuracy can be exploited to reduce OPC complexity. For example, transistor gate dimensions require tighter dimensional control than interconnect features on the polysilicon layer. Furthermore gate features typically occupy less area than interconnect. When relaxed OPC accuracy requirements are applied to the interconnect features, but not the gate features, the overall complexity of the polysilicon mask pattern can be significantly reduced without losing accuracy where it counts.

While the layout provided by designers has traditionally been regarded as the "best" specification of the intended silicon layout, there is today a growing trend towards "geometry tuning" after design tape-out. These changes are usually made to improve the manufacturability of the physical design and/or to simplify the pattern processing required for mask production. However, because the original design was used for electrical parameter determination and for timing analysis, great care must be taken to insure that such design-intent modifications do not adversely affect circuit behavior. This caution also applies to "frugal" OPC where relaxed OPC tolerances are used to reduce mask layout complexity[1].

To insure that modifications to the original design do not create problems in the integrated circuit, tolerance information specifying the ranges of acceptable shapes should ideally be provided with the design layout. In this paper we explore methods for embedding design intent latitude in layout databases, propose an "envelope method" for estimating worst-case device and timing behavior, and discuss techniques for using this information to tune the design and OPC behavior to improve chip manufacturability.

Keywords: OPC, RET, frugal correction, process window optimization, target modification, mask design rules

1. BACKGROUND

Post-design layout modifications are motivated by a need to "tune" shapes for better lithographic performance and to reduce mask layout complexity. Foremost are changes made to feature dimensions and spaces to improve the quality of the structures on silicon. In general, enlarging feature spacing and widths improves optical contrast and minimizes dimensional variation, thus reducing the probabilities for electrical shorts or opens. Design layouts are drawn to obey process design rules that specify, among other things, minimum line width and minimum space between features. Although designs are compliant with specified rules there are many locations where larger dimensions could be used with no density penalty. Enlarging features and/or spaces in some areas can provide incremental yield improvements.

1.1 Simplifying mask complexity

With OPC and other resolution enhancement software treatments, simpler geometric shapes can be used when silicon structure shapes are allowed to deviate from the original design target. With relaxed edge placement tolerances, for example, accuracy can be safely sacrificed to reduce correction aggressiveness. Figure 1 illustrates a method where silicon edge placement is specified with minimum and maximum bounds. Using such a "pliant target"[1] in OPC

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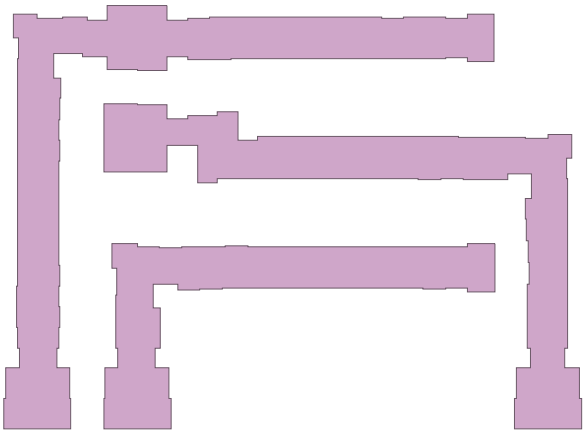
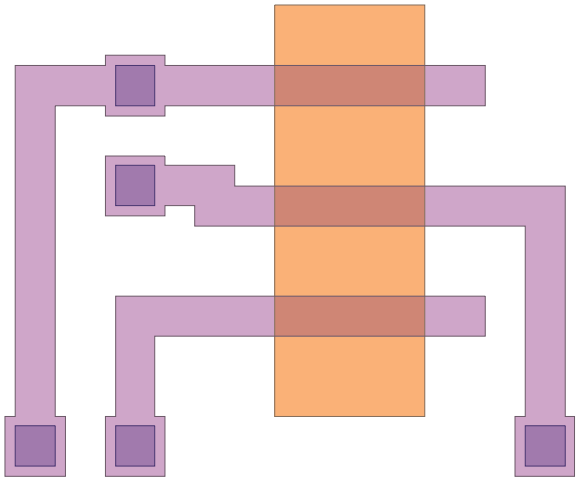
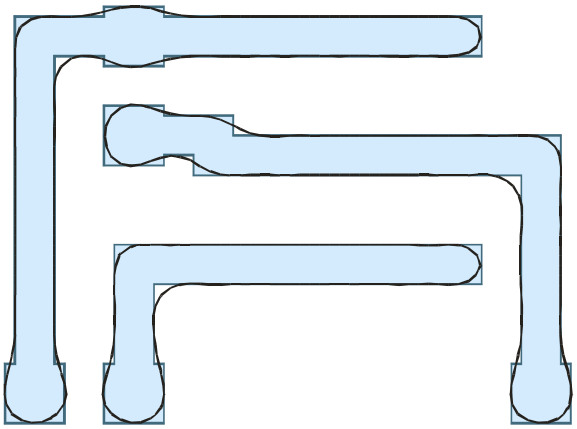
generation allows sufficient correction with simpler geometries – those with fewer jogs, serifs and notches. Subsequent downstream processing is thus simplified through mask generation, resulting in faster cycle times and lower mask costs.



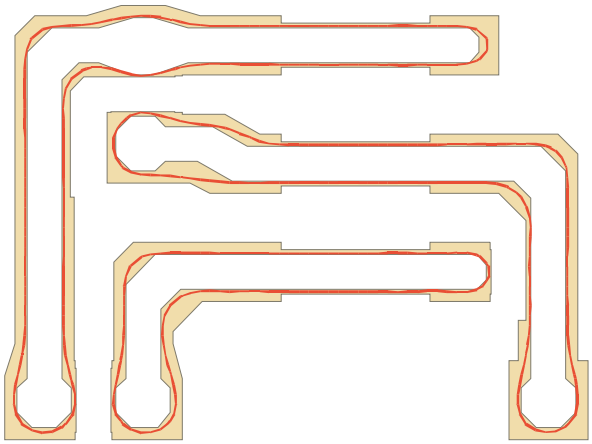
a. Correction to minimize edge placement error on all edges. (6X pattern data size increase)



b. "Frugal" correction to maintain edges within tolerance bands specified by pliant target. (15% pattern data size increase)



c. With correction (a) predicted silicon edges align closely with design pattern



d. Silicon edges from correction (b) are maintained within pliant target. Correction accuracy on gates is same as (c).

Figure 1: "Frugal correction allows silicon shapes to deviate from design.

1.2 Effects of process window variation

When wafers are printed under real process conditions, the final silicon structure shapes will vary. For the mask layout pattern in figure 2, the curved bands show where the silicon edges may actually appear under influence of typical process variations in defocus, dose, and mask dimensional uniformity. The pliant target, such as shown in figure 1, can be used by the OPC algorithm to center the expected feature variations within the specified minimum and maximum edge locations.[2, 3]

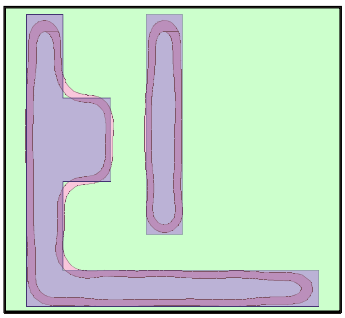


Figure 2: Edge position ranges through process variations.

1.3 Modifications to improve accuracy

Another benefit of allowing OPC treatments to deviate from the original layout is to achieve better accuracy. For example, figure 3 illustrates a situation where the mask polygon edges must be constrained to a mask grid. From the standpoint of fitting to target edge locations, the best correction is a shape falling somewhere between correction cases **a** and **b**. With grid constraints, correction **b** provides the least edge placement error. However correction **c** provides the best dimensional accuracy even though the edge placement errors are larger than in **b**, and the silicon feature position is shifted. Furthermore, the OPC treatment of **c** is asymmetric, despite the fact that the original figure is symmetric. This result is displeasing at first look, however in many situations such asymmetric corrections can provide the best results. Which treatment is best depends on what's important for different features: a transistor gate correction should strive for accurate dimensional control, whereas a contact should maintain its position for overlay. Interconnect features can usually tolerate both position and dimensional deviations except where they interact with a via.

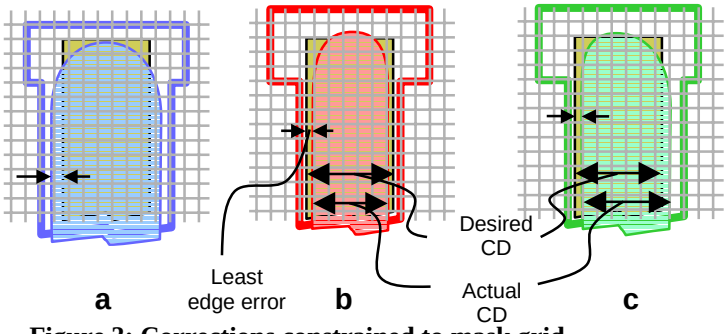
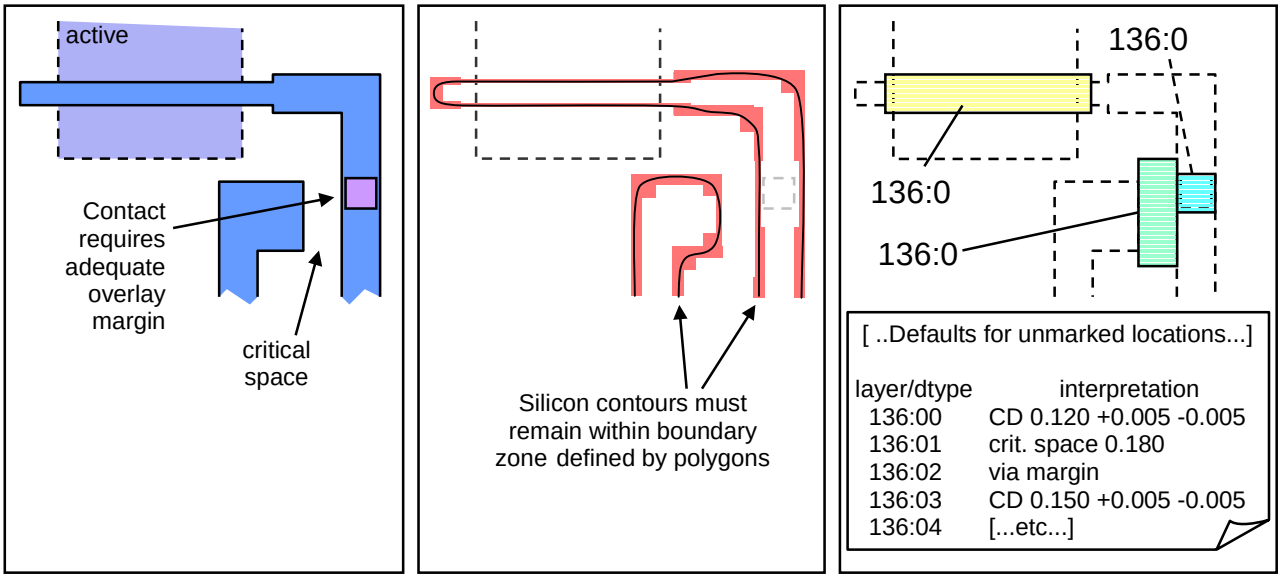


Figure 3: Corrections constrained to mask grid.

1.4 Types of information needed in addition to standard design layout layers



a. Original design layout b. Edge location tolerances c. Dimensional tolerance flags

Figure 4: Alternative target encoding schemes

A single design layer does not contain enough information to determine how to best make optimizing trade-offs involving target modifications. Figure 4 illustrates some alternatives for embedding such guidance in additional layers to be provided to the OPC algorithm. In general, OPC is performed one layer at a time, and it should not make changes that affect key alignments to other layers. For gate level correction (polysilicon layer) access to via and active layers (figure 4a) provides guidance on where contacts must be positioned, and identifies the locations of transistor gates. A pliant target (figure 4b) can be used to specify minimum and maximum silicon edge locations for process window optimization and for frugal correction. Dimension tolerance features shown in figure 4c can be used in conjunction with the pliant target to guide trade-offs among CD, edge, placement, and center position accuracy. In summary, the additional information should *independently* define extents of permissible edge locations, and feature-specific dimensional tolerances.

Such additional layout information could be embedded in the design database, or the layers could virtually exist by synthesizing them as needed by way of specified boolean layer operations.

In addition to providing a more complete specification of design intent to OPC, these layers can be directly applied to generate checks for model-based mask layout verification[4]. We believe having such additional information available in the physical synthesis phase also will prove useful for extracting device parameter value ranges and performing worst-case timing analysis, as discussed below.

2. POST-LAYOUT DESIGN MODIFICATION AND CIRCUIT PERFORMANCE

Circuit performance and timing behavior is typically derived from the completed design layout, which is assumed to represent the expected shapes of silicon structures. Any deviations from this ideal representation will affect the electrical characteristics of the circuit. One way to insure that post-design modifications do not adversely affect circuit performance is to explicitly specify the range of permissible modifications in the design, and use this information to find the worst-case impact on circuit performance. (Conversely, such a worst-case analysis could be used to determine bounds of the modification ranges). For example, Figures 5a and 6 show the as-drawn polysilicon and metal-1 layers, respectively, for an actual[5] standard-cell layout (0.13μm), with additional "envelope" layers demarcating *possible* locations for features. Alternative feature layouts that stay within the envelope region, and that cover the contact regions, are guaranteed to conform to layout design rules and to have no effect on circuit function. Figure 5b shows an original as-drawn configuration. Figure 5c shows a post design modification that reduces figure complexity, and 5d shows a modification that could be used to avoid a mask design rule violation involving corner serifs. Both modifications are contained within the envelope, and they overlay the contact regions properly.

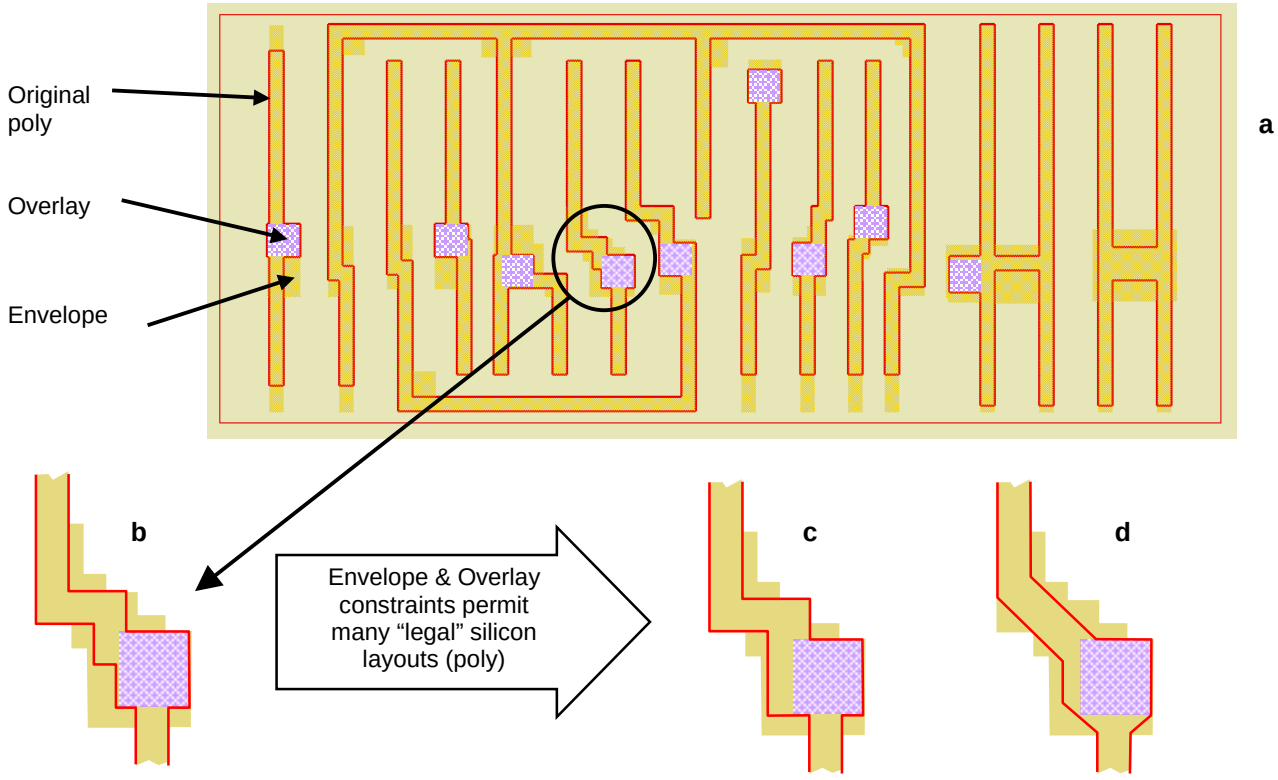


Figure 5: Envelope layer and contact regions bound permissible post-layout polysilicon design modifications.

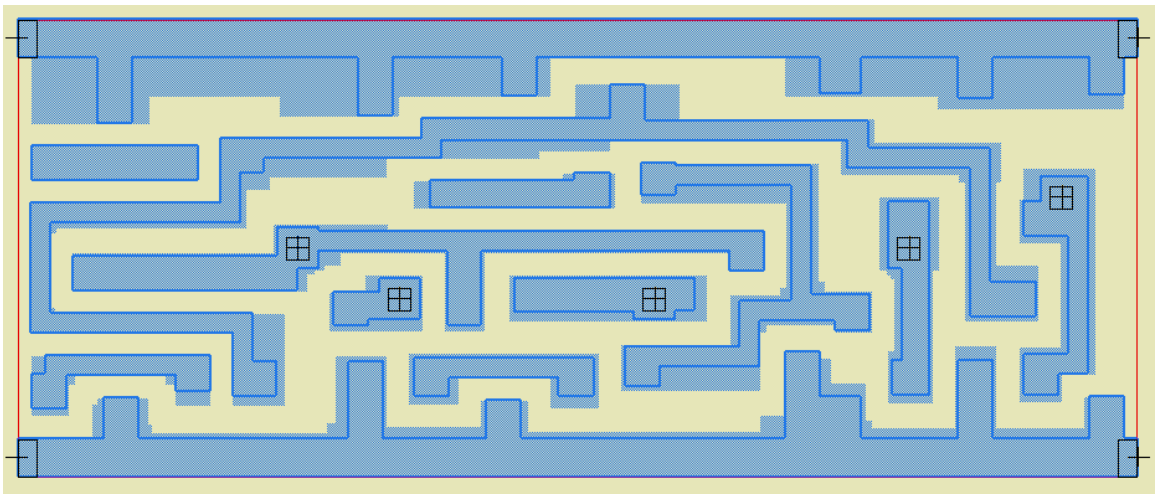


Figure 6: Envelope for metal 1.

One way to evaluate the effect of possible modifications is to generate a suite of variations, extract electrical parameters from each case, and then find the slowest configuration. However, we took a conservative approach by using the entire envelope layer for extracting maximum possible parasitic capacitance, and using the original drawn figures to estimate maximum resistance, thus bounding the worst-case timing effect.

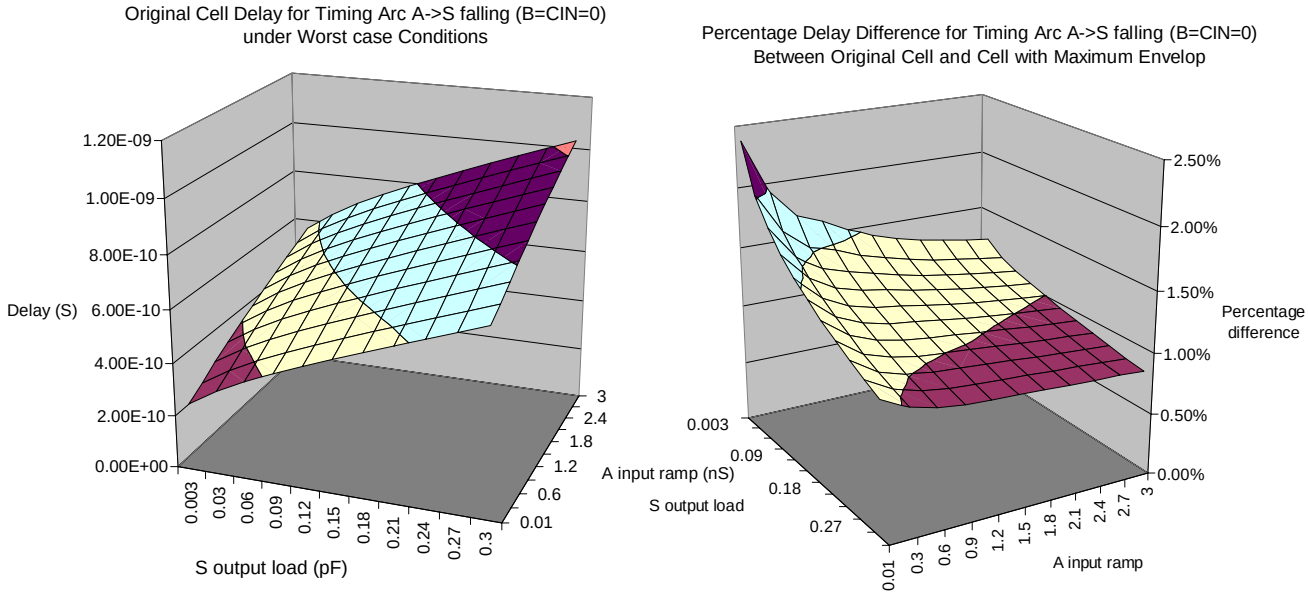


Figure 7: Timing surface for original 1-bit adder and timing difference to worst-case surface.

Figure 7 shows the simulated timing surface for the original configuration (7a) under various load and input ramp conditions, and the difference (7b) to the timing surface for the worst-case configuration extracted from the envelopes. Note that the timing delays are affected by less than 2%. Figure 8 compares output waveforms for original and worst-case layout configurations. Actual modifications will not span the entire envelope, thus parasitic capacitance will be lower than worst-case. For this process it is clear that minor modifications to poly and metal interconnect features has negligible impact on circuit timing.

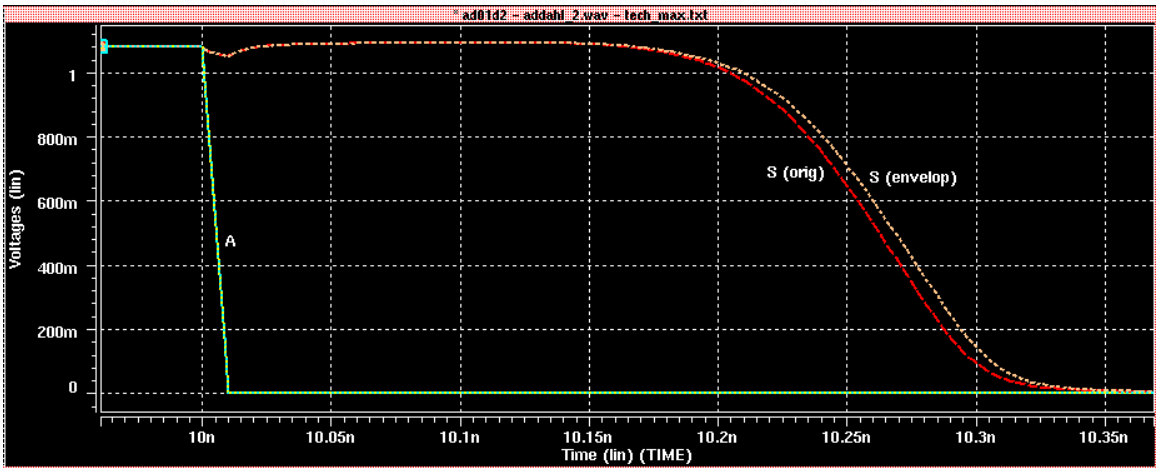


Figure 8: Output waveforms at input ramp = 0.01nS, Cload = 0.003pF.

A similar strategy may be employed for evaluating the effect of moving transistor gate locations, however we have not completed such an analysis at this time.

3. CONCLUSIONS

We believe that "ideal" target layouts based on current process design-rule methodologies are insufficient for advanced, low k1 lithography processes. In some configurations design-rule compliant layouts over-specify what's actually needed on silicon, and in other cases, better lithographic results can be obtained by tweaking edge and feature positions. In summary, providing design intent tolerance specifications to augment drawn layers can be used to:

- Decrease mask layout complexity to reduce cost and cycle time.
- Guide OPC and RET algorithms in making trade-offs among dimensional accuracy, feature position, and feature uniformity to optimize chip performance and yield.
- Take guesswork and risk out of post-design optimization by providing a basis for worst-case parameter extraction and timing analysis.
- Provide a rigorous specification for mask layout verification.

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