Maintaining Lithographic Quality during OPC for low k1 and MEEF processes constrained by Mask Dimensional Rules.

Christopher Cork, Lawrence S. Melvin III, Mike Miller, Robert Lugg, Michael L. Rieger
Synopsys Inc.
Synopsys Technology Park
2025 NW Cornelius Pass Rd.
Hillsboro, OR 97124

ABSTRACT

Mask fabrication rules can interfere with the ability of OPC and RET shape generation to achieve the best lithographic quality on silicon. With low k1 lithography, ideal correction shapes dictated by lithography-based simulation frequently violate mask geometry constraints. Because the scaled spatial bandwidth of the wafer lithography process is lower than that of the mask process there are some degrees of freedom in OPC shape generation to optimize for lithographic accuracy and mask compliance together. In this paper we discuss strategies to embed mask rule compliance in correct-by-construction model-based OPC.

Key Words: Mask Rule Check, MRC, OPC

1. INTRODUCTION.

Mask rules specify layout geometry constraints driven by mask-writing and inspection equipment limitations and by mask process capabilities. Prior to the adoption of mask synthesis layout treatments, these rules were merely combined with silicon lithography and processing constraints into a single set of design rules applied at design tape out (design rule check, DRC). With mask synthesis – optical proximity correction (OPC) and layout treatments for resolution enhancements techniques (RET) – the wafer layout and the mask layout geometries are incongruent. Silicon design rules are irrelevant to mask layouts, and post mask synthesis layouts are subject to an independent set of mask rule checks (MRC).

In an ideal world, layouts are 100% correct by construction and verifications result in zero errors. In practice where design rule violations can occur there are three options: repair the geometry, waive the error, or re-spin a correct-by-construction layout. For design rule violations, repairing mildly offending geometry is often the most expedient solution providing it can be done without introducing violations of other rules. Waiving an error may be necessary when there are two or more competing constraints among which there is no solution. An expensive re-spin is the path of last resort. A fourth option, “relax the rule,” is rarely invoked because no one wants to take the career risk.

For mask rule violations, making repairs post OPC is an option but is never a good option. Small adjustments to mask edges can significantly affect the wafer image and such “blind” repairs can wipe-out OPC effectiveness. Typically, a mask rule violation arising from model-based OPC is a case where the most accurate OPC shape conflicts with the offended rule. This problem is particular acute with low MEEF configurations, such as alternating phase shift apertures, where large correction amplitudes are needed. However, because of the band-limited nature of the lithography system, there are many possible OPC shape configurations that provide nearly identical post-exposure corrected behavior, of which some may relieve a mask rule violation. Deriving such compliant shapes post OPC is difficult because any modification at one location requires compensating adjustments to many other nearby shapes. The best way to derive MRC compliant shapes is to embed the mask constraints within the OPC relaxation algorithm itself.

Mask rule compliant OPC is effective to the point where there is no mitigating solution that maintains the required silicon accuracy. At this juncture, the choices are limited to waiving the mask rule, or modifying the original design layout to eliminate the problem configuration. But these are topics for another paper.

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In this work we outline key characteristics of mask compliance rules and we describe MRC correct-by-construction techniques for model-based OPC.

2. The uniqueness of an OPC Solution

For any given configuration there many OPC correction variations that will provide an adequately corrected silicon result. There are in fact many that will give almost identical results on silicon and many more that would be considered acceptable. This means that although a high-accuracy correction may lead to certain segments together creating an MRC violation, there may be other suitable correction configurations that give a nearly equivalent lithographic image without causing an MRC violation. Similarly, MRC violations can involve two segments for a face-to-face violation and four for a corner-to-corner violation. There also exist a large variety of ways to move these segments to return an MRC compliant solution. Sometimes the best solutions may involve an asymmetric movement of the segments as one edge may have a tighter dimensional constraint than the other, e.g. for a critical transistor or contact enclosure. A suitable algorithm will therefore be needed to either evaluate many different possible solutions or to converge consistently onto a suitable one.

The premise of MRC-compliant OPC therefore is that within some range of alternative corrected shapes, there exists a configuration that simultaneously provides the required correction on the wafer without violating mask fabrication constraints.

3. Mask fabrication constraints – a tour.

Figure 1 illustrates how OPC can introduce a basic type of mask constraint – minimum space between mask features. In this example the two "bumps" dictated by simulation create a space violation (figure 1a) across the adjacent lines. A simple "blind" repair strategy could symmetrically remove feature at the violation until the space criteria is achieved (figure 1b). However, the correction accuracy of these repaired edges is degraded. An alternative repair strategy is one (figure 1c) where OPC accuracy is partially restored by preserving local area, in this case by increasing the length of bumps to offset the area loss. If the criticality of offending features is known, repair adjustments could be asymmetrically applied so that the most critical feature is minimally affected (figure 1d).

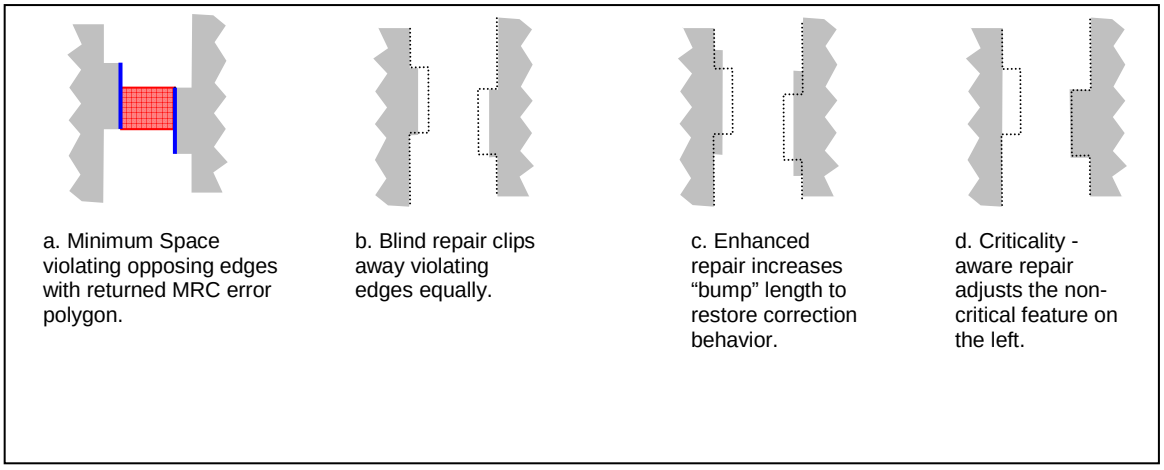

Figure 1. Minimum space violation and possible repair strategies

Acceptable results may be obtained from these approximate repair strategies, but fully optimized results cannot be achieved unless the cleaned shapes and the shapes within their lithographic environment are tuned in a model-based environment. Take the method of figure 1d, for example. The original correction on the right-hand figure was derived in the presence of the corrected shape of the left hand figure. By

removing the left hand bump for repair, the correction shape needed on the right hand figure is actually different than that originally calculated. In principle, any changes made to one part of a configuration should propagate to changes in all surrounding features. This effect is the compelling reason for embedding MR constraints into the correction process directly, so that an optimum, complying result can be obtained.

Figure 2 shows two approaches to solving a corner-to-corner violation, either using the sizing and Boolean "cut" technique or by moving edges. The Boolean cut method affects only two of the four edges involved in the violation, and this restriction limits the ability to maintain OPC accuracy. Doubling the degrees of freedom by adjusting all four edges improves our ability to find an optimized configuration. Changing segment length and leveraging criticality can be applied more effectively.

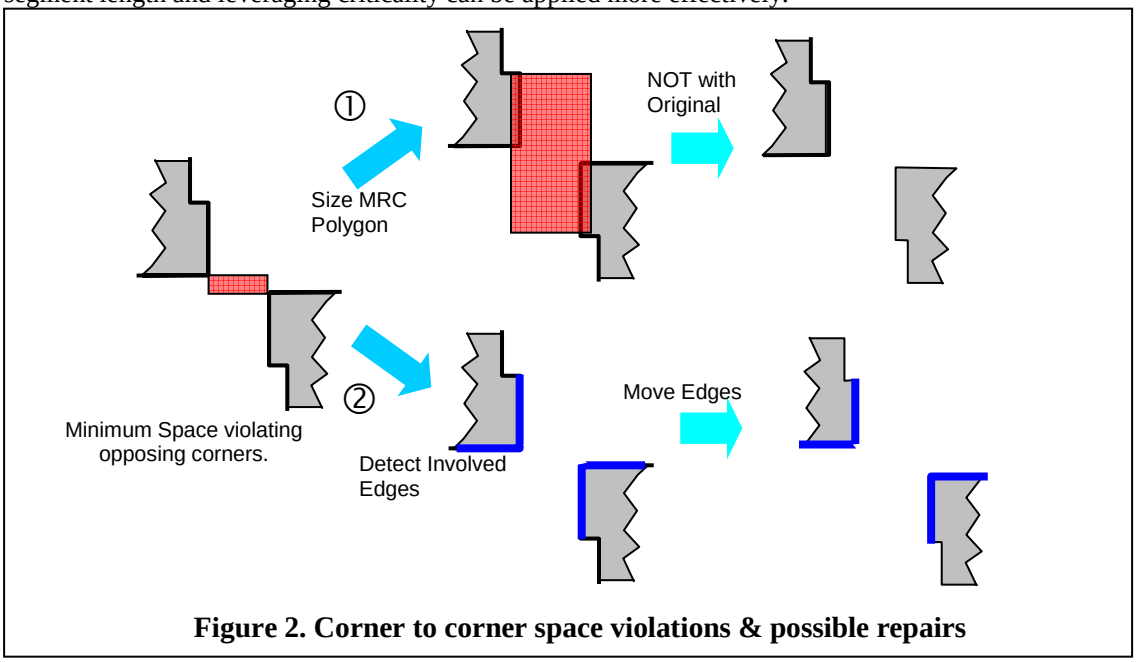

Figure 2. Corner to corner space violations & possible repairs

Figure 3 shows the added complexity when 45° edges are involved. The sizing and Boolean approach would either result in mouse bites or impose asymmetric corrections on these structures. Although edge based solutions fare much better, the complexity of the OPC logic can increases dramatically as each topological case needs to be detected and handled differently.

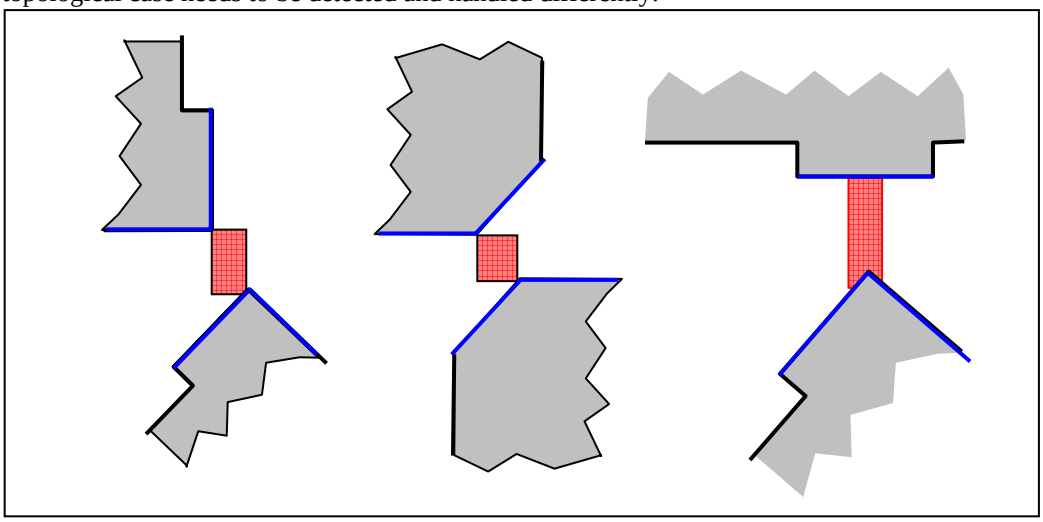

Figure 3. Complications multiply when MRC violations include angled edges.

4. Approaches to enforcing MRC compliance using the OPC tool

To achieve MRC compliant OPC with optimal lithographic correction, the constraint mechanisms must be tightly integrated with the model-based optimization mechanisms. The most robust way to do this is to detect MR dimensional limits on every edge in all correction iterations. When MR constraints on edge movements compete with model-directed edge movements, optimization strategies involving neighboring edges are invoked. This assures that when a lithographically viable, compliant configuration exists, it will be found through an iterative relaxation process, and that resulting OPC quality is minimally affected everywhere in the vicinity of the constraint stress point.

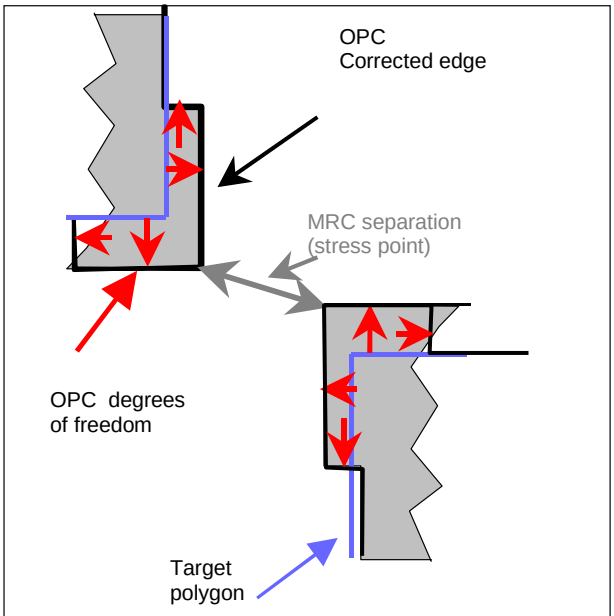

Figure 5 – Illustrates 8-degrees of freedom available for OPC accuracy

Figure 5 illustrates eight degrees of freedom (edges that can be moved) in the vicinity of a corner to corner stress point.

In cases where no compliant and lithographically-accurate configuration exists, there are a few options based on user criteria. MR compliance can be programmed to trump lithographic accuracy, or vice versa, or the difference can be split by user-defined preference. These decisions can be keyed from companion criticality marker layers provided with the target pattern. In all cases the offending stress point will be marked in the OPC output.

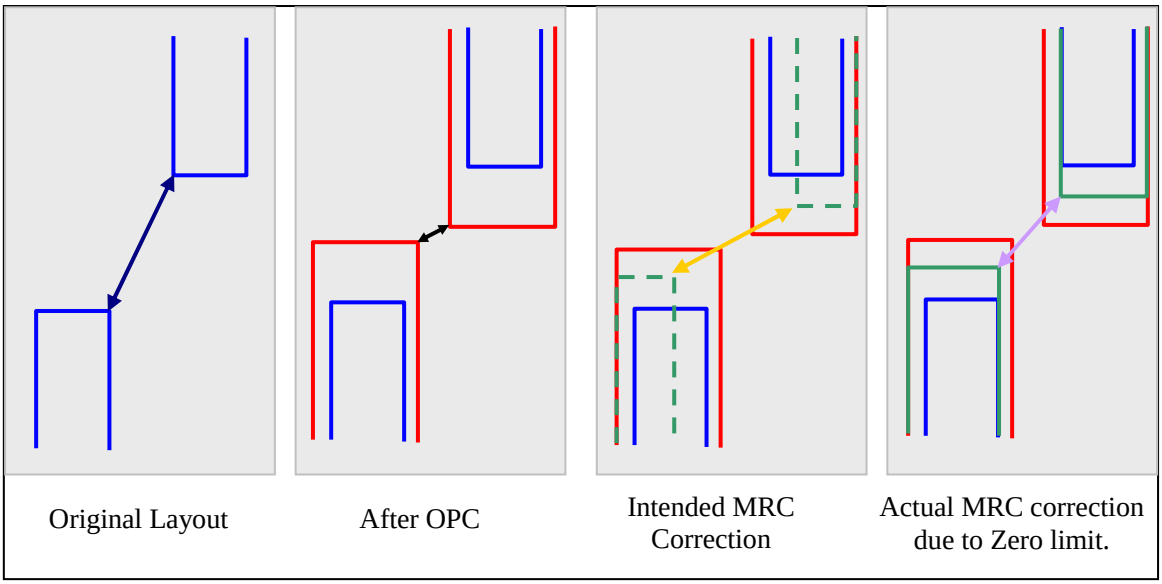

Figure 6 – Limitations of correction along post-OPC corner-to-corner Vector for offset opposing line-ends.

Figure 6 shows offset opposing line ends which, after OPC correction, have a larger correction perpendicular to the line-end but only a small correction in width. This causes an MRC error vector that lies relatively flat. If the correction is then applied along the direction of this vector--the direction one would expect would require the smallest segment displacement--the amount of horizontal adjustment could be significantly more than was applied by the OPC. This could result in the segment moving back from its original design position, possibly leading to a width based MRC error if not trapped by the code.

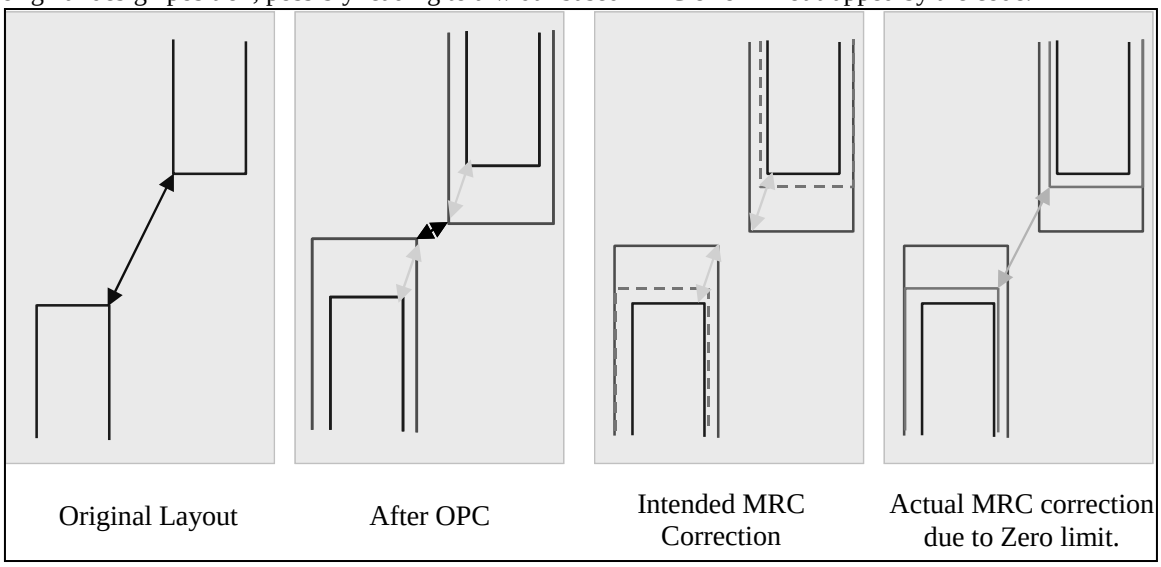

Figure 7 – Improvements to enforceability of MRC correction when applied along the vector of the OPC correction.

Figure 7 shows another approach, where the adjustment is made along the vector of the OPC correction. In this case the segments that made the biggest contribution to the MRC error are those that have to move the most to compensate for it. Although the first algorithm may lead to the minimal change in chrome area and maybe also the minimum lithographic impact, this technique is the safest in terms of avoiding new MRC errors (assuming the pre-corrected pattern was MRC compliant). An optimal approach will probably switch between the two techniques depending on the geometries involved.

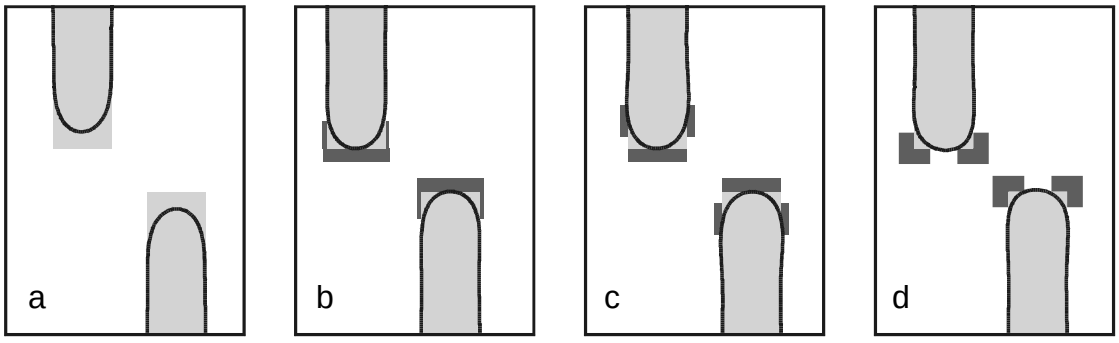

Figure 8: Alternative line end treatments with different corner-spacing implications

Basic correction style can influence susceptibility to MRC violations. Figure 8 illustrates three alternative line-end correction styles (b,c,d) that provide equivalent nominal corrections (lithographic differences are more pronounced in defocus conditions). By inspection we see that style d is the most susceptible, and style c is the least.

5. Integrating MRC compliance enforcement into the OPC correction flow

OPC is typically applied in a number of iterations (see Fig. 9), with a fraction of the determined ideal segment offset actually being applied after each iteration. This means the segments tend to move towards their ideal positions determined from the latest segment offsets, but allow the impact of their neighbors' correction to also have an influence on where that ultimate ideal position may be. At any time in this iteration loop there may be an MRC violation between two or more segments. By applying the MRC error detection and enforcement algorithm, these offending segments can be moved back and excluded from further OPC corrections. This allows their neighboring segments to perhaps move further than they would have otherwise to compensate for their "frozen" neighboring segments. Having the MRC enforcement program as an OPC subroutine makes integration of this into a correction recipe very easy.

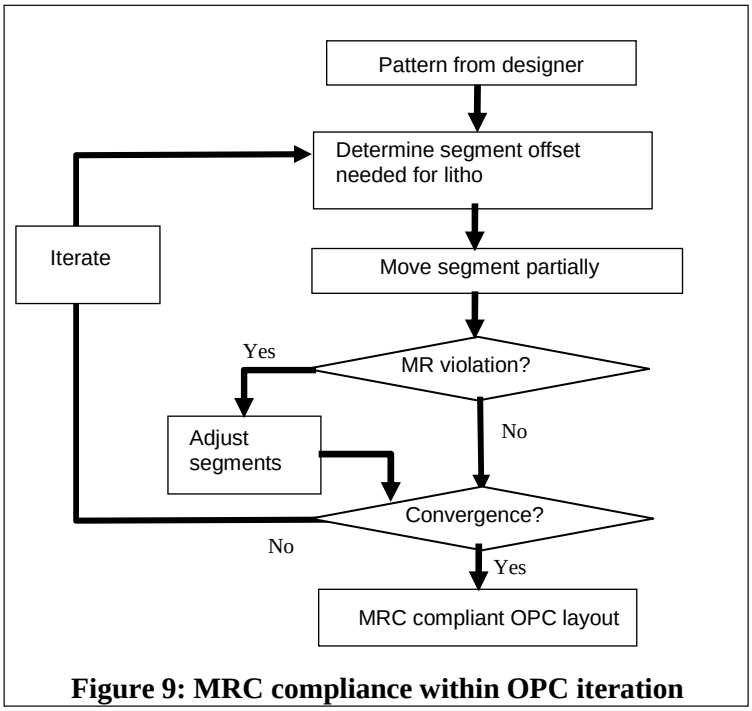

Figure 9: MRC compliance within OPC iteration

An example of the difference between integrated and non-integrated MRC enforcement is shown in Figure 10. Here a narrow poly transistor is terminated in an asymmetric end-cap defined by a trim and a Phase Shift Mask. This process has a low MEEF and results in large segment offsets, particularly across the critical transistor where the narrow chrome spacing starts to see a corner. In this example two approaches to MRC enforcement are compared. In the first case, MRC enforcement occurs only after the OPC correction is completed, for instance by analyzing the corrected pattern in a DRC tool. In this case we see that two opposing segments have moved inwards resulting in an MRC violation. The cleanup simply returns these two segments to their original position without any consideration of lithographic impact. The actual effect of this is to create a shallower rounding of the end cap, widening the transistor at the Active Area edge. When the MRC constraint is integrated into the OPC recipe and applied after each iteration, we see that the segments next to the previously MRC corrected segment have compensated for the previously violating segments being pinned (by not moving so far out) and the corner rounding in the simulated image is less. This leads to tighter CD control at the gate edge.

6. Conclusions

Mask layout rule compliance (MRC) has evolved from Design Rule compliance (DRC) to be an independent set of constraints governing mask synthesis. Relative to the design space, geometry in the mask space is highly interdependent – a change in one location can propagate to many other features in the vicinity of the change. Therefore mask rule compliance strategies must be tightly integrated into the

model-based correction environment to ensure the highest possible lithographic accuracy, as we have demonstrated.

Nonetheless, mask rule constraints are colliding with accuracy requirements. New strategies are needed to resolve layout configurations that have no correction that provides required silicon accuracy while simultaneously complying with all mask fabrication constraints. We expect solutions to emerge from two fronts: 1) more degrees of freedom in doing OPC from access to variable tolerance specifications associated with the original design artwork, and 2) relaxation of certain mask constraints – especially those driven by algorithmic weakness in mask tool architectures not bearing on lithography physics or mask process.

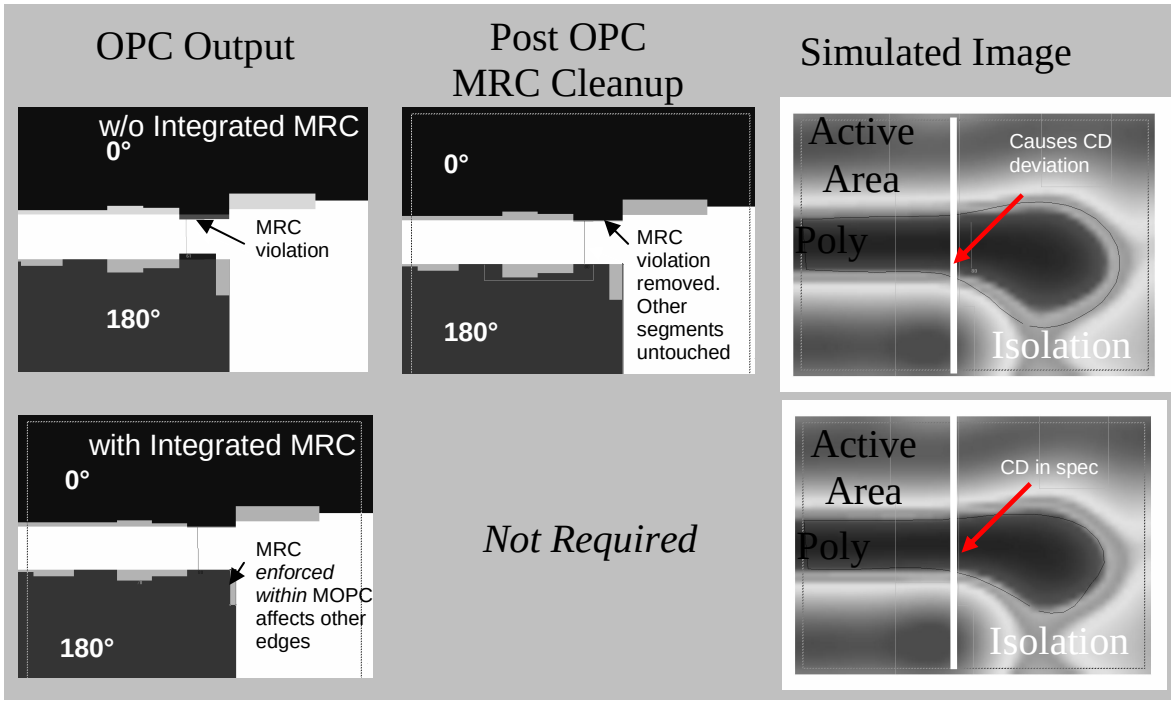

Figure 10 - Improved Pattern Fidelity achievable by doing MRC after each OPC iteration, compared to doing only a post-OPC MRC cleanup

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