Full-chip Process Window aware OPC capability assessment *

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ABSTRACT

In the past technology generations, Optical Proximity Correction (OPC) has been applied using a model capturing the Optical proximity effects in a single focal plane. In the newer generations, this method is more and more difficult to maintain because of very small process windows in specific situations. These specific situations include 1D configurations (e.g. isolated small lines) but increasingly complex 2D configurations.

In the more advanced technology nodes 2D configuration are starting to play a much bigger role. Process windows need to be preserved in all cases, and so this brings about another challenge for the OPC flow. The more traditional OPC approaches may result in un-acceptable small process window in such cases, whereas well characterized Process Window aware OPC (PW-OPC) can provide better results, with much less engineering interventions.

In this paper the method of Process Window aware OPC is applied on special designed test structures and on a larger scale (full chip). Verifications and assessments are demonstrated and compared with alternatives. In the past OPC engineers have been pushing for more and more design constraints in order to allow the OPC flow to be successful. The PW-OPC approach is more adaptive compared with traditional single focal plane OPC, and can still converge to an acceptable solution in complicated (unforeseen) layout configurations, without the need to introduce complicated design constraints.

Keywords: OPC Process window, Process window aware OPC, layout DoE

INTRODUCTION

The typical OPC product flow is aimed to achieve best edge placement error (EPE) at nominal process condition with best focus and nominal exposure dose. This flow has been working well for generation up until 90nm. However at the more advanced technology with low k1 lithography the correction with best the EPE at nominal condition could possibly result in serious CD variation or pinch/bridge at process conditions away from the best focus and exposure condition [1]. To ensure good process window performance under realistic focus and exposure variations, the simulated non-ideal process conditions need to be taken into account during the OPC evaluations.

In this paper the basic principle of process window aware OPC is demonstrated. After this explanation, the technique is applied on different lines as function of pitch. In this analysis it is clear that process window of certain CD pitch combinations can be improved at the cost of CD performance or EPE at best best focus. Finally it is applied on real data. For this a 45nm logic technology metal pattern is used.

In order to make the recipe tuning more efficient a novel optimization technique is used and demonstrated towards the end of this paper. Using the Synopsys test pattern generator (STPG) layouts are synthesized in which certain parameters are varied in a DoE like manner. Since these layouts are rather small, OPC runtime is kept to a minimum, which allows quick cycles in recipe tuning possible. This in turn allows for faster recipe development cycles.

PROCESS WINDOW AWARE OPC

* paper number 6730-98

Photomask Technology 2007, edited by Robert J. Naber, Hiroichi Kawahira
Proc. of SPIE Vol. 6730, 67302U, (2007) · 0277-786X/07/$18 · doi: 10.1117/12.746839

In the process window aware based based OPC recipe, traditional model-based OPC using a nominal model is applied to the pattern for the first iterations. In the following OPC iterations, process window checking and correction is added to locate and fix any unacceptable contour deviations. During the process window check, the recipe samples a region parallel to each segment both inside and outside the pattern. Depending on the geometry, this region may extend past the ends of the segment, as shown in Figure 1.

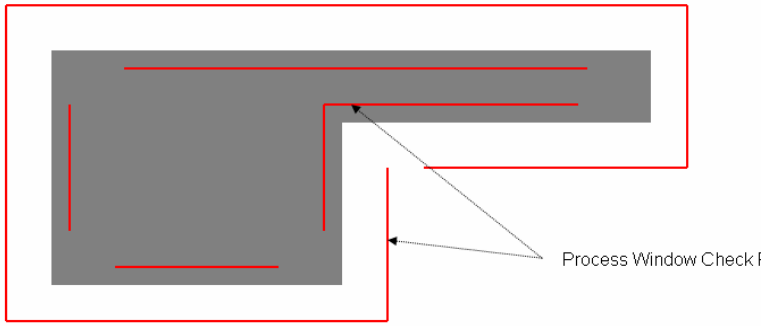


Figure 1: The process window recipe samples a region parallel to each segment.

Process window corner models are used to determine the worst process deviation on the segment. Figure 2 shows that if a violation is found using any model, an additional constraint is added to the segment for the remaining correction iterations.

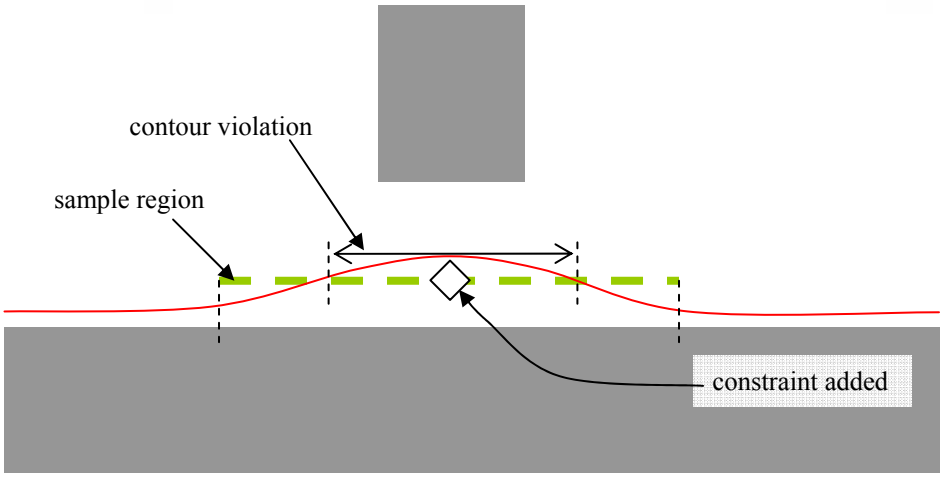


Figure 2: If during any iteration a violation is encountered in any of the models, an additional constraint is added for the remaining iterations.

While traditional model-based OPC attempts to find the edge position that minimizes the contour error at a single location, PW-OPC balances the error at the segment's evaluation point with any other constraints

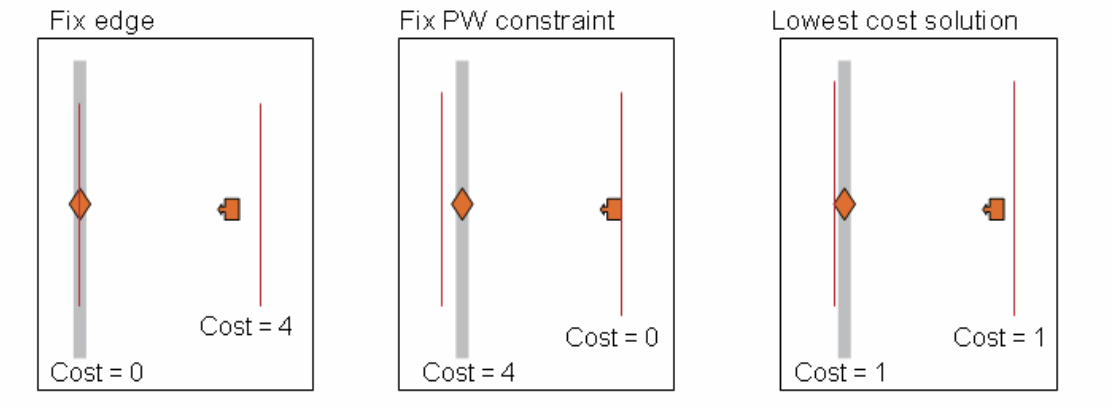


Figure 3: The process window recipe uses a cost function to achieve the best possible solution. To the left is the classic edge based approach.

due to process violations. This is accomplished using a cost function that places a weight on the error for each constraint. The correction then finds the minima for the cost function in order to determine the best possible edge position.

RECIPE ANALYSIS AND TUNING APPROACH

For the development and evaluation of the process window based recipe, two sources of geometric data are used. The first dataset is obtained by shrinking and re-sizing the metal1 patterns of an older generation logic-type design. For this purpose a 65nm node Synopsys generated logic layout was shrunk and re-sized to match 45nm metal1 design rules with minimum width and space of 65nm. The main objective of this pattern is to help identify problematic configurations, by running a complete logic type of design. A full Silicon versus Layout (SiVL) analysis is used to track the problem areas in the layout.

The second method of data generation gives us the ability to generate more specific study cases. The Synopsys test pattern generator (STPG) is a layout synthesizer, designed to generate small layout configurations in a design of experiment (DoE) fashion. STPG is used to automatically generate very flexible model calibration test patterns or recipe tuning test patterns. It also automatically generates required information about these test patterns such as user documentation, formatted model building input tables, and automatic SEM measurement recipe files for several metrology vendors. This makes a detailed study of certain known problem areas possible. In Figure 4 an example of such a layout detail is shown. This structure is a well-known critical layout configuration for a gate poly correction recipe. The STPG tool can easily and quickly generate a large set of such structures, with programmed variations for various parameters, including assessment gauge locations. The whole test pattern is still small, which makes it possible to make quick cycles during the recipe tuning, and allows for a more systematic and faster recipe development and tuning.

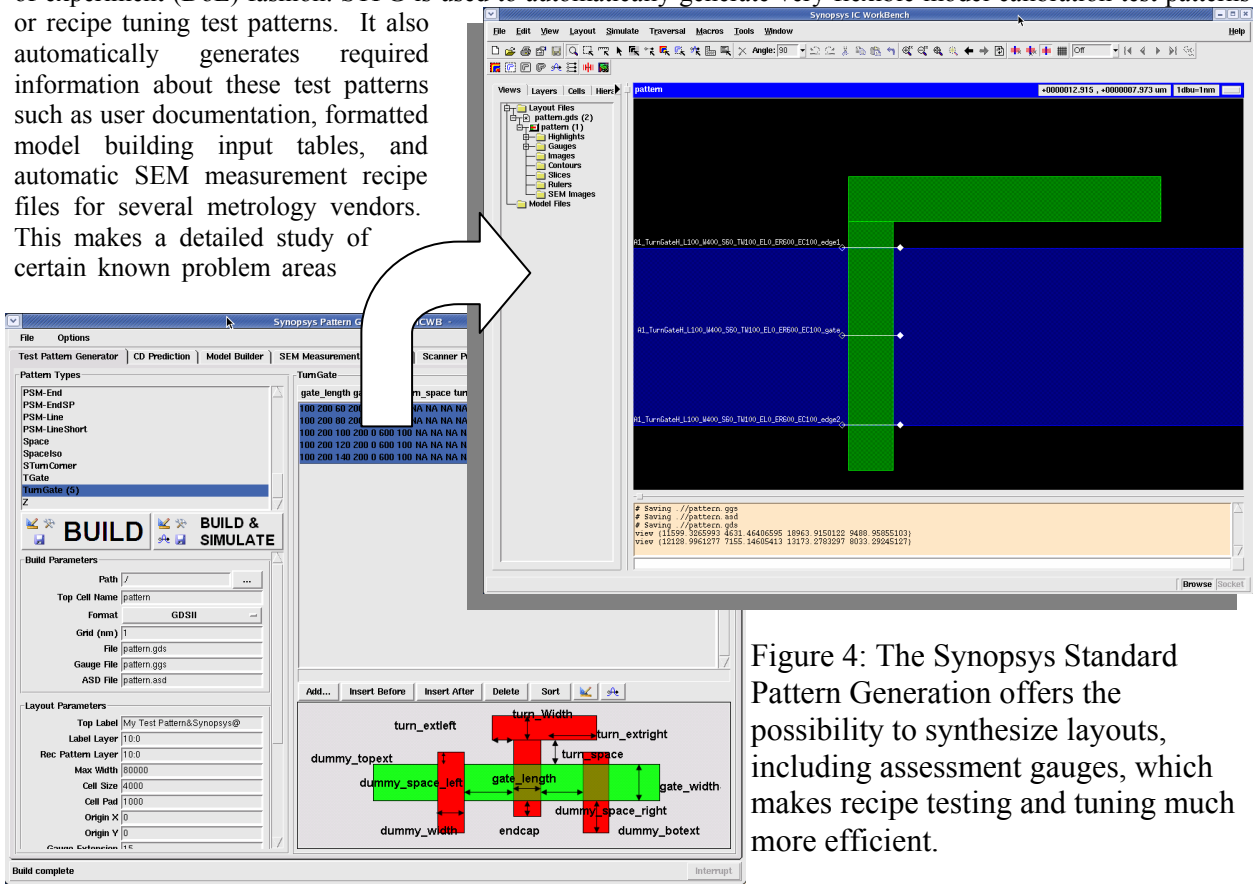


Figure 4: The Synopsys Standard Pattern Generation offers the possibility to synthesize layouts, including assessment gauges, which makes recipe testing and tuning much more efficient.

EXPERIMENTAL RESULTS

For the testing and demonstration purposes, a 45nm metal1 process is used. For this purpose the following Process Window model is created:

- NA: 1.07 (immersion)
- Illumination: Annular (σ = 0.68 … 0.93)
- Defocus window: +/-80nm
- Exposure dose variation: +/- 3%

The nominal exposure is set such that a 65nm mask (1X) line on a 130nm pitch prints as a 65nm line in resist. This model has a film stack with parameters, which can be considered common for 45nm metal1 patterning. In this experimental analysis example, 3 types of analysis are carried out. At first a simple 1D analysis is studied comparing a conventional OPC and a process window aware OPC, which shows clearly that by sacrificing the best focus CD performance a little bit, a significant improvement can be achieved as far as the overall process window. Then the same comparison is done on some real 45nm metal data, and finally a case study of a known critical feature is studied and results of this are shown.

Depending on the type of layer, the success criteria need to be set. For this metal layer study, 3 criteria are set:

- minimum pinch CD deviation through the full process window of the model
- minimum bridge CD space it is possible to set success criteria
- minimum contact coverage percentage through the full process window of the model

Clearly for other layers different target values are required, and even a certain differentiation may be desirable, for example field poly versus gate poly.

1D PATTERN EVALUATION

The effect of process window aware OPC can best be demonstrated using simple 1D structures with a varying pitch, shown in the little inset in Figure 5. We generated two sets of 1D patterns using STPG to evaluate the basic performance of the Process aware recipe. In one set the line width is kept to one value (65nm) and the space is used

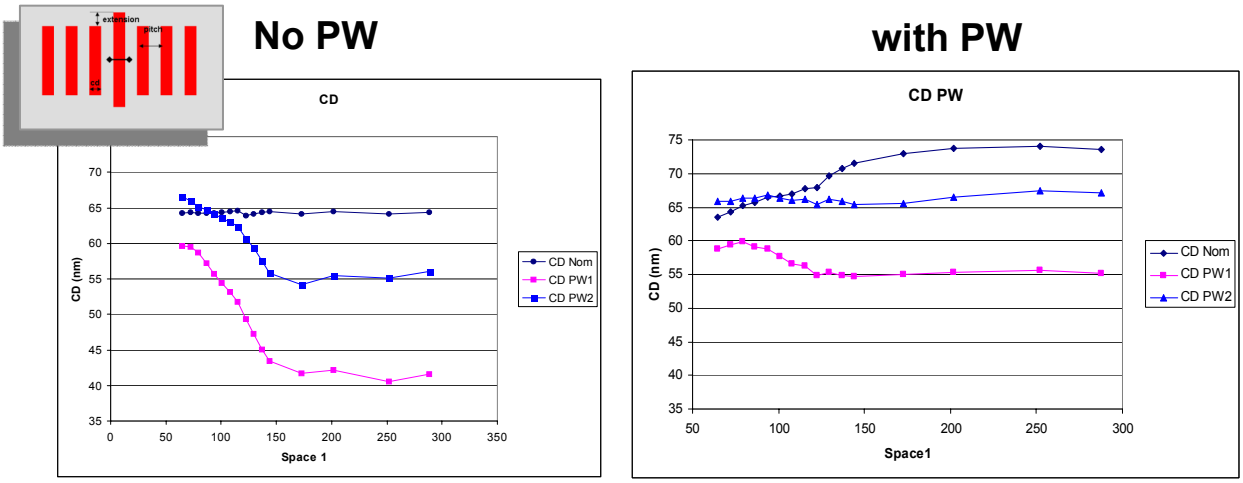


Figure 5: In this study CD vs pitch structures are OPC corrected with a normal OPC recipe (right) and a process window aware OPC recipe (left). By slightly sacrificing the best focus EPE, it is possible to improve the overall process window. The PW1 model has a maximum defocus and dose to the lower limit, while PW2 has the same defocus number but a maximum overdose value.

as a free parameter (65nm and up) to assess line CD control through process window. In a second the space is kept fix at its minimum value (65nm) and with width of the line is varied from 65nm and up.

We first evaluate if certain success criteria are feasible with these test patterns and this OPC recipe. Then process window constraint parameters are optimized using test patterns in order to achieve these success criteria. In this example these success criteria for this metal layer are set to 15% change in CD and space. Proteus OPC is applied on the test patterns with both a normal OPC recipe and a process window aware OPC recipe. The CD assessment is done in the ICWB layout analyzer with a nominal model and two process window corner models. PW1 is a model with maximum defocus and lowest dose while PW2 is also maximum defocus and maximum over dose.

Plots of analysis with the constant line CD versus space are shown in Figure 5. Without process window aware OPC the CD of an isolated line evaluated with PW1 model reaches a value of around 40nm. After we turn on process aware feature and with proper PW constraint setting worst case CD with process variations is around 55nm which is within our success criteria, and thus in-spec. The price we paid to achieve this improvement is very obvious from the left graph in Figure 5: the best focus CD error for a 300 nm spaced line goes from practically zero up to 9nm. If this is an acceptable tolerance under the given process variations, no assisting features are required for this process.

Through this simple 1D pattern study we conclude that our success criteria are achievable if we allow for some sacrifice of the CD control at nominal process condition. If tighter CD control is required under the same process variations, insertion of assisting features (AFs) is a logical next set.

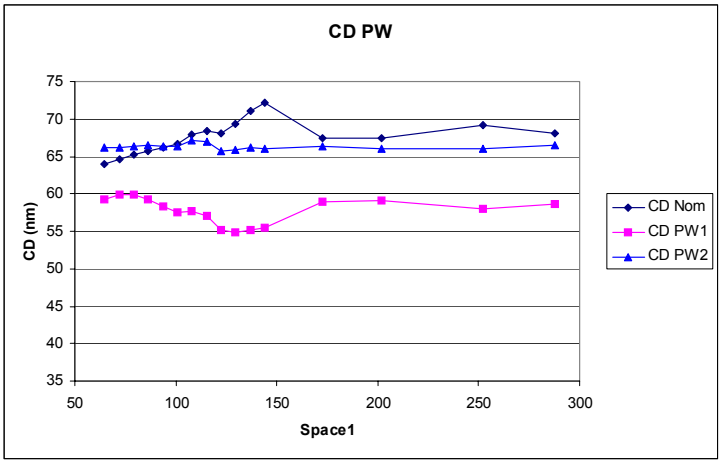


Figure 6: If the CD variation as a function of space and process variations are too big, it can be improved when assisting features are introduced. Compare this graph with the graphs in Figure 2. By comparing these graphs one can see that AF area inserted at a space of 150nm.

We next analyze what the impact of assisting features is. Assist features are inserted using Proteus AF on this pattern group. CD assessment is evaluated after Process window aware OPC. The result is shown in Figure 6. CD control is improved for lines with spaces larger than 150nm. Clearly below 150nm there is no change because there

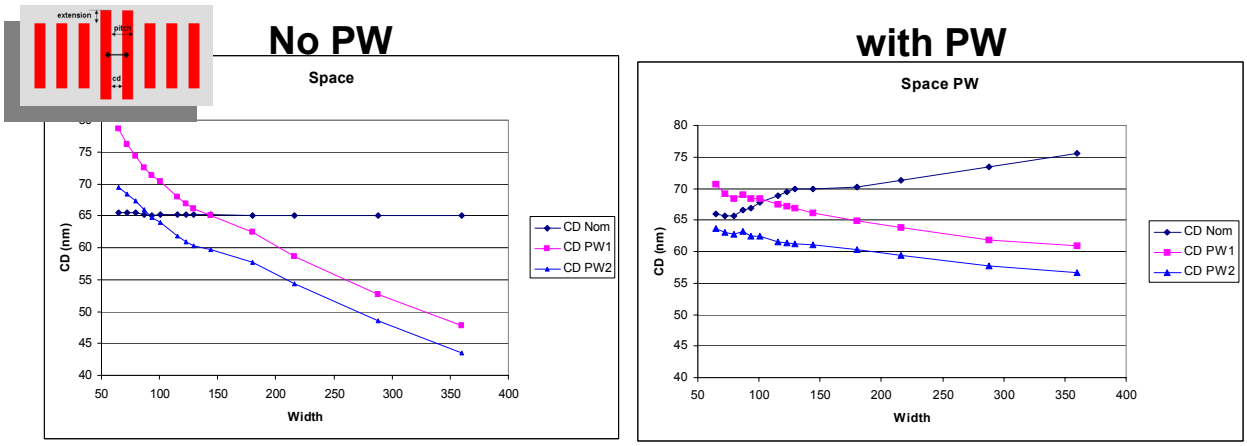


Figure 7: These graphs show the impact of the process aware OPC recipe: better process window at the cost of space CD control for wider lines.

is no space to insert AFs.

In our study of the metal layer, we were able to achieve the required process window for all line-space combinations, and thus the use of AFs was not required. This simplifies the RET flow as well as the mask.

Similar to the method used on CD width plots, we evaluated the space CD control with different width through process window. From this 1D pattern study we can draw the same conclusion as for the line CD study: the specs for the space CD control can be achieved without the use of (negative) AFs by the use of a process aware OPC recipe. Naturally negative sizing of metal features at a small space can have a derogatory electrical device impact if the negative sizing was performed in areas where contacts or vias connect to the metal.

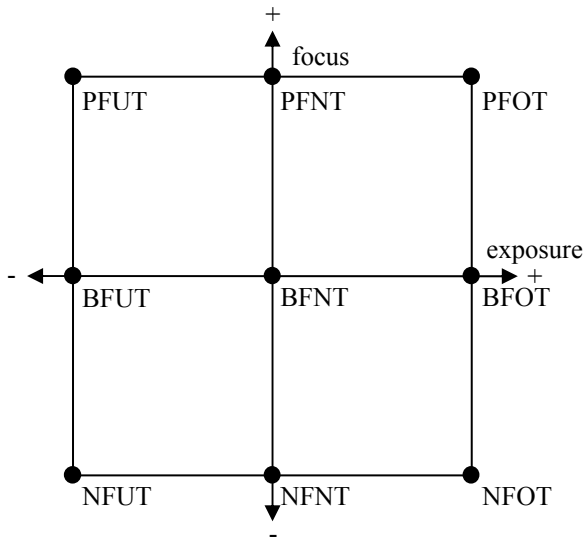


Figure 8: During the SiVL run 9 process conditions are evaluated: the 9 corners plus the centre (nominal) condition.

FULL CHIP EVALUATION

In this chapter we describe the results of a full chip assessment of the process window aware OPC recipe. For this purpose we used the earlier described metal 1 pattern of a 65nm design, scaled and sized to mimic a 45nm design. Two OPC recipes are applied to the data in two separate runs. Then the two resulting OPC correction results are assessed using SiVL.

For the SiVL run 9 process conditions are evaluated (see Figure 13). For this purpose the following Process Window model is created:

- BFNT: Best Focus Nominal threshold
- BFOT: Best Focus over threshold
- BFUT: Best Focus under threshold
- PFNT: Positive Defocus Nominal threshold
- PFOT: Positive Defocus over threshold
- PFUT: Positive Defocus under threshold
- NFNT: Negative Defocus Nominal threshold
- NFOT: Negative Defocus over threshold
- NFUT: Negative Defocus under threshold

Note that for a metal 1 pattern (at a given defocus value) the over threshold condition will have CDs smaller than at nominal threshold and visa-versa for under threshold.

The two dot plot charts [2] of the SiVL run for the line pinch error is shown in Figure 9, with the normal nominal OPC run on the right and the process window aware OPC run on the right. The 1D analysis already indicated that without the process window aware option, a lot of CDs would be out of specification. This SiVL run of the best focus OPC run shows that very clearly. With the process window aware OPC recipe, there are hardly any SiVL violations left. There is no difference in the nominal condition in terms of error flags. Clearly the CD in the nominal case *is* changed, as is clear from the 1D case study. But the graphs in Figure 9 only show SiVL violations, which in fact are 'out of spec' situations. There is significant improvement in pinch control overall, the most significant improvement is at worst process corner at defocus over threshold. In this case the worst case pinch is improved from around 35nm to 54nm.

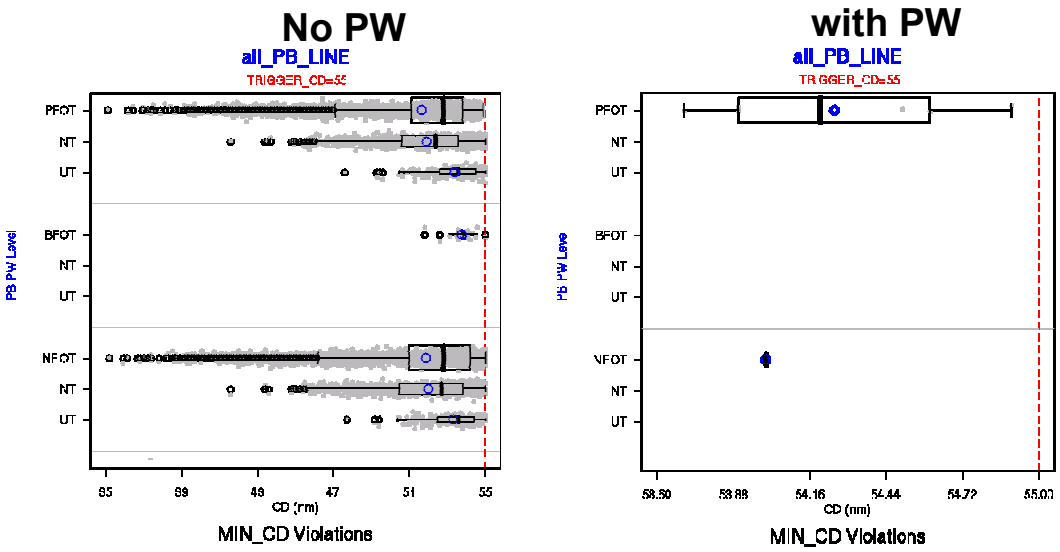


Figure 9: SiVL error reports for the different process conditions of the process window aware OPC recipe (right) and the standard recipe (left). Note that the scale on the X-axis is quite different. The process window aware OPC recipe eliminates almost all SiVL violations avoiding the need of assisting features.

In Figure 10 a few snapshots of post OPC layout and contour simulated with the worst case model are shown. The process window for an isolated line end and corner is obviously enlarged with the process aware recipe. The process window aware recipe is able to deliver an almost perfect result with very little development effort.

For the space structures a similar improvement is achieved. There too the results are almost perfect. The dot plot charts of the SiVL space bridge runs are shown Figure 11. Worst case space bridging through the process window is improved from around 50.5nm to 54.5nm.

The last check performed by SiVL is the contact overlap check, again using the same 9 process conditions as with the lines and spaces. The dot plot charts of the remaining SiVL violations are shown in Figure 12. Worst case contact coverage through the process window is improved from 72% to 88%.

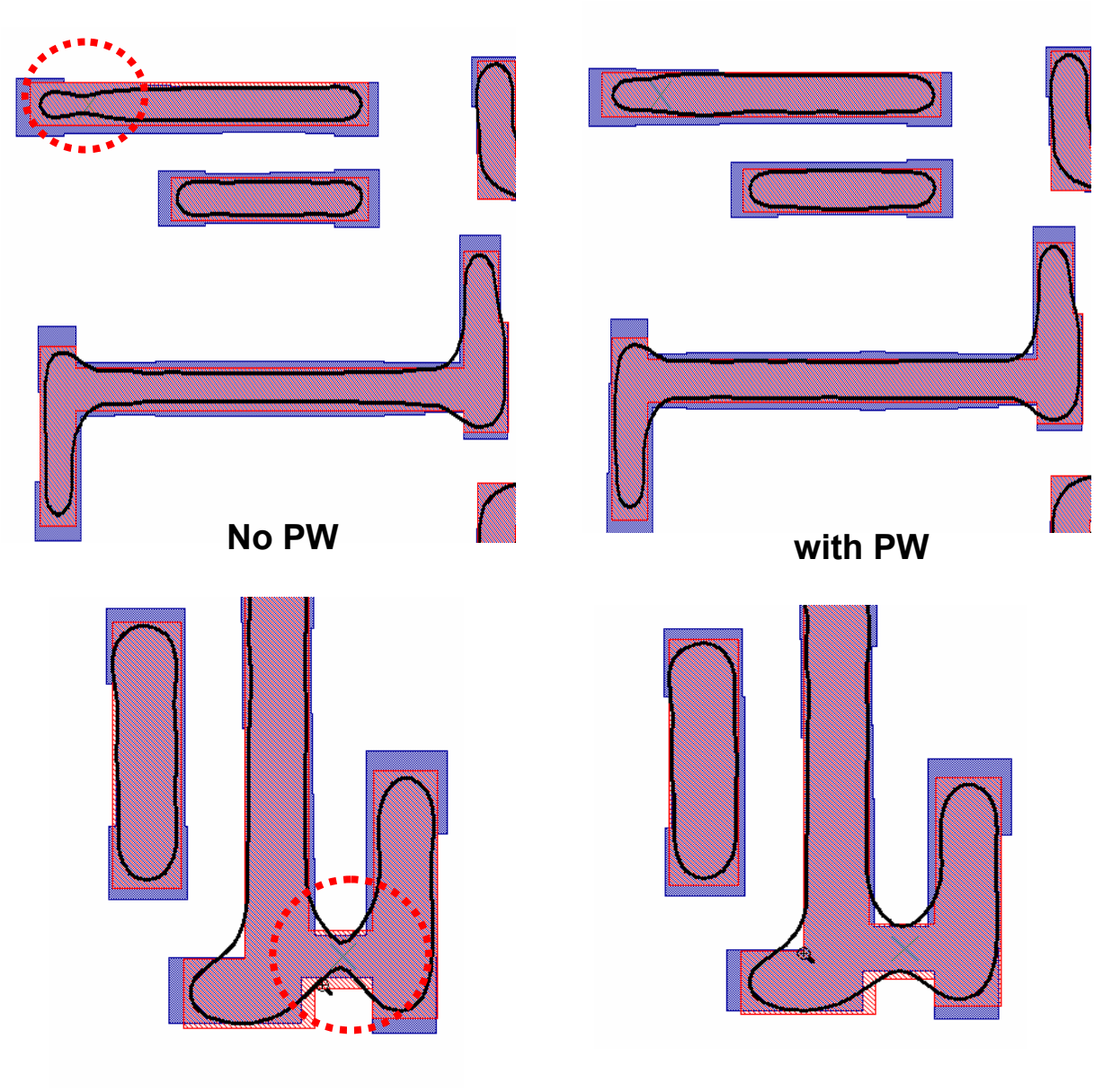


Figure 10: This figure shows 2 locations with and without the process window aware option switched on. The contour shows the PFOT process condition. Note that the difference in OPC is very subtle.

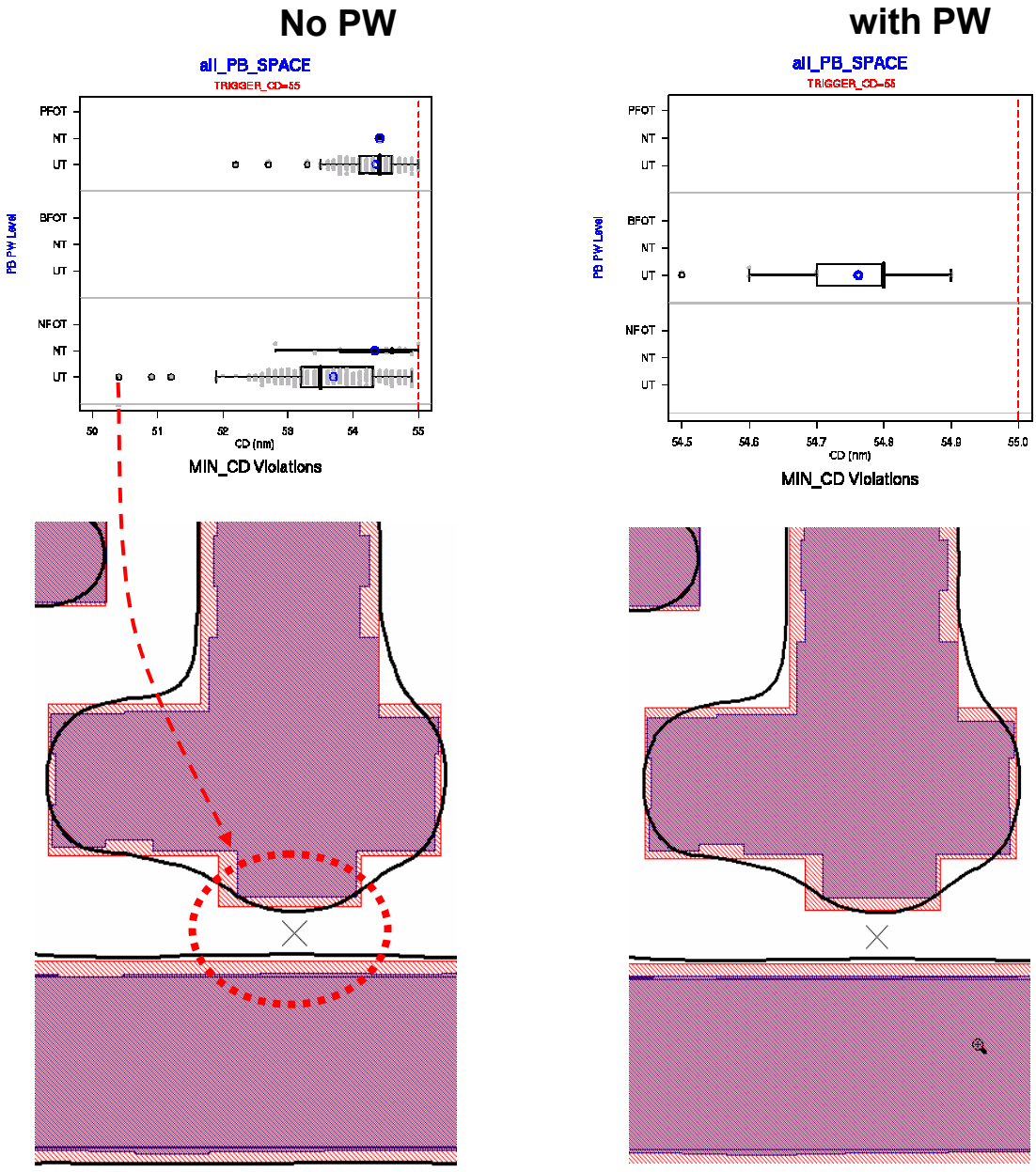


Figure 11: The results of the SiVL analysis, plus the worst case location. The process window aware resolved almost all violations. Note that the scale in the graphs are not the same.

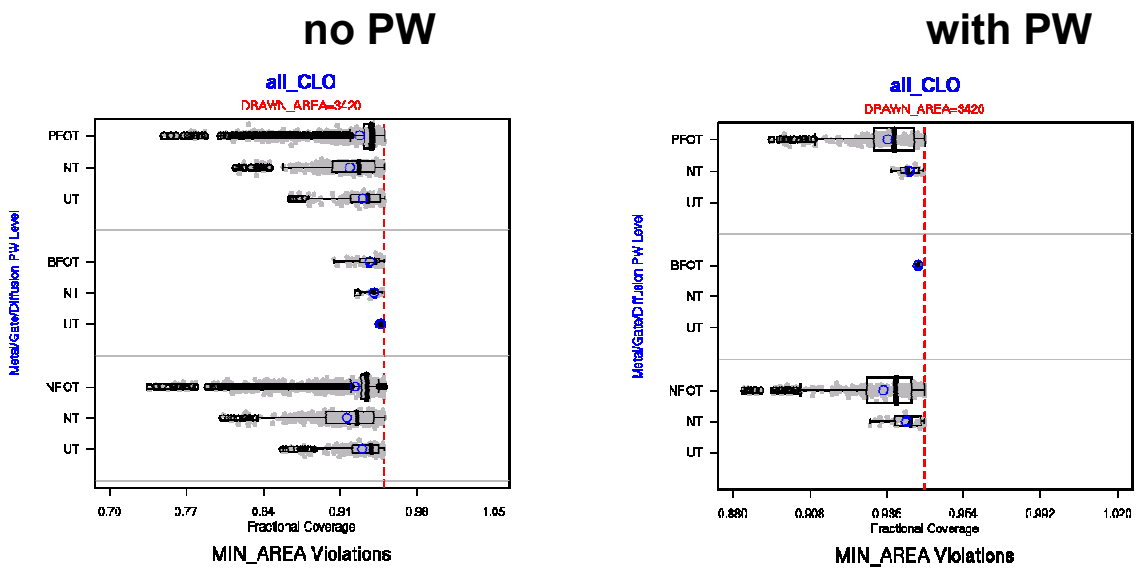
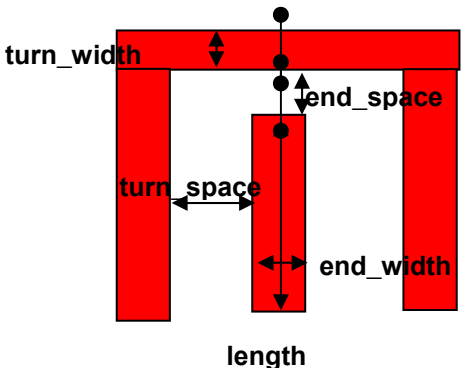


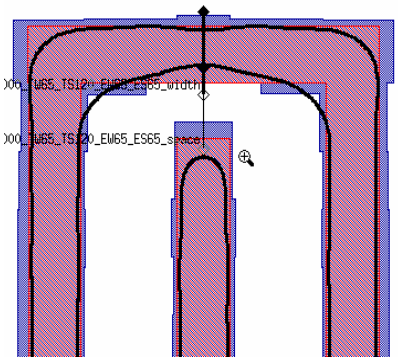
Figure 12: The results of the contact overlap SiVL check for the two OPC solutions, with and without the process window aware feature. Note the difference in X-axis scale.

PATTERN DOE STUDY EXAMPLE

To test robustness of the recipe and ensure more pattern coverage, we use STPG to generate a challenging 2D pattern which can be considered 'typical' for metal layouts patterns. Based on the metal design rules stated in the above text, a set of this type of pattern is generated. The gauges which are generated along with the test patterns are then assessed in ICWB.

A pattern library with few DOE variables is created in STPG. We create a pattern DOE to generate a group of test patterns within design rule constraints. Then we run the pattern library through Proteus OPC, and do the assessment in ICWB using the assessment gauges. A full SiVL check is not needed, because at this point it is





turnSpace	CD PW
65	58.03345
70	51.72736
75	58.38697
80	59.50606
85	50.87665
90	49.20766
95	45.84648
100	42.39951
105	46.24412
110	40.4549
115	44.53752
120	39.9667
125	42.75555

Figure 13: An example of a layout DoE, which is used in recipe optimization.

known to the engineer where the most critical width or space is going to occur. In this particular case we found the

layout parameter *turnSpace* is the most critical parameter, as depicted in Figure 13. As can be seen, pinch control was initially not ideal in this DoE element. By using this approach we will find worst case layout configurations to challenge the recipe and then can tune the OPC recipe to improve them.

CONCLUSIONS

In this paper a typical 45nm process metal RET flow was studied, and a process window aware OPC recipe was analyzed and compared with a traditional nominal-only process condition recipe. The Process window aware recipe produced a result with very little remaining SiVL violations with very little effort. With the model and the design rules used in this study, we were able to produce results with a decent process window, without the use of assisting features.

The Synopsys STPG is a very practical tool to generate layout details, which can be used for OPC recipe development and tuning. STPG not only generates the layouts in a DoE like fashion, but also creates assessment gauges on programmed locations. The size of the generated gds file is small, which makes the OPC runtime small and allows for efficient assessment and thus fast recipe tuning cycles

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