

ECEN 454

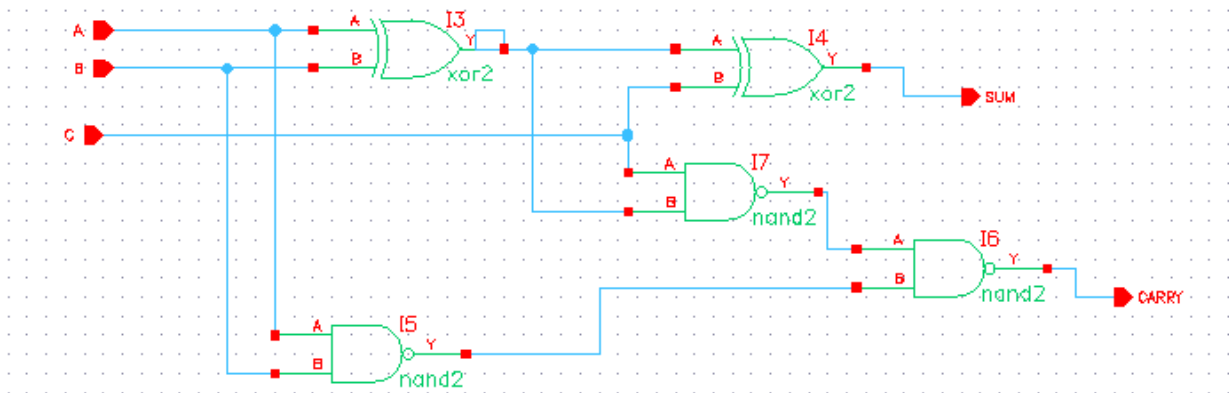
Lab 1

Roberto Luis

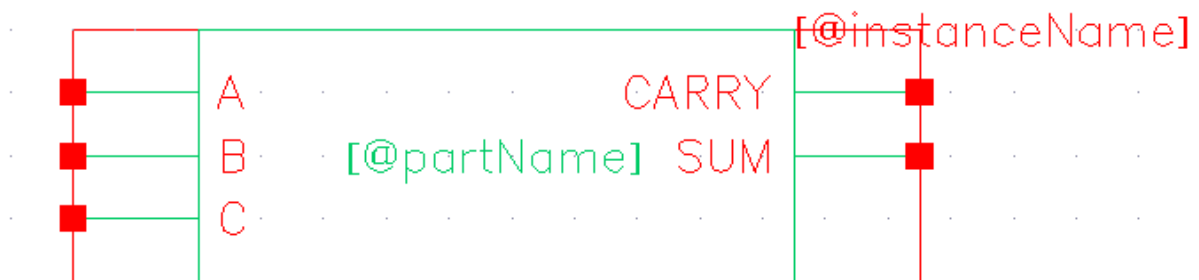
Section 505 - Rahul

Full Adder

Schematic:



Symbol:



testfixture.verilog:

```
testfixture - Notepad
File Edit Format View Help
// Verilog stimulus file.
// Please do not create a module in this file.

// Default verilog stimulus.

initial
$monitor ($time," A=%b, B=%b, C=%b, SUM=%b, CARRY=%b", A, B, C, SUM, CARRY);

initial
begin
    A = 1'b0;
    B = 1'b0;
    C = 1'b0;

    #50 A=1'b0; B=1'b0; C=1'b1;           //ABC=001
    #50 A=1'b0; B=1'b1; C=1'b0;           //ABC=010
    #50 A=1'b0; B=1'b1; C=1'b1;           //ABC=011
    #50 A=1'b1; B=1'b0; C=1'b0;           //ABC=100
    #50 A=1'b1; B=1'b0; C=1'b1;           //ABC=101
    #50 A=1'b1; B=1'b1; C=1'b0;           //ABC=110
    #50 A=1'b1; B=1'b1; C=1'b1;           //ABC=111
end
```

simout.tmp:

```
simout - Notepad
File Edit Format View Help
|
ncx1mode: *W,DLCVAR (/home/ugrads/r/roberto.jluis/cds.lib,1): cds.lib Invalid environment variable ''.

-----
Relinquished control to SimVision...
ncsim>
ncsim> source /opt/coe/cadence/INCISIVE152/tools/inca/files/ncsimrc
ncsim> database -open shmWave -shm -default -into shm.db
Created default SHM database shmWave
ncsim> probe -create -shm test -all -depth 1
Created probe 1
ncsim> run

      0 A=0, B=0, C=0, SUM=0, CARRY=0
      50 A=0, B=0, C=1, SUM=1, CARRY=0
     100 A=0, B=1, C=0, SUM=1, CARRY=0
     150 A=0, B=1, C=1, SUM=0, CARRY=1
     200 A=1, B=0, C=0, SUM=1, CARRY=0
     250 A=1, B=0, C=1, SUM=0, CARRY=1
     300 A=1, B=1, C=0, SUM=0, CARRY=1
     350 A=1, B=1, C=1, SUM=1, CARRY=1

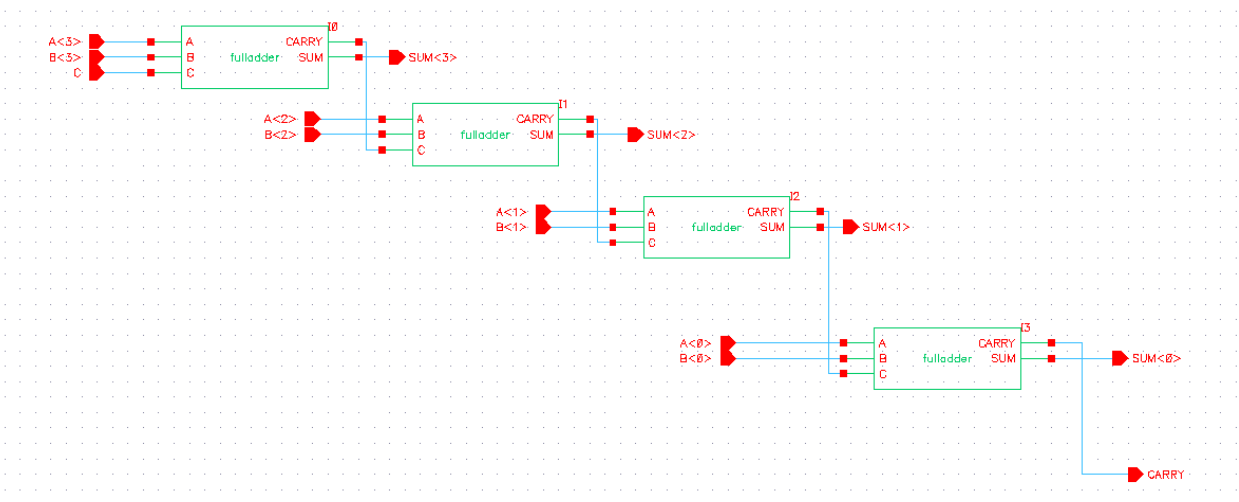
ncsim> reset
Loaded snapshot worklib.test:template
ncsim> run -adjacent

      0 A=0, B=0, C=0, SUM=0, CARRY=0
      50 A=0, B=0, C=1, SUM=1, CARRY=0
     100 A=0, B=1, C=0, SUM=1, CARRY=0
     150 A=0, B=1, C=1, SUM=0, CARRY=1
     200 A=1, B=0, C=0, SUM=1, CARRY=0
     250 A=1, B=0, C=1, SUM=0, CARRY=1
     300 A=1, B=1, C=0, SUM=0, CARRY=1
     350 A=1, B=1, C=1, SUM=1, CARRY=1

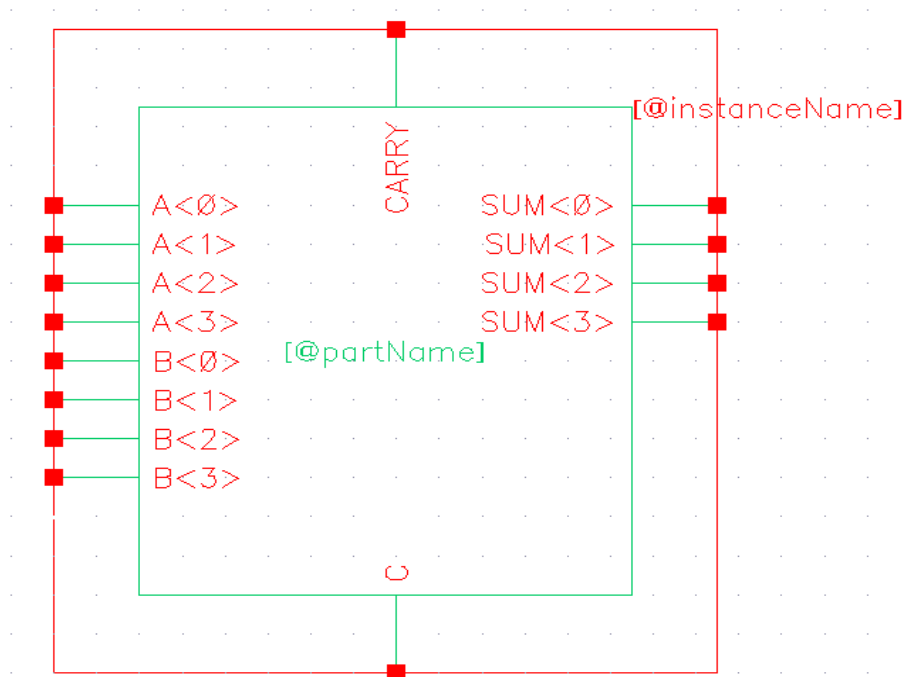
ncsim> reset
<
Ln 1, Col 1    100%    Unix (LF)    UTF-8
```

4 bit adder

Schematic:



Symbol:



testfixture.verilog

```
File Edit Format View Help
// Verilog stimulus file.
// Please do not create a module in this file.

// Default verilog stimulus.

initial
begin
    A[0] = 1'b0;
    A[1] = 1'b0;
    A[2] = 1'b0;
    A[3] = 1'b0;
    B[0] = 1'b0;
    B[1] = 1'b0;
    B[2] = 1'b0;
    B[3] = 1'b0;
    C = 1'b0;

#50 A=4'b0001; B=4'b0000; C=1'b0;           //ABC=000
#50 A=4'b0000; B=4'b0001; C=1'b0;           //ABC=000
#50 A=4'b0001; B=4'b0001; C=1'b0;           //ABC=000
#50 A=4'b0010; B=4'b0010; C=1'b0;           //ABC=000
#50 A=4'b0100; B=4'b0100; C=1'b0;           //ABC=000
#50 A=4'b1000; B=4'b1000; C=1'b0;           //ABC=000
#50 A=4'b1010; B=4'b1010; C=1'b0;           //ABC=000
#50 A=4'b1111; B=4'b1111; C=1'b1;           //ABC=001
#50 A=4'b0101; B=4'b0101; C=1'b1;           //ABC=000
#50 A=4'b0000; B=4'b0000; C=1'b1;           //ABC=000

end

initial
$monitor ($time," A=%b, B=%b, C=%b, SUM=%b, CARRY=%b", A, B, C, SUM, CARRY);
```

simout.tmp:

```
simout - Notepad
File Edit Format View Help
SOFTINCLUDE $SYSTEM_CDS_LIB_DIR/cds.lib
|
ncxlmode: *W,DLCVAR (/home/ugrads/r/roberto.jluis/cds.lib,1): cds.lib Invalid environment variable ''.
SOFTINCLUDE $SYSTEM_CDS_LIB_DIR/cds.lib
|
ncxlmode: *W,DLCVAR (/home/ugrads/r/roberto.jluis/cds.lib,1): cds.lib Invalid environment variable ''.
SOFTINCLUDE $SYSTEM_CDS_LIB_DIR/cds.lib
|
ncxlmode: *W,DLCVAR (/home/ugrads/r/roberto.jluis/cds.lib,1): cds.lib Invalid environment variable ''.

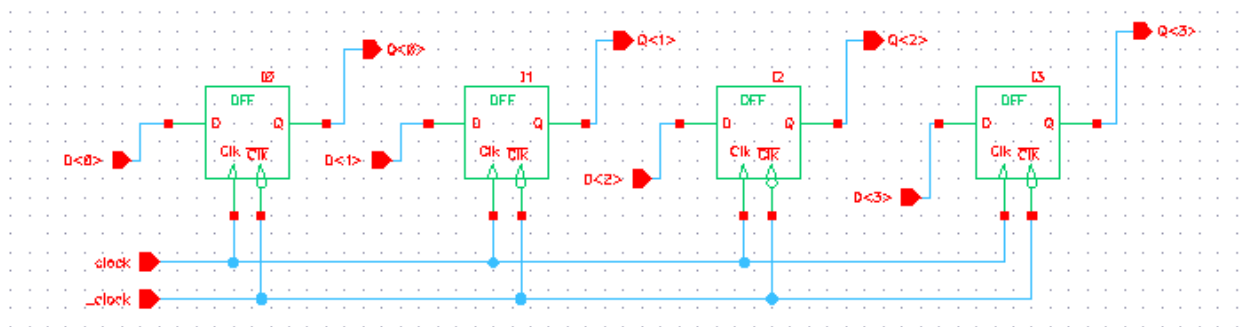
-----
Relinquished control to SimVision...
ncsim>
ncsim> source /opt/coe/cadence/INCISIVE152/tools/inca/files/ncsimrc
ncsim> database -open shmWave -shm -default -into shm.db
Created default SHM database shmWave
ncsim> probe -create -shm test -all -depth 1
Created probe 1
ncsim> run

      0 A=0000, B=0000, C=0, SUM=0000, CARRY=0
      50 A=0001, B=0000, C=0, SUM=0001, CARRY=0
     100 A=0000, B=0001, C=0, SUM=0001, CARRY=0
     150 A=0001, B=0001, C=0, SUM=0010, CARRY=0
     200 A=0010, B=0010, C=0, SUM=0100, CARRY=0
     250 A=0100, B=0100, C=0, SUM=1000, CARRY=0
     300 A=1000, B=1000, C=0, SUM=0000, CARRY=1
     350 A=1010, B=1010, C=0, SUM=0100, CARRY=1
     400 A=1111, B=1111, C=1, SUM=1111, CARRY=1
     450 A=0101, B=0101, C=1, SUM=1011, CARRY=0
     500 A=0000, B=0000, C=1, SUM=0001, CARRY=0

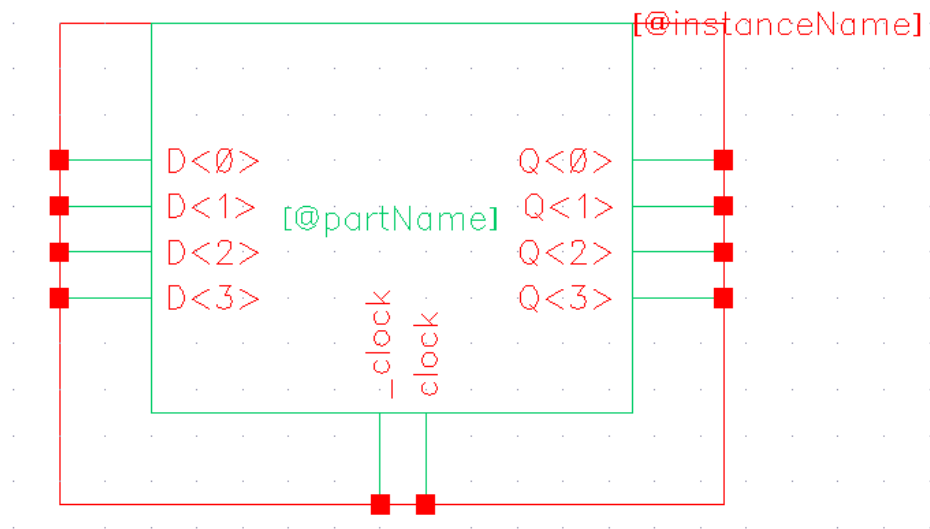
ncsim>
```

4 bit register:

Schematic:

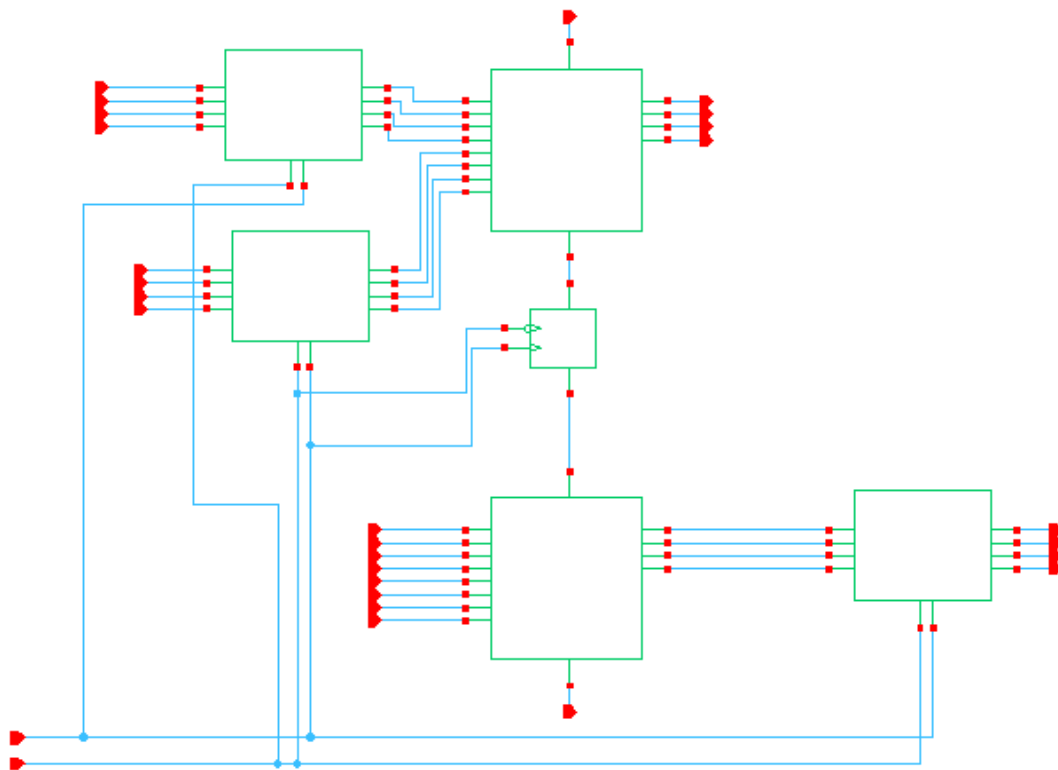


Symbol:

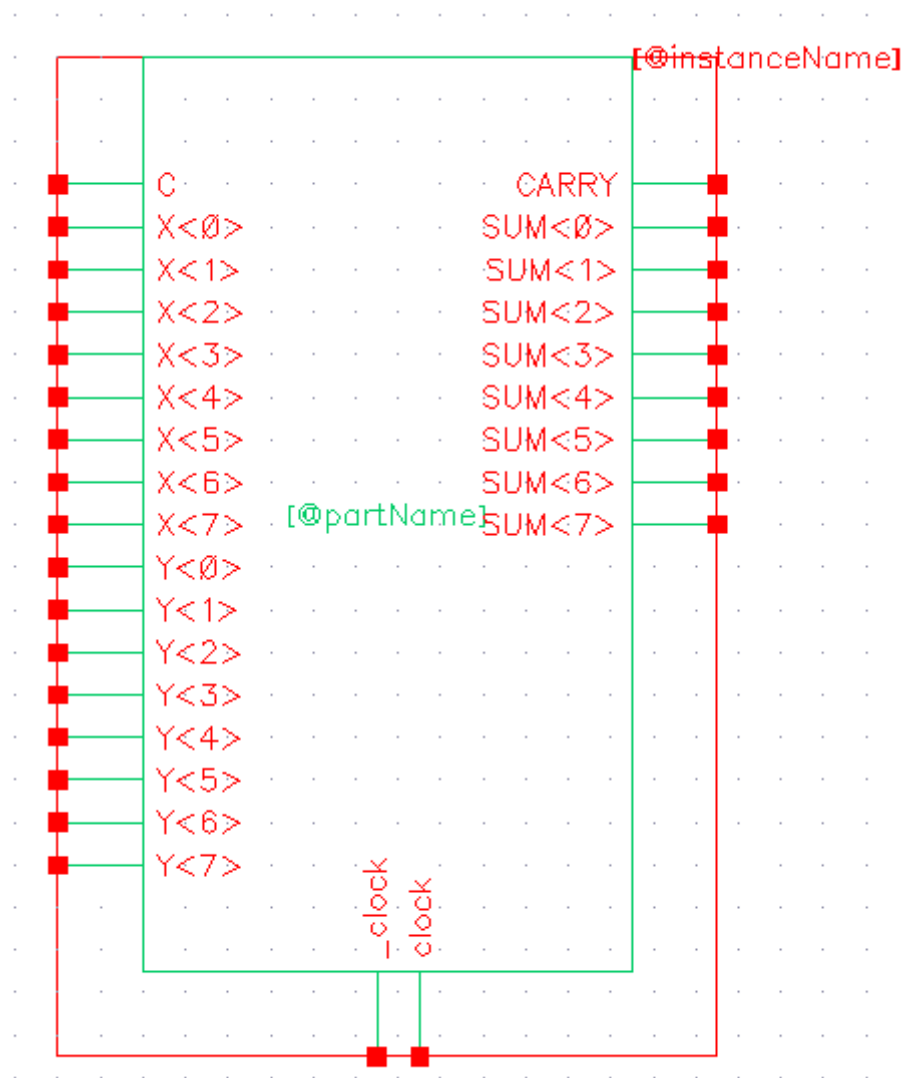


8-bit adder

Schematic:



Symbol:



testfixture.verilog:

```
testfixture - Notepad
File Edit Format View Help

// Verilog stimulus file.
// Please do not create a module in this file.

// Default verilog stimulus.

initial
begin
    C = 1'b0;
    X[0] = 1'b0;
    X[1] = 1'b0;
    X[2] = 1'b0;
    X[3] = 1'b0;
    X[4] = 1'b0;
    X[5] = 1'b0;
    X[6] = 1'b0;
    X[7] = 1'b0;
    Y[0] = 1'b0;
    Y[1] = 1'b0;
    Y[2] = 1'b0;
    Y[3] = 1'b0;
    Y[4] = 1'b0;
    Y[5] = 1'b0;
    Y[6] = 1'b0;
    Y[7] = 1'b0;
    _clock = 1'b0;
    clock = 1'b0;

#50 X=8'b00000000; Y=8'b00000000; C=1'b0; clock=1'b0; _clock=1'b1; //X=00000000 Y=00000000 C=0 clock=0
#50 X=8'b00000000; Y=8'b00000000; C=1'b0; clock=1'b1; _clock=1'b0; //X=00000000 Y=00000000 C=0 clock=1
#50 X=8'b01111110; Y=8'b11100111; C=1'b0; clock=1'b0; _clock=1'b1; //X=01111110 Y=00000000 C=0 clock=0
#50 X=8'b01111110; Y=8'b11100111; C=1'b0; clock=1'b1; _clock=1'b0; //X=01111110 Y=00000000 C=0 clock=1
#50 X=8'b11111111; Y=8'b00000000; C=1'b1; clock=1'b0; _clock=1'b1; //X=11111111 Y=00000000 C=1 clock=0
#50 X=8'b11111111; Y=8'b00000000; C=1'b1; clock=1'b1; _clock=1'b0; //X=00000000 Y=00000000 C=1 clock=1
#50 X=8'b10101010; Y=8'b01010101; C=1'b0; clock=1'b0; _clock=1'b1; //X=10101010 Y=01010101 C=0 clock=0
#50 X=8'b10101010; Y=8'b01010101; C=1'b0; clock=1'b1; _clock=1'b0; //X=10101010 Y=01010101 C=0 clock=1
#50 X=8'b10101010; Y=8'b01010101; C=1'b1; clock=1'b0; _clock=1'b1; //X=10101010 Y=01010101 C=1 clock=0
#50 X=8'b10101010; Y=8'b01010101; C=1'b1; clock=1'b1; _clock=1'b0; //X=10101010 Y=01010101 C=1 clock=1
#50 X=8'b11001100; Y=8'b00110011; C=1'b0; clock=1'b0; _clock=1'b1; //X=11001100 Y=00110011 C=0 clock=0
#50 X=8'b11001100; Y=8'b00110011; C=1'b0; clock=1'b1; _clock=1'b0; //X=11001100 Y=00110011 C=0 clock=1
#50 X=8'b11001100; Y=8'b00110011; C=1'b1; clock=1'b0; _clock=1'b1; //X=11001100 Y=00110011 C=1 clock=0
#50 X=8'b11001100; Y=8'b00110011; C=1'b1; clock=1'b1; _clock=1'b0; //X=11001100 Y=00110011 C=1 clock=1

end

initial
$monitor ($time," X=%b, Y=%b, C=%b, SUM=%b, CARRY=%b, clock=%b, _clock=%b", X, Y, C, SUM, CARRY, clock, _clock);
```

Ln 1, Col 1	100%	Unix (LF)	UTF-8
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simout.tmp:

```
simout - Notepad
File Edit Format View Help
|
ncxlmode: *W,DLCVAR (/home/ugrads/r/roberto.jluis/cds.lib,1): cds.lib Invalid environment variable ''.

-----
Relinquished control to SimVision...
ncsim>
ncsim> source /opt/coe/cadence/INCISIVE152/tools/inca/files/ncsimrc
ncsim> database -open shmWave -shm -default -into shm.db
Created default SHM database shmWave
ncsim> probe -create -shm test -all -depth 1
Created probe 1
ncsim> run
      0 X=00000000, Y=00000000, C=0, SUM=xxxxxxx, CARRY=x, clock=0, _clock=0
     50 X=00000000, Y=00000000, C=0, SUM=xxxxxxx, CARRY=x, clock=0, _clock=1
    100 X=00000000, Y=00000000, C=0, SUM=00000000, CARRY=0, clock=1, _clock=0
    150 X=01111110, Y=11100111, C=0, SUM=00000000, CARRY=0, clock=0, _clock=1
    200 X=01111110, Y=11100111, C=0, SUM=01100101, CARRY=1, clock=1, _clock=0
    250 X=11111111, Y=00000000, C=1, SUM=01100101, CARRY=1, clock=0, _clock=1
    300 X=11111111, Y=00000000, C=1, SUM=00000000, CARRY=1, clock=1, _clock=0
    350 X=10101010, Y=01010101, C=0, SUM=00000000, CARRY=1, clock=0, _clock=1
    400 X=10101010, Y=01010101, C=0, SUM=11111111, CARRY=0, clock=1, _clock=0
    450 X=10101010, Y=01010101, C=1, SUM=11111111, CARRY=0, clock=0, _clock=1
    500 X=10101010, Y=01010101, C=1, SUM=00000000, CARRY=1, clock=1, _clock=0
    550 X=11001100, Y=00110011, C=0, SUM=00000000, CARRY=1, clock=0, _clock=1
    600 X=11001100, Y=00110011, C=0, SUM=11111111, CARRY=0, clock=1, _clock=0
    650 X=11001100, Y=00110011, C=1, SUM=11111111, CARRY=0, clock=0, _clock=1
    700 X=11001100, Y=00110011, C=1, SUM=00000000, CARRY=1, clock=1, _clock=0

ncsim> ^C
ncsim> exit
TOOL:  ncxlmode      15.20-s078: Exiting on Feb 07, 2022 at 23:54:22 CST (total: 00:05:43)
```