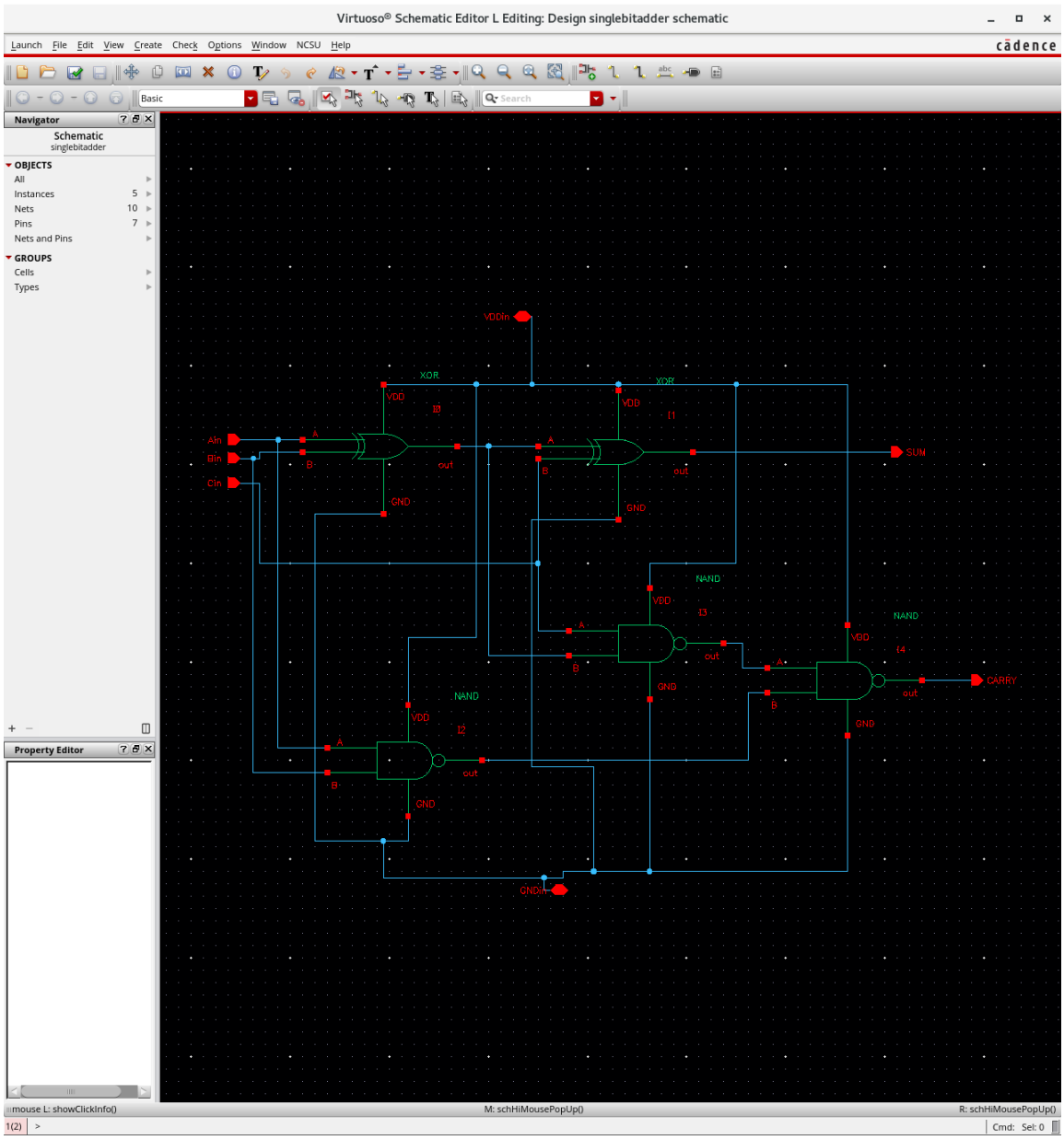
ECEN 454
Lab 4

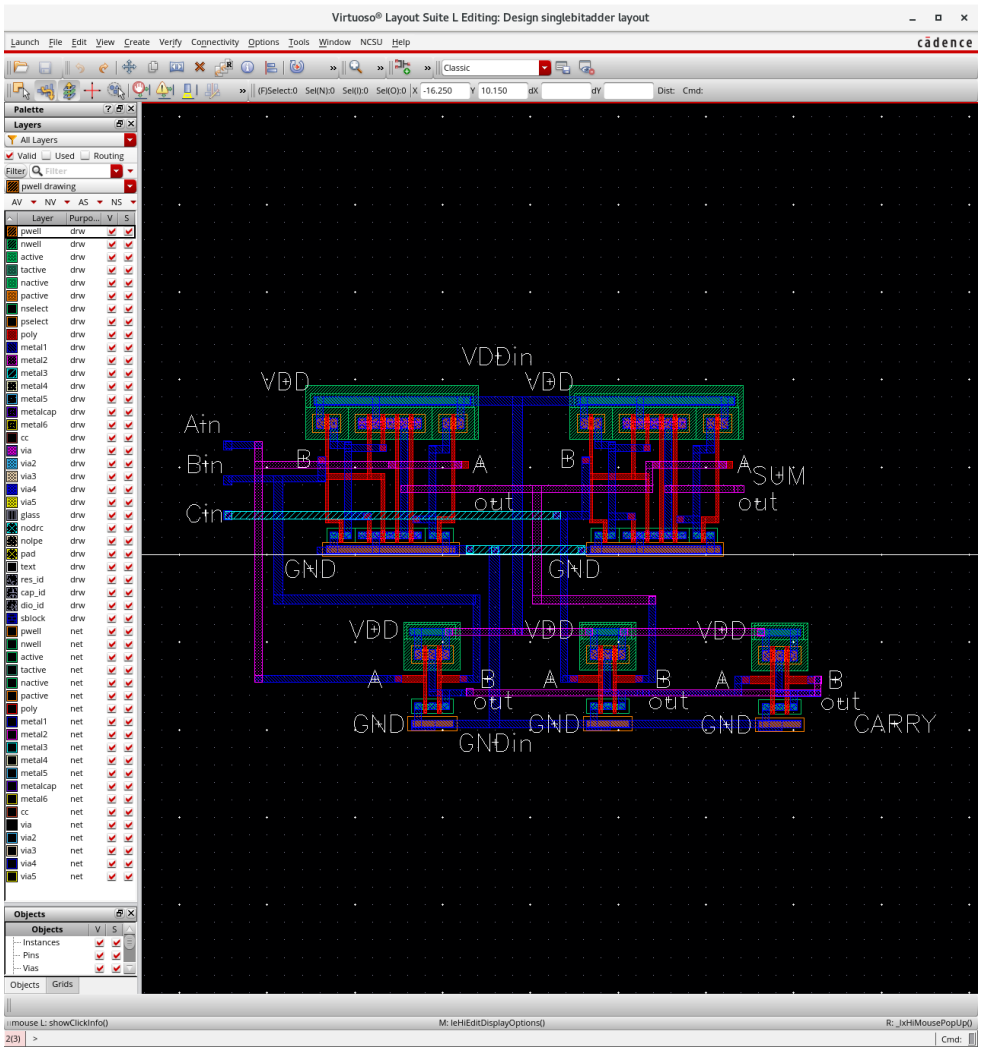
Roberto Luis
Section 505 - Rahul

1-bit Adder

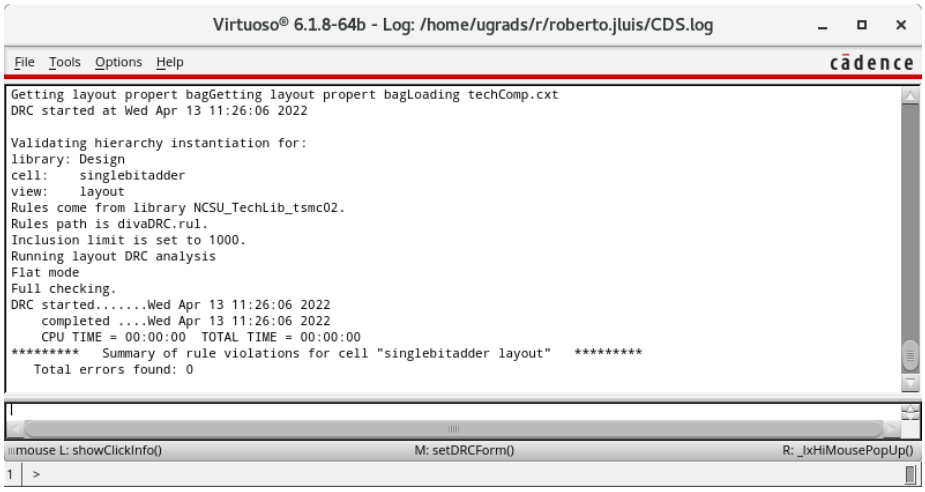
Schematic:



Layout:


Virtuoso® Layout Suite L Editing: Design singlebitadder layout
cadence
VDDin
VDD
VDD
Ain
Bin
Cin
B
A
B
A
SUM
out
out
GND
GND
VDD
VDD
VDD
A
B
A
B
A
B
out
out
out
GND
GND
GND
GNDin
CARRY

DRC:


Virtuoso® 6.1.8-64b - Log: /home/ugrads/r/roberto.jluis/CDS.log
File Tools Options Help
cadence
Getting layout propert bagGetting layout propert bagLoading techComp.cxt
DRC started at Wed Apr 13 11:26:06 2022
Validating hierarchy instantiation for:
library: Design
cell: singlebitadder
view: layout
Rules come from library NCSU_TechLib_tsmc02.
Rules path is divaDRC.rul.
Inclusion limit is set to 1000.
Running layout DRC analysis
Flat mode
Full checking.
DRC started.....Wed Apr 13 11:26:06 2022
completed ....Wed Apr 13 11:26:06 2022
CPU TIME = 00:00:00 TOTAL TIME = 00:00:00
********* Summary of rule violations for cell "singlebitadder layout" *********
Total errors found: 0
mouse L: showClickInfo()
M: setDRCForm()
R: _lxHiMousePopUp()

LVS:

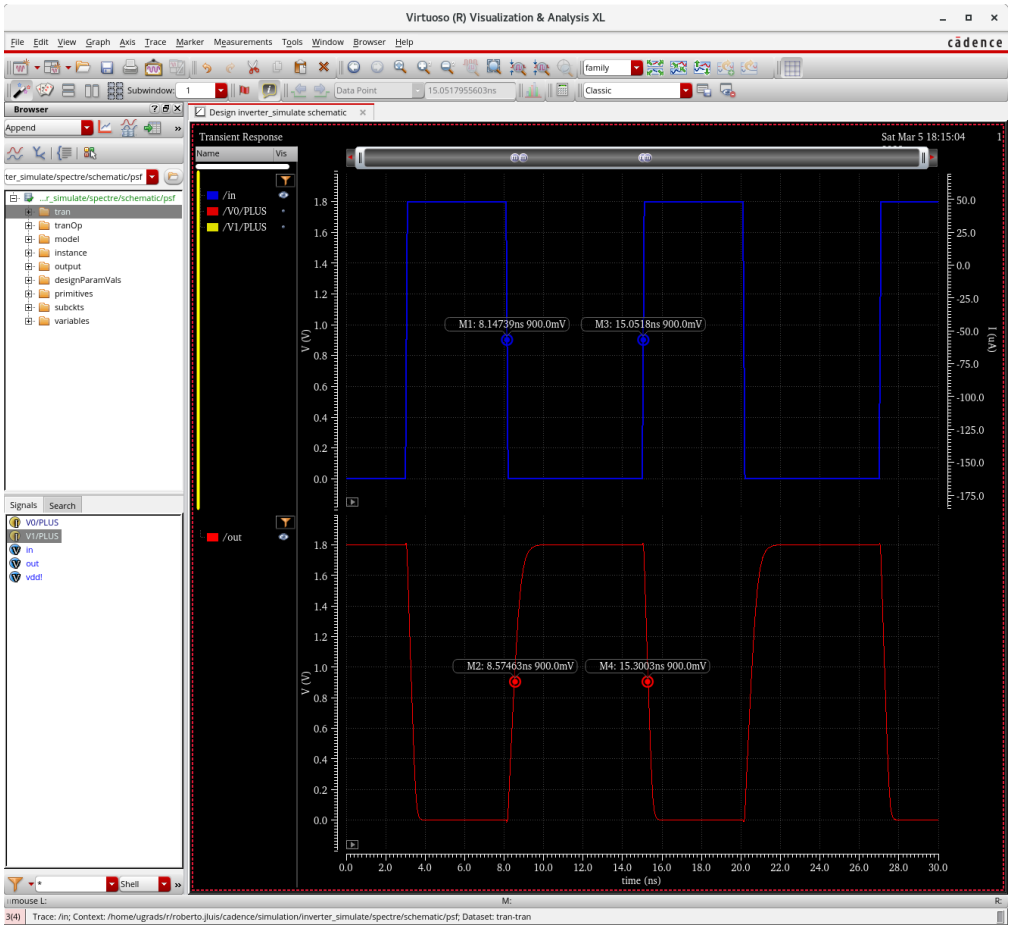
Open | si.log ~/ecen454/LVS | Save

```
Virtuoso Framework License (111) was checked out successfully. Total checkout time was 0.02s.

Running simulation in directory: "/home/ugrads/r/roberto.jluis/ecen454/LVS".

INFO (TECH-150003): The technology database "NCSU_TechLib_tsmc02" has been automatically
updated from revision 226610(DM 0) to revision 227612(DM 3) in virtual memory.


Begin netlist:    Apr 13 11:45:40 2022
        view name list  = ("auLvs" "extracted" "schematic")
        stop name list  = ("auLvs")
        library name    = "Design"
        cell name       = "singlebitadder"
        view name       = "extracted"
        globals lib     = "basic"
Running Artist Flat Netlisting ...
*WARNING* Parameter 'lxUseCell' already exists.
End netlist:    Apr 13 11:45:40 2022

Moving original netlist to extNetlist
Removing parasitic components from netlist
        presistors removed:  0
        pcapacitors removed: 99
        pinductors removed:  0
        pdiodes removed:     0
        trans lines removed: 0
        25 nodes merged into 25 nodes


Begin netlist:    Apr 13 11:45:40 2022
        view name list  = ("auLvs" "schematic")
        stop name list  = ("auLvs")
        library name    = "Design"
        cell name       = "singlebitadder"
        view name       = "schematic"
        globals lib     = "basic"
Running Artist Flat Netlisting ...
End netlist:    Apr 13 11:45:41 2022

Moving original netlist to extNetlist
Removing parasitic components from netlist
        presistors removed:  0
        pcapacitors removed: 0
        pinductors removed:  0
        pdiodes removed:     0
        trans lines removed: 0
        64 nodes merged into 64 nodes

Running netlist comparison program:  LVS
Begin comparison:    Apr 13 11:45:41 2022
@(#)$CDS: LVS version 6.1.8-64b 08/04/2020 19:19 (cpgsrv11) $

The net-lists match.

                            layout  schematic
                               instances
        un-matched             0       0
        rewired                0       0
        size errors            0       0
        pruned                 0       0
        active                 36      36
        total                  36      36

                                 nets
        un-matched             0       0
        merged                 0       0
        pruned                 0       0
        active                 25      25
        total                  25      25

                               terminals
        un-matched             0       0
```

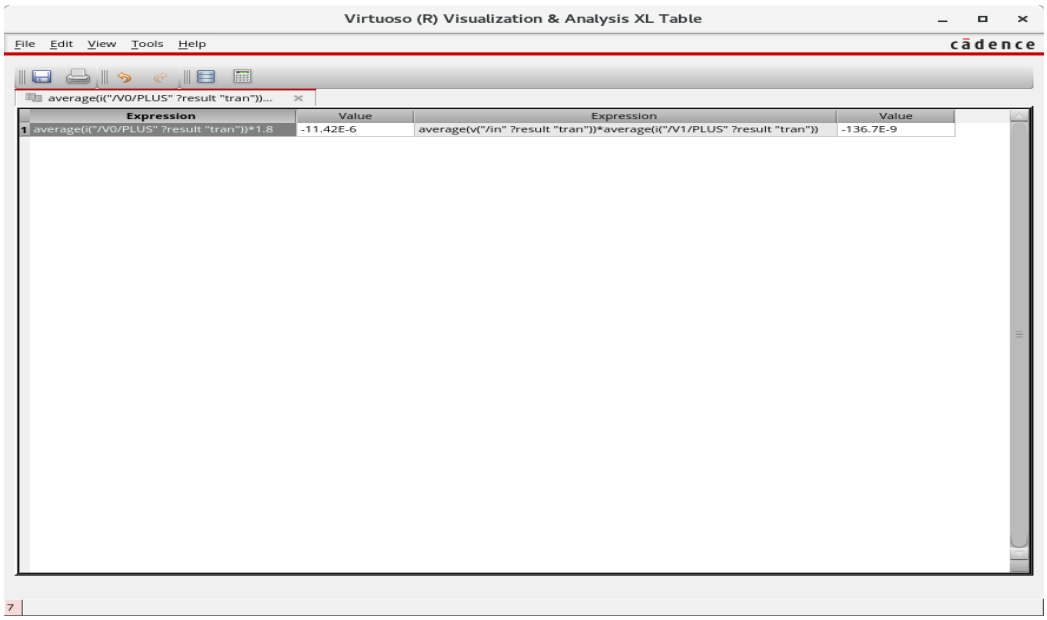
Plain Text | Tab Width: 8 | Ln 1, Col 1 | INS

Delay, Waveforms and Power:

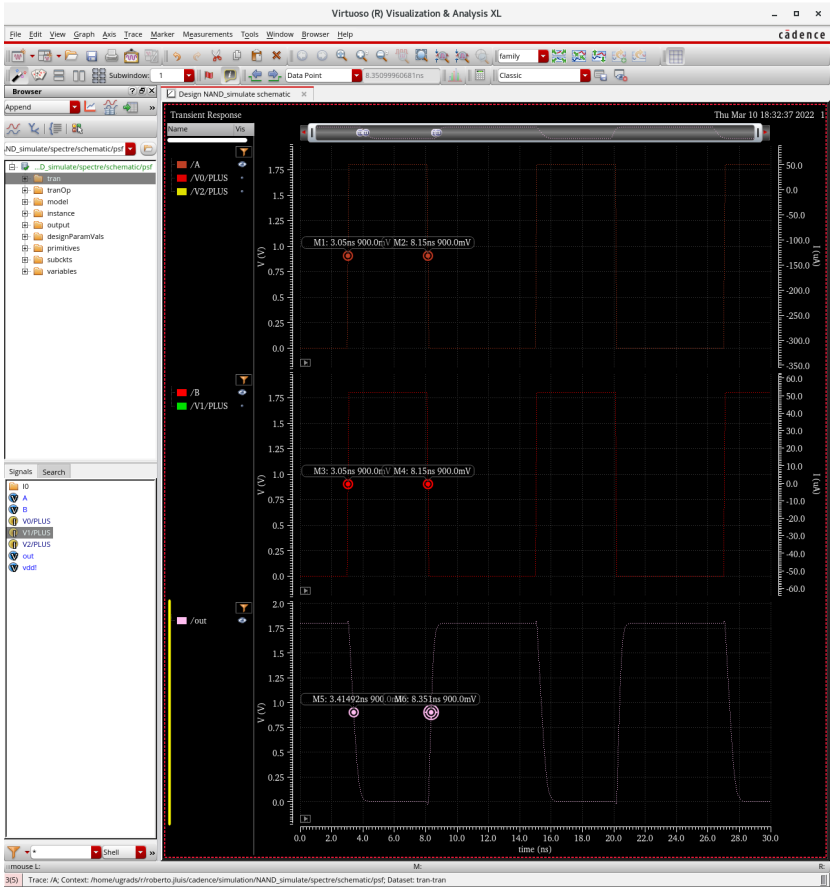
Inverter:



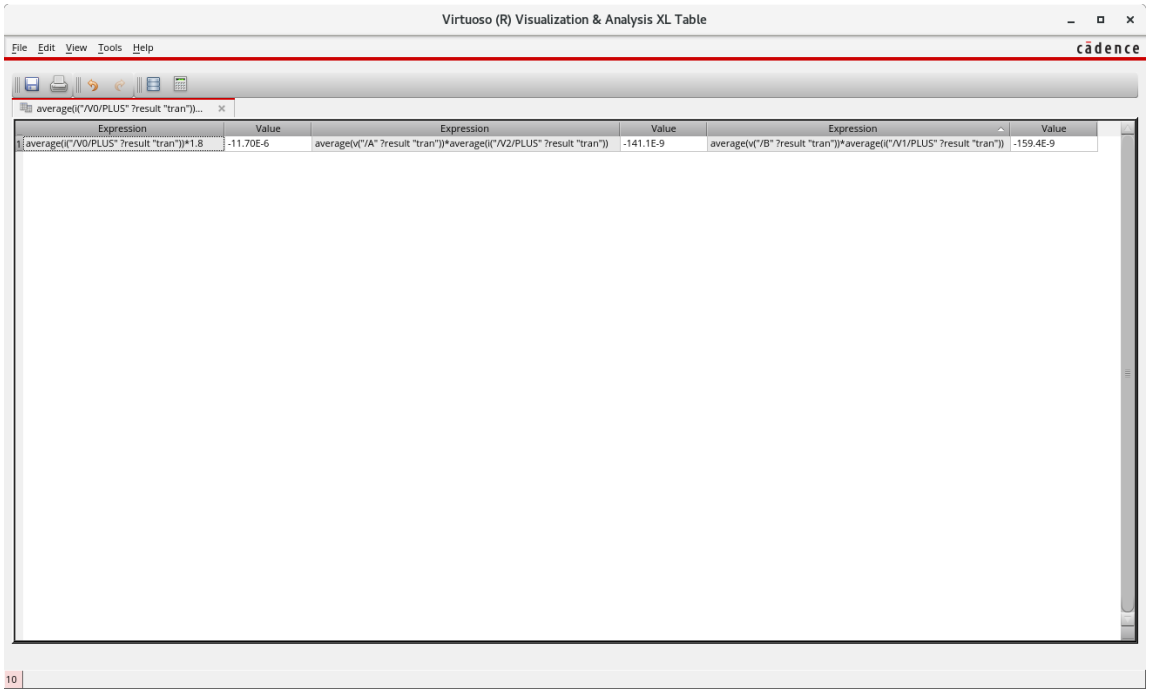
Rising = 8.57 - 8.15 ns = 0.42 ns Falling = 15.3 - 15.05 = 0.25 ns



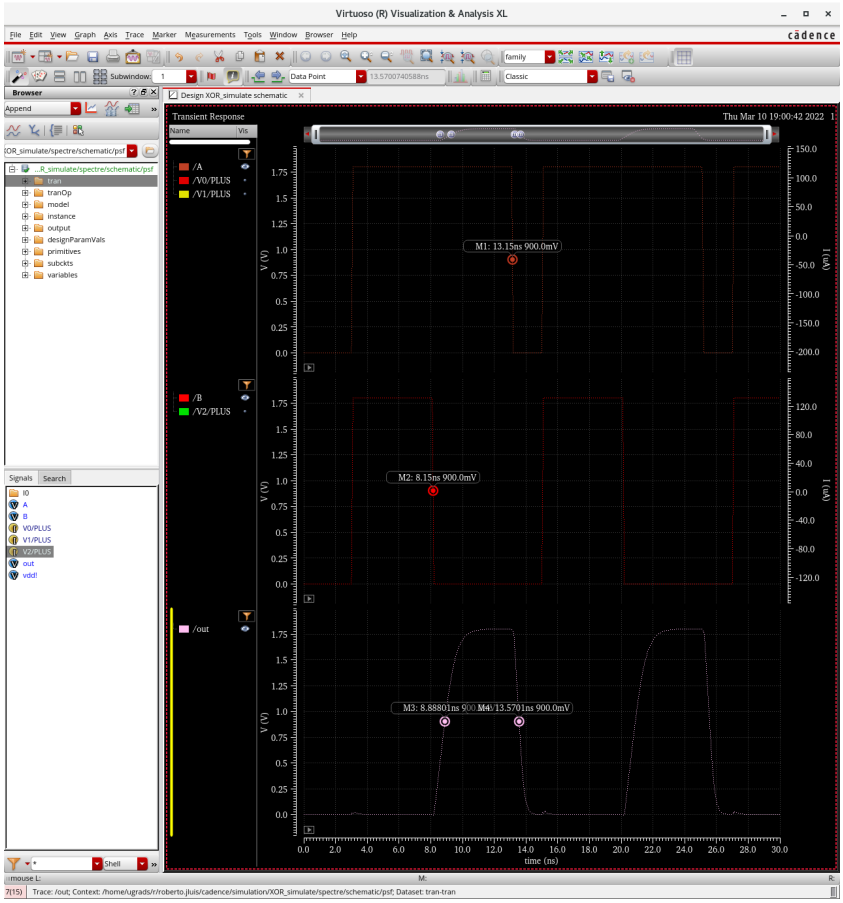
Nand:



Rising = 8.35 - 8.15 = 0.2 ns Falling = 3.41 - 3.05 = 0.36 ns

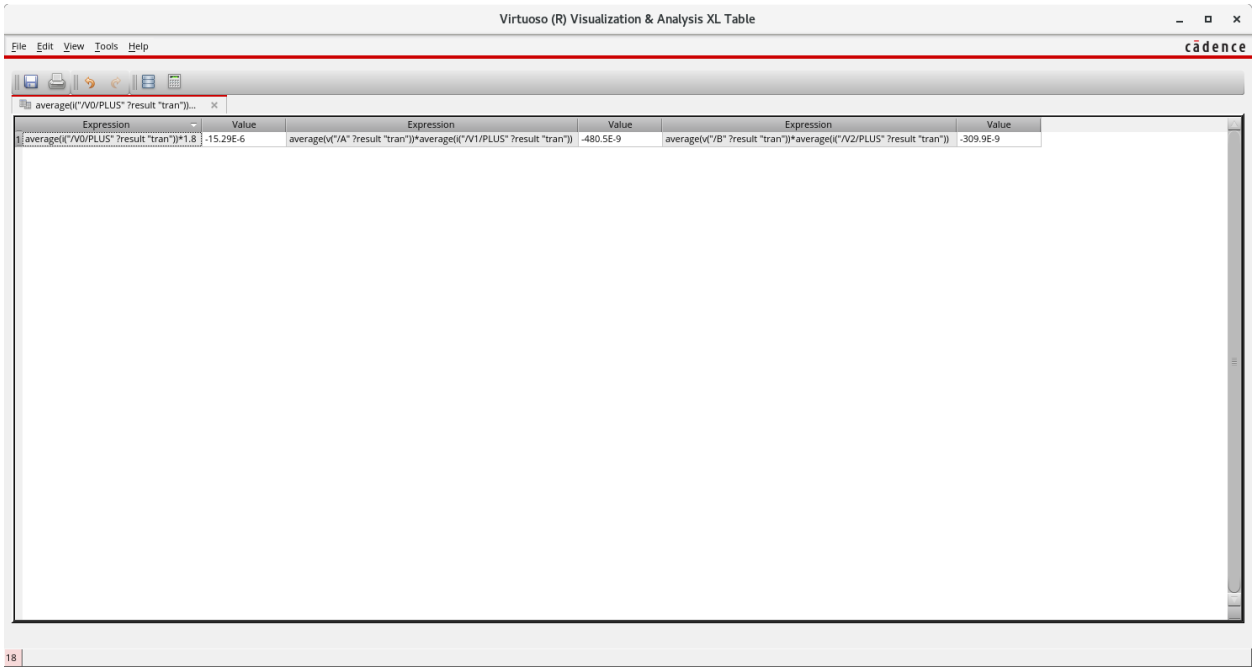


Xor:

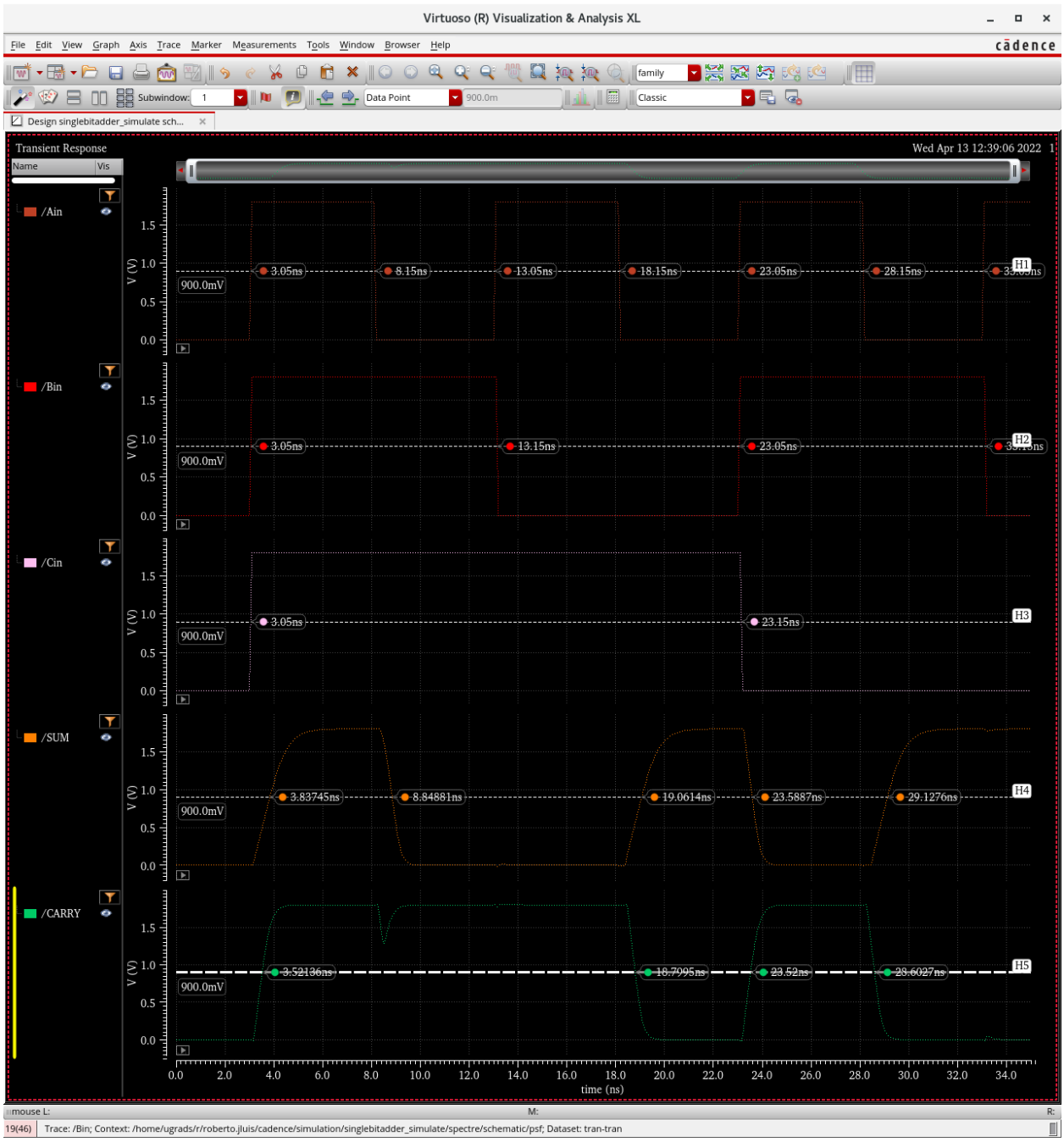


Rising = 8.89 - 8.15 = 0.74 ns

Falling = 13.57 - 13.15 = 0.42 ns

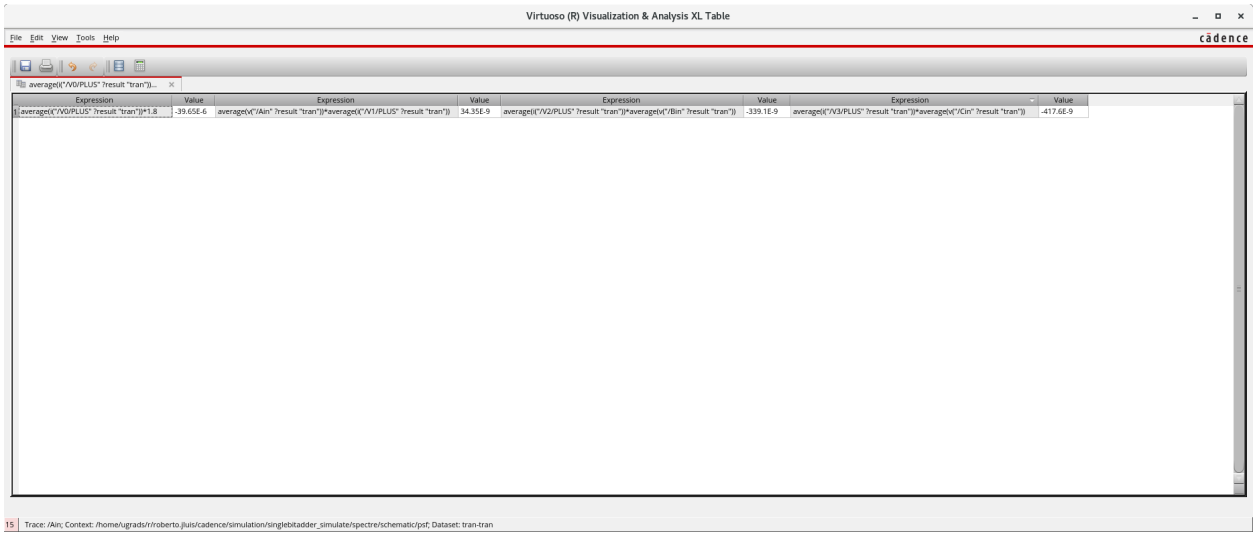


1-bit Adder:

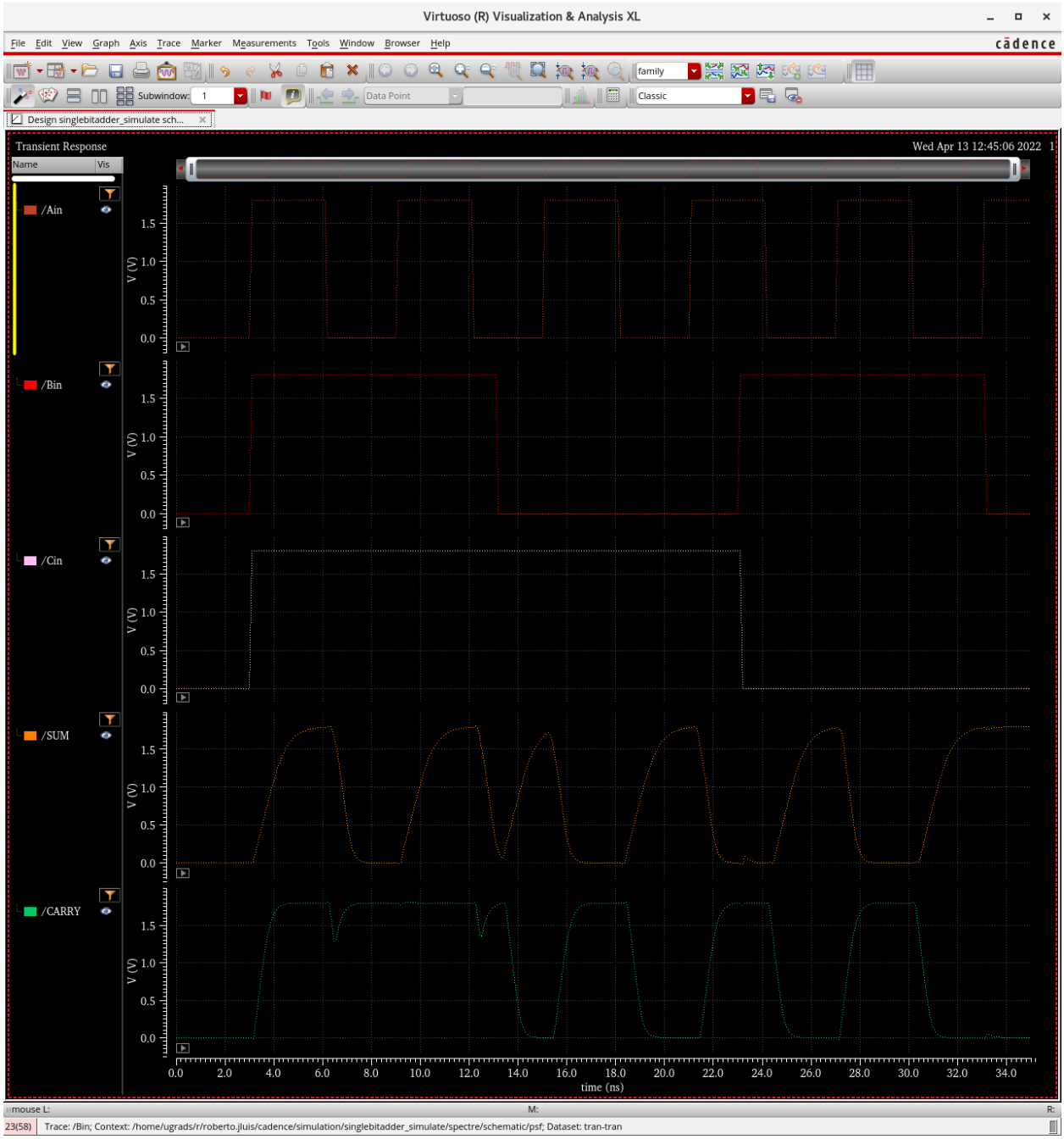


Sum: Rising = 3.84 - 3.05 = 0.79 ns Falling = 8.85 - 8.15 = 0.70 ns

Carry: Rising = 3.52 - 3.05 = 0.46 ns Falling = 18.80 - 18.15 = 0.65 ns



Max frequency = ⅛ ns


Virtuoso (R) Visualization & Analysis XL
File Edit View Graph Axis Trace Marker Measurements Tools Window Browser Help
cadence
Design singlebitadder_simulate sch...
Transient Response
Wed Apr 13 12:45:06 2022
Name
Vis
/Ain
/Bin
/Cin
/SUM
/CARRY
V (V)
time (ns)
mouse L:
M:
R:
Trace: /Bin; Context: /home/ugrads/r/roberto.jluis/cadence/simulation/singlebitadder_simulate/spectre/schematic/psf; Dataset: tran-tran