ECEN 454
Lab 3

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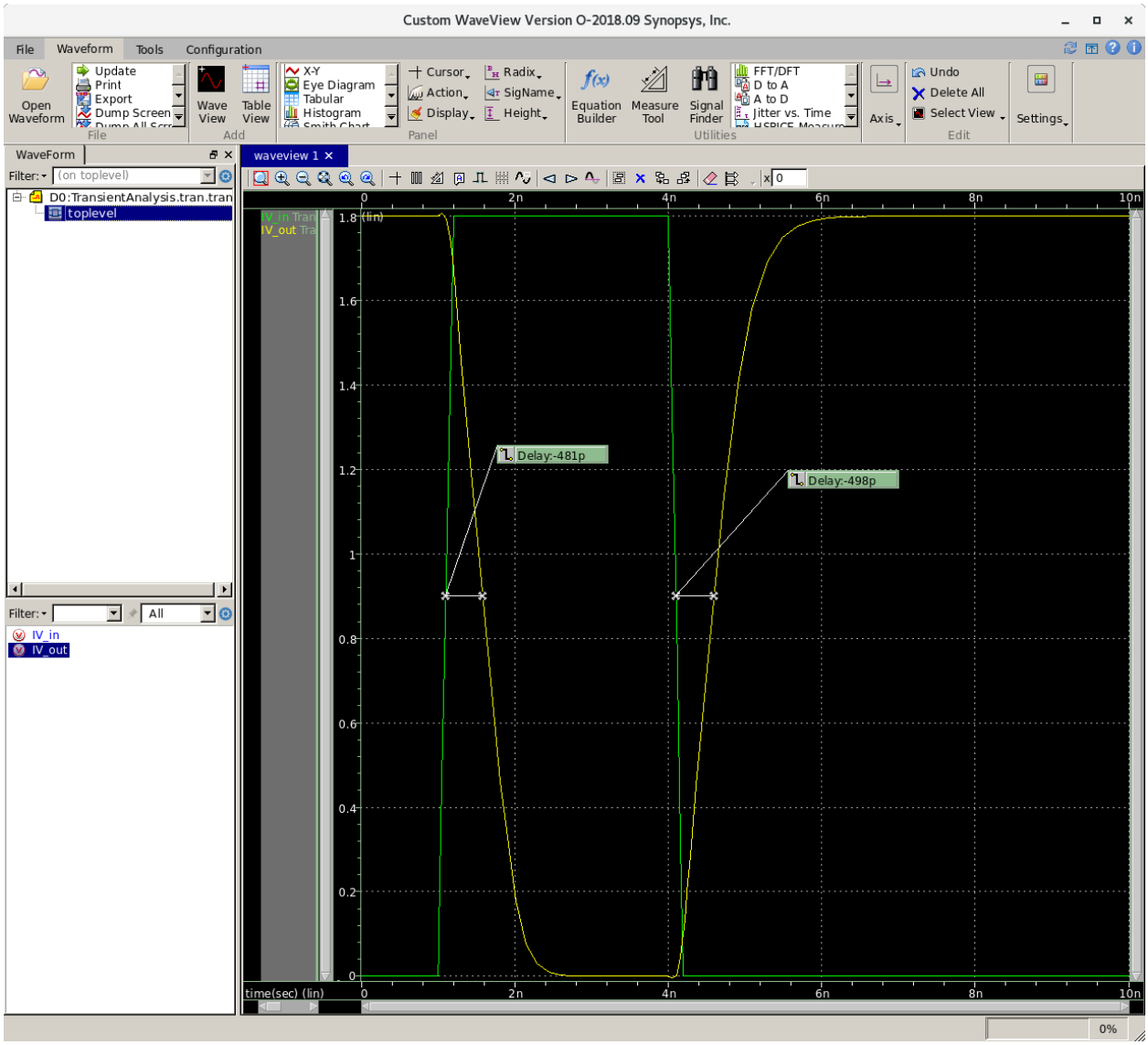
Section 505 - Rahul

Inverter:

Waveform:



Simfile:

Open | inverter.spi ~/ecen454/cellcharacs | Save

model18.spi | inverter.spi

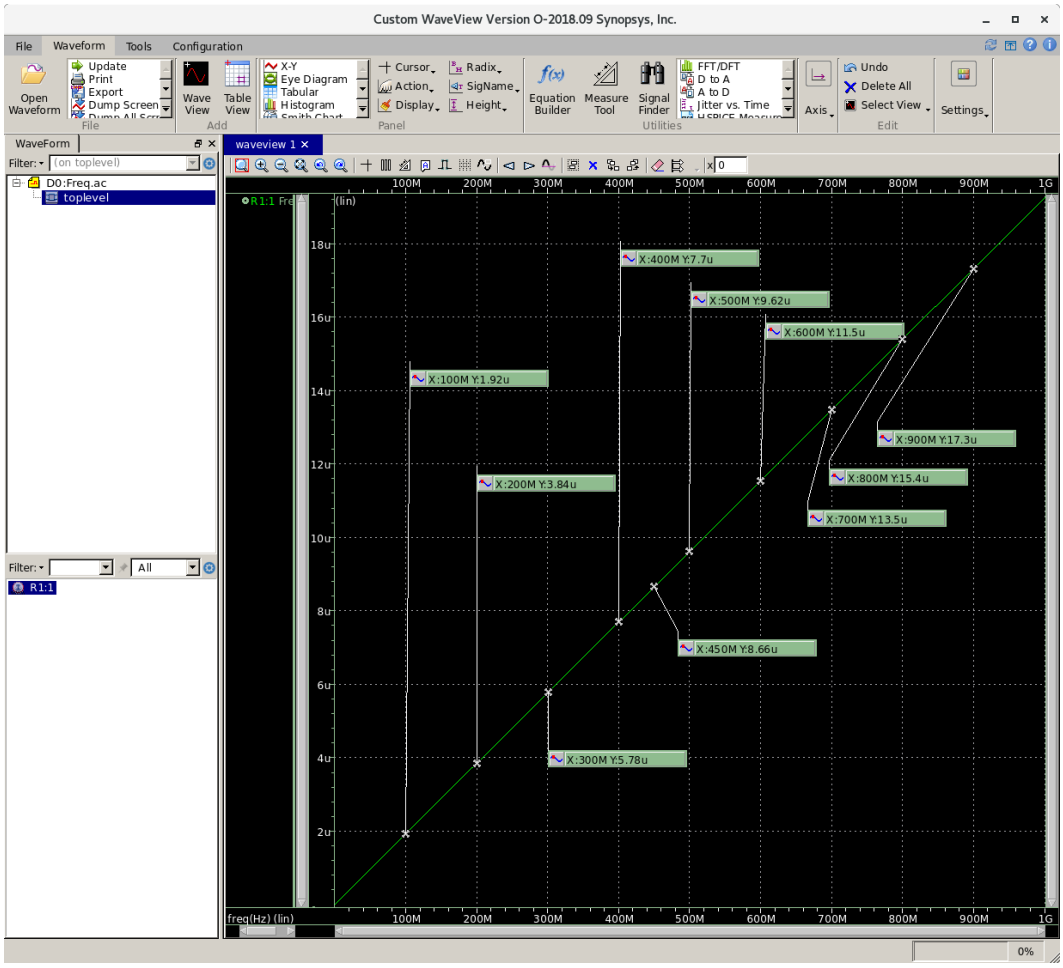
```
;Spice netlist for an inverter and a capacitor
simulator lang=spectre

include "~/ecen454/cellcharacs/model18.spi"
include "~/ecen454/cellcharacs/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

vpwl (IV_in 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n 0]

X1 (IV_in IV_out vdd gnd) IV wp=0.9u lp=0.2u wn=0.3u ln=0.2u

R1 (IV_out 1) resistor r=1
C1 (1 0) capacitor c=100f

TransientAnalysis tran start=0 stop=10ns step=1ps
save IV_in IV_out
```

Plain Text | Tab Width: 8 | Ln 12, Col 36 | INS

Delay table:

capacitance (fF)	rising delay (ps)	falling delay (ps)	error
1	-27.1	-45.2	0.667896679
5	-57.7	-74.5	0.2911611785
10	-85.8	-101	0.1771561772
20	-131	-144	0.09923664122
25	-153	-166	0.08496732026
30	-175	-188	0.07428571429
40	-219	-232	0.05936073059
50	-262	-277	0.0572519084
55	-284	-297	0.04577464789
60	-306	-321	0.04901960784
70	-351	-368	0.04843304843
80	-393	-410	0.04325699746
90	-439	-451	0.02733485194
95	-460	-476	0.0347826087
100	-481	-498	0.03534303534

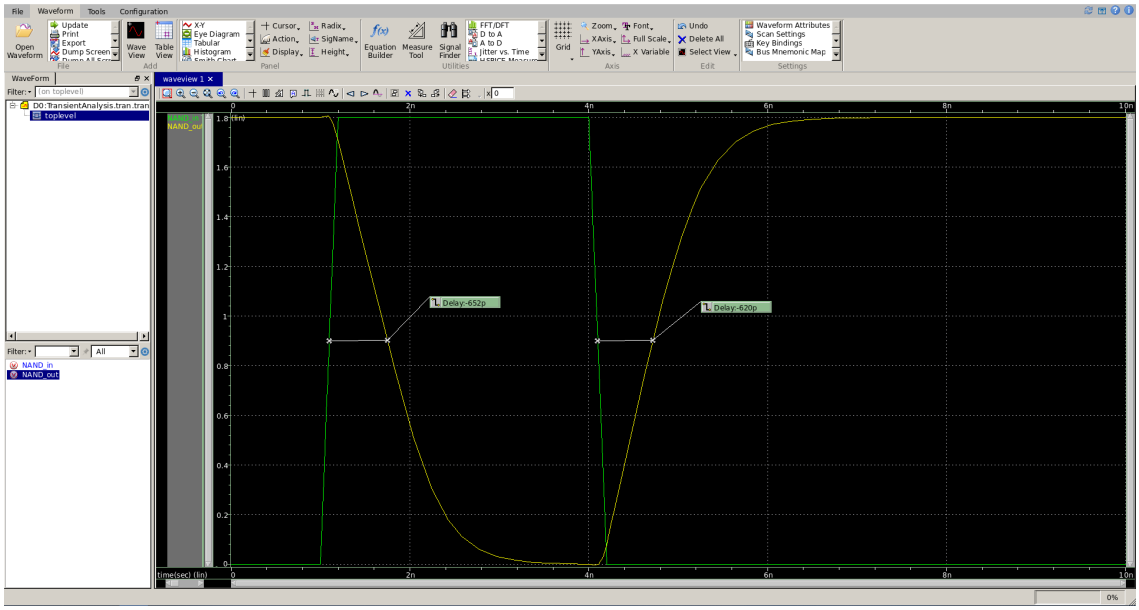
Sink capacitance:



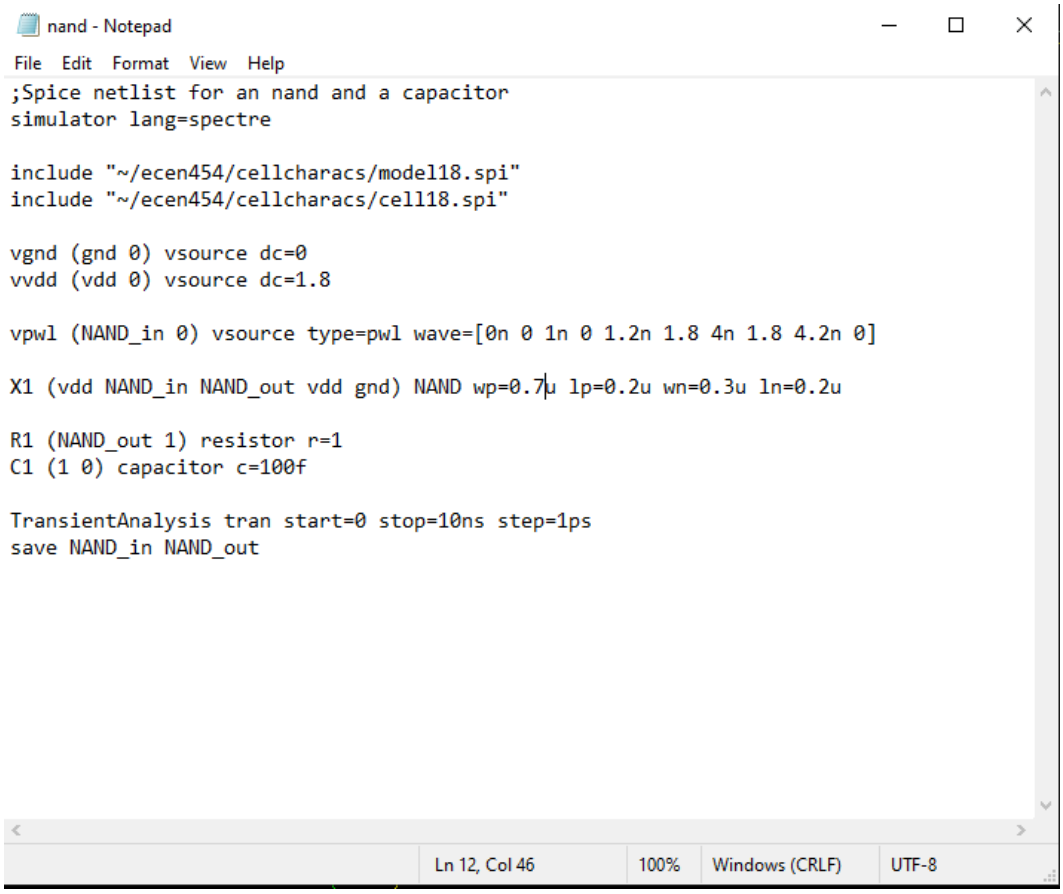
Average = 9.522 uF

Nand:

Waveform:



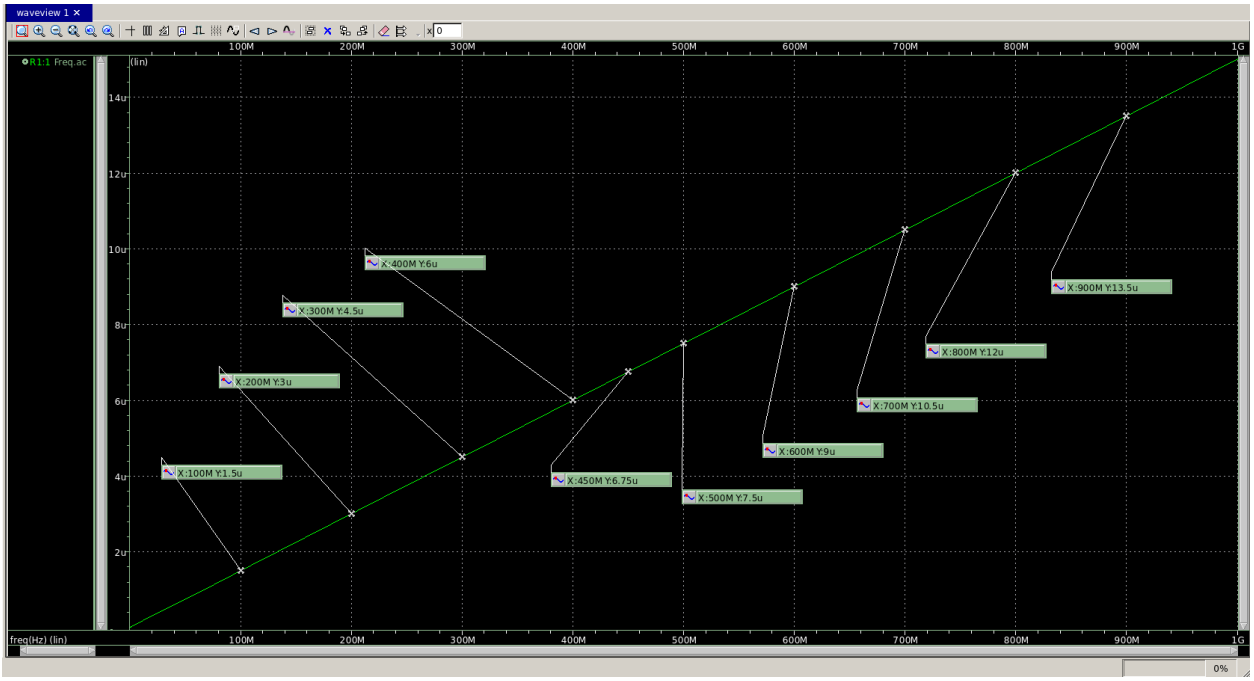
Sim file:



Delay table:

capacitance (fF)	rising delay (ps)	falling delay (ps)	error
1	-35.2	-63.6	0.8068181818
5	-68.5	-92.9	0.3562043796
10	-102	-121	0.1862745098
20	-164	-176	0.07317073171
25	-194	-204	0.05154639175
30	-225	-232	0.03111111111
40	-287	-288	0.003484320557
50	-347	-343	0.01152737752
55	-379	-371	0.02110817942
60	-409	-400	0.02200488998
70	-470	-454	0.03404255319
80	-530	-509	0.03962264151
90	-591	-566	0.04230118443
95	-621	-592	0.04669887279
100	-652	-620	0.0490797546

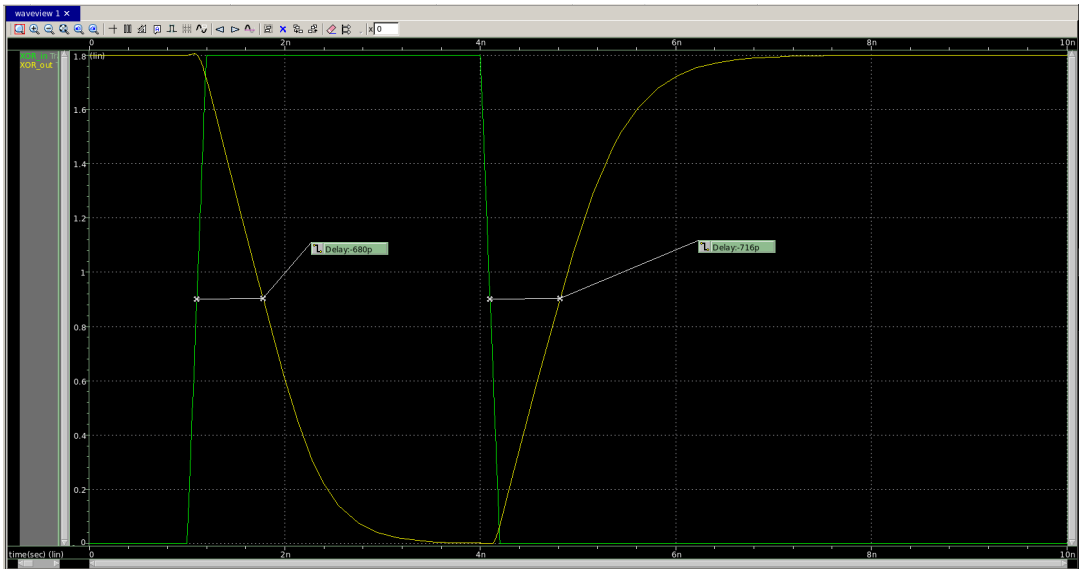
Sink capacitance:



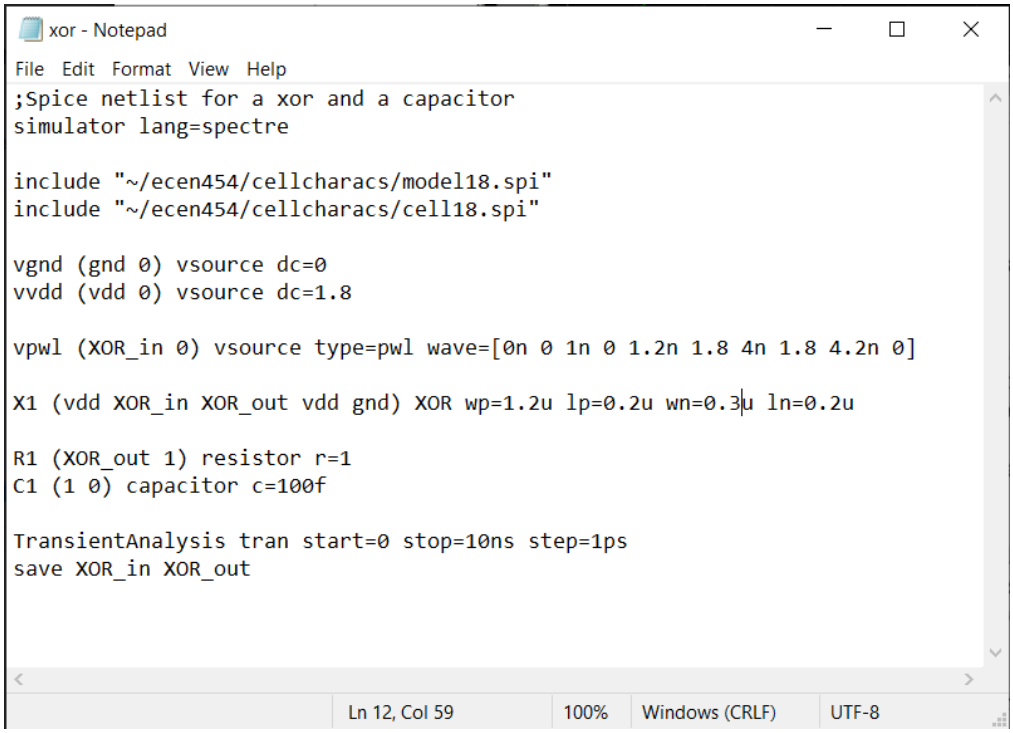
Average = 7.417 uF

XOR:

Waveform:



Sim file:



Delay table:

capacitance (fF)	rising delay (ps)	falling delay (ps)	error
1	-35.2	-63.6	0.8068181818
5	-68.5	-92.9	0.3562043796
10	-102	-121	0.1862745098
20	-164	-176	0.07317073171
25	-194	-204	0.05154639175
30	-225	-232	0.03111111111
40	-287	-288	0.003484320557
50	-347	-343	0.01152737752
55	-379	-371	0.02110817942
60	-409	-400	0.02200488998
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80	-530	-509	0.03962264151
90	-591	-566	0.04230118443
95	-621	-592	0.04669887279
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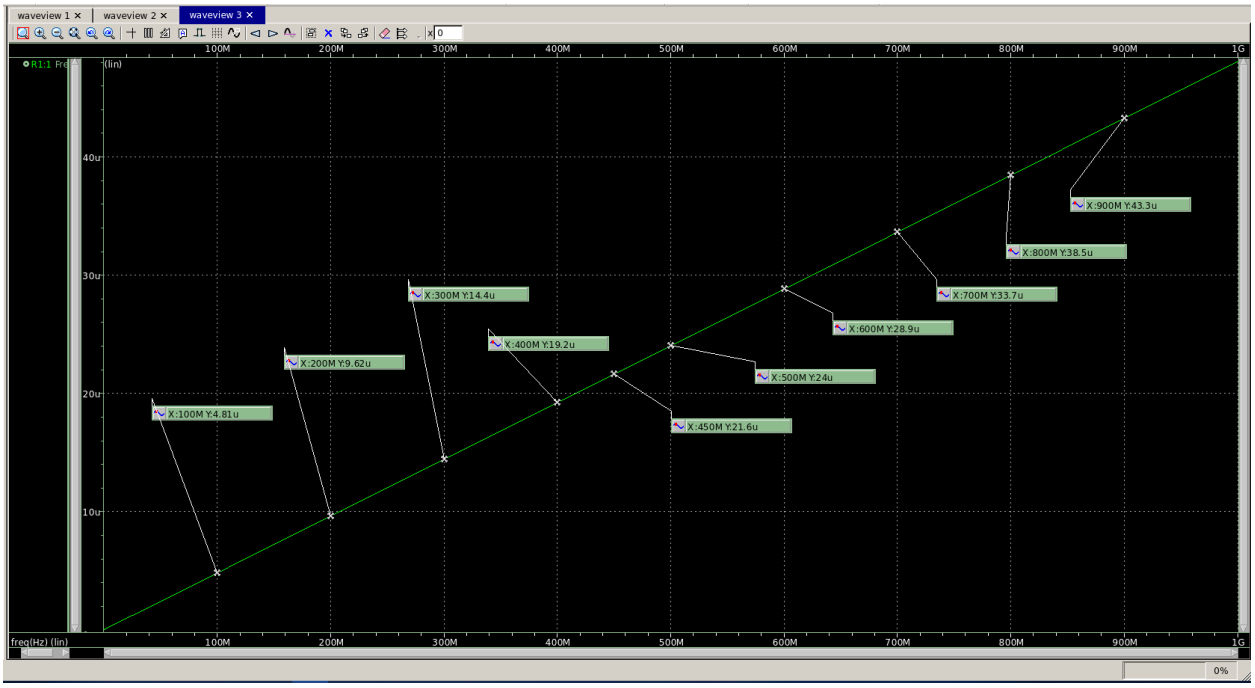
Sink capacitance:



Average = 23.803 uF

Cell file:

cell18 - Notepad

File Edit Format View Help

```
//Spice netlist for an inverter
simulator lang=spectre
subckt IV (input output VDD VSS)
        parameters wp=0.6u lp=0.2u wn=0.3u ln=0.3u
        M1 output input VDD VDD tsmc18P w=wp l=lp
        M2 output input VSS VSS tsmc18N w=wn l=ln
ends IV
subckt NAND (input1 input2 output VDD VSS)
        parameters wp=0.6u lp=0.2u wn=0.3u ln=0.3u
        M1 output input1 VDD VDD tsmc18P w=wp l=lp
        M2 output input2 VDD VDD tsmc18P w=wp l=lp
        M3 output input1 net1 VSS tsmc18N w=wn l=ln
        M4 net1 input2 VSS VSS tsmc18N w=wn l=ln
ends NAND
subckt XOR (input1 input2 output VDD VSS)
        parameters wp=0.6u lp=0.2u wn=0.3u ln=0.3u
        M1 net1 input1 VDD VDD tsmc18P w=wp l=lp
        M2 net1 input1 VSS VSS tsmc18N w=wn l=ln
        M3 net2 input2 VDD VDD tsmc18P w=wp l=lp
        M4 net2 input2 VSS VSS tsmc18N w=wn l=ln
        M5 VDD input2 net3 VDD tsmc18P w=wp l=lp
        M6 VDD net2 net4 VDD tsmc18P w=wp l=lp
        M7 net3 net1 output VDD tsmc18P w=wp l=lp
        M8 net4 input1 output VDD tsmc18P w=wp l=lp
        M9 output net1 net5 VSS tsmc18N w=wn l=ln
        M10 output input1 net6 VSS tsmc18N w=wn l=ln
        M11 net5 net2 VSS VSS tsmc18N w=wn l=ln
        M12 net6 input2 VSS VSS tsmc18N w=wn l=ln
end XOR
```

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