ECEN 454
Lab 2

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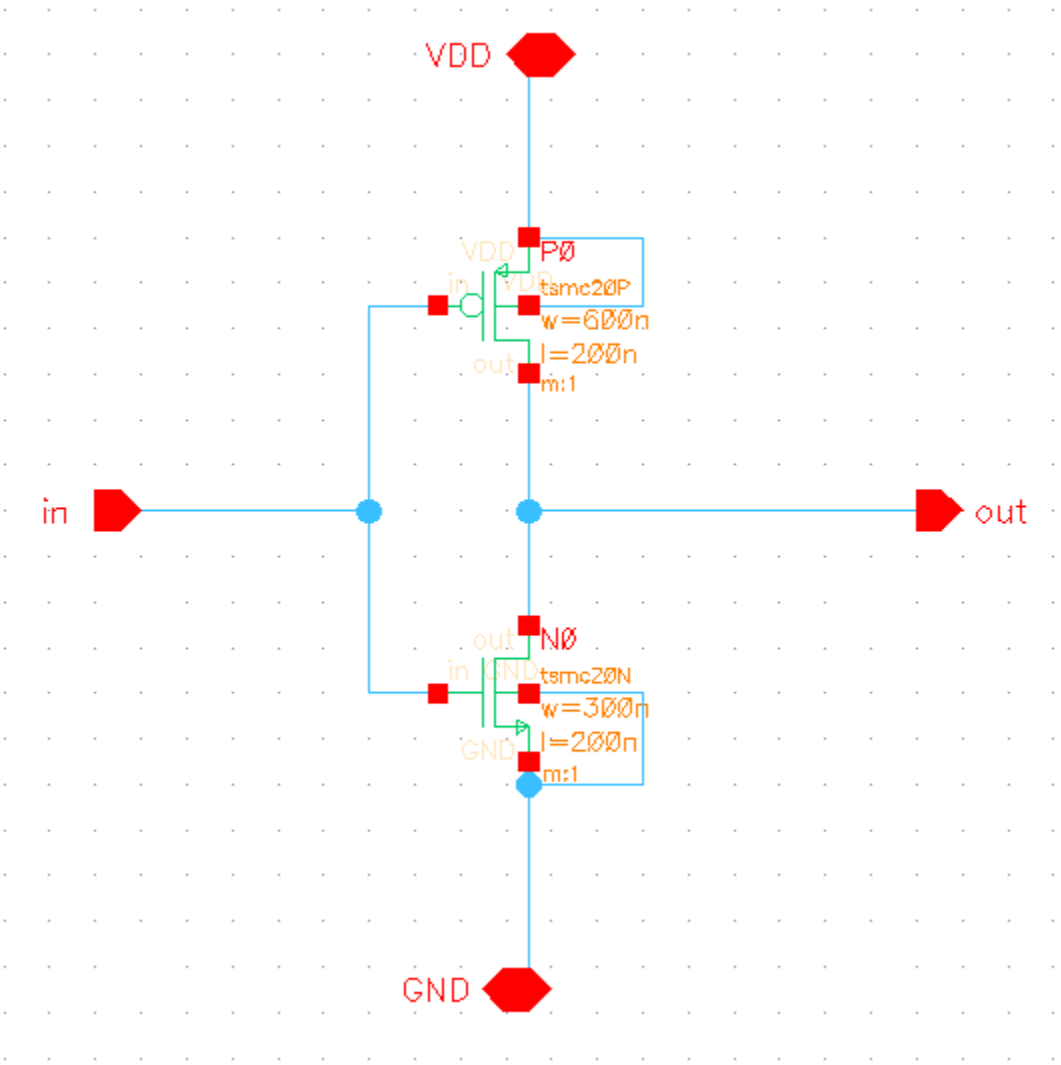
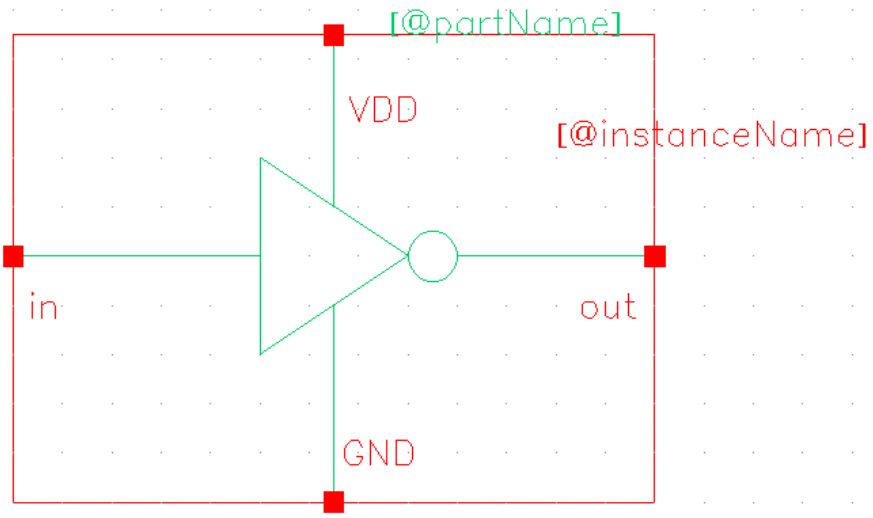
Section 505 - Rahul

Inverter:

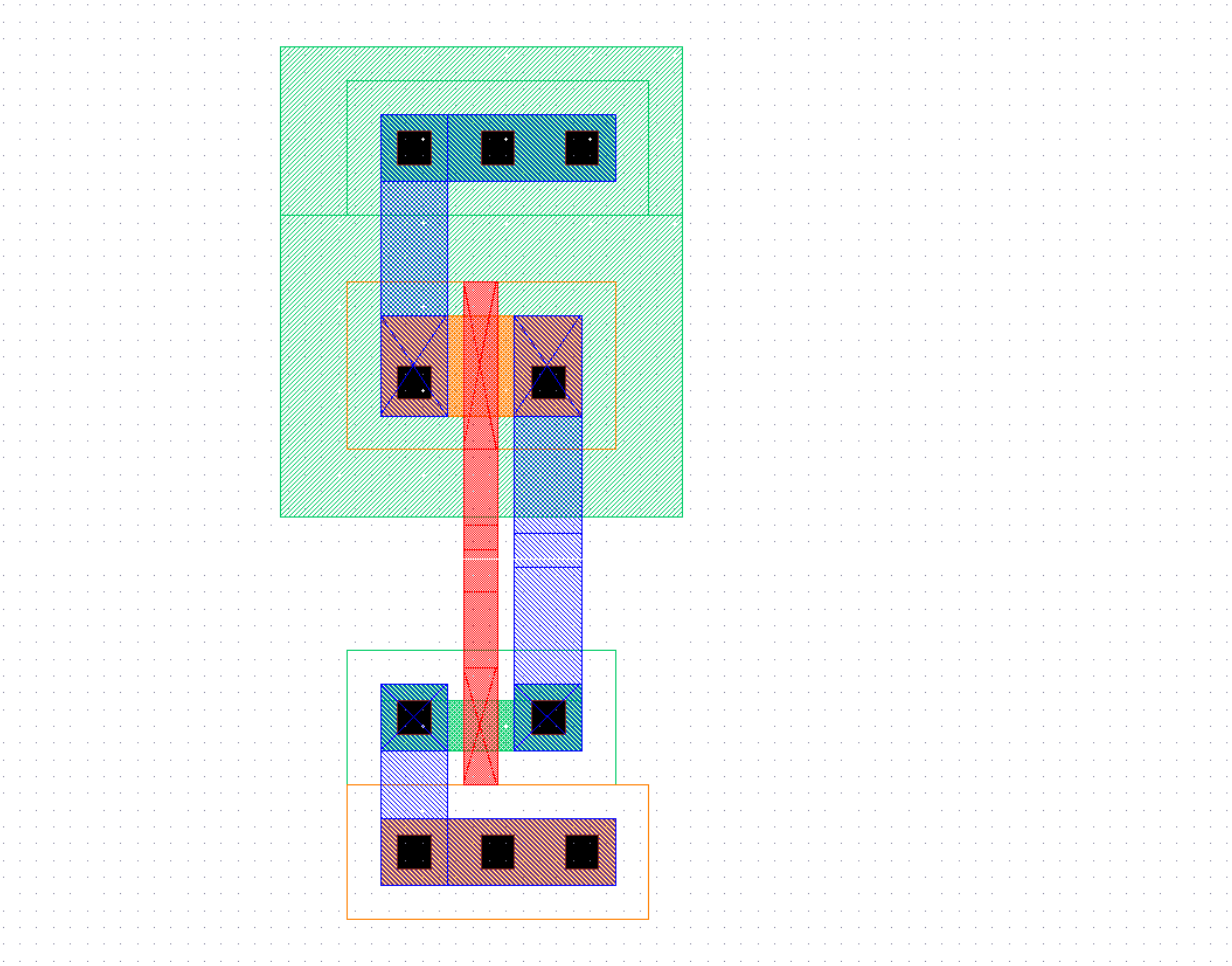
Schematic:



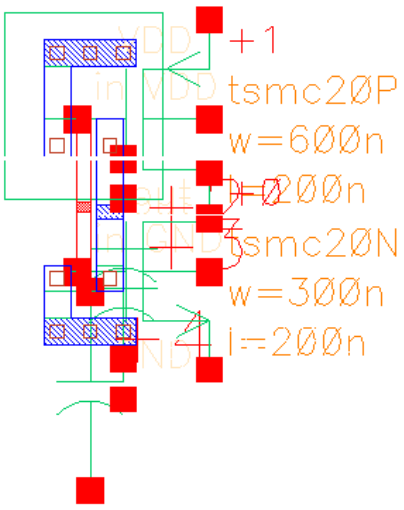
Symbol:



Layout:



Extracted:



LVS report:

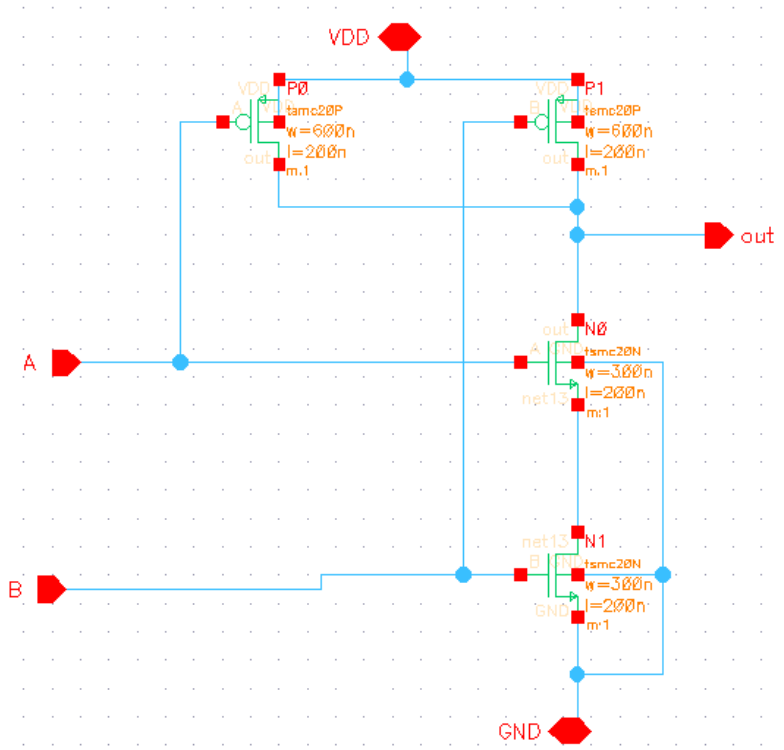
si.out
~/ecen454/LVS

```
The net-lists match.

                          layout  schematic
                             instances
        un-matched              0       0
        rewired                 0       0
        size errors             0       0
        pruned                  0       0
        active                  2       2
        total                   2       2

                               nets
        un-matched              0       0
        merged                  0       0
        pruned                  0       0
        active                  4       4
        total                   4       4

                             terminals
        un-matched              0       0
        matched but
        different type          0       0
        total                   4       4


Probe files from /home/ugrads/r/roberto.jluis/ecen454/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:
```

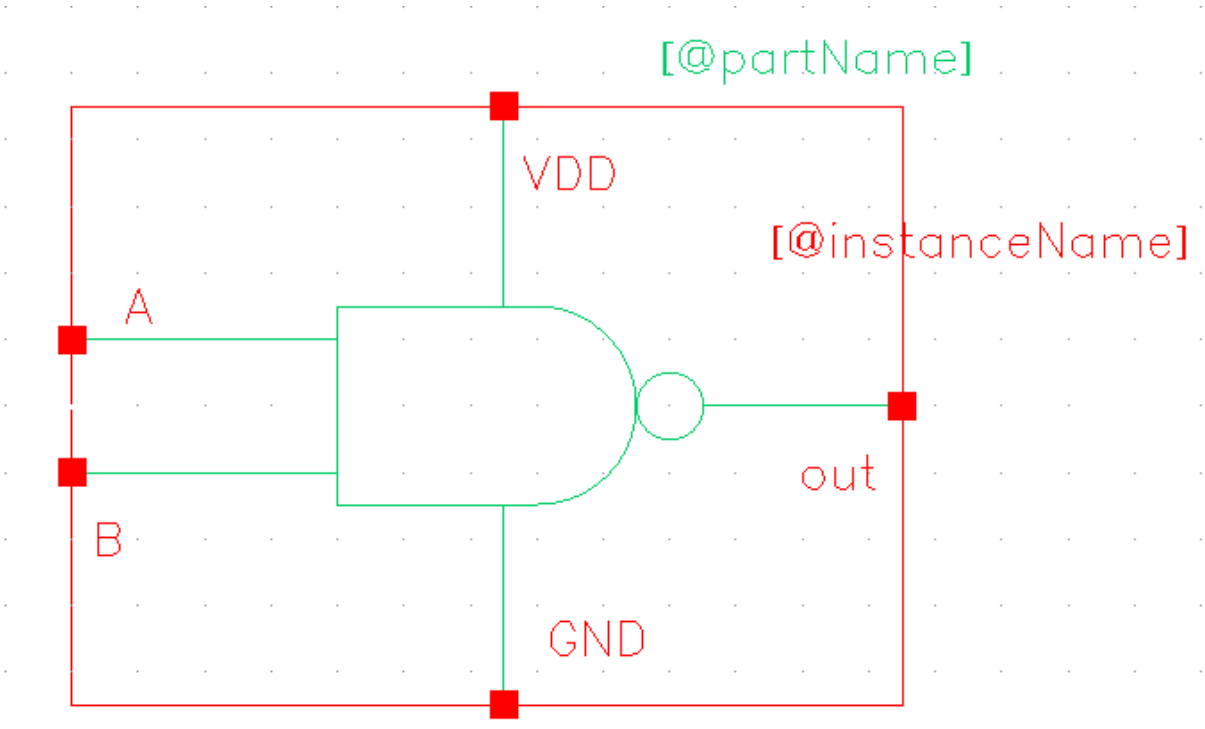
Plain Text Tab Width: 8 Ln 91, Col 11 INS

NAND:

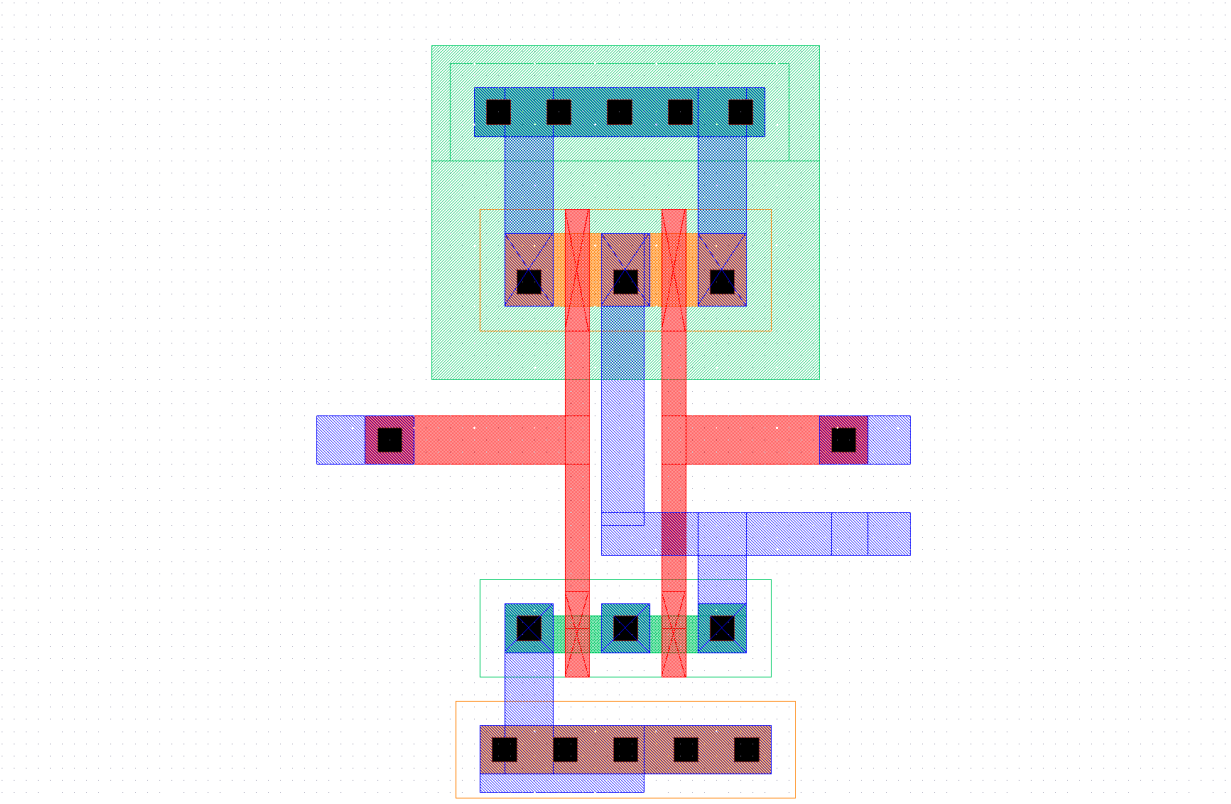
Schematic:



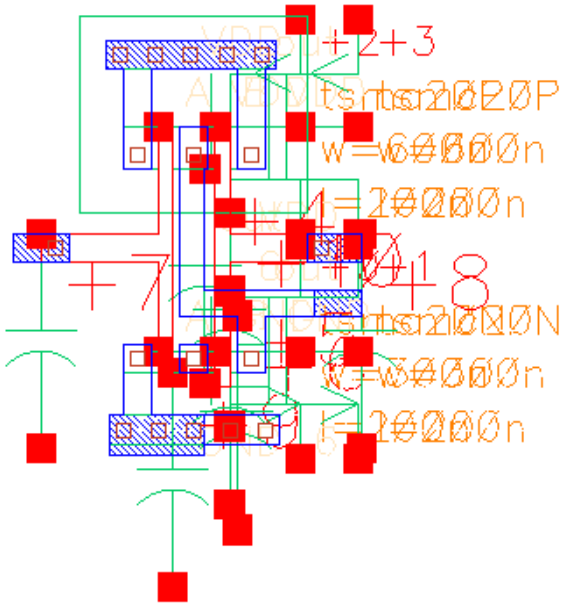
Symbol:



Layout:



Extracted:

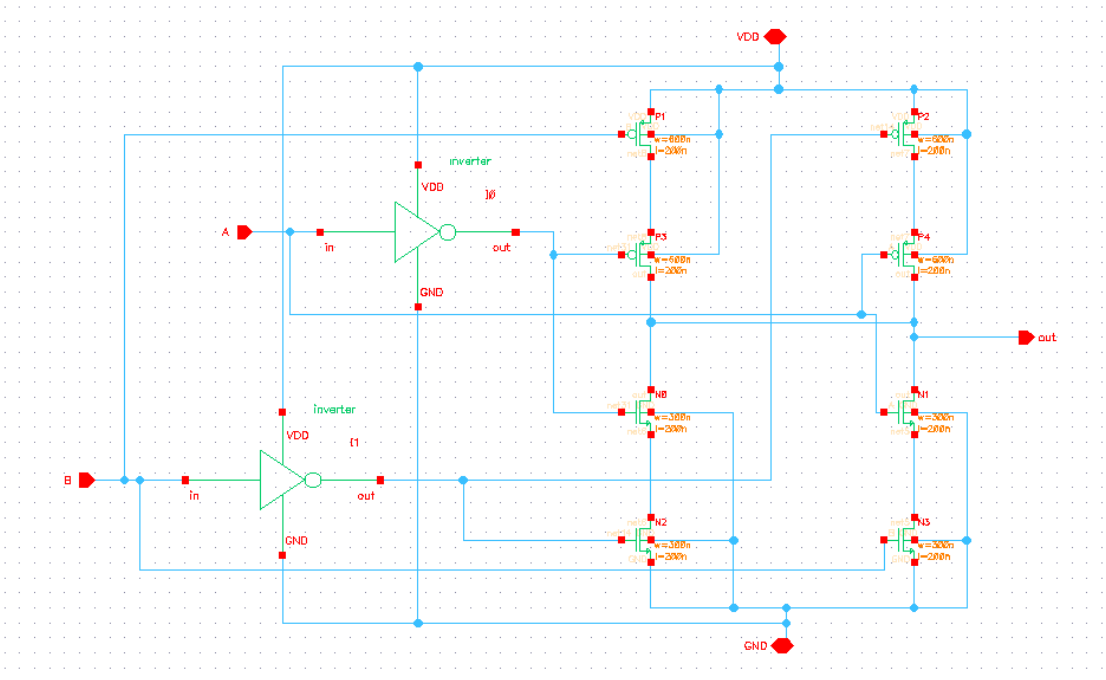


LVS report:

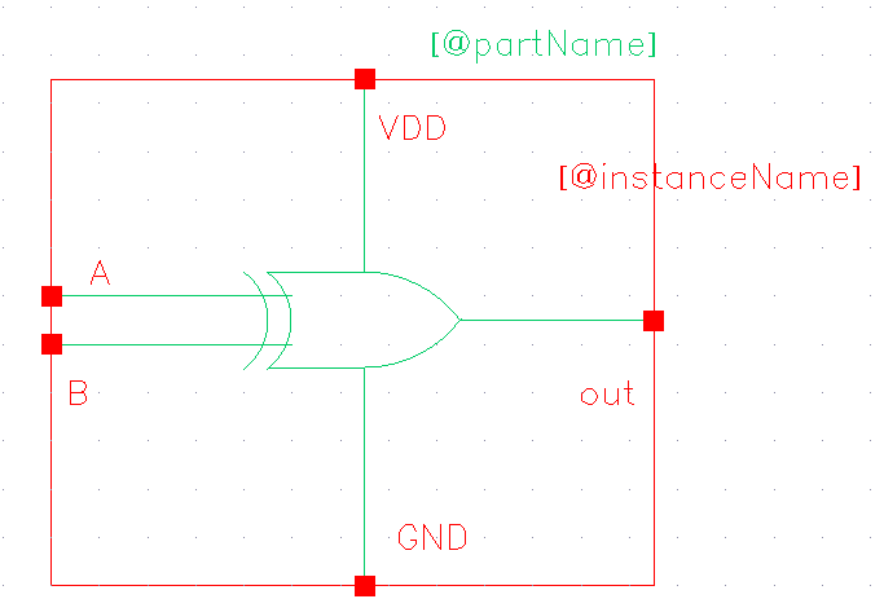
```
cap nfet pfet nmos4 pmos4

The net-lists match.

                          layout  schematic
                             instances
    un-matched               0       0
    rewired                  0       0
    size errors              0       0
    pruned                   0       0
    active                   4       4
    total                    4       4

                               nets
    un-matched               0       0
    merged                   0       0
    pruned                   0       0
    active                   6       6
    total                    6       6

                             terminals
    un-matched               0       0
    matched but
    different type           0       0
    total                    5       5
```

XOR:

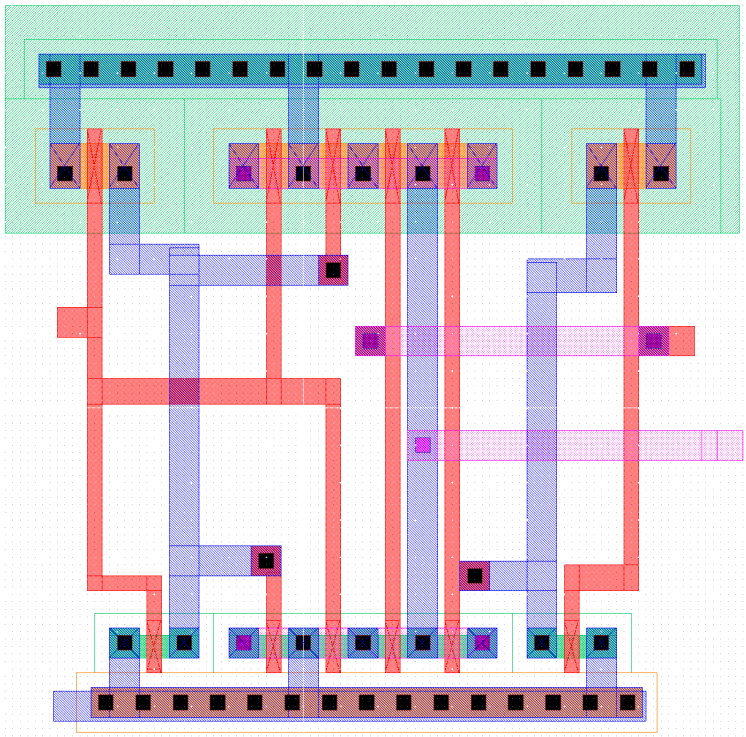
Schematic:



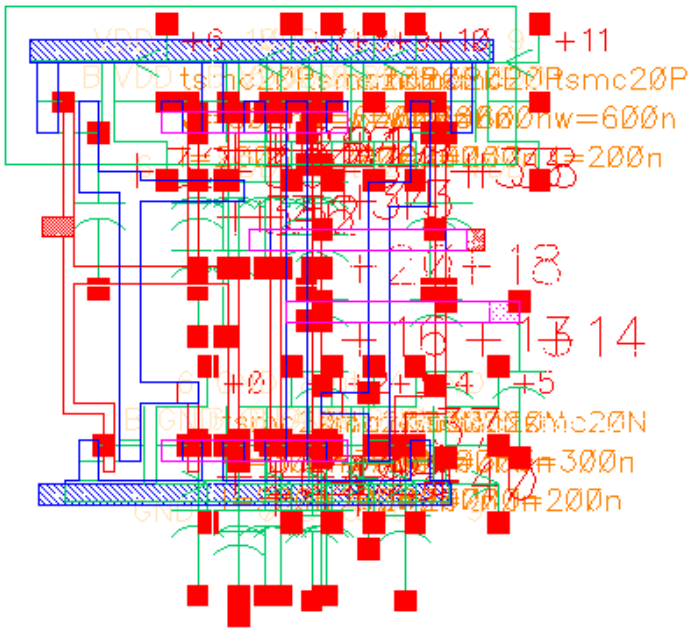
Symbol:



Layout:



Extracted:



LVS report:

```
The net-lists match.

                           layout  schematic
                              instances
        un-matched               0       0
        rewired                  0       0
        size errors              0       0
        pruned                   0       0
        active                   12      12
        total                    12      12

                                nets
        un-matched               0       0
        merged                   0       0
        pruned                   0       0
        active                   11      11
        total                    11      11

                              terminals
        un-matched               0       0
        matched but
        different type           0       0
        total                    5       5
```

Note: The pins did not come out when I exported the image for the layouts but they are there.