ECEN 454
Lab 6

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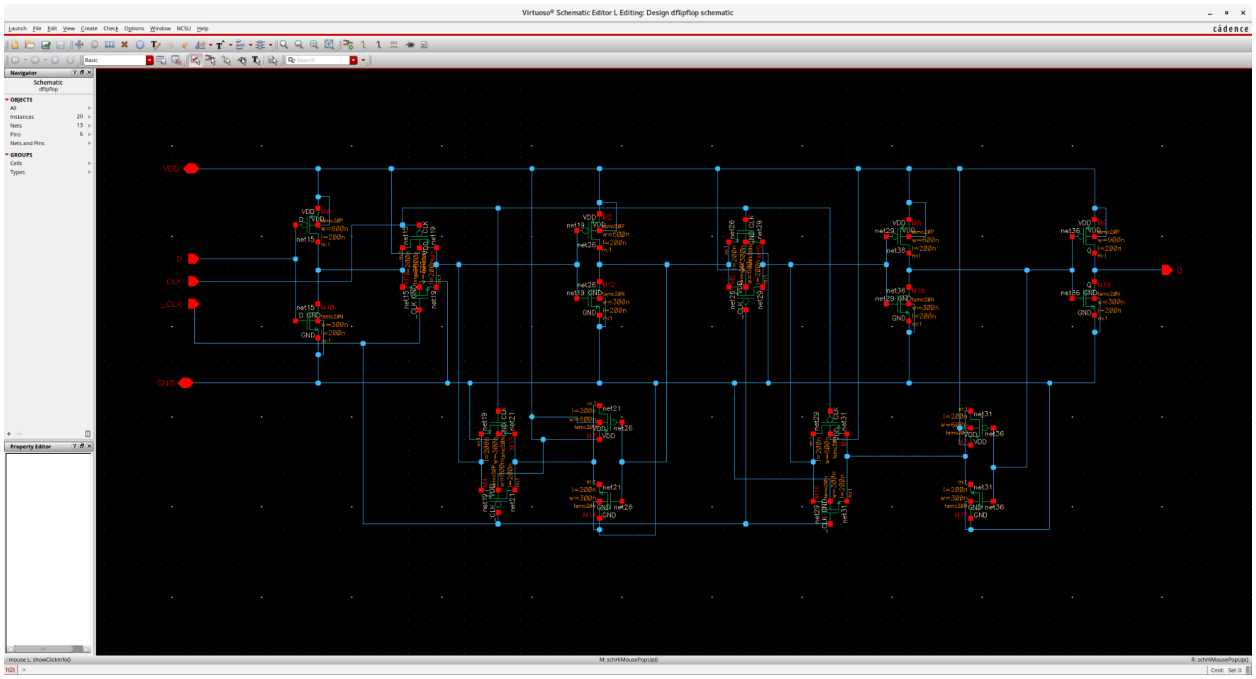
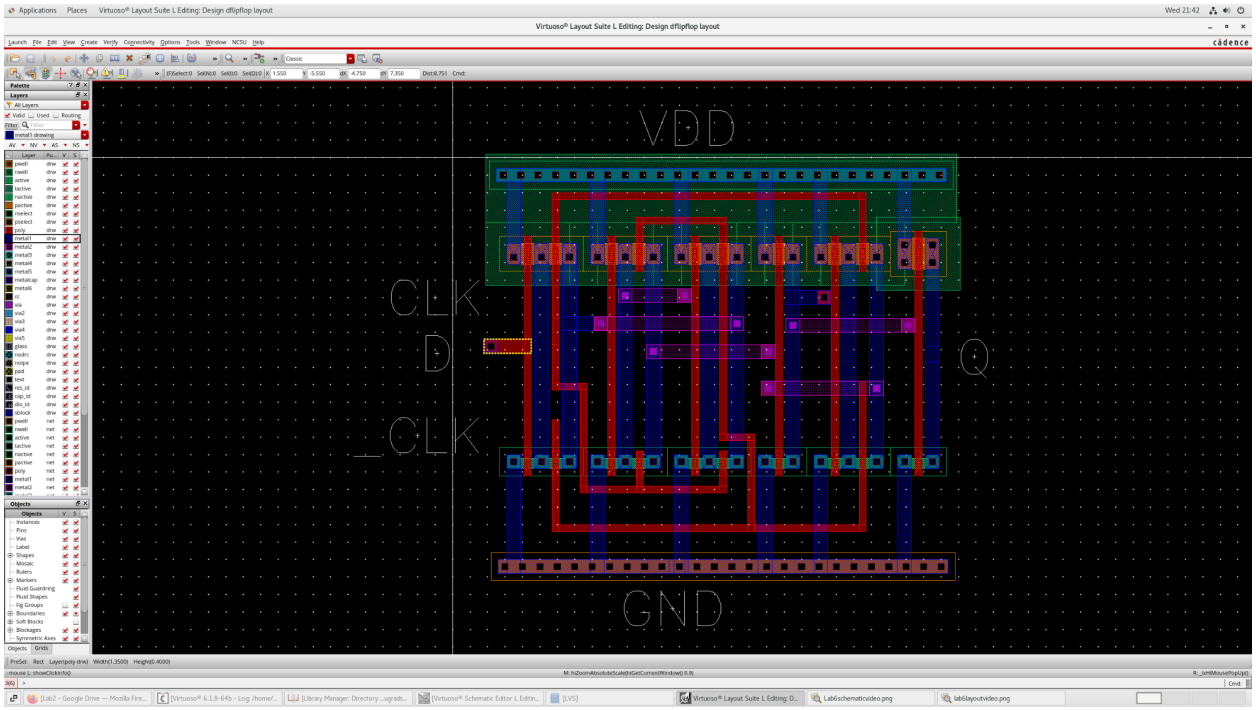
D flip flop:

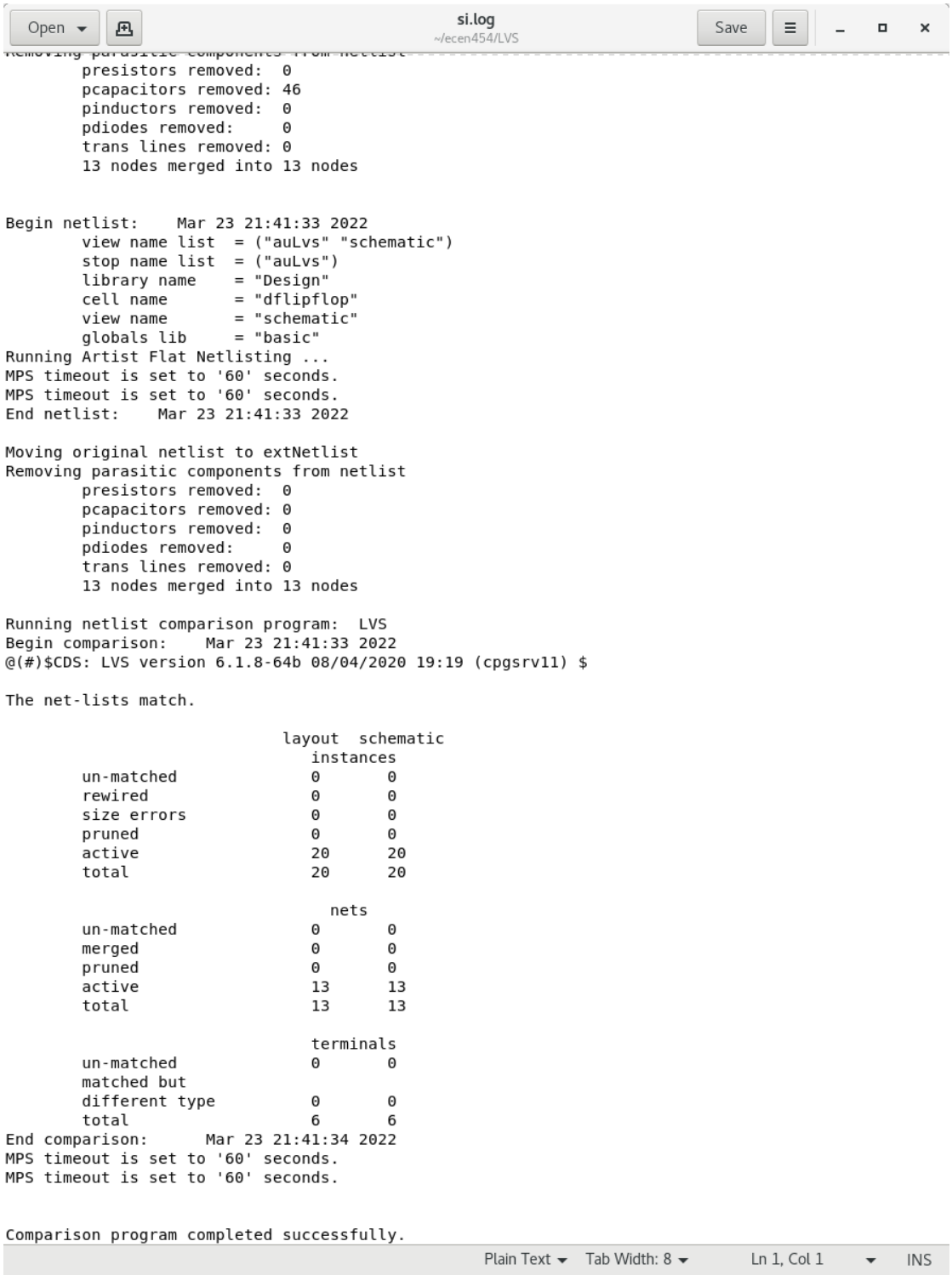
Schematic:



Layout:

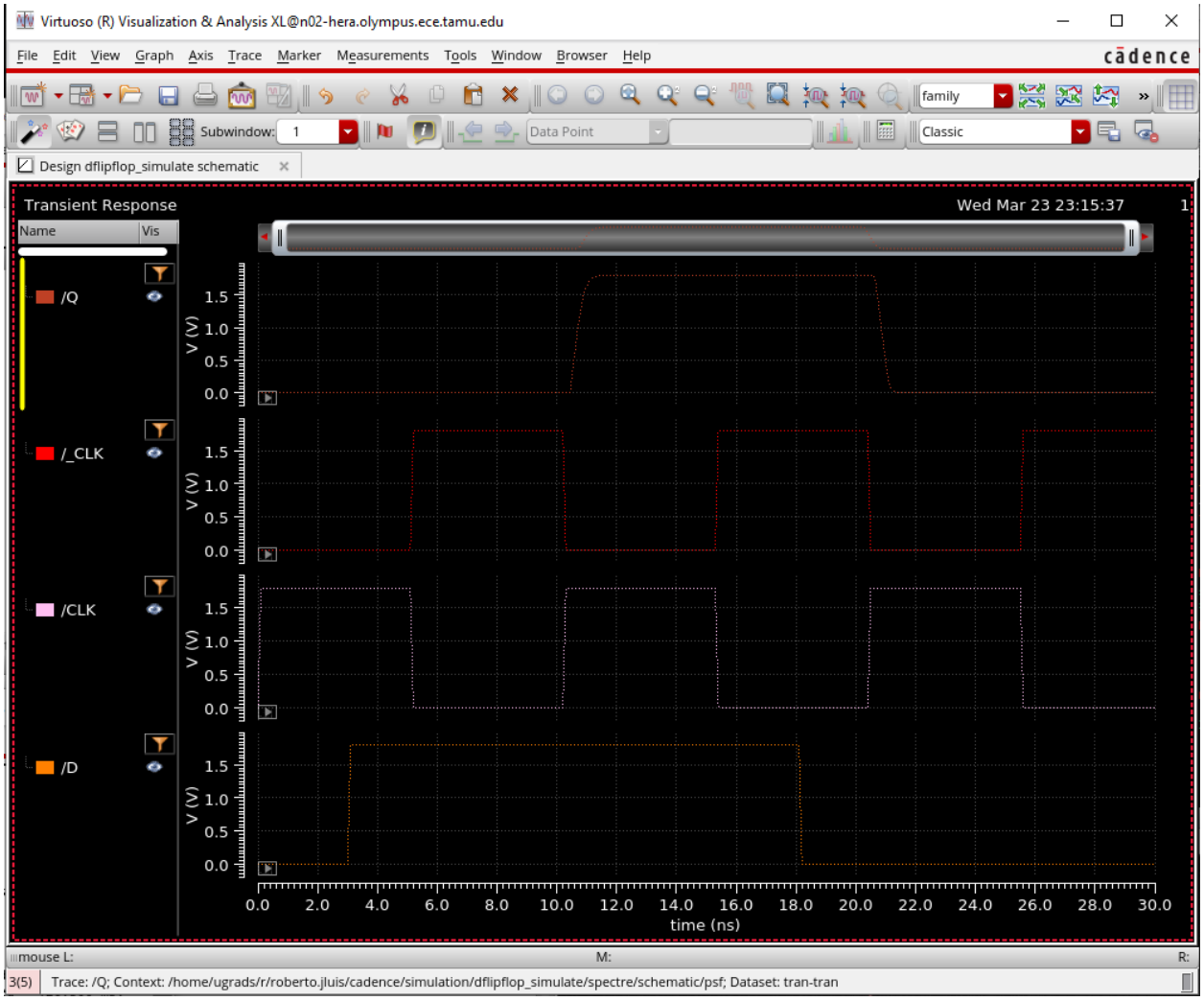


LVS:




```
        presistors removed:  0
        pcapacitors removed: 46
        pinductors removed:  0
        pdiodes removed:     0
        trans lines removed: 0
        13 nodes merged into 13 nodes


Begin netlist:    Mar 23 21:41:33 2022
        view name list  = ("auLvs" "schematic")
        stop name list  = ("auLvs")
        library name    = "Design"
        cell name       = "dflipflop"
        view name       = "schematic"
        globals lib     = "basic"
Running Artist Flat Netlisting ...
MPS timeout is set to '60' seconds.
MPS timeout is set to '60' seconds.
End netlist:    Mar 23 21:41:33 2022

Moving original netlist to extNetlist
Removing parasitic components from netlist
        presistors removed:  0
        pcapacitors removed: 0
        pinductors removed:  0
        pdiodes removed:     0
        trans lines removed: 0
        13 nodes merged into 13 nodes

Running netlist comparison program:  LVS
Begin comparison:    Mar 23 21:41:33 2022
@(#)$CDS: LVS version 6.1.8-64b 08/04/2020 19:19 (cpgsrv11) $

The net-lists match.

                            layout  schematic
                               instances
        un-matched             0       0
        rewired                0       0
        size errors            0       0
        pruned                 0       0
        active                 20      20
        total                  20      20

                                 nets
        un-matched             0       0
        merged                 0       0
        pruned                 0       0
        active                 13      13
        total                  13      13

                               terminals
        un-matched             0       0
        matched but
        different type         0       0
        total                  6       6
End comparison:      Mar 23 21:41:34 2022
MPS timeout is set to '60' seconds.
MPS timeout is set to '60' seconds.


Comparison program completed successfully.
```

Waveform:



Delay table:

capacitance fF	Q rising ns	Q falling ns	CLK rising ns	CLK falling ns	Rising delay ns	falling delay ns	error %
1	10.4522	20.6453	10.25	20.45	0.2022	0.1953	3.412462908
10	10.4989	20.6988	10.25	20.45	0.2489	0.2488	0.04017677782
25	10.5665	20.7685	10.25	20.45	0.3165	0.3185	0.6319115324
40	10.633	20.8348	10.25	20.45	0.383	0.3848	0.4699738903
50	10.677	20.8788	10.25	20.45	0.427	0.4288	0.4215456674
60	10.7206	20.9228	10.25	20.45	0.4706	0.4728	0.4674883128
70	10.7651	20.9666	10.25	20.45	0.5151	0.5166	0.2912055911
80	10.8088	21.0107	10.25	20.45	0.5588	0.5607	0.3400143164
90	10.853	21.0543	10.25	20.45	0.603	0.6043	0.2155887231
100	10.8964	21.0986	10.25	20.45	0.6464	0.6486	0.3403465347

Capacitance:

frequency	current	capacitance
1.00E+08	1.51E-06	2.40973E-15
2.00E+08	3.14E-06	2.49662E-15
3.00E+08	4.71E-06	2.49645E-15
3.80E+08	5.96E-06	2.49625E-15
4.60E+08	7.21E-06	2.49603E-15
5.00E+08	7.84E-06	2.49585E-15
6.00E+08	9.41E-06	2.49550E-15
6.60E+08	1.03E-05	2.49533E-15
7.20E+08	1.13E-05	2.49486E-15
8.00E+08	1.25E-05	2.49436E-15
9.00E+08	1.41E-05	2.49383E-15
	Average =	2.48771E-15

Setup delay table:

rising Q ns	rising CLK ns	delay	
10.7126	10.05	0.6626	
10.7132	10.05	0.6632	
10.7156	10.05	0.6656	
10.7185	10.05	0.6685	
10.7281	10.05	0.6781	
10.7524	10.05	0.7024	
10.8212	10.05	0.7712	<- setup time
20.7241	10.05	10.6741	
falling Q ns	falling CLK ns	delay	
20.6651	20.05	0.6151	
20.6838	20.05	0.6338	
20.7354	20.05	0.6854	
none			

The setup delay is where the last value is the correct output as the input gets closer to the rising edge of the clock. The setup is the largest value of the rising and falling delay that is still the correct value.