

Reverse Engineering of an MP4 Player Platform (SPC Internet 8488, 8 GB, 2014)

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Jan. 2026 – Present

Abstract— This portfolio article documents an ongoing personal reverse-engineering effort on the *SPC Internet 8488* MP4 player (8 GB, 2014). The work focuses on reconstructing the hardware architecture and design intent under scarce public documentation, producing reusable engineering artifacts (verified KiCad libraries, functional models, and progressively refined schematic hypotheses). The end goal, after full hardware characterization, is to propose a modernized, optimized architecture aligned with current design practices.



Figure 1: SPC Internet 8488 (8 GB, 2014): reference product used for reverse engineering.

1 Project Scope and Motivation

This project aims to reverse engineer a consumer MP4 player platform with limited public information, moving from physical product inspection to reconstructed design artifacts. The emphasis is not only on identifying parts, but on building a coherent technical narrative: power domains, clocks, storage subsystem, audio chain, and IO, along with the probable engineering trade-offs behind the original design decisions.

1.1 Physical Product Identification

The first step is to anchor the analysis on the real device: exact model, storage variant, external interfaces, and any revision clues. This bounds the plausible SoC families, storage topology, and power architecture typical of the 2013–2014 time frame.

This is anchored on the real device used as reference, shown in Figure 1.

1.2 PCB Teardown and Early Layer-Stack Hypothesis

After disassembly, the PCB is inspected to identify reference designators, test points, copper density, and via patterns. Without destructive methods, visual evidence already suggests a multi-layer board. Based on routing density, via distribution, and the presence of large uninterrupted copper areas that resemble planes,

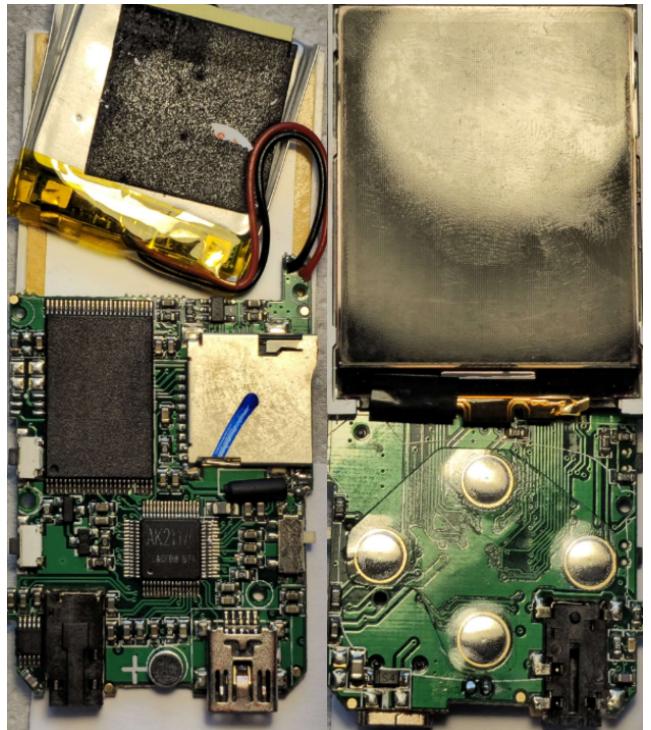


Figure 2: Real PCB photographs: component identification, routing constraints, and a first estimate of a 4-layer stack-up.

the current working hypothesis is a **4-layer PCB** (signal/plane/plane/signal), a common compromise for compact consumer electronics where return paths and EMC matter but cost is constrained.

Representative PCB photographs supporting this assessment are provided in Figure 2.

1.3 Documentation Search Under Scarce-Information Constraints

A major difficulty is that many consumer-electronics platforms use SoCs and companion parts with minimal public documentation. The workflow therefore relies on multi-source triangulation: part-marking interpretation, archived PDFs, distributor remnants, and cross-checking partial datasheets. Typically, the result is fragmented—sometimes enough to infer pin functions and interface families, but rarely enough to reconstruct the design directly from documentation.

The documentation recovery is illustrated in Figure 3.

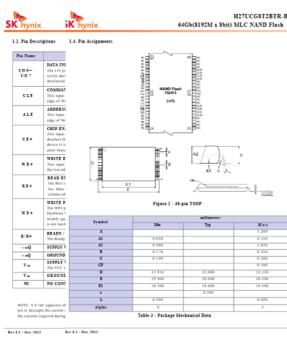


Figure 3: Documentation recovery approach: identifying parts and cross-checking scattered information from multiple sources.

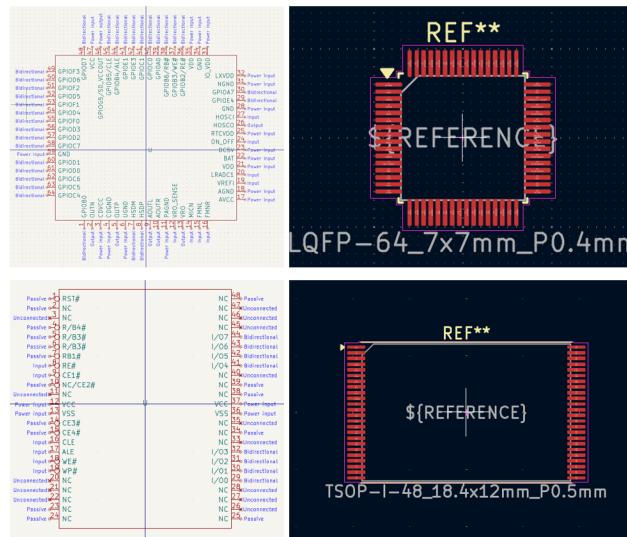


Figure 4: Custom KiCad symbols and footprints created to rebuild missing design libraries.

1.4 KiCad Library Reconstruction: Custom Symbols and Footprints

Once key parts and connectors are identified, the project transitions into rebuilding a clean CAD foundation. Dedicated KiCad symbols and footprints are created for specific packages and uncommon connectors, enabling consistent annotation, net naming, and future schematic capture. This is essential because reverse engineering is also the reconstruction of engineering assets that were never available.

Examples of the custom libraries produced during this phase are shown in Figure 4.

1.5 Footprint Verification and Mechanical Consistency Checks

Footprints must be verified against the real PCB to avoid propagating subtle errors. The verification strategy includes pitch and body-size consistency, overlay alignment with high-resolution PCB photos, and sanity checks against any available mechanical drawings. The objective is a set of libraries that are not merely plausible, but **manufacturing-accurate** and reusable.

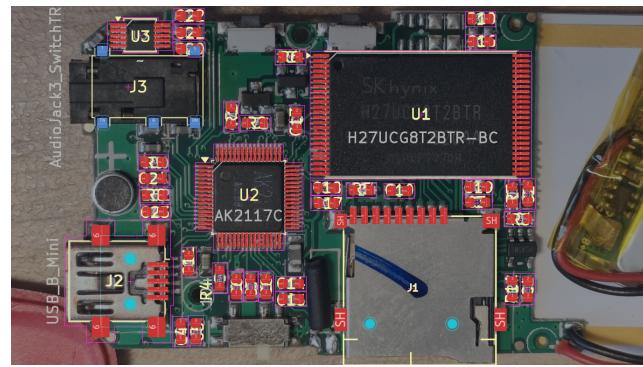


Figure 5: Footprint verification workflow: overlay checks and dimensional consistency against the real PCB.

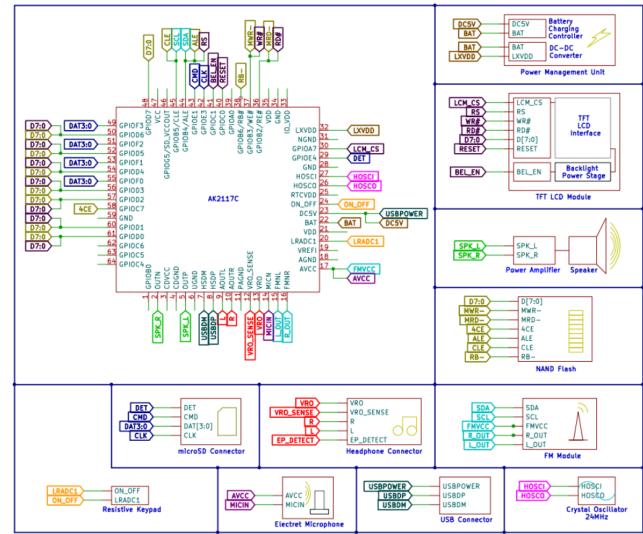


Figure 6: Proposed functional block diagram structuring the current architectural hypotheses.

The verification workflow and consistency checks are summarized in Figure 5.

1.6 Functional Block Diagram: From Observations to Architecture

With enough evidence collected (parts, placement, interface clues, and routing patterns), a functional block diagram is proposed. It is intentionally iterative: it separates confirmed from inferred blocks and helps identify what must be measured or proven next (power distribution, clocking, audio path, storage connectivity, and user IO).

The current architecture-level hypothesis is synthesized in the functional block diagram of Figure 6.

1.7 Early Schematic Hypotheses and Progressive Reconstruction

The next stage is schematic reconstruction: mapping power rails, decoupling strategy, storage interface, and audio output chain. At this point, schematics are hypotheses that evolve as more nets become confirmed and as pin-level assumptions are validated. The aim is to converge toward a consistent set of schematics that

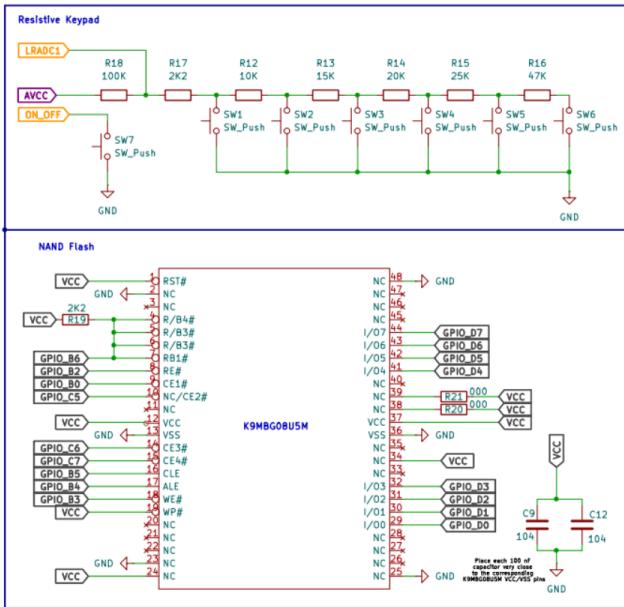


Figure 7: Initial schematic reconstruction attempts: progressively refined as nets and hypotheses are validated.

explains both the physical routing and the expected functional behavior.

Selected schematic hypotheses illustrating the reconstruction process are presented in Figure 7.

2 Preliminary CAD Reconstruction in KiCad

In parallel with schematic hypothesis development, a preliminary 3D CAD reconstruction of the PCB has been initiated in KiCad. This early-stage model does not aim to replicate the exact original board routing, but rather to validate footprint consistency, mechanical clearances, connector alignment, and approximate component placement coherence based on the reverse-engineered data collected so far.

The objective of this step is twofold: first, to ensure that the reconstructed libraries integrate correctly within a realistic PCB environment; and second, to begin visualizing how the identified functional blocks may physically map onto a manufacturable layout. Even at this premature stage, spatial constraints and placement logic already provide additional insight into probable design intentions and layout trade-offs.

Although this model remains incomplete, it serves as an important intermediate validation layer between schematic reasoning and potential architectural redesign.

A preliminary 3D CAD model derived from the reverse-engineered data is presented in Figure 8.

3 Current Status and Next Steps

At the current stage, I am still identifying additional schematic fragments, verifying expected behaviors using circuit simulations (notably with LTspice), and

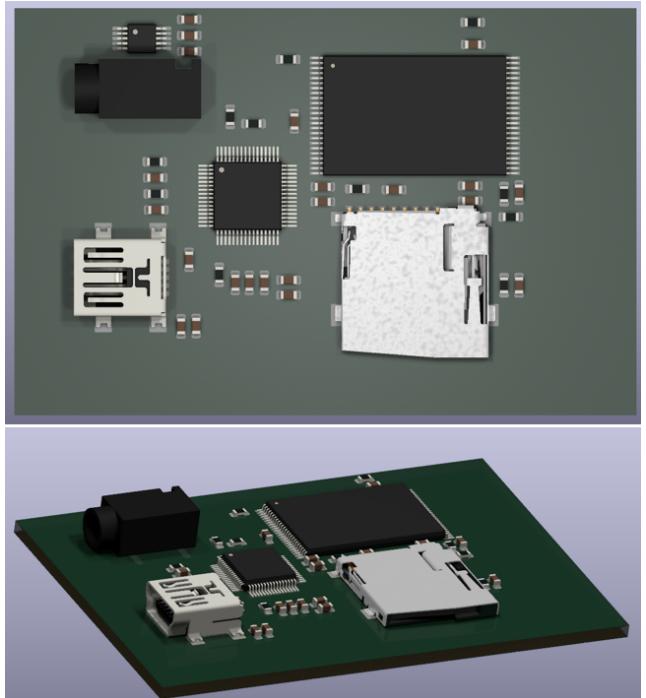


Figure 8: Preliminary 3D CAD model of the reconstructed PCB in KiCad. This version represents an early structural approximation derived from reverse-engineered data.

analyzing plausible subsystem operating modes. The immediate objective is to reduce uncertainty via electrical consistency checks (power sequencing, analog biasing, interface constraints, and realistic component behavior).

After the full hardware reverse engineering is completed, the next step will be to propose a **modernized and optimized architecture** aligned with current best practices: improved power efficiency, updated storage and interfaces, enhanced ESD/EMC robustness, and clean documentation from day one.

4 Personal Context

This is a **personal project** conducted outside of my formal studies at **INSA Toulouse**. Its objective is to deepen my understanding of real-world hardware architectures and design rationale, while strengthening my ability to document, model, and analyze systems that ship with limited documentation. Due to its iterative nature, it may require **several additional months** of continued refinement.

Although Figure 7 presents selected schematic hypotheses, the complete set of reconstructed diagrams and net-level mappings is not disclosed. This document is intended solely as a **portfolio-oriented technical overview**, highlighting methodology and engineering depth rather than serving as a full technical dossier or step-by-step reconstruction guide.

Only representative fragments are shown to illustrate the complexity of the work, while maintaining professional and ethical responsibility regarding potential intellectual property considerations.