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Specification of the Front-End Readout Chip for the PCT Tracker (pCTFE64)

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# Introduction

The pCTFE64 chip is the front-end of the data acquisition for the silicon-strip tracking detector of the proton-CT detector system. This document began as the design specification of the pCTFE64 chip, but it has been updated throughout the design process to correspond to the actual design. Therefore, it also serves as documentation of the as-built chip.

# Overview

Refer to the block diagram, Fig. 1. The front end is based on one two-stage charge-sensitive amplifier per channel. A programmable option switches an inverter into the circuit between the preamplifier and shaping amplifier and adjusts the preamplifier baseline, to adapt the chip to detectors of opposite polarity while maintaining maximum dynamic range. The preamplifier is AC coupled to the shaping amplifier, and the shaping amplifier output is DC coupled to a discriminator. The common threshold of the 64 discriminators is set by a DAC, which has a low range (for taking data) and a high range (for calibration scans). The DAC is set by loading its register via a dedicated command.

The amplifiers are continually sensitive, and on each cycle of a nominally 20 MHz clock each channel’s discriminator status is latched into a 32-clock-deep “Hit Buffer” according to whether the rising edge of the channel’s amplifier output crossed the discriminator threshold. Individual channels may be suppressed via the data mask from contributing to the Hit Buffer.

The Trigger-Request signal is an asynchronous OR of the outputs of all 64 discriminators, after passing through the trigger mask. It is to be used by the experiment’s trigger logic to form the Trigger-Acknowledge that is returned to the front-end chips after a fixed delay. Typically the trigger logic would be a coincidence of two or more tracking layers or even a coincidence with the calorimeter.

When the Trigger-Acknowledge signal is received, an event is immediately moved from the Hit Buffer into one of four event processors, along with the 2-bit trigger tag that comes with the Trigger-Acknowledge signal. The location chosen to read from the Hit Buffer can be adjusted to correspond to the round-trip time of the trigger logic

Each event processor maps to a single location in the event output buffer. Therefore, up to four events can be processed in parallel, and four events can be buffered at the output awaiting read commands. An event processor takes the 64 channel bits, plus the 3-bit trigger word, and processes them into a formatted cluster list, which is stored in the corresponding output buffer. An event is sent off-chip from the output buffer following receipt of a Read command.

The internal calibration system consists of a calibration DAC and a mask register, together with a pulse generator. It allows an arbitrary set of channels to be pulsed, all at the same amplitude as set by the DAC.

The command decoder contains a configuration register to be used for modifying the settings of the chip, in addition to the mask and DAC registers mentioned above. Each individual register may be read back by dedicated command via the data output, to verify the register loading. The read back is non-destructive. The registers have reasonable power-up default settings, but each may be set per individual chip by command.

Except for the 64 analog channel inputs, all communication with the chip takes place via LVDS-type differential pairs.

# Performance and Timing Specifications

The chip must function with any input clock frequency from 1 kHz to 120 MHz. In particular, the number of clock edges between the time of the issued read command and the time for which the output data are assumed to be valid must be invariant and independent of the clock rate. This is so that the DAQ can know exactly on which clock cycle to expect the data to arrive (although in principle it could just wait for the start bit). Therefore, the rise time of the data output must be significantly less than the period of the fastest clock.[[1]](#footnote-1)

The chip must be able to handle a Poisson-distributed trigger rate with a mean of up to 2 MHz with no more than 10% dead time, assuming that each trigger results in a Poisson-distributed number of clusters of mean equal to or less than one. This assumes that the DAQ requests events from a given chip as soon as they are ready, without waiting for all other chips in the system also to be ready.

# Amplifier Chain

The analog requirements for the amplifiers follow from these considerations. For a 200 micron thick detector, a 250 MeV proton will deposit about 4.8 fC of charge, almost twice minimum ionizing. A 2.4 MeV proton will deposit about 150 fC of charge.

The channel input capacitance is expected to be about 11 pF for single strips or 22 pF for two strips ganged together. The specifications are derived for the worst case: 22 pF.[[2]](#footnote-2)

The nominal peaking time of the amplifier shall be 200 ns, but a longer peaking time of 400 ns may be selected in the configuration register. The longer shaping time is primarily intended to be used for operating with minimum-ionizing cosmic rays. The equivalent noise charge with the 200 ns peaking time shall be no more than 0.2 fC (1250 electrons) for the 11 pF strips and no more than 0.32 fC (2000 electrons) for the 22 pF strips.

## Charge Amplifier

The amplifiers have two choices of gain, selected by the configuration register, to allow detection of incoming 250 MeV protons (and MIPs) on the highest gain setting and slow protons, following the phantom, on the lower gain setting. The integration time constant of this stage shall be no longer than about 100 ns, and the gain shall be approximately as follows (for negative input signals, these apply to the preamplifier plus inverter put together):

* Low gain: 3 mV/fC
* High gain: 9 mV/fC

The dynamic range shall be large enough that in the low gain setting two closely spaced 150 fC charge depositions will not saturate.

## Inverter

For a negative expected signal an inversion is programmed into this stage. For a positive expected signal the stage is programmed to pass the signal through unchanged.

## Shaping Amplifier

This amplifier has two choices of time constant as well as two gain choices, selected by the configuration register, to allow detection of MIPs on the slowest setting and optimization of front versus back layers (fast versus slow protons) for the faster setting. The gain settings shall be approximately as follows (the ratio of shaper peak amplitude to preamplifier output amplitude:

* Low gain: 6 (20 mV/fC overall)
* High gain: 9 (80 mV/fC overall)

The coupling from the preamplifier to the shaping amplifier shall be AC. The coupling to the discriminator shall be DC, with the shaping amplifier output baseline controlled to the specifications given in the discriminator section below.

## Discriminator

The discriminator threshold shall not vary by more than ±10% rms across the 64 channels of a chip. This includes contributions to the offset due to the channel-to-channel matching of the shaping amplifier output baseline and to the amplifier gain matching from channel to channel.

## Threshold DAC

This is a 7-bit DAC with two ranges, for a total of 8 control bits. The 8-bit register must include a non-destructive read. The two linear ranges are as follows (note the offset: a DAC setting of 0 yields 1 LSB, not zero):

|  |  |  |  |
| --- | --- | --- | --- |
| **Range** | **LSB** | **Nominal** | **Maximum** |
| Low | 4 mV | (1.2 fC) 96 mV | 512 mV |
| High | 16 mV | N/A | 2048 mV |

These values refer to the difference between the shaper reference voltage (nominally 0.8 V), which sets the shaper output baseline, and the absolute threshold voltage. The DAC must provide both levels. The nominal value is intended for operation with the 200 ns peaking time and 22 pF load. With the high gain setting it corresponds to 1.2 fC, one fourth of the nominal signal from a 250 MeV proton. The high range is primarily intended for diagnostic purposes, allowing threshold scans to be carried out over the full dynamic range of the shaping amplifier output.

The default setting of the threshold DAC is 96 mV (1.2 fC) on the low range, corresponding to a setting of 8’h17. The DAC will require a couple of microseconds to settle into a new setting.

## External Current References

Three external pads are designed to be connected to analog power or analog ground via external resistors, to program bias currents in the chip:

* IFE: sets the bias current of the input transistor. This is nominally 200 μA, but it can be increased substantially if needed to improve noise performance.
* IBias: sets most bias currents in the chip. This is nominally 33 μA via a resistor connected to the AVDD supply.
* IShaper: sets the reset currents of the shaping amplifier. This is nominally 50 μA via a resistor connected to the AVDD supply, but it may need to be adjusted to get the desired shaper response.
* IPreamp: sets the reset currents of the preamplifier. This is nominally 50 μA via a resistor connected to the AVDD supply, but it may need to be adjusted to get the desired response.

Depending on experience with the first prototype, it may be possible to get rid of some of these pads and external current sources in the final production design.

# Clock

The clock input is nominally a 100 MHz differential pair. The system is not wedded to this clock speed. For example, a 50 MHz clock could be used with a 25 MHz Hit Buffer clock, or a 40 MHz clock could be used with a 20 MHz Hit Buffer (but in that case the system could probably not keep up with a 2 MHz trigger).

It is important that all major circuits used during data taking are clocked continuously during data taking, particularly shift registers, in order to maintain a constant power load. For example, a readout register should shift on every clock cycle regardless of whether it is being used. This helps prevent transients from being seen by the sensitive preamplifiers. For example, when a read command is received we do not want the power load to increase as shift registers suddenly start up. This is not an issue for any of the configuration, mask, or DAC registers, which are always static throughout data taking.

# Channel Masks

## Trigger Mask

One bit per channel determines whether the discriminator output contributes to the Fast-OR trigger output. The mask register must include a non-destructive read. The default setting of the trigger mask is to enable all channels.

## Data Mask

One bit per channel determines whether the discriminator output goes into the event buffer when a trigger acknowledge is received. In the case that a channel is masked off, a zero is written into the event buffer. The mask register must include a non-destructive read. The default setting of the data mask is to enable all channels.

# Calibration System

## Calibration Mask

One bit per channel determines whether the calibration pulse reaches the respective channel. The switch needs to be designed such that the calibration signal does not capacitively propagate through the open switch. That can be accomplished by providing a second switch that connects the calibration input to ground when the switch from the calibration pulser is open.

The mask register must include a non-destructive read. The default setting of the mask is to enable all channels. This was a convenient design setting. Useful settings have to be achieved by loading the register by command.

## Calibration DAC

This is a 7-bit DAC with two ranges, for a total of 8 control bits. The 8-bit register must include a non-destructive read. The DAC output is switched by a control signal to provide a 2048 clock long (about 34 μs) square pulse to the calibration capacitors on the channel inputs selected by the calibration mask. The two ranges are defined as follows:

|  |  |  |  |
| --- | --- | --- | --- |
| **Range** | **LSB** | **Nominal** | **Maximum** |
| Low | 2 mV | 48 mV (1.2 fC) | 254 mV (6.2 fC) |
| High | 12 mV | 240 mV (6.0 fC) | 1524 mV (37 fC) |

These values assume a calibration capacitor of 25 fF. With 32 channels pulsed simultaneously the rise time of the pulse should be a few tens of nanoseconds.

The default setting of the calibration DAC is the low range at about 48 mV (4.8 fC), corresponding to a setting of 8’h17. With the 25 fF calibration capacitor, the injected charge should be 1.2 fC. The DAC will require a couple of microseconds to settle into a new setting.

## Calibration Strobe

A calibration event is initiated by the Calibration Strobe command. The 8-bit data for the command specify how many clock cycles to wait (bits 7:2) before issuing internally a Trigger Acknowledge, as well as the trigger tag (bits 1:0) to use. During the wait time between Strobe and Trigger Acknowledge the external Trigger Acknowledge shall be disabled.

# Trigger

## Fast-OR Output

This is a logical OR of all 64 discriminator outputs, after passing through the trigger mask. It is asynchronous, with LVDS output. Logic on the front-end board will accomplish a logical OR of these signals from all front-end chips on the detector layer.

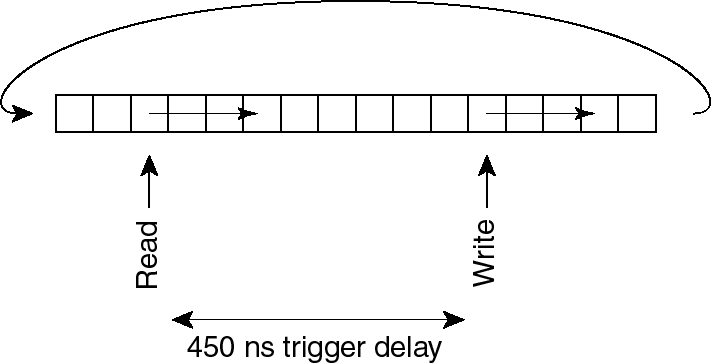
## Trigger Receiver

This receiver monitors the trigger acknowledge output and looks for a start bit. When the start bit is detected it reads the following 2 bits and stores them along with the event as a trigger tag that is subsequently used to verify that events are not mixed from chip to chip up by the DAQ.

# Edge Sensitive Latch

The status of each discriminator output is sampled every 50 ns (nominal) by synchronous logic. Each time the discriminator status goes from low to high the output will remain high (depending on the setting) for two clock cycles (100 ns nominal) or three clock cycles (150 ns nominal) and then return to low, unless the input stays high for only a single clock cycle, in which case the output is also high for only a single clock cycle. The choice of 3 versus 2 clock cycles is set by a bit in the configuration register.

# Hit and Output buffers

On every cycle of the sample clock (20 MHz nominal) the contents of the edge sensitive latch are copied into the hit buffer at the current position of the write pointer. The write pointer increments with each 20 MHz clock cycle, and after 32 cycles (1.6 microseconds, TBR) the buffer wraps around and starts to overwrite itself.

When the Trigger-Acknowledge signal is received, an event and the 2-bit trigger tag that comes with the Trigger-Acknowledge are immediately moved from the Hit Buffer into one of the four event processors, selected by the trigger tag. Up to four such processors operate in parallel in order to keep up with a maximum trigger rate of 2 MHz. The correct event in the Hit Buffer is selected by a read pointer that follows behind the write pointer, separated by a fixed delay that is set by bits in the configuration register. This delay should correspond to the round-trip time of the trigger logic. Since the edge sensitive latch (previous section) keeps a hit channel high for two clock cycles, then events that occur near a clock edge should have all hits overlapping in one word of this memory, as long as the rise time of the signals is fast enough. For high efficiency the trigger jitter has to be less than the 100 ns resolution. Otherwise the clocking of the Hit Buffer would have to be slowed down to avoid missing hits.

Each event processor maps to a single location in the output buffer. Therefore, up to four events can be processed in parallel, and four events can be buffered at the output awaiting read commands.

An event processor takes the 64 channel bits, plus the 3-bit trigger word, and processes them into a formatted cluster list, which is stored in the corresponding output buffer. An event is sent off-chip from the output buffer following receipt of a Read command, which includes a data field of two bits that selects which output buffer to use. Up to 4 Read commands, one for each output buffer, may be sent in succession at any time. The chip will save them until the corresponding events are ready in the corresponding output buffers. A Read command is ignored, however, if the corresponding buffer is already holding a previous Read command, waiting for the buffer to be ready. Note that the Trigger-Acknowledge and Read commands determine which event-processor/output-buffer pair is used. Buffer control is thus left up to the data acquisition system, which must continuously run a buffer model of the front end in order to know which buffers are available for use.

# Communication

## External Signaling

All digital signals input to the chip and sent from the chip must be low-voltage differential, compatible with commercial LVDS chips. It does not necessarily adhere to all aspects of the LVDS standard TIA/EIA-644, TBD. In particular, the voltage swing on signals confined to a single PCB can be smaller than the standard (e.g. 150 mV across a 75Ω termination, instead of 350 mV across 100Ω). The chip has four choices of transmitter drive current, set by two bits in the configuration register, as specified in the table describing the configuration register, assuming a 50μA reference current on the ILVDS pin. (The highest current setting will give a voltage swing of 300 mV across 100Ω.) Termination of the input LVDS lines must be provided by discrete resistors on the PCB, since those signals are generally viewed in parallel by several ICs on the same PCB.

All digital signals are received or sent MSB first, LSB last.

## Command Decoder, Addresses, and Command List

|  |  |  |
| --- | --- | --- |
| Command Name | Command Code | Data |
| NULL | 0 (0000) |  |
| RESET | 1 (0001) | None |
| READ | 2 (0010) | 2 bits (Trigger Tag) |
| READ CAL DAC | 3 (0011) | None |
| READ THRESH DAC | 4 (0100) | None |
| READ CONFIG REG | 5 (0101) | None |
| READ DATA MASK | 6 (0110) | None |
| READ TRIG MASK | 7 (0111) | None |
| READ CALIB MASK | 8 (1000) | None |
| LOAD CAL DAC | 9 (1001) | 8 bits  [7]: range select  [6:0] voltage setting |
| LOAD THRESH DAC | A (1010) | 8 bits  [7]: range select  [6:0] voltage setting |
| LOAD CONFIG REG | B (1011) | 19 bits (see below) |
| LOAD DATA MASK | C (1100) | 64 bits |
| LOAD TRIG MASK | D (1101) | 64 bits |
| LOAD CALIB MASK | E (1110) | 64 bits |
| CALIBRATION STROBE | F (1111) | 8 bits  [7:2] Trigger delay (number clock cycles)  [1:0] Trigger tag |

All commands may either be addressed to an individual chip (00 through 1E) or broadcast simultaneously to all chips (1F). Each command string consists of, in order, the following fields

1. Start bit (1)
2. 5-bit address of the chip to be commanded, or 1F for broadcast to all chips
3. 4-bit command code
4. Parity bit (do not count the start bit in the parity calculation)
5. Data field of 0 to 64 bits, depending on the command

## Data Transfer and Data Format

Data are sent by each chip to the DAQ on a single differential pair. The data transfer rate is one bit per clock cycle. The formatted event list is sent via this serial output following reception of a read command.

The logic that forms the output list needs to scan all 64 channels. Doing this serially in 64 clock cycles at 60 MHz (1.1 μs) is too slow for a 2 MHz trigger rate. Therefore there are four engines that do this scan in parallel, each initiated by a different Trigger Acknowledge tag code. Each engine maps to a separate event buffer where its output is stored pending readout.

The error bit in the header word indicates that an error occurred in the event processor identified by the trigger tag either with this event or an event in the past, since the last reset. The error was either a read command received without a prior trigger or a trigger received while the processor was busy. The error code may be read from the configuration register. The only way to clear the error flag is to reset the chip (“soft” reset command). Such errors generally result in the data stream getting out of sync, such that the trigger tag will not match from one chip to the next.

The data output format is a list of 6-bit words as follows

1. Header word:
   * Start bit (1)
   * Packet type: 0=data
   * 2-bit trigger tag (also identifies the event processor that was used)
   * Error bit. If set, read the configuration register to get the error code. This includes the two buffer-control error bits, but not the parity-error bit.
   * Parity bit (this parity calculation includes the start bit)
2. Number of clusters (0 to 10) (>32 clusters is not possible for the 64-channel chip, but the number is truncated to a maximum of 10). The highest order bit is set if the data list was truncated.
3. Cluster 1, number of strips minus 1 (0 to 63)
4. Cluster 1, address of the first strip (0 to 63)
5. Cluster 2, number of strips minus 1 (0 to 63)
6. Cluster 2, address of the first strip (0 to 63)
7. Etc.

For read-back of registers the format is different:

1. Header word:
   * Start bit (1)
   * Packet type: 1=register read-back
   * 3-bit register identifier
     + 1= Calibration DAC register
     + 2= Threshold DAC register
     + 3= Configuration register
     + 4= Data mask register
     + 5= Trigger mask register
     + 6= Calibration mask register
   * Empty bit (not used, but generally set to 1)
2. Eleven 6-bit words containing the 64-bit register information, padded at the end with two additional 1 bits. For registers shorter than 64 bits the unused bits are padded with 1 bits.

The data acquisition system looks for the start bit to start reading a data packet. There must be at least one zero on the data line following a data packet and preceding the start bit of the next packet.

When the mask registers are read back, the first bit of the mask to be read out is Channel 0, and the last bit is Channel 63.

## Configuration Register and Read-back

The following table describes the 22 bits of the register. Note that only the first 19 are loaded by the load-configuration-register command. The last 3 bits are error bits set internally during operation.

|  |  |  |  |
| --- | --- | --- | --- |
| **Name** | **Bits** | **Default (dec)** | **Description** |
| Polarity | 0 | 0 | Set to engage the inverter between preamp and shaper |
| 1-Shot | 1 | 0 | If low (0), then the trigger output is the logical-OR of all channels following the edge-sensitive latch. That is, one hit will produce only a 100 ns long pulse. If high (1), then the trigger output is the logical-OR of the discriminator outputs and will stay high as long as a shaper output is above threshold. This would allow the TOT to be measured, probably only for diagnostics. |
| Gain | 2 | 0 | Low (1) versus High (0) gain settings |
| Shaping Time | 3 | 0 | Short (0) versus Long (1) shaping times |
| Buffer speed | 6:4 | 3 | By how much to divide the system clock (60 MHz nominal) to derive the Hit Buffer clock (20 MHz nominal). The divisor is this value plus one, so the period can be multiplied by any number 1 through 8. |
| Trigger delay | 11:7 | 4 | Number of clock cycles (at the buffer speed) between the write and read pointers of the Hit Buffer |
| Trigger Window | 12 | 0 | 0=2-clock window; 1=3-clock window |
| Output Drive | 14:13 | 2 | Output current setting for the LVDS driver. Assuming a 50μA reference current, the following are the predicted currents.  00=0.25 mA  01=1.2 mA  10=2.2 mA  11=3.1 mA |
| Max Clusters | 18:15 | 4 | Maximum number of clusters output. Must be in the range 1 to 10. |
| Error code | 21:19 | 0 | 3-bit error code set internally  bit 0 (lsb): Read command sent with no prior trigger  bit 1: Trigger received while previous one was in  progress  bit 2: Parity error detected on the command line |

The configuration register includes a non-destructive read, used to verify the contents and also retrieve the error code. The read returns all 22 bits. The default is 000 0100 00 0 00100 011 0000 if there are no errors flagged.

Loading the configuration register causes the output drive current to change during the serial shift in of the bits, even if the driver setting is not being changed. This disrupts the balance of the driver. The user must allow at least ¼ of a millisecond before trying to read data from the TReq and Data outputs.

Loading the configuration register also disrupts all of the 64 channel amplifiers, so operations must allow at least 10 microseconds for the amplifiers to settle before commencing data taking. Loading the register might also cause the calibration strobe to fire, in which case 20 or more microseconds of settling time would be needed. In general, to be safe one should wait a few milliseconds after loading the configuration register before doing anything with the chip.

## Trigger Acknowledge

The Trigger Acknowledge signal consists of a start bit and a 2-bit trigger tag. The trigger tag selects which readout-engine/output-buffer combination to use, and it is stored with the event, to be used by the DAQ to check that events don’t get mixed up from one chip to the next.

## Resets

All of the configuration registers (masks, DACs, etc.) and state machines have a set or reset. The event memories do not need any set or reset. There is no automatic power-on reset. After power-on either a hard or a soft reset should be issued.

### Hard Reset

The chip includes an external pad that if pulsed low for at least one clock cycle causes all of the state machines and read/write pointers of the chip to be reset and also resets contents of the configuration register, the masks, and the DAC registers. The signal should pull high internally, such that if there is not a connection the chip will not be reset. This hard reset is for just in case the command interpreter gets stuck (in principle that cannot happen), as its only difference from the soft reset command is that it resets the state machine of the command interpreter.

### Soft Reset

The RESET command resets the read/write pointers of the Hit Buffer and all state machines except those in the command interpreter. (There is no sense resetting the command interpreter, since if it isn’t working then it cannot receive this command.) It also puts all of the registers into their default settings. The command interpreter should always go into the state that looks for a new command after a finite number of clock cycles, so that a soft reset can be sent after power-on. Since the soft reset command clears the error flags in the configuration register, then parity checking does not likely work for this one command. The parity error flag will be cleared as soon as it is set.

## Calibration Strobe

A pulse of amplitude set by the Calibration DAC and duration 2048 clock cycles is sent to those channels selected by the Calibration Mask. After a delay of a number of clock cycles set by the data word of the Calibration Strobe command, a Trigger Acknowledge is issued internally. The calibration pulse is inverted if the 0th bit of the configuration register is set (i.e. when the amplifier is configured for negative input signals). Note that the falling edge of the calibration strobe will inject the amplifiers with the wrong-sign signal, so calibration operations have to allow sufficient settling time between successive calibration pulses.

# ESD Protection, Grounding, Power

All external non-power pads include ESD protection circuits. The capacitance of the channel input pads does need to be kept very small compared with the minimum detector capacitance of 11 pF, and their series resistance should not exceed 50 ohms.[[3]](#footnote-3)

The analog and digital parts of the chip have separate grounds, each tied to the substrate. An implanted barrier the length of the chip separates the substrate on the digital side from that on the analog side. The boundary between the two sides occurs after the two CMOS inverters on the discriminator output, which is on the analog side, and the input of the edge sensitive latch, which is on the digital side. The two DACs and their associated registers operate on the analog side, and the calibration mask is also on the analog side. Note that those registers never shift during data acquisition, so they do not present a noise issue.

The analog and digital power supplies are also separate. The analog power has two voltages. The lower voltage supplies current only to the preamplifier input transistor. A separate pad named QVDD supplies the bias voltage to the well of the input transistor. It is connected to the analog high voltage (AVDD) via a large external resistor. An external capacitor couples it to the analog low voltage (AVDD), forming a low-pass filter to keep the well free of noise.

The digital supply voltage is less than that of the analog supply, so logic levels passing between the two halves of the chip need to be level shifted.

|  |  |  |  |
| --- | --- | --- | --- |
| Power Supply Name | Nominal Voltage | Current | Description |
| AVDD2 | 2.0 V | 13 mA | Analog low voltage, for the input transistor bias current. This can be raised as high as 3.3 V, if necessary. |
| AVDD | 3.3 V | 5.7 mA | Analog high voltage. |
| QVDD | Same as AVDD | negligible | Bias voltage for the input transistor well. |
| DVDD | 2.5 V |  | Digital supply voltage |

# Physical Layout

## Chip Dimensional Constraints

We assume that a pitch-adapter circuit will be used to fan in the signals from the 228 micron pitch SSDs. Therefore, the channel pitch can be about 85 microns, resulting in a chip that will fit within the MOSIS project size. The other dimension can be adjusted as necessary to fit in all of the circuitry and the pad frame. Unlike the Fermi chip, there will be no wire-bond connections from one chip to the next, so the size of the gap between chips is not important. The final layout dimensions are 1.800 mm by 5.963 mm, but the final cut size will be determined by MOSIS. The pitch of the input pads within a row is 170 microns. The pad pitch on the back side of the chip is 200 microns. On the small ends the pitch varies from 190 microns to 250 microns.

## Input Pad Specification and Layout

All of the 64 analog input pads are on one long side of the chip, using a double row of pads to ensure sufficiently large pads for easy wire bonding. They need to be large enough to allow a second wire bond to be made in case of an initial bonding failure, without bonding on top of the old foot.[[4]](#footnote-4) The final bond pads are of dimension 130 μm by 150 μm.

## Chip Pin-Out

There is a total of 101 bond pads, numbered sequentially in a clockwise direction around the chip, of which one is used for test structures not associated with the chip itself. All other pads besides the 64 analog inputs are on the opposite side of the chip in a single row or on the two short edges. The pads on the short edges will bond to power pads on the printed circuit board that will be located between chips.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Name | Pin | Type | Dir. | Pol. | Description |
| Channel Inputs | 0…  63 | Signal | In |  | Analog channel inputs, to be connected to the detector strips. Pin 63 is Channel-0, while Pin 0 is Channel-63. |
| AVDD2 | 64  100 | Power | DC |  | Analog Power Low (2.0 V) |
| AVDD | 65  99 | Power | DC |  | Analog Power High (3.3 V) |
| QVDD | 74 | Power | DC |  | Analog Power High filtered for input transistor well bias |
| AGND | 66  98 | Power | DC |  | Analog Ground |
| IFE | 75 | Bias | DC |  | Analog current 330μA (connect 7.5kΩ to AVDD) |
| IBIAS | 72 | Bias | DC |  | Analog current 35μA (connect 68kΩ to AVDD) |
| ISHAPER | 71 | Bias | DC |  | Analog current 50μA (connect 51kΩ to AVDD) |
| IPREAMP | 73 | Bias | DC |  | Analog current 15μA (connect 180kΩ to AVDD) |
| VTX | 76 | Bias | DC |  | 1.2 V voltage reference for the LVDS transmitters & DACs |
| ILVDS | 85 | Bias | DC |  | 50 μA current for LVDS circuits (about 40kΩ to GND) |
| DVDD | 68  96  79 | Power | DC |  | Digital Power (2.5 V) |
| DGND | 67  97  78 | Power | DC |  | Digital Ground |
| TACKP  TACKM | 88  89 | LVDS | In | H | Trigger Acknowledge |
| CMDP  CMDM | 92  93 | LVDS | In | H | Command |
| CLKP  CLKM | 90  91 | LVDS | In | H | Clock (60 MHz or higher) |
| DATAP  DATAM | 86  87 | LVDS | Out | H | Data |
| TREQP  TREQM | 69  70 | LVDS | Out | H | Trigger Request (Fast OR) |
| A0 | 84 | CMOS | DC |  | Address Bit 0 (internal pull down) |
| A1 | 83 | CMOS | DC |  | Address Bit 1 (internal pull down) |
| A2 | 82 | CMOS | DC |  | Address Bit 2 (internal pull down) |
| A3 | 81 | CMOS | DC |  | Address Bit 3 (internal pull down) |
| A4 | 80 | CMOS | DC |  | Address Bit 4 (internal pull down) |
| RESETP  RESETM | 94  95 | LVDS | In |  | Hard Reset |
| TestPad | 77 | CMOS | In |  | Test pad with ESD protection cell and pull-down |

## 

## Internal Test Pads

Each channel shall have an internal probe pad at the shaper output and at the discriminator output. Probe pads are also necessary at the DAC outputs. Internal pads shall also be place on digital signals going into and out of the logic blocks, to the extent that is practical. The following is a table of the probe pads, not including those on the separate test structures (see below). In general the signals are buffered, such that probing them should not significantly affect the performance of the circuitry.

|  |  |
| --- | --- |
| Signals | Description |
| VThresh, Vref | Threshold and reference voltages from the threshold DAC. |
| CalVPulse | Analog calibration pulse output from the calibration DAC. |
| CalPulse | Digital calibration pulse, input to the calibration DAC. |
| TACKB | Inverted output from the TACK LVDS receiver. |
| RESETB | Inverted output from the RESET LVDS receiver. |
| CLKB | Inverted output from the Clock LVDS receiver. |
| CMDB | Inverted output from the Command LVDS receiver. |
| ShaperOut | Output of each of the 64 shaping amplifiers. |
| InvOut | Output of each of the 64 discriminators. |
| PreampOut | Output of preamplifier for only channel 0 (pin 63). |
| Clust3 | Output of the fourth 120-bit cluster shift register. |
| rrwlp31 | 32nd read word line in the HitBuffer. |
| lwwlp31 | 32nd write word line in the HitBuffer. |
| eo0 | Last channel output from the mask registers. |
| f63 | Last channel output from the HitBuffer. |
| q630 | Output from the first of the 64-bit parallel-in, serial-out shift registers. |
| Clock | Internal clock in the top-level schematic. |
| ClkEn | Internal data sampling clock in the top-level schematic. |
| CalMaskIn | Input data when loading the calibration mask. |
| DataMaskIn | Input data when loading the data mask. |
| TrigMaskIn | Input data when loading the trigger mask. |

## Test Structures

The following test structures are place in otherwise unused areas of silicon and are logically separate from the chip itself. (They are not visible in the plot of the chip shown above.)

1. An input pad (pad 77) with ESD protection and a pull-down transistor, plus an internal probe pad inside of the pad ring, on the opposite side of the ESD protection.
2. Both an NFET and a PFET, each of minimum length and 10 micron width, with 4 fingers. Probe pads are on the gates, sources and drains, while the substrates are tied to digital VDD or VSS.
3. An analog input PFET, of the same size and geometry as used in the preamplifiers, with internal wire-bond pads on all four connections, including the NWell. This is intended to be used for spectral noise measurements.
4. A digital ring oscillator made of a NAND gate and 17 inverters.
5. A resistor test structure with 14 polysilicone resistors in series with 7 probe pads tapping various points. See the schematic for the resistor values.

1. A point is made of this here because an early version of the Fermi GTFE chip had insufficient output drive, such that the time of arrival of the output data changed by a clock cycle between low and high frequency operation. [↑](#footnote-ref-1)
2. The capacitance might be 50% higher if the detectors are thin (i.e. 200 micron). [↑](#footnote-ref-2)
3. At room temperature 50 ohms produces 0.9 nV/√Hz, or 0.8 μV for τ=200 ns. With a 22 pF detector that corresponds to an rms noise charge of 110 electrons. [↑](#footnote-ref-3)
4. That was possible on the Fermi GTFE chip, which had 90 μm by 210 μm pads, and to a slightly lesser extent on the Fermi GTRC chip, for which the pads were 120 μm by 150 μm. [↑](#footnote-ref-4)