HW7

CSc 137, Fall 2015, Faroughi

Due Nov. 18 (Wed.) in class

Problems 5.2, 5.7 (use from right to left the input sequence 0101011; i.e., x = 1, then x = 1, then x = 0, etc.), 5.8, 5.15a (Verilog: Use structural models for NSG and OG and behavioral model for the FFs. Also see Example 5.9 for how to generate a clock signal), and 5.32 but assume IN = 6 (Hint: Buffer is full if IN = OUT and previous_IN +1 = OUT; buffer is empty if IN = OUT and previous_OUT + 1 = IN. Also, note that in Part c, Gray code values of IN and OUT are 1st converted to binary before buffer "full" or "empty" decisions are made).