Midterm Exam Study guide

CSc 137, Fall2015, Faroughi

Closed book, closed notes, and NO cheat sheets, calculators, cell phones, etc.

The study guide is presented with type of questions. The list is just a sample and does not mean the exam questions will be selected from this list. The exam questions will be similar.

1. All homework and project assignments prior to exam
2. Lecture topics as of 10/28/2015
3. Number representations and conversions: unsigned, signed magnitude, 2's complement, and floating point numbers (16 and 32 bits)
4. ILP, SIMD, multi-core architectural concepts and reasoning
5. Combinational circuit design: Block diagram, truth table, minimization (K-map, SOP, POS), and the final circuit
6. Designing with NAND or NOR gates
7. Buffer and tri-state buffers and applications
8. Fan-in and Fan-out: Can you describe them. Why are they problem; what do we need to do to resolve them
9. Basic combinational circuit modules: full-adder, decoder, encode, mux
10. 2's complement arithmetic and overflow
11. Propagation delay estimation
12. Transistor count and power
13. Combinational circuit timing diagram, glitches, and why glitches can increase power consumption
14. Bit-serial design methodology (e.g., project 1 where 2-bit CLA slices were used to design a CPA).
15. CPA (RCA), CLA, and hybrid; motivations for CLA;
16. Latches: SR Latch core (NOR gate version), Clocked SR latch, D latch. Purpose for the clock signal?
17. D Flip Flop (how does it work as edge triggered: set up and clock-to-q times: what do they mean and how they are used).
18. Clock period and frequency estimation
19. Multi-function register: How they are designed and operated
20. FSDs from a problem definition
21. FSM designs: Moore and Mealy: FSD; detailed block diagrams with FFs, NSG, and OG blocks showing all the signal connections; truth tables; finding minimal expressions (SOP or POS), and drawing the final circuit with FFs, OG, and NSG circuits
22. Counter design
23. Verilog behavioral models using "assign" statement.
24. Verilog structural models using primitive gates and known (predesigned) modules.
25. Verilog test-bench