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Homework 9
December 7, 2015

6.3b

Estimated Max Clock Frequency: Single Cycle =

$$\tau_{singlecycle} = 2\Delta_{add} + \Delta_{add/sub} + \tau_{st} + \tau_{cq} + \tau cs$$
$$\tau_{singlecycle} = 2 * (0.8ns) + 1.1ns + 0.05ns + 0.05ns + 0.05ns$$
$$\tau_{singlecycle} = 2.05ns$$

Estimated Max Clock Frequency: Pipeline =

$$\tau_{pipeline} = \Delta_{add/sub} + \tau_{st} + \tau_{cq} + \tau cs$$
$$\tau_{pipeline} = 1.1ns + 0.05ns + 0.05ns + 0.05ns$$
$$\tau_{pipeline} = 1.25ns$$

Estimated Pipeline Performance:

$$T_{pipeline} = k * \tau_{pipeline} + (N-1)\tau_{pipeline}$$

Estimated Pipeline Performance:

$$T_{singlecycle} = N * k * \tau_{pipeline}$$

Estimated Speedup : Pipeline vs Single Cycles

$$Speedup = \frac{T_{singlecycle}}{T_{pipeline}}$$

$$Speedup = \frac{N*k*\tau}{k\tau+(N-1)\tau}$$

$$Speedup = \frac{Nk}{k+N-1}$$

$$Speedup = \frac{1000*4}{4+1000-1}$$

$$Speedup = 3.988$$

8.7

Longest Path : Acc-ISA single-cycle data path

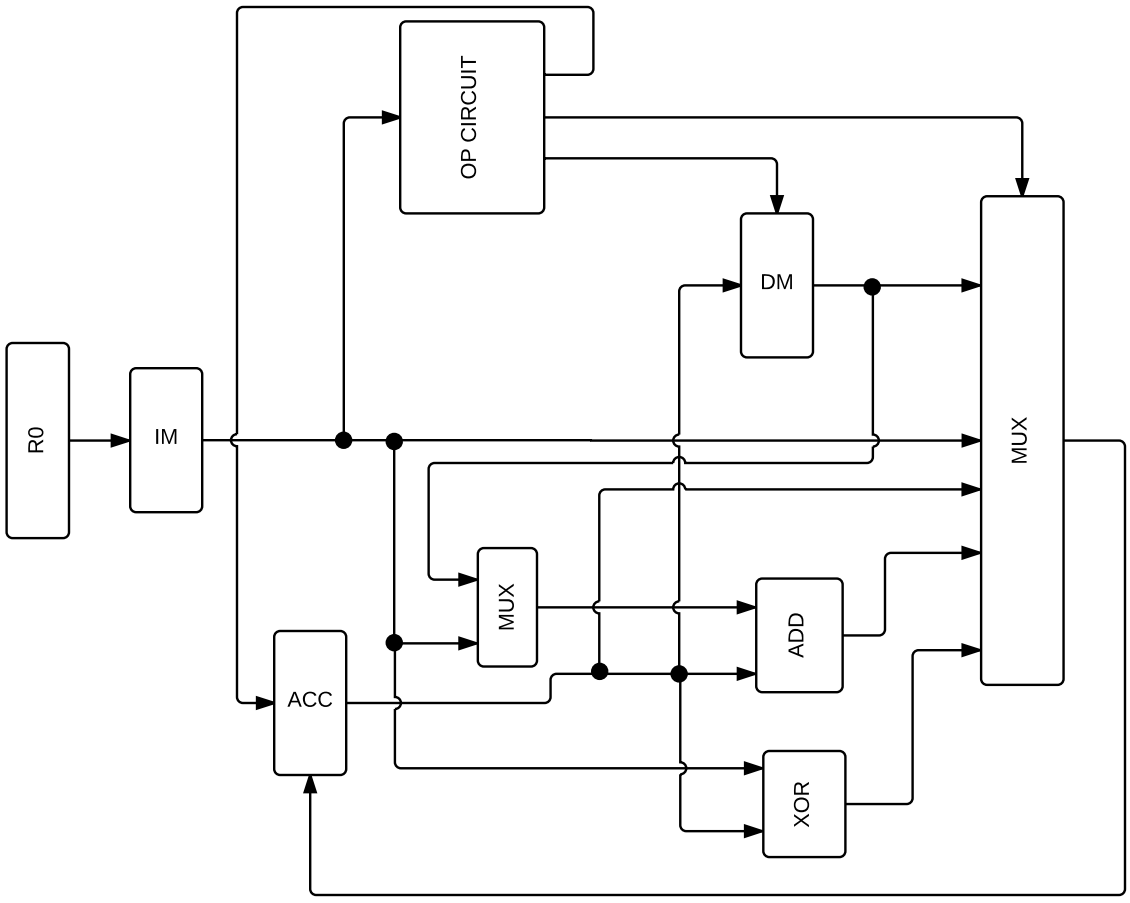
$$\tau_{cpu} = \Delta_{IM} + \Delta_{add} + \Delta_{MUX} + \Delta_{DM} + \Delta_{MUX} + \tau_{st} + \tau_{cq} + \tau cs$$
$$\tau_{cpu} = 1.2ns + 0.8ns + 0.3ns + 1.2ns + 0.3ns + 0.05ns + 0.05ns + 0.05ns$$
$$\tau_{cpu} = 3.95ns$$

8.2a

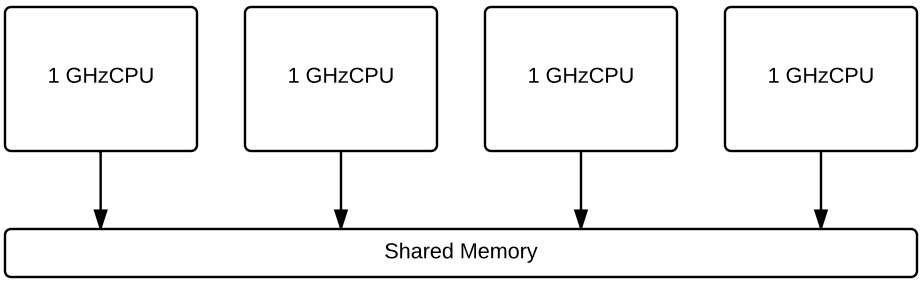
```
.code
LD 0
LD -2
ST mem(X)
LD 6
ST mem(Y)
LD 11
ST mem(Z)
LD mem(X)
ADD mem(Y)
ST mem(T)
LD 1
XOR mem(Z)
ADD 1
ADD mem(T)
ST mem(T)

.data
X: RB 1
Y: RB 1
Z: RB 1
T: RB 1
```

8.2b

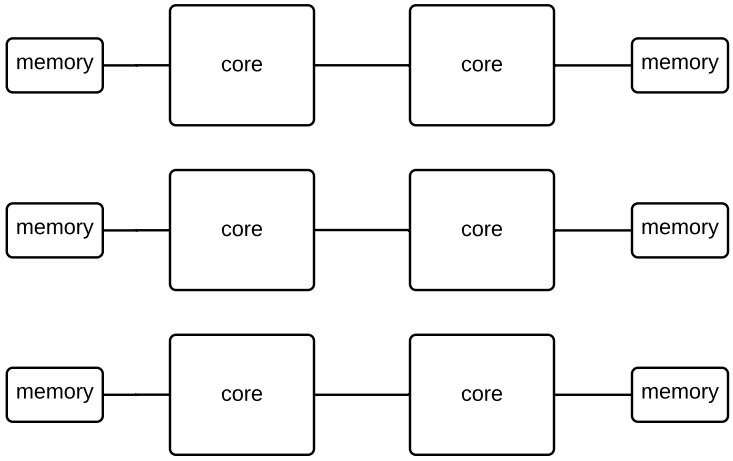


9.1a



$$\frac{10\% * 1\ GHz}{4\ \frac{Byte}{cycle}} = \frac{100\ M\ \frac{cycle}{sec}}{4\ \frac{Byte}{cycle}} = \frac{100\ MB}{4\ s} = 25\ MB/s$$

9.4



10.1

$$\begin{aligned} Main\ Memory\ peak\ bandwidth &= 800M\ \frac{cycle}{sec} * 4\ \frac{B}{cycle} \\ &= 3.2\ GB/s \\ Main\ Memory\ latency &= \frac{32\ B}{3.2\ GB/s} \\ &= 10\ ns \end{aligned}$$

$$\begin{aligned} Average\ Latency &= (0.95)(1ns) + (1-0.95)(0.90)(3ns) + (1-0.95)(1-0.90)(10ns) \\ &= 0.95ns + 0.135ns + 0.05ns \\ &= 1.135ns \end{aligned}$$