Project 2 ALU design
CSc 137, Fall 2015, Faroughi
Due in class on Nov. 23

Design an 8-bit, bit-parallel ALU with the following functions:

The list of ALU functions.

f2	f1	f0	Function
0	0	0	Not used
0	0	1	Add
0	1	0	Sub
0	1	1	Increment
1	0	0	Decrement
1	0	1	Bit-wised AND
1	1	0	Bit-wised XOR
1	1	1	Bit-wised NOT

Procedure:

1. Use your 8-bit hybrid adder to design an 8-bit 2's complement adder/subtractor module. Specifically, do:

    a. Design a behavioral Verilog model of an 8-bit inverter circuit with active-high control using an "if-else' statement.

    b. The adder/subtractor module shall also output overflow flag. Design the overflow flag generator using an "assign" statement. Also see part c.

    c. Combine the inverter and hybrid adder modules to create a structural Verilog model of the adder/subtractor. You may choose to generate the overflow-flag here.

2. Use an "if-else" statement to define an 8-bit 2-to-1 MUX module, and then use it to create a structural model for an 8-bit 4-to-1 MUX.

3. Use a "case" statement to model your Map circuit.

4. Use an "assign" statement to enter the Boolean expression for the Mask circuit. Note that the overflow bit is masked and would be displayed as zero (not active) when ALU performs a bitwise logic function.

5. Combine all the modules to create an structural model of the 8-bit ALU module.

6. Create a test-bench for your ALU module with the following test vectors:

    8'h7f + 8'h01

8’h80 – 8’h01
8’h00 – 8’h01
8’h01 + 8’hFF
8’hFF + 8’hFF
(8’hFF)++ //increment, use 8’hxx for B
(8’h00) -- //decrement, use 8’hxx for B
8’hFF AND 8’hFF
8’hFF ⊕ 8’hFF
8’h55 ⊕ 8’hAA
NOT 8’h55 //use 8’hxx for B
8’h55 ? 8’hAA //where ? identifies the not-used case, F = 0.

7. Order the outputs as follows and use hex format for values that are 8 bits and binary format for values that are less than 8 bits. Do not output values in decimal. Use “$display” to output time, F, A, and B, and “$monitor” to output also time and R and ovf.

Time F A B R ovf

8. Make sure the outputs are what you would expect them to be (do them by hand too).

9. Turn in your project following the format outlined in Project 1 and also include a complete block diagram of your ALU internal.