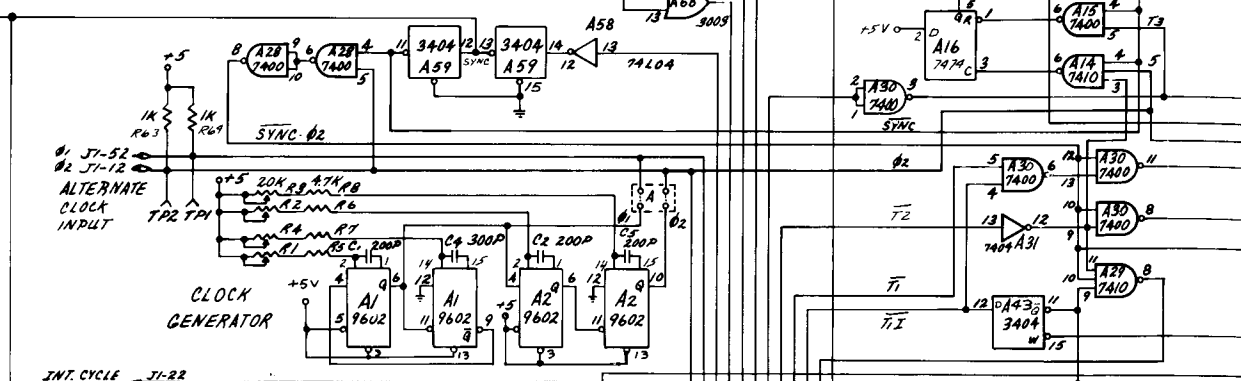


SYNC J1-75



WAIT J1-40

J1-41

J1-42

J1-43

J1-44

J1-45

J1-46

J1-47

J1-48

J1-49

J1-50

J1-51

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J1-86

J1-87

J1-88

J1-89

J1-90

J1-91

J1-92

J1-93

J1-94

J1-95

J1-96

J1-97

J1-98

J1-99

J1-100

RAM DATA IN

MPX MEMORY DATA INPUT PORT 0 INPUT PORT 1

(NORMALLY TO +5V) J1-29 DATA COMPLEMENT

MPX MEMORY DATA INPUT PORT 0 INPUT PORT 1

INTERRUPT INSTRUCTION PORT

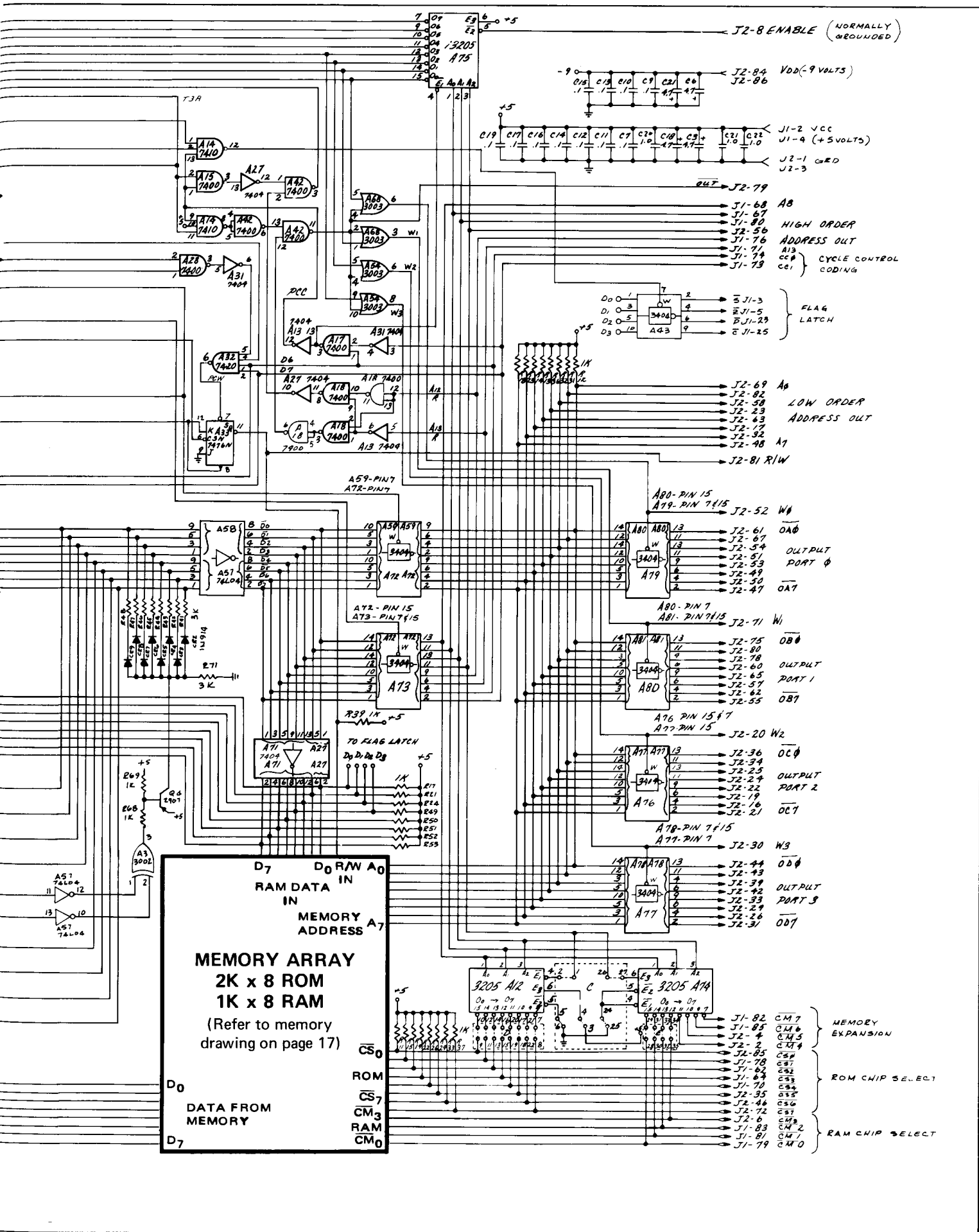


Figure 10. Complete SIM8-01 Schematic