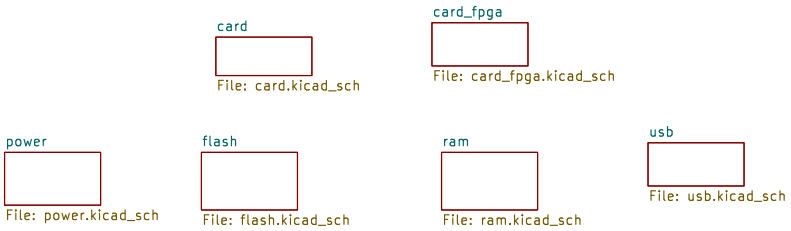
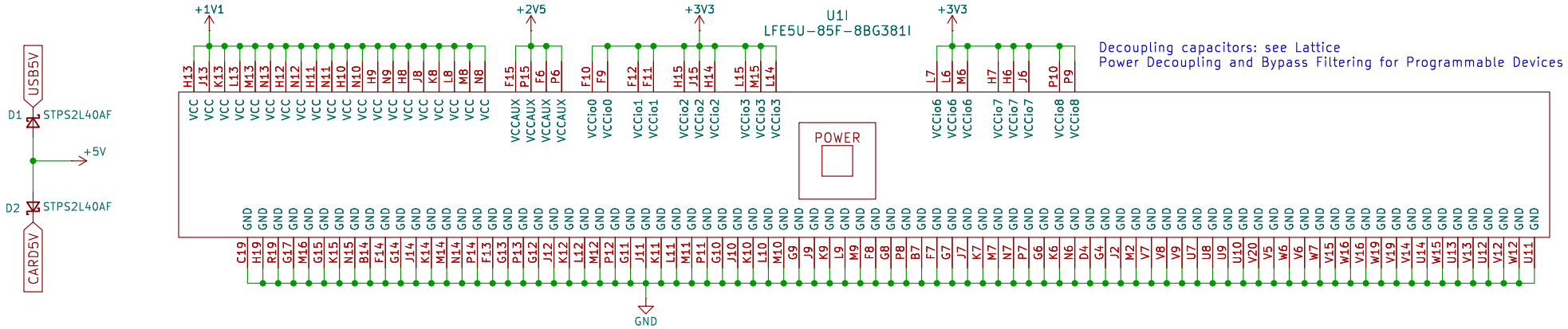
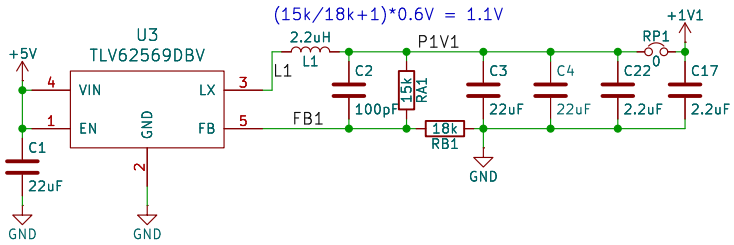


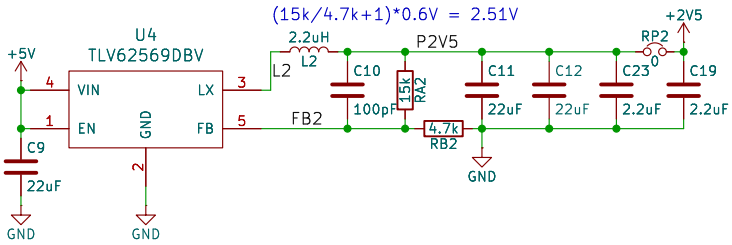
Sheet: /
File: project_byte_hamr.kicad_sch

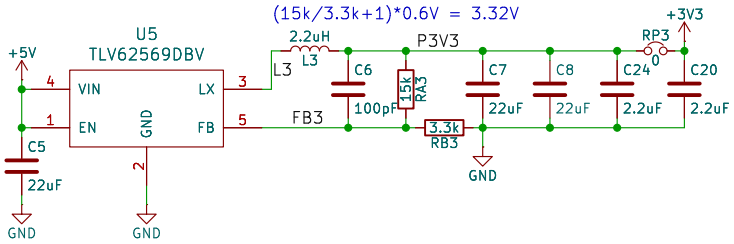
Title: Byte Hamr – Apple II FPGA Peripheral Card

Size: A4	Date: 2025-11-30	**Rev: 1.0.0**
KiCad E.D.A. 9.0.6		Id: 1/7





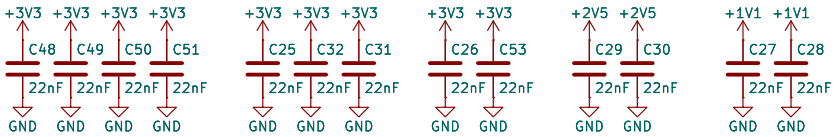




voltage setting: 0.6V at FB pin
Vout = (RA/RB+1)*0.6V

Switching regulators 2A SOT23-5
Texas instruments TLV62569DBV (2A) (best)
Dioo microcircuits DIO6015B (1.5A) (osc. acceptable)
Microsemi LX7172 (1.2A) (osc. unacceptable)
Diodes AP3429/A (2A) – (will damage board)

L1,L2,L3: Isat>3A Rdc<100mohm L=2.5-5.8mm W<3mm
Murata DFE322512F-2R2M=P2, DFE252012P-2R2M=P2
Bourns SRP2512A-2R2M



Capacitors near J1,2 connector

Power Dual 5V input (USB and Apple II card slot) through Schottky diode OR.
Three TLV62569 buck converters generating 1.1V (FPGA core), 2.5V (FPGA aux), and 3.3V (I/O). Decoupling capacitors for all FPGA power pins. Ferrite beads on each rail for noise filtering.

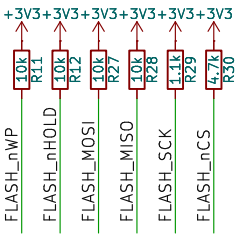
Sheet: /power/
File: power.kicad_sch

Title: Power Supply – 5V Input, 1.1V/2.5V/3.3V Rails

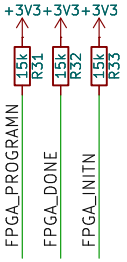
Size: A4	Date: 2025-11-30	**Rev: 1.0.0**
KiCad E.D.A. 9.0.6		Id: 2/7

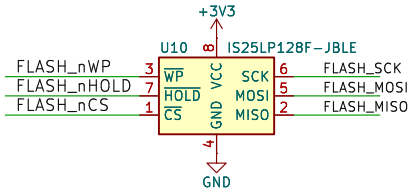
Deviation from TN1260 in pullup:
values for BOM simplification.
Correct values should be 1k
but 1.1k is used.

pullups for Master SPI (MSPI) required by
TN1260: lattice ECP5 sysCONFIG guide p.6

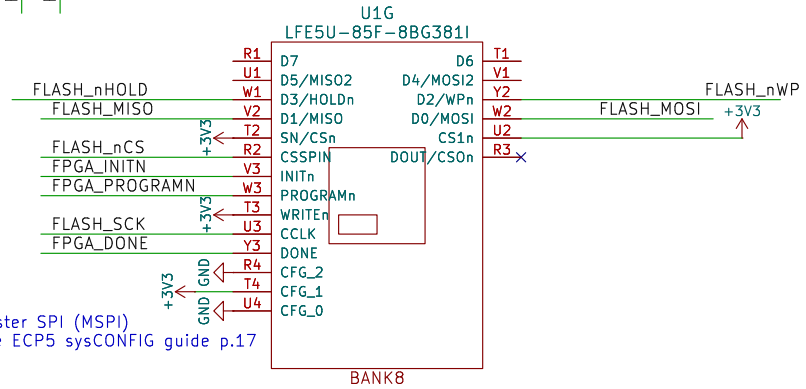


pullups to allow entering USER mode
TN1260: lattice ECP5 sysCONFIG guide p.6, p.8, p.13





For programming Flash thru JTAG see
Lattice FPGA-TN-02050



CFG select Master SPI (MSPI)
TN1260: lattice ECP5 sysCONFIG guide p.17

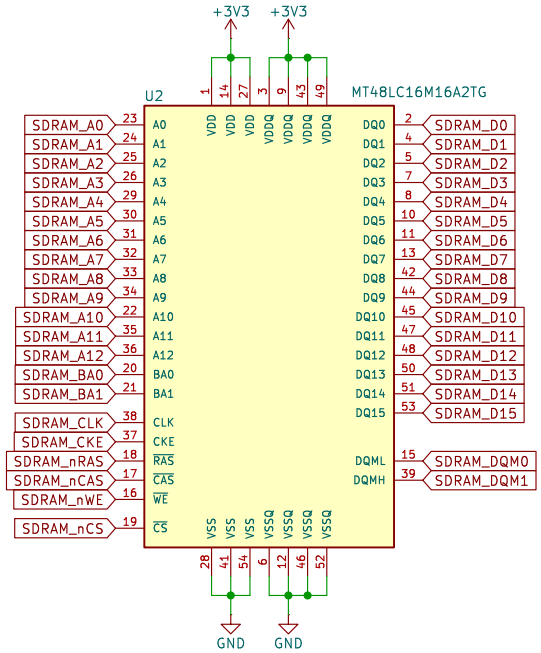
Some address lines for A[0:15] are better placed on this port.
Pins used are general I/O ports when not in use. See Section 4.1 ECP5 Datasheet

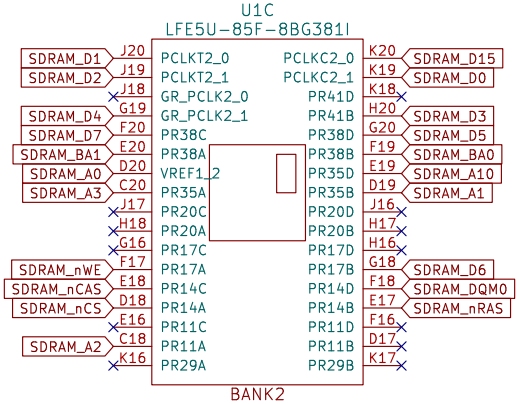
IS25LP128F SPI flash for FPGA bitstream storage. Directly connected to ECP5 configuration pins. Pullups on all SPI lines per Lattice guidelines. CFG pins set for Master SPI boot mode. PROGRAMN, DONE, and INITN signals for configuration control.

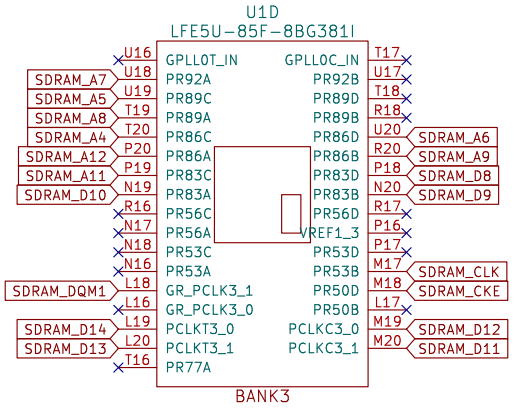
Sheet: /flash/
File: flash.kicad_sch

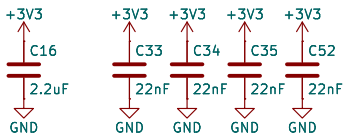
Title: FPGA Configuration – SPI Flash & Boot

Size: A4	Date: 2025-11-30	**Rev: 1.0.0**
KiCad E.D.A. 9.0.6		Id: 3/7







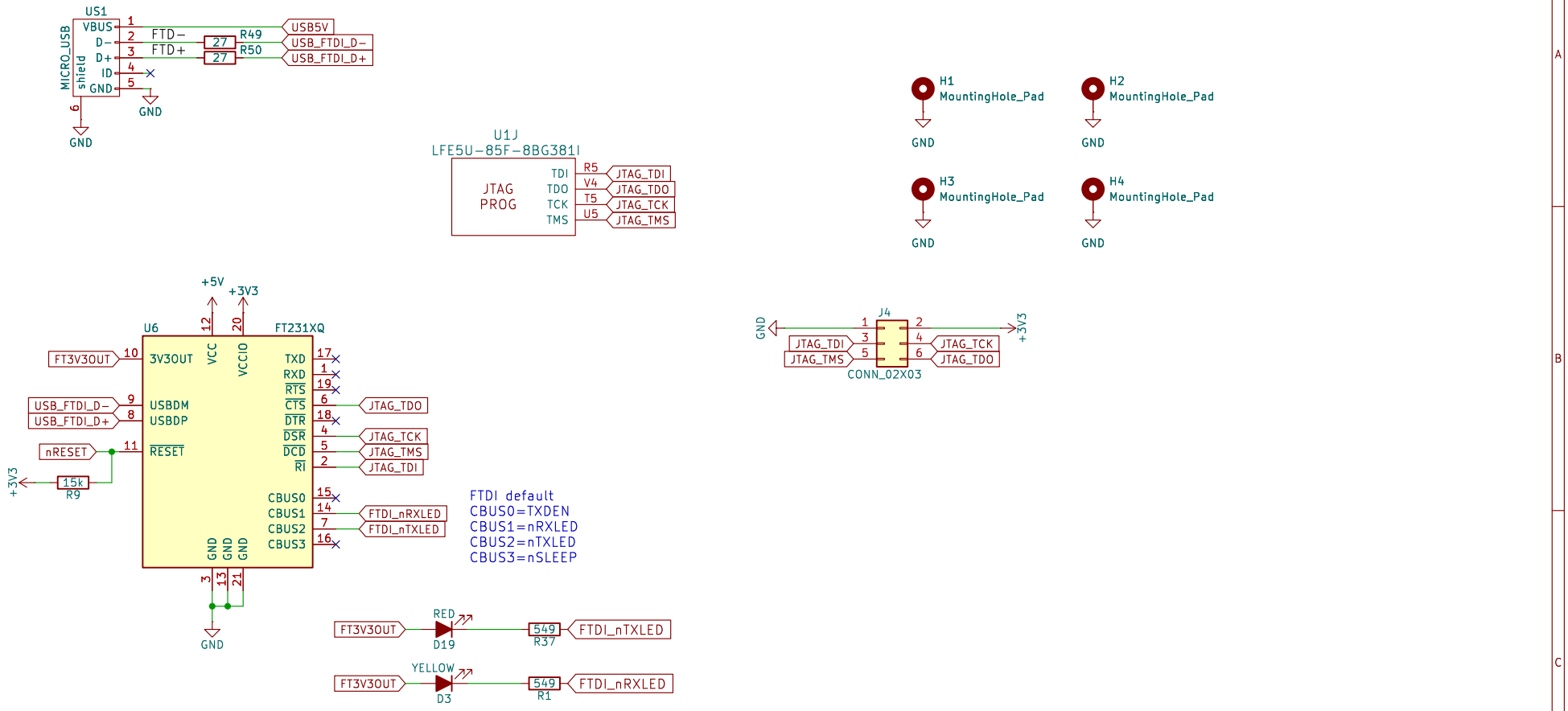


RAM MT48LC16M16A2TG SDRAM (16-bit, 32MB). Connected to FPGA banks 2 and 3. Full address bus (A0-A12), 16-bit data bus, bank select, and control signals (RAS, CAS, WE, CS, CKE, CLK, DQM). Decoupling capacitors for clean power.

Sheet: /ram/
File: ram.kicad_sch

Title: SDRAM - 32MB

Size: A4	Date: 2025-11-30	**Rev: 1.0.0**
KiCad E.D.A. 9.0.6		Id: 4/7

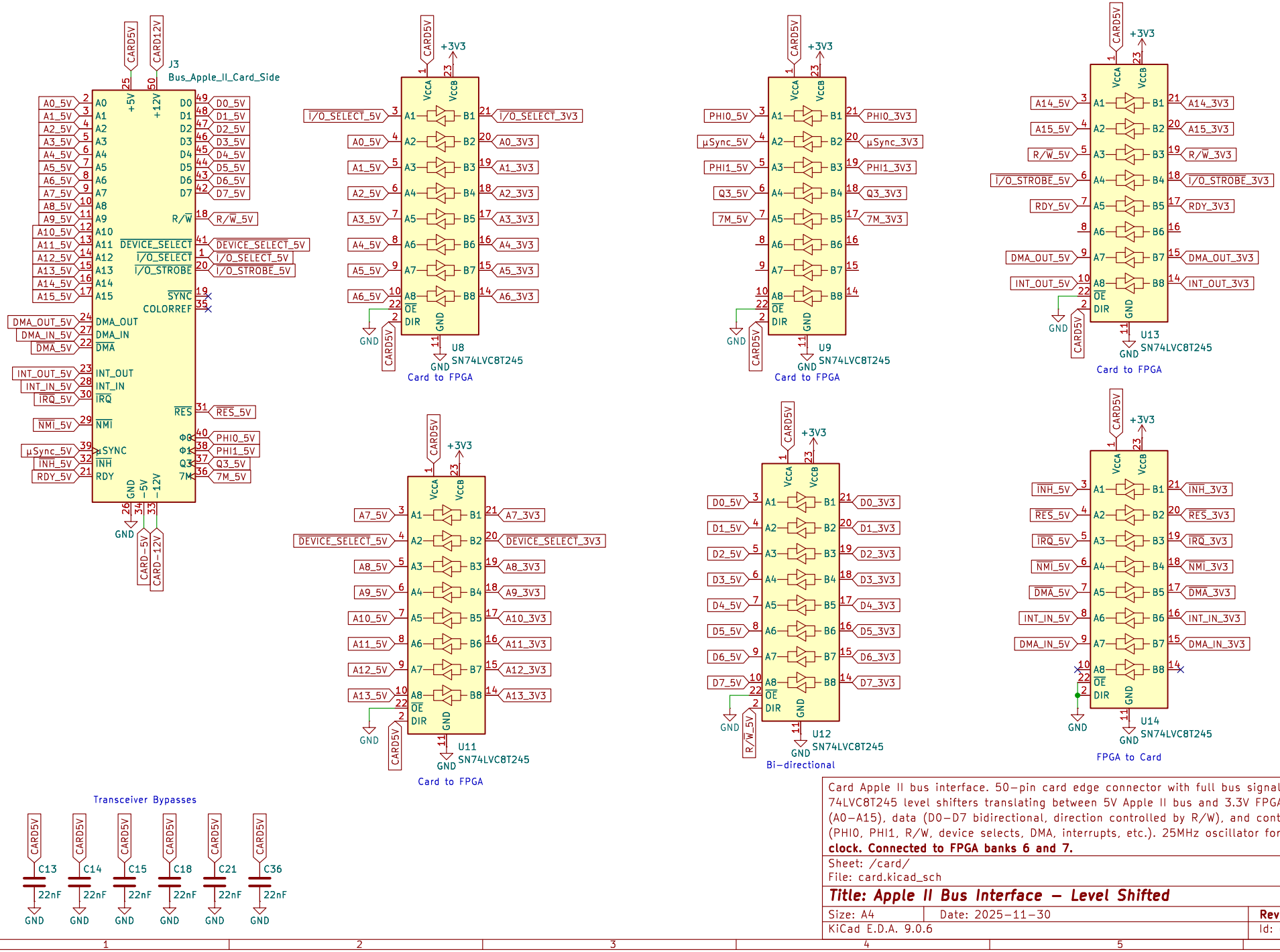


USB Micro−USB connector for power and programming. FT231XQ USB−to−serial chip with JTAG signals bit−banged over serial pins (CTS→TDO, DSR→TCK, DCD→TMS, RI→TDI). TX/RX activity LEDs. External 6−pin JTAG header as backup. 27Ω series resistors on USB data lines.

Sheet: /usb/
File: usb.kicad_sch

Title: USB Programming Interface − JTAG

Size: A4	Date: 2025−11−30	**Rev: 1.0.0**
KiCad E.D.A. 9.0.6		Id: 5/7

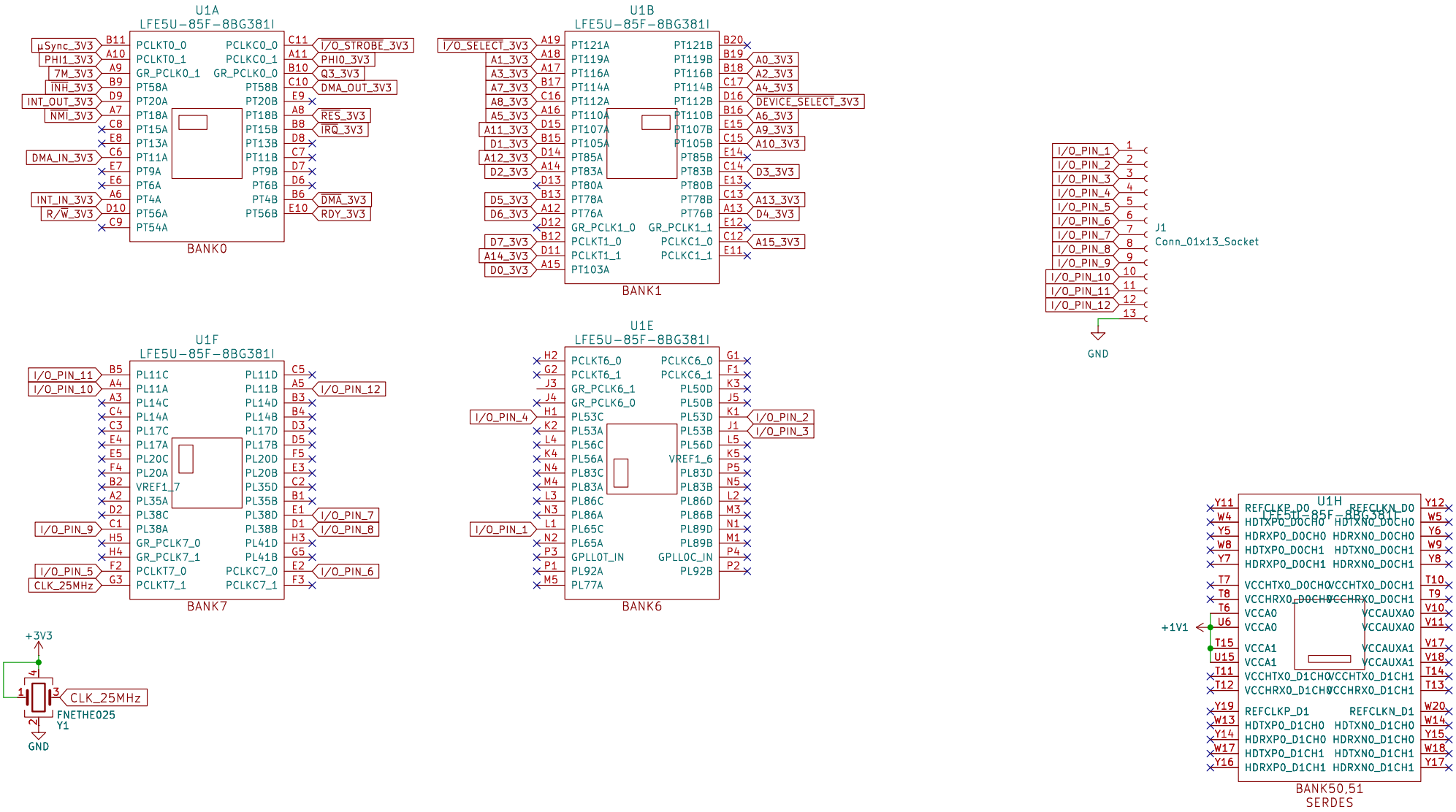


Card Apple II bus interface. 50-pin card edge connector with full bus signals. Six 74LVC8T245 level shifters translating between 5V Apple II bus and 3.3V FPGA. Address (A0-A15), data (D0-D7 bidirectional, direction controlled by R/W), and control signals (PHI0, PHI1, R/W, device selects, DMA, interrupts, etc.). 25MHz oscillator for FPGA system **clock. Connected to FPGA banks 6 and 7.**

Sheet: /card/
File: card.kicad_sch

Title: Apple II Bus Interface – Level Shifted

Size: A4	Date: 2025-11-30	**Rev: 1.0.0**
KiCad E.D.A. 9.0.6		Id: 6/7



Sheet: /card_fpga/		
File: card_fpga.kicad_sch		
Title: Byte Hamr – Apple II FPGA Peripheral Card		
Size: A4	Date: 2025-11-30	**Rev: 1.0.0**
KiCad E.D.A. 9.0.6		Id: 7/7