

# Project 1 Report

**Power Electronics: Modern Topics and Practice**

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# **Introduction**

In applications where power electronics is just a necessity, an engineer who can implement a controller into a simple design would be suitable to hire. However, as electric cars become more popular and grid systems require smarter electronics, the market demands more specialized power electronic engineers. These engineers need the intuition to be able to design high-efficient and reliable converters for multiple scenarios. Without being aware of concepts such as parasitics, load-step transients, and output voltage limits, products become unreliable and less competitive. It is imperative that students learn the fundamentals into good power converter design to prevent multiple design restarts as well. Thus, a product to show these concepts, while still acting as a functional PWM converter, was requested. This report will show that the product meets all the required features while also meeting extra, elective features.

# **Product Design**

## **Component Ratings**

The developed setup can operate as a buck, boost, or a buck-boost converter. The components are common between all three configurations, where changing from one configuration to another is performed by a four pole three throw (4P3T) switch. The EG4319A was selected as the 4P3T switch, where its pin map is illustrated in Figure 1. The power stage of this setup is made by a canonical cell that is shown in Figure 2. The canonical cell

is made by two MOSFETs and an inductor, where the labeled ports  $C_1$ ,  $C_2$ , and  $C_3$  are connected to the load ( $R+$ ), power supply ( $B+$  and  $B-$ ), and ground according to Table 1. In addition to the labeled power stage ports, there are three signal ports the microcontroller's GPIOs read to determine the current configuration. If the assigned GPIO status is high, the converter works in that configuration. Otherwise, that mode of operation is not selected.

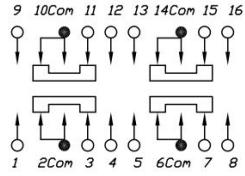


Figure 1: 4P3T Switch Pin Map

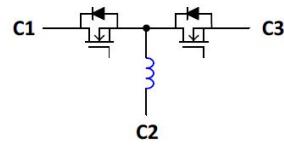


Figure 2: Canonical Cell Topology

Table 1: Power stage configuration for buck, boost, and buck-boost modes

Terminals	Buck	Boost	Buck-Boost
$B+$ connected to 2	C1 and 1 short circuit	C2 and 3 short circuit	C1 and 4 short circuit
$B-$ connected to 6	C3 and 5 short circuit	C3 and 7 short circuit	C2 and 8 short circuit
$R+$ connected to 10	C2 and 9 short circuit	C1 and 11 short circuit	C2 and 12 short circuit
$+3.3V$ connected to 14	GPIO $x=+3.3V$	GPIO $y=3.3V$	GPIO $z=+3.3V$

The selected nominal values for input voltage, output voltage, and switching frequency for operating in boost and buck-boost are provided in Table 2. The component voltage and current stresses can be considered only for the boost and buck-boost modes, since in the buck topology the inductor voltage never exceeds the input voltage unlike the other modes. Therefore, the following calculations for switch stresses only consider the boost and buck-boost configurations. The exact values for the power inductor and capac-

itor are not standard values in the market, thus a greater standard value was selected for these components.

Table 2: Nominal and Maximum Operating Condition Values

Parameter	Value
Nominal input voltage ( $V_{in}$ )	15 V
Maximum output voltage ( $V_{out}$ )	40 V
Switching frequency ( $f_s$ )	200 kHz
Maximum load (R)	270 Ω
Maximum output power ( $P_{out}$ )	6 W

$$I_{ave,ind} = \frac{P}{V_{out}(1 - D)} \quad (1)$$

According to (1), the maximum  $I_{L-avg}$  in the boost and buck-boost configurations are 400 mA and 550 mA, respectively.

$$L = \frac{DV_{in}}{f_s \Delta i} \quad (2)$$

According to (2), in buck-boost mode for limiting the inductor current ripple to 20%, the inductor value should be 496 μH. The 680μH SRR1260A-681K inductor was chosen, with a saturation current rating of 750 mA and a self-resonance frequency at 2 MHz.

$$C = \frac{DV_{in}}{f_s \Delta V_{out}} \quad (3)$$

According to (3) for limiting the output voltage ripple to 2%, the capacitor should be more than 675 nF. The output capacitor is made up of four 50 nF, 100 V rated ceramic capacitors and a 1 μF 60 electrolytic capacitor in parallel. This was to ensure that the output voltage ripple will be limited to less than 1%.

The peak current stress happens at buck-boost mode where the peak current is equal

to inductors peak current with less than 20% ripple. Considering the boundary conduction mode at lower than nominal switching frequency, the peak current stress on the MOSFETs is 1.1 A. The peak voltage stress in buck-boost mode can be calculated by (4), where it is equal to 56.5 V at nominal input voltage. In the case of maximum input voltage, i.e.  $V_{in} = 20V$ , the peak voltage stress is 66.5V. The n-channel power MOSFET with CSD19538Q3A part number was chosen with  $V_{ds,max} = 100V$  and  $I_D = 14A$ , so that it will tolerate the peak current and voltage stresses.

$$V_{peak} = V_{in} + V_{out} + \frac{\Delta V_{out}}{2} \quad (4)$$

## Schematic and Layout Design

### Developed Setup

The developed setup and controller are shown in Figure 3. The setup is designed with a four layer PCB layout and has been connected to the Texas Instruments LAUNCHXL-F280049C evaluation board through two pairs of 2-row, 20 position, 2.54 mm head ribbon cables.

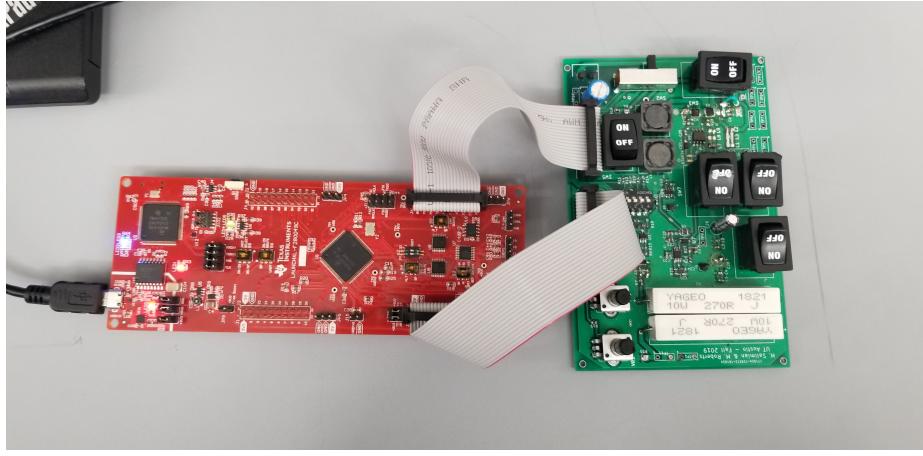


Figure 3: Developed Converter with F280049C Controller

## Power Stage

As described in the previous section, the power stage is made up of the input power port, canonical cell, resistive load, and the 4P3T switch. The input power is received from an external 0-25 V DC power supply that is connected to the two port phoenix connector J1 shown in Figure 4. A 60 V electrolytic capacitor is placed in parallel with J1 to make the input voltage constant with negligible ripple. Multiple test pins (TP) are placed at different locations to sense voltage across the signal. For example, TP10 shows the test pin for input voltage.

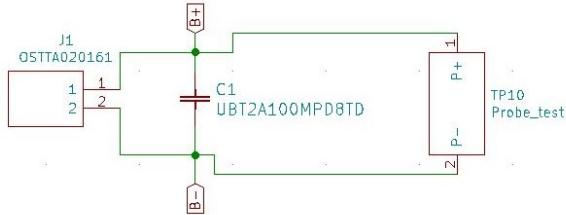


Figure 4: Converter Input Power Stage

The canonical cell is shown in Figure 5. In layout design, MOSFETs are placed close to each other to minimize the switching loop inductance. The capacitors  $C_6$  and  $C_7$  are in parallel to reduce the inductance by making the switching loop conduction path wider. These capacitors are connected to top MOSFET in the top layer and the switching loop is closed via the second layer to the bottom MOSFET. These capacitors need to be able to tolerate 65 volts. A few X7S, 100V rated, 10 nF ceramic capacitors were chosen, both to meet the voltage rating and be within a reasonable tolerance value. In order to show effect of the switching loop inductance on switch node voltage, three extra inductors are added to the circuit through  $L_1$ ,  $L_2$ , and  $L_3$ . Based on LTspice simulation results, The effect of gate inductance can be observed with a  $4.7 \mu\text{H}$  inductor. By closing the SW3 rocker switch, these inductances will be bypassed and clean waveforms can be seen. Opening SW3 should show ringing on the switch node voltage.

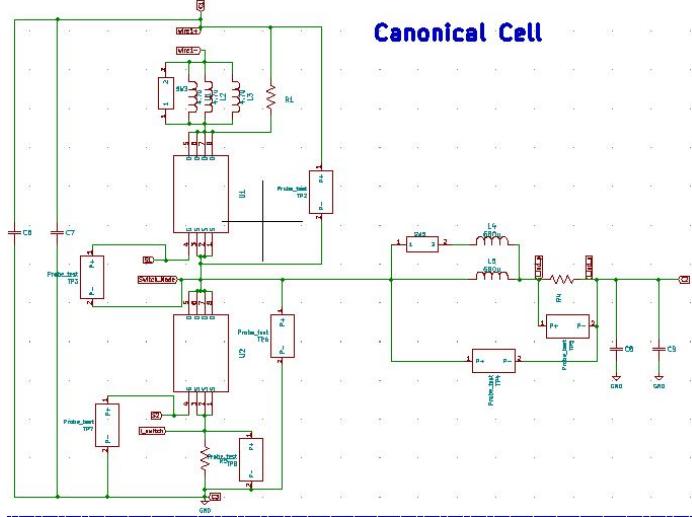


Figure 5: Canonical Cell Schematic

As mentioned in previous section, a  $680 \mu\text{H}$  inductor is selected for the canonical cell. However, for showing the effect of changing inductor value on current ripple and entering to

the discontinuous conduction mode (DCM) at a higher frequency,  $L_4$  and SW5 are added to canonical cell in parallel with  $L_4$ . In normal operation, SW5 is open and only  $L_5$ , a 680  $\mu\text{H}$  inductor, is in the current path. By closing SW5,  $L_4$  and  $L_5$  are in parallel and the inductance of canonical cell results in 340  $\mu\text{H}$ .

For observing the current in inductor and bottom MOSFET,  $R_4$  and  $R_5$  shunt resistors are added in their current path. These resistances should be selected large enough to show the current waveform clearly, while also minimizing its effect on the circuit from its voltage drop. Therefore, 240 m $\Omega$  resistors with 1% error were used for limiting the voltage drop to 200 mV at the peak current and observing a clear waveform on the probe. The top MOSFET current can be observed by a Hall Effect current probe that measures the current between the positive wire and the negative wire ports.

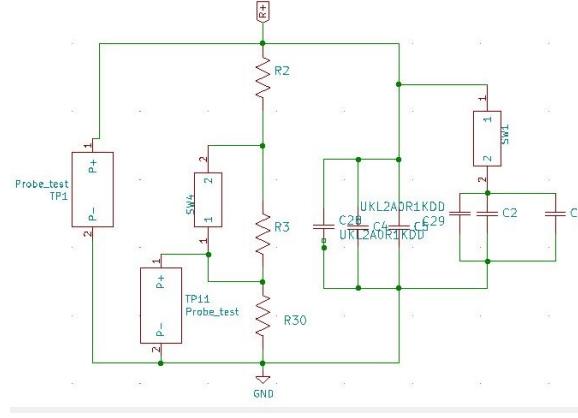


Figure 6: Load and Capacitive Filter

The load is shown in Figure 6, where the resistor and capacitive filter are connected in parallel. By closing SW4, the load results in the nominal 270  $\Omega$  resistor. Opening SW5 results in  $R_2$  and  $R_3$  being in series, creating a 540  $\Omega$  load.  $R_{30}$  is a 240 m $\Omega$  shunt

resistor that measures the output current. SW1 is the rocker switch that changes the output capacitor filter value. If SW1 is closed, the equivalent capacitance is  $1.2 \mu\text{F}$ . If SW1 is open, the equivalent capacitance is  $100 \text{ nF}$ .

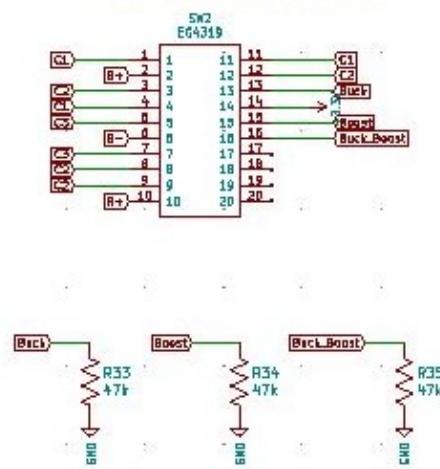


Figure 7: 4P3T Switch and Mode Read Pins

The 4P3T switch is illustrated in Figure 7. Buck, boost, and buck-boost pins are connected to GPIO pins 6, 7, and 2, respectively. At any moment, only one of these pins can be connected to 3.3V, or high, while two other pins remain disconnected. In order to connect these pins to ground and avoid floating pin, pull down resistors  $R_{33}$ ,  $R_{34}$ , and  $R_{35}$  are placed between these pins and signal ground. The pull down resistors were chosen to be  $47 \text{ k}\Omega$ , so that the current drawn from 3.3V pin would be at most  $330 \mu\text{A}$ .

## Gate driver

For turning on the MOSFET, the gate to source voltage should be higher than 6 V. Therefore, based on provided information in the data sheet and for having a low on-resistance, the gate source voltage is selected as 12 V. For generating this voltage, a

small boost is designed to convert the controllers 5 V to 12 V as shown in Figure 8. The TPS61085TDGKR is the boost controller IC that performs the voltage conversion at 650 kHz or 1.2 MHz switching frequency. By connecting pin 7 to 5 V, the 1.2 MHz switching frequency is selected. Using a  $4.7 \mu\text{H}$  inductor as  $L_6$ , the inductor current ripple is limited to less than 10%, while the output voltage ripple is limited to 1% by using a  $20 \mu\text{F}$  capacitive filter. The output voltage value is sensed by resistive divider formed by  $R_{26}$  and  $R_{27}$  equal to  $18 \text{ k}\Omega$  and  $158 \text{ k}\Omega$ , respectively.

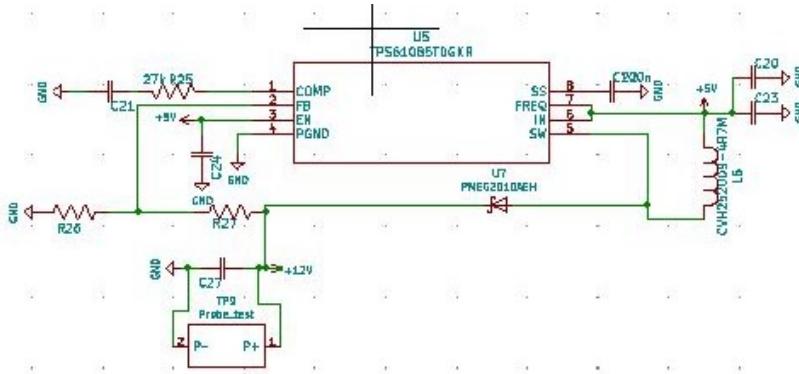


Figure 8: 5 V to 12 V Boost Converter

The high side MOSFETs source is connected to the switching node. Hence, the gate driver for high side and low side should have different ground. In order to avoid using an isolated gate driver, which increases the complexity and price of the setup, a LM5109BMA half-bridge gate driver was chosen as shown in Figure 9. This half-bridge is a non-isolated bootstrap gate driver that provides level-shifted voltage for the high side MOSFETs gate while also allowing variable dead time control between high and low MOSFETs as well as asynchronous rectification. The maximum voltage rating of top MOSFET gate driver is 90 V compared to the peak 66.5 V in buck-boost configuration. The gate signal path contains zero ohm resistors so that clean gate to source signals can be observed while allowing for

adding gate resistance through the path.  $R_{28}$  and  $R_{29}$  are created to show the effect of gate resistance on ringing or on the gate and MOSFET turn-on time. Moreover, an extra inductor can be added the path of top MOSFET gate by turning off the rocker switch SW7. During the period that this switch is on, there is no extra inductance in the path and the gate to source voltage should be cleaner. Based on simulation results, after inserting 100 nH in the gate path by turning off SW7, the gate to source voltage will have ringing during turn-on or turn-off period with about 50% overshoot.

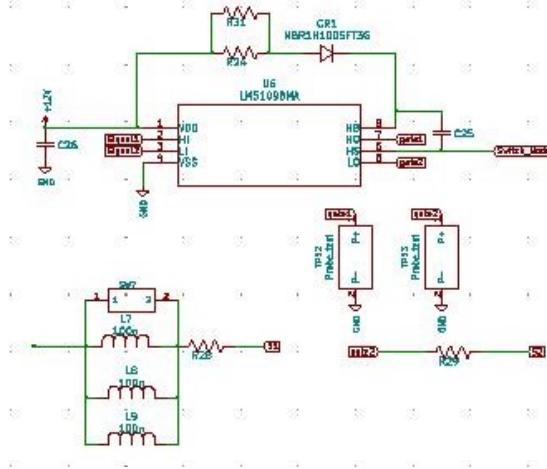


Figure 9: Half-Bridge Bootstrap Gate Driver

## Voltage and Current Sensing

In this design, the ADC receives the input voltage, output voltage, and inductor current at ADCINA0, ADCINC3, and ADCINC5, respectively. The measured signals can vary from 0 to 3.3 V. These signals are being used for output voltage limiting and buck closed loop control. The op-amps that are used for input voltage and inductor current measurements are the OP325 with 10 MHz bandwidth, requiring a 5 V supply voltage. In all three measurements, a low pass RC filter is placed before the ADC that removes the

high frequency noise from the signal. The ADC filter R is set to  $100\ \Omega$  and the ADC filter C is set to  $1\ nF$ , resulting in a cutoff frequency of  $1.59\ MHz$ . The  $3.3\ V$  Zener diode is placed for ADC protection so that the ADC voltage does not exceed  $3.3\ V$ .

Since the input voltage is not connected to the ground in the buck-boost configuration and its negative voltage can potentially be  $40\ V$ , a resistive divider cannot be used. For measuring the input voltage, a differential amplifier was selected as shown in Figure 10. Based on (5), for  $25V$  input voltage and  $R_6 = R_{23} = 4.7k\Omega$  and  $R_{15} = R_{18} = 56k\Omega$ , the voltage at ADCINA0 will be  $2.09\ V$ , resulting in less than the maximum ADC voltage rating.

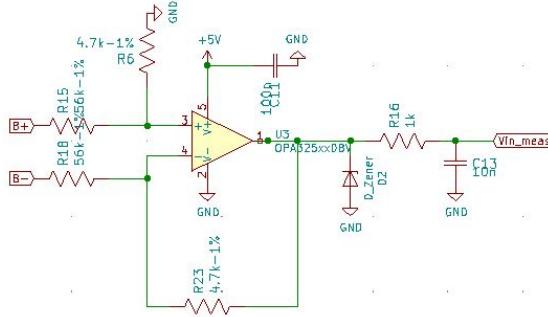


Figure 10: Input Voltage Sensing Circuit

$$V_{sense,input} = \frac{R_6}{R_{15}}(V_{B+} - V_{B-}) \quad (5)$$

One side of the load is always connected to the ground, therefore, a simple resistive divider has been used as shown in Figure 11. According to (6), the measured voltage at ADCINC3 is for maximum  $40\ V$  output voltage is  $2.69\ V$  for  $R_9 = 4.7k\Omega$  and  $R_7 = R_8 = 33k\Omega$ . However, the effect of load is not considered in this equation and measured voltage might be higher than this value.

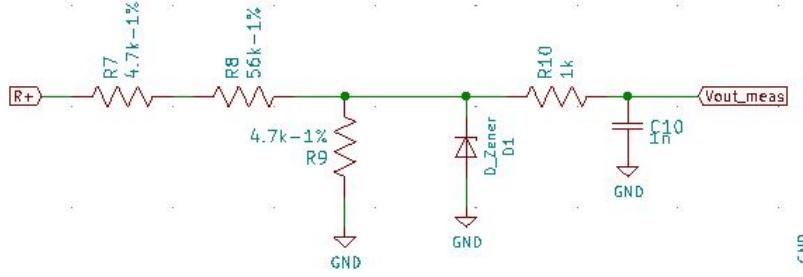


Figure 11: Output Voltage Sensing Circuit

$$V_{sense,output} = \frac{R_9}{R_7 + R_8 + R_9} V_{out} \quad (6)$$

The inductor current measurement is performed by LMP8640HVMK low/high side, high speed, voltage output current sensing amplifier with 20 V/V gain. The inductor current passes through a  $200\text{ m}\Omega$  1% resistor and the output voltage of the current sensing amplifier will be according to (7). The current measurement circuit is shown in Figure 12.

$$V_{sense,inductor-current} = gR_{32}I_{ind} \quad (7)$$

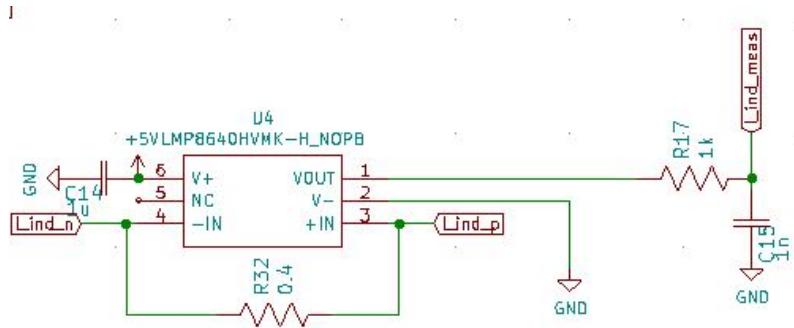


Figure 12: Inductor Current Sensing Circuit

## Operation Mode Selection

For enabling the customer to control the operating mode of the converter, a 4 position DIP switch has been used. The configuration of DIP switch and connection is shown in Figure 13. At the input side, the DIP switch is connected to 3.3 V and the output ports are Preset, OL-CL, Sync-Async, and Shutdown that are connected to GPIO14, GPIO15, GPIO26, and GPIO03, respectively. If one of the DIP switches is on, 3.3 V will be sensed by associated GPIO, otherwise it will be pulled down to ground by  $R_{11}$ ,  $R_{12}$ ,  $R_{13}$ , or  $R_{14}$  as shown in Figure 12.

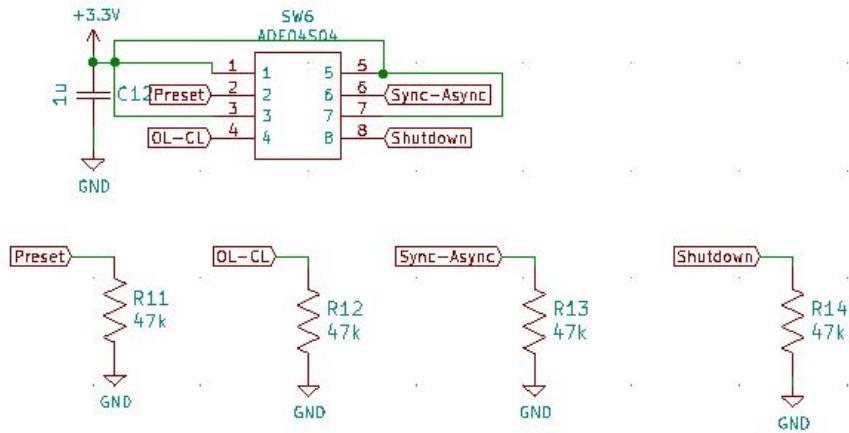


Figure 13: Operation Mode Selection with 4 DIP Switches

By turning on the Preset mode, the converter works with 200 kHz switching frequency and 50% duty cycle, regardless of converter configuration. However, if the output voltage is higher than 40 V, the duty cycle will be limited to make sure that output voltage does not go higher than 40 V in boost and buck-boost operation.

If the Preset mode is off and OL-CL switch is on, the converter will work as a buck

converter in closed-loop mode with 12 V output. The Sync-Async switch selects whether the converter is working in diode rectification or synchronous rectification mode. If the Sync-Async mode is on, the converter works in asynchronous rectification and the bottom MOSFET operates as a diode. Otherwise, it works in the synchronous rectification mode. By turning on the Shutdown switch, both MOSFETs receive off command on their gates and the converter does not operate.

By turning off Preset and Shutdown switches, the frequency and duty cycle will be commanded by Freq-Knob and Duty-Cycle-Knob. The configuration of Freq-Knob and Duty-Knob is shown in Figure 14. The knobs are both 10 k $\Omega$  potentiometers that are connected in series with a 47 k $\Omega$  resistor. The knob's output voltage are sent to ADCINB6 and ADCINC14. RC filters are connected after the knobs to limit high frequency noise on ADCs.

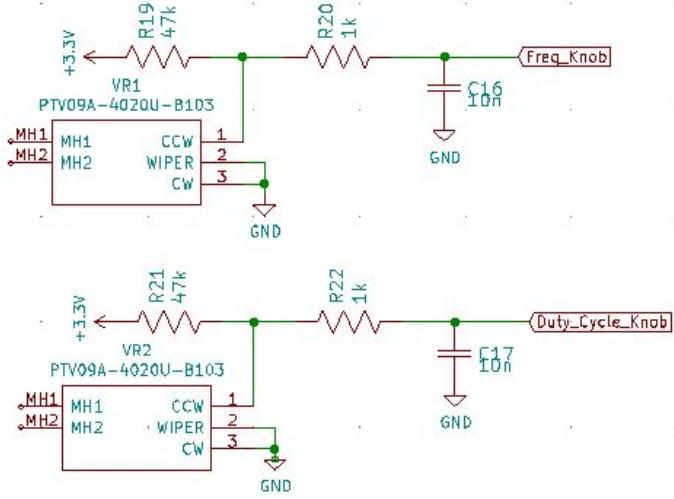


Figure 14: Frequency Knob and Duty Cycle Knob Selector

# Results

## Required Features

### 4P3T Demonstration

The first required feature of the converter is that the converter must show working operation in each mode, preferably through the use of the 4P3T switch configuration described in the Component Ratings section. The results below in Figures 15, 16, and 17 show the input voltage on Channel 1 and the output voltage on Channel 2. These waveforms were taken while the converter was operating in asynchronous rectification, with a duty cycle of 50% and at a switching frequency of 100 kHz.

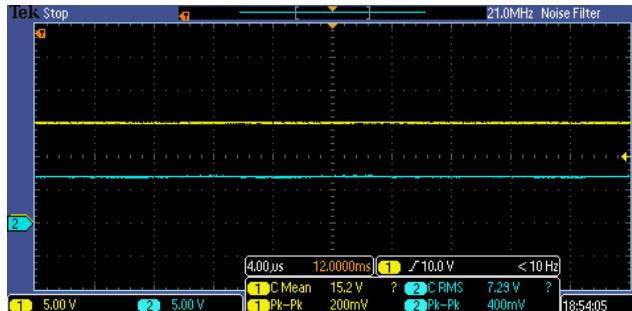
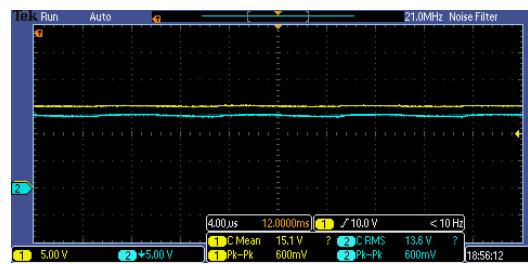
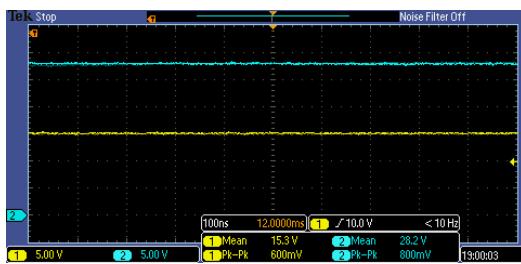


Figure 15: Input and Output Voltages in Buck Mode



## Sensing Power Stage Wave forms with Ripples

The second required feature is that the converter should have its inductor current and capacitor voltages be measurable. This also includes that the inductor current and capacitor voltage ripples be verifiable with the ripples chosen in the design. The measurements were taken when the converter was operating at 50% duty cycle and at a switching frequency of 100 kHz, with the exception of the buck mode measurements being 200 kHz. It also should be noted that the converter was in asynchronous mode and that the power inductance was set at the minimum inductance,  $340 \mu\text{H}$ , so as to see larger ripples. Figures 18, 19, and 20 show the inductor current in the various modes. Figures 21, 22, and 23 show the capacitor voltage in the various modes.

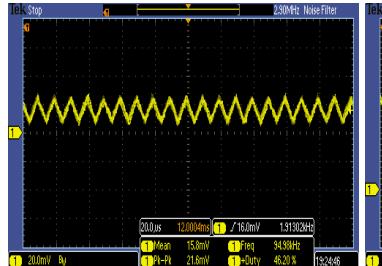


Figure 18: Inductor Current in Buck Mode

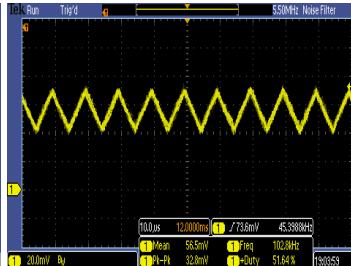


Figure 19: Inductor Current in Boost Mode

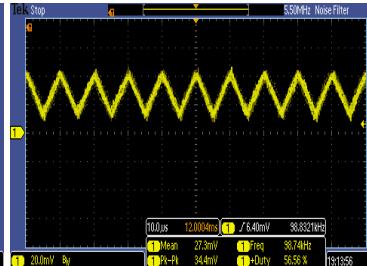


Figure 20: Inductor Current in Buck-Boost Mode

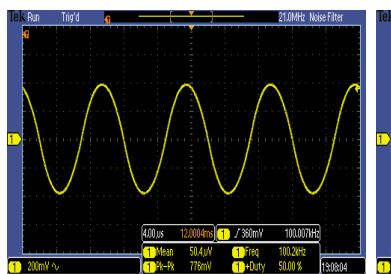


Figure 21: Capacitor Voltage in Buck Mode

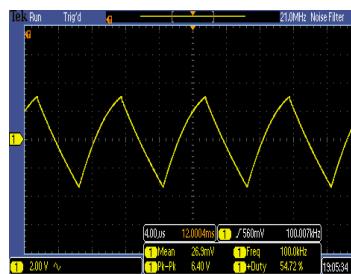


Figure 22: Capacitor Voltage in Boost Mode

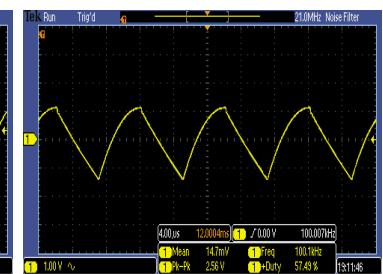


Figure 23: Capacitor Voltage in Buck-Boost Mode

## Gate-Source and Drain-Source Voltage Sensing

The third required feature is that the converter should have at least one of its device's gate-source and drain-source voltages be measurable. Figures 24, 25, and 26 show the gate-source voltage (Channel 1) and the drain-source (Channel 2) of the high side MOSFET in the various modes. The measurements were taken when the converter was operating at a switching frequency of 100 kHz and a duty cycle of 50% while in asynchronous mode.

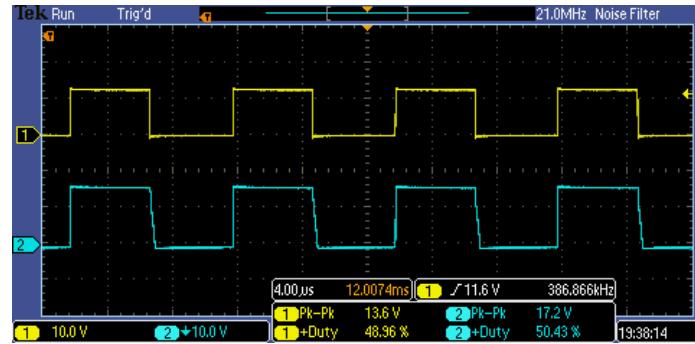


Figure 24: Gate-Source and Switch Node Voltages in Buck Mode

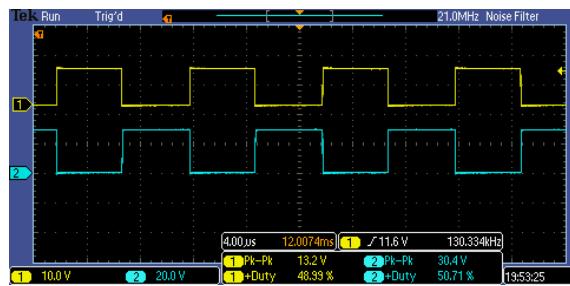


Figure 25: Gate-Source and Switch Node Voltages in Boost Mode

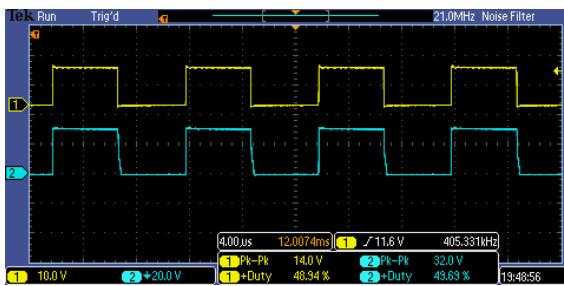


Figure 26: Gate-Source and Switch Node Voltages in Buck-Boost Mode

## Effect of Variable Inductance and Capacitance

The fourth required feature is that one can show the effects of changing the power inductor and capacitor values in the converter. Figures 27 and 28 show the inductor current of two separate inductances,  $680\mu\text{H}$  and  $340 \mu\text{H}$ . Figures 29 and 30 show the capacitor voltage of two separate capacitances. As mentioned previously in Power Stage, rocker switches were implemented to the allow the changing between the inductance and capacitance values in the canonical cell and load. The measurements were taken under the same circumstances as before; When the converter was operating in asynchronous mode at a switching frequency of 100 kHz and a duty cycle of 50%.

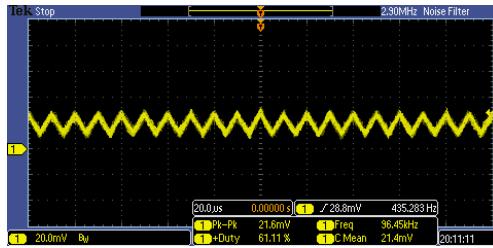


Figure 27:  $680\mu\text{H}$  Inductor Current in Buck

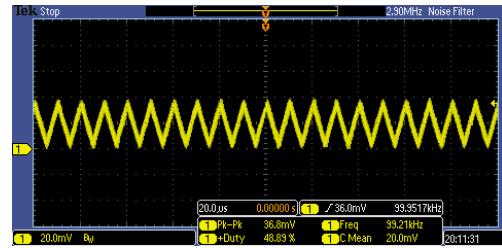


Figure 28:  $340\mu\text{H}$  Inductor Current in Buck

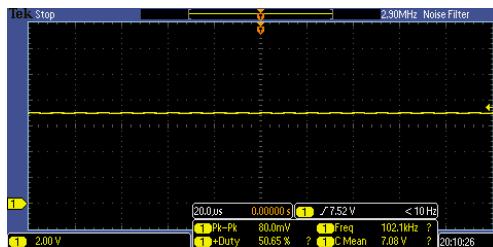


Figure 29:  $100\text{nF}$  Capacitor Voltage in Buck

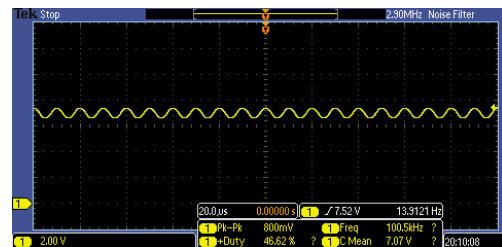


Figure 30:  $1.2\mu\text{F}$  Capacitor Voltage in Buck

## Diode Operation and Synchronous Rectification

The fifth required feature is that the converter can demonstrate both asynchronous and synchronous rectification. The results should show a difference between efficiencies between the two modes across various deadbands. For all figures in this section, Channel 1 represents the diode or switch voltage, while Channel 2 represents the diode or switch current. Figures 31, 32, 33, and 34 show both of the device's voltage and current waveforms in the asynchronous mode. 35 and 36 represent the 80 ns deadband, high side switch voltage and current, while 37 and 38 show the 170 ns deadband, low side switch voltage and current. The converter was operating in boost mode at a switching frequency of 200 kHz and a duty cycle of 50% for all the below figures. Since the switch is rated for 14 A and the current going through the switch is around 200 mA, there is hardly a noticeable change for turn-on times between asynchronous and synchronous modes. The effect of efficiency for conduction loss is difficult to notice with the results below:

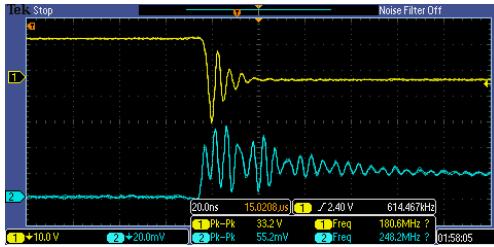


Figure 31: Diode Voltage and Current during Turn-On

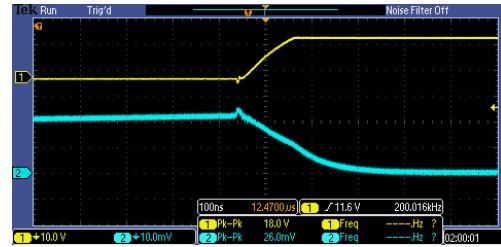


Figure 32: Diode Voltage and Current during Turn-Off

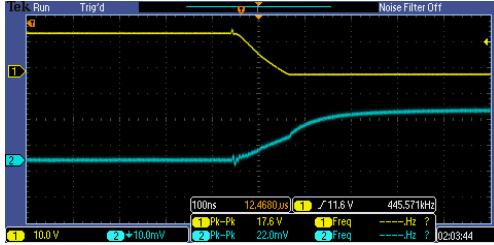


Figure 33: Asynchronous Low-Side Switch Voltage and Current during Turn-On

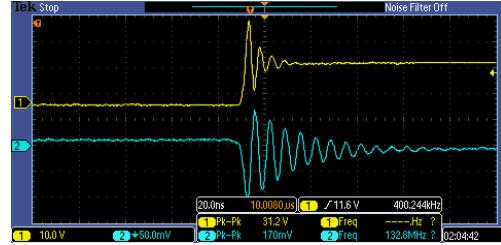


Figure 34: Asynchronous Low-Side Switch Voltage and Current during Turn-Off

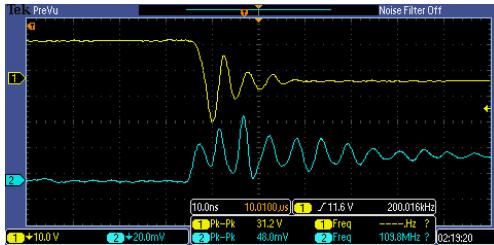


Figure 35: Synchronous High-Side Switch Voltage and Current during Turn-On, 80ns of Deadband

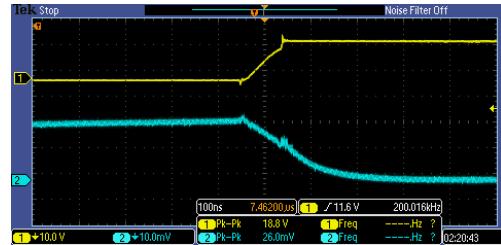


Figure 36: Synchronous High-Side Switch Voltage and Current during Turn-Off, 80ns of Deadband

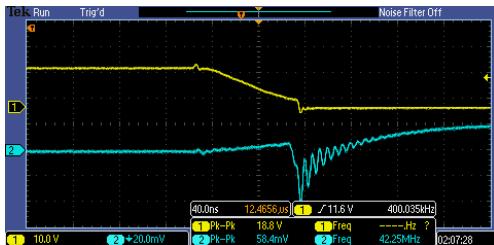


Figure 37: Synchronous Low-Side Switch Voltage and Current during Turn On, 170ns of Deadband

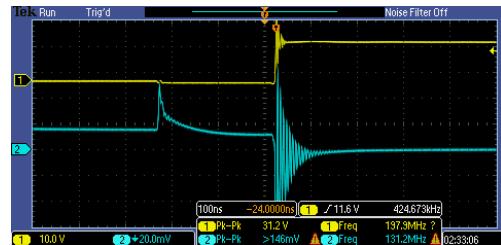


Figure 38: Synchronous Low-Side Switch Voltage and Current during Turn-Off, 170ns of Deadband

## Effect of Adding Inductance to Gate-Source Loop

The sixth required feature is that the converter can demonstrate both asynchronous and synchronous rectification. The results should show a difference between efficiencies between the two modes across various deadbands. For all figures in this section, Channel 1 represents the diode or switch voltage, while Channel 2 represents the diode or switch current. Figures 31, 32, 33, and 34 show both of the device's voltage and current waveforms in the asynchronous mode. 35 and 36 represent the 80 ns deadband, high side switch voltage and current, while 37 and 38 show the 170 ns deadband, low side switch voltage and current. The converter was operating in boost mode at a switching frequency of 200 kHz and a duty cycle of 50% for all the below figures.

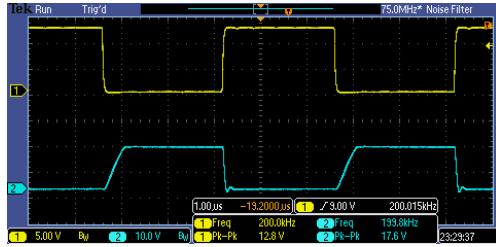


Figure 39: High-Side Gate-Source and Drain-Source Voltages

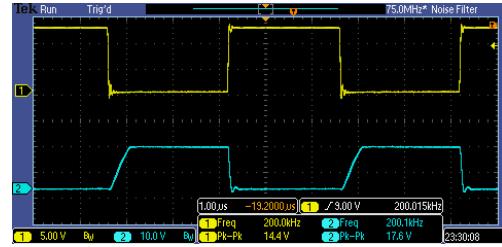


Figure 40: High-Side Gate-Source and Drain-Source Voltages, with added Gate Inductance

## Switching Loss

The seventh required feature is to demonstrate the presence of switching loss through a device's voltage and current. Using the figures posted above, there is a clear overlap between voltage and current in every waveform. This overlap where both the switch current

and voltage are greater than zero results in power being lost in the form of switching loss. Figure 32 shows a good example of switching loss in the diode while Figure 36 shows a suitable example of switching loss in an active switch.

## Diode Reverse Recovery

The eighth required feature is to demonstrate the presence of diode reverse recovery through a diode's voltage. Figure 31 shows a dip in the diode voltage far below 0 V along with some additional ringing. This action is attributed to immediately changing the diode's bias, resulting in a large amount of free carriers that need to be extinguished. During this time that the electrons return to the n-region and the holes return to the p-region, the diode's bias changes very quickly, allowing voltage to swing both to positive and negative amounts. These non-zero amounts of voltage result in additional switching losses. This effect of reverse recovery will be more noticeable in during Valley Switching.

## Varying Switching Frequency

The ninth required feature is to demonstrate the effects of varying switching frequency. As the frequency increases, the inductor and capacitor ripples should decrease. These can be shown in Figure 41 having the largest peak to peak voltage and current, while Figure 43 shows having the smallest peak to peak voltage and current. Channel 1 represents the capacitor voltage while Channel 2 represents the inductor current, both AC coupled. The converter operated in asynchronous mode, at an input voltage of 20 V in the buck mode.

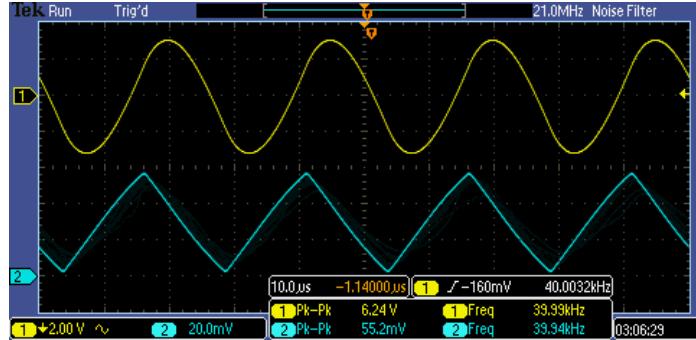


Figure 41: Inductor Current and Capacitor Voltage Ripples at 50 kHz

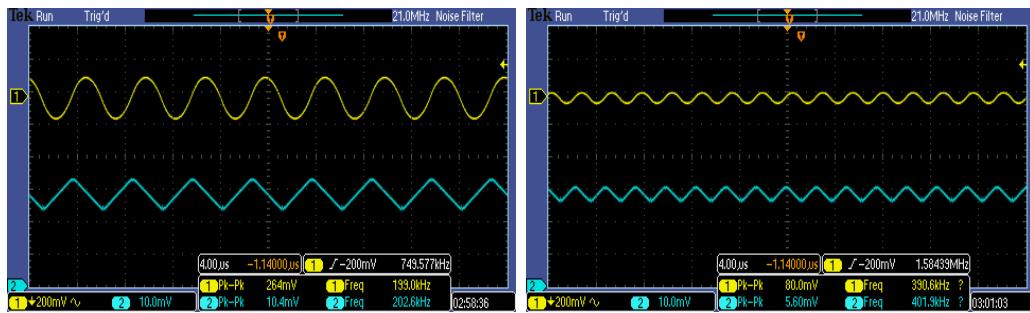


Figure 42: Inductor Current and Capacitor Voltage Ripples at 200 kHz

Figure 43: Inductor Current and Capacitor Voltage Ripples at 400 kHz

## CCM, DCM, BCM, and Valley Switching

The tenth required feature is to demonstrate various conduction modes. This includes Continuous Conduction Mode (CCM), Discontinuous Conduction Mode (DCM), Boundary Conduction Mode (BCM), and valley switching. In Figures 44, 47, and 49, Channel 1 represents the high side switch voltage and Channel 2 represents the high side switch current. In Figure 46, Channel 1 represents the output voltage, while Channel 2 represents the inductor current.

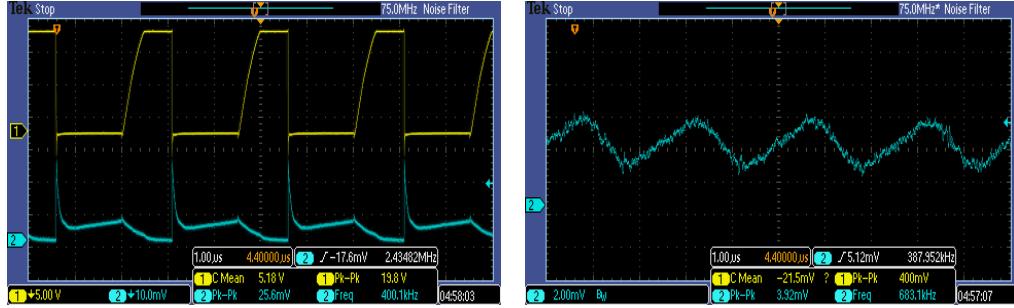


Figure 44: High-Side Switch and Output Voltage in CCM

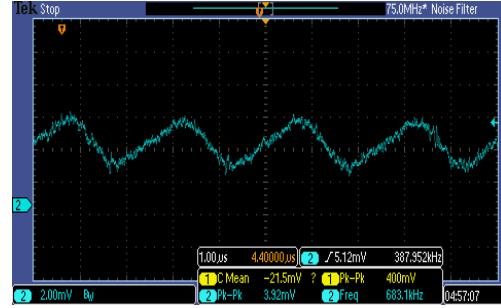


Figure 45: Inductor Current in CCM

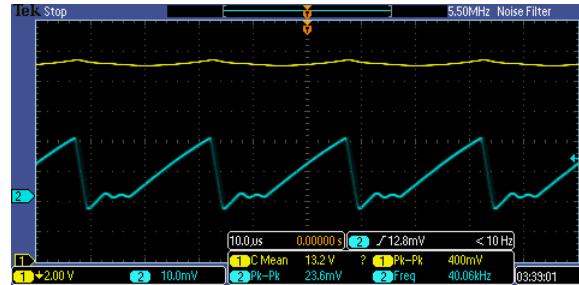


Figure 46: Output Voltage and Inductor Current in DCM

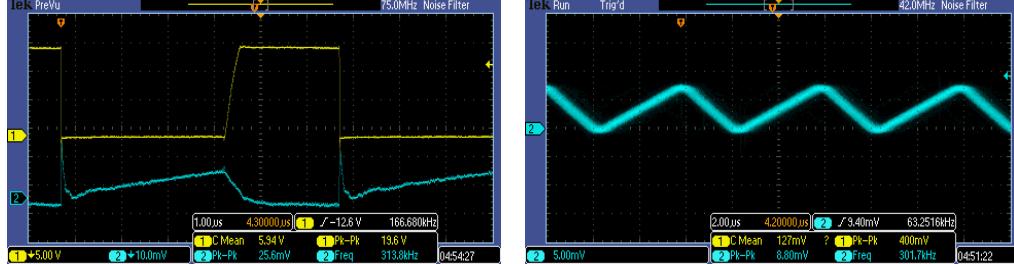


Figure 47: High-Side Switch and Output Voltage in BCM

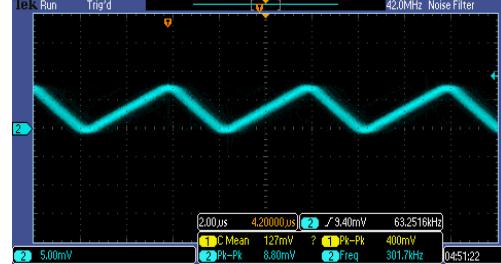


Figure 48: Inductor Current in BCM



Figure 49: High-Side Switch and Output Voltage using Valley Switching

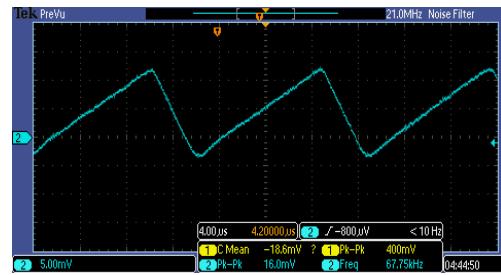


Figure 50: Inductor Current using Valley Switching

## Automatically Limiting Output Voltage

The eleventh required feature is to implement a method to automatically limit the output voltage in both the boost and buck-boost modes. These limits are 40 V across the output in both modes. To limit the output voltage, the input voltage and the current duty cycle from the duty cycle knob were read through microcontroller's ADCs. By using the gain equations for both topologies, maximum duty cycle limits are made dynamically. Since the microcontroller manages the duty cycle of the PWMs, the duty cycle never exceeds these limits, no matter what the duty cycle knob position is. Figures 51 and 52 show that the output voltage (Channel 2) stops increasing while the input voltage (Channel 1) continues to increase. Simply, the duty cycle is changed in real time to prevent changes from the input voltage from becoming too high. Figures 53, 54, and 55 include watch expressions on the current position of the duty cycle knob (KnobDuty1), the actual duty cycle of the PWM (KnobDuty2), and the calculated duty cycle limit (Dmax).



Figure 51: Limiting Output Voltage to 30 volts in Boost Mode

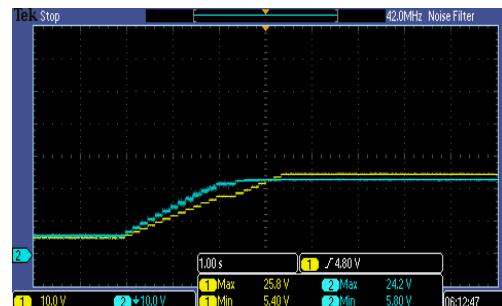


Figure 52: Limiting Output Voltage to 25 volts in Buck-Boost Mode

Expression	Type	Value	Address
0x KnobDuty1	float	0.61675626	0x0000A814@Data
0x KnobDuty2	float	0.605737507	0x0000A818@Data
0x Dmax	float	0.608112693	0x0000A820@Data

Figure 53: Current Knob on Duty Limit

Expression	Type	Value	Address
0x KnobDuty1	float	0.59864372	0x0000A814@Data
0x KnobDuty2	float	0.649220171	0x0000A818@Data
0x Dmax	float	0.495580196	0x0000A820@Data

Figure 54: Current Knob slightly past Duty Limit

Expression	Type	Value	Address
0x KnobDuty1	float	0.60074999	0x0000A814@Data
0x KnobDuty2	float	0.16441333	0x0000A818@Data
0x Dmax	float	0.163118813	0x0000A820@Data

Figure 55: Current Knob far past Duty Limit

## Load Step with Transient Response

The twelfth required feature of the converter was to be able to show a transient response given a change in the value of the load. By using a rocker switch, the load step could be introduced simply by flipping the switch. During the results, the converter was operating in the buck mode at a switching frequency of 200 kHz, with an input voltage of 20 V. Since the load step was not very drastic, the differences between the open loop and closed loop responses were small, even between the synchronous and asynchronous modes.

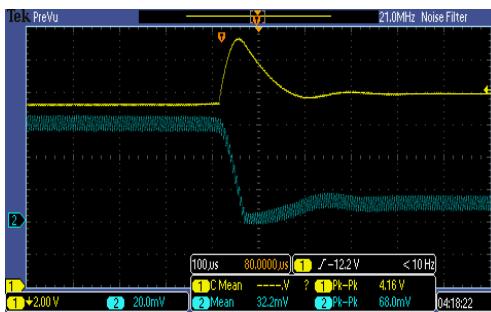


Figure 56: Open Loop Load-Step Transient Response in Output Voltage and Inductor Current, Asynchronous

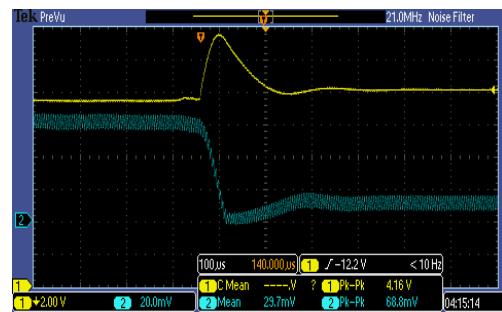


Figure 57: Closed Loop Load-Step Transient Response in Output Voltage and Inductor Current, Asynchronous

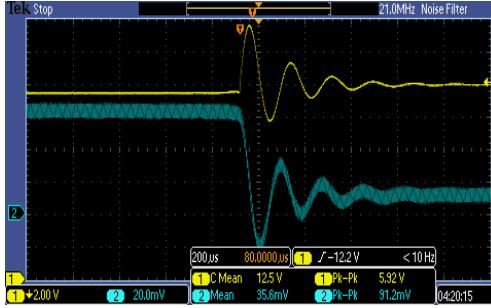


Figure 58: Open Loop Load-Step Transient Response in Output Voltage and Inductor Current, Synchronous

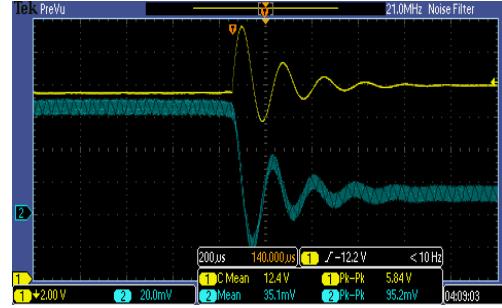


Figure 59: Closed Loop Load-Step Transient Response in Output Voltage and Inductor Current, Synchronous

## Miscellaneous Features

The thirteenth required feature asked to make the converter future proof. This means that physical items be used as part of the converter design, like switches and knobs. This converter includes nearly an excessive amount of switches as well as two knobs that all make meaningful impacts in the results.

The fourteenth required feature asked to protect high voltage nodes from human touch. There are no touch points, excluding the ground pins. Each test point is within the PCB, which will prevent any issues with inaccurate measurements due to touch.

## Elective Features

### Triangular Conduction Mode

An additional, not listed, elective feature is the addition of adding Triangular Conduction mode. The converter was operating in the boost mode, at a switching frequency of 23.75 kHz in the synchronous mode. In Figure 60, Channel 1 represents the gate-source

voltage while Channel 2 represents the drain-source voltage.



Figure 60: High-Side Gate-Source and Drain-Source Voltages using Triangular Conduction

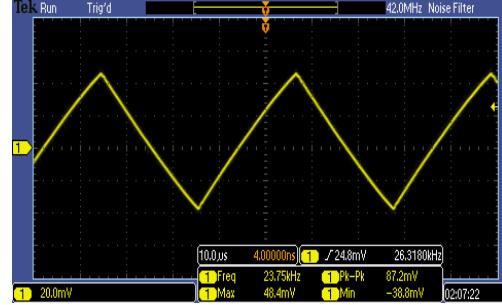


Figure 61: Inductor Current using Triangular Conduction

## Variable Resistance/Inductance in Gate-Source Loop and Switching Loop

The fourth listed elective feature is to be able to have variable inductance and resistance across the gate-source loop, as well as have variable inductance across the switching loop. The variable inductances were implemented through using rocker switches, while a zero  $\Omega$  resistor was put along the gate-source path so that resistance could be added later. The converter operated in the buck mode, at a switching frequency of 200 kHz and at a duty cycle of 50%.

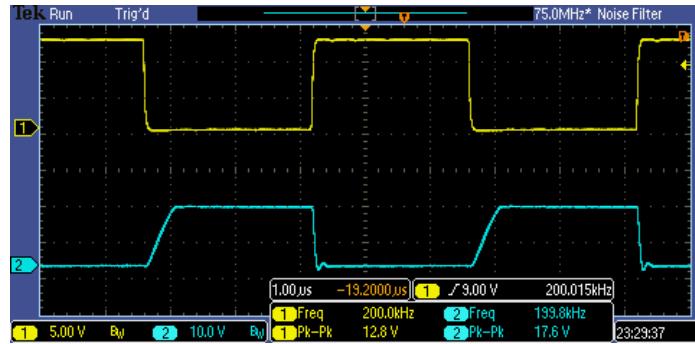


Figure 62: High-Side Gate-Source and Drain-Source Voltages

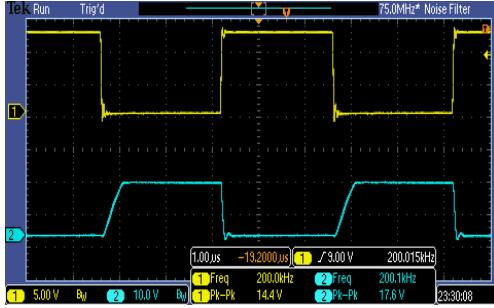


Figure 63: High-Side Gate-Source and Drain-Source Voltages, with added Gate Inductance



Figure 64: High-Side Gate-Source and Drain-Source Voltages, with added Gate Resistance

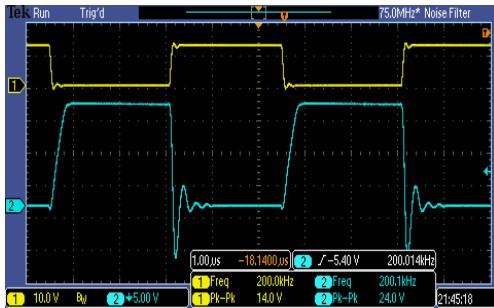


Figure 65: High-Side Gate-Source and Drain-Source Voltages, with added Gate Switch Node Inductance and Gate Resistance

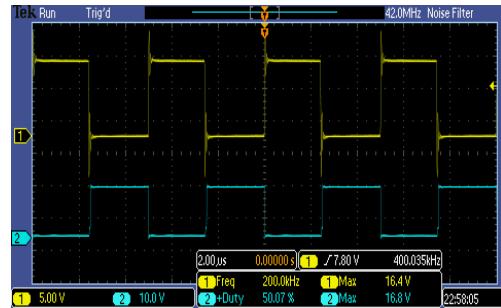


Figure 66: High-Side Gate-Source and Drain-Source Voltages, with added Gate Inductance and Resistance

## Reaching Preset Operating Points Easily

The sixth listed elective feature is that the converter should be able to reach preset operating points easily. A DIP switch was implemented to easily switch between several operating points, including the Preset, open loop and closed loop, synchronous rectification, and the Reset points. The Preset mode is a point that prevents any changes to duty cycle and frequency, and sets them to a fixed value. The default duty cycle and frequency in this mode are 50% and 200 kHz as mentioned before. The Reset mode is a mode that prevents any current from being drawn to the output in the buck and buck-boost modes. This is to

add another safety feature and make it more difficult to tamper with the converter. These modes can be observed in action in the Video Demonstration. These modes can be observed in action in the Video Demonstration.

## Video Demonstration

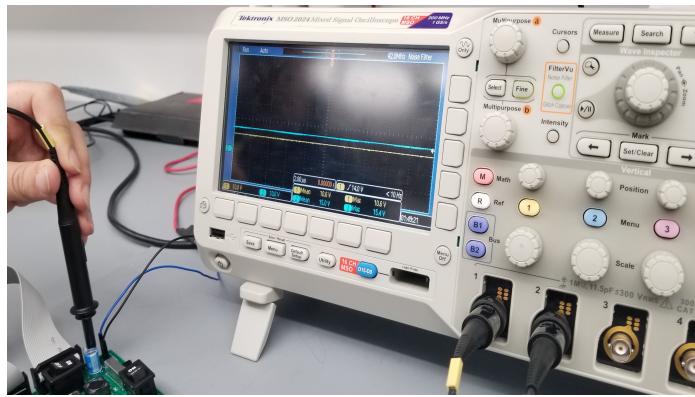


Figure 67: Preset, Sync/Async, Knobs, and Reset. [LINK](#)

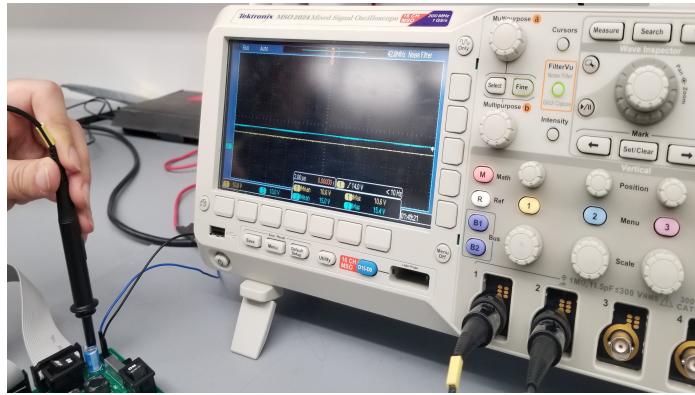


Figure 68: Limiting Output Voltage and Closed Loop Control. [LINK](#)

## Improvements

The converter meets all the required features as well as multiple elective features.

It would be more practical to feed the microcontroller through an isolated power supply, which is supplied directly from the grid. In the current version, the controller is connected to the computer which when plugged in, is connected to the wall outlet. While by supplying the voltage through the grid, the computer can be disconnected and controller can run via memory and work properly. The advantage of using isolated DC/DC converter is separating the oscilloscope ground from the setup ground, which makes operation in all configurations safer. Additional experiments, including testing the effect of gate driver voltage on the conduction resistance and turn on voltage threshold could be investigated to add more insight for future students.