# ROBERT SZAFARCZYK

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## EDUCATION

**PhD Computing Science, University of Glasgow, UK** 2021–2025

- Compiler/hardware co-design in High-Level Synthesis. Extended loop pipelining to enable selective dynamic scheduling. Four years of LLVM experience writing passes in the Intel SYCL FPGA compiler [code, pdf].
- Advanced the state-of-the-art in performance, power, and area of HLS compilation for irregular code, winning a best paper award from the FPGA community.
- Designed hardware, including a Load-Store Queue, a DRAM data unit enabling dynamic loop fusion, and memory speculation techniques that can be parameterized by the compiler.
- Used compiler graph representations and analyses in my own transformations, such as SSA, CFG, DDG, reachability, dominance, dependence distance, SCEV, polyhedral representation, etc.
- Applied computer architecture principles and made informed trade-offs of balancing out-of-order execution windows, speculation, pipelining, etc., when designing compiler transformations.
- Gained debugging skills in large systems, including interfacing with external components such as memory controllers. Learned to set up controlled experiments to debug such systems.
- Worked on a rewrite rules system in Haskell to declaratively trade FPGA memory for compute in Fortran stencil codes, which included compiling Fortran to a functional DSL called TytraCL.
- Learned to write clear, technical documents. Presented technical talks at international conferences. Collaborated with fellow researchers in my field. Taught and mentored students.

**BSc Computer Science w Year in Industry, University of Liverpool, UK** 2017–2021

- Obtained a high First Class degree while working an average 25h per week to support myself.
- Dissertation on accelerating dynamic programming sequence alignment algorithms on Nvidia Kepler GPU. Used CUDA and PTX assembly language. [code, pdf]
- Took Advanced Artificial Intelligence and Computer Vision modules, where I learned about traditional machine learning (decision trees, knn, linear regression, etc.) and deep learning. Implemented a CNN image classifier in PyTorch as part of coursework.

## EXPERIENCE

**Wireless Software Engineer Intern, Intel Corporation, Swindon, UK** 2019–2020

- Part of a team modeling performance of future Intel architectures for signal processing workloads.
- Implemented 5G Layer 1 algorithms (LDPC, MLD) for an experimental dataflow architecture.
- Implemented various FFTs using Intel AVX-512 and experimental AMX extensions.
- Worked on internal tools: contributed to a C++ AMX emulation library; maintained and extended a Python embedded DSL generating assembly code for a dataflow architecture; created a library of higher-order functions to compose assembly code in the DSL; implemented a Web App for graphical access to Intel profiling tools; reported compiler bugs in internal icc versions.
- Collaborated with international teams and presented my work to both internal and external technical teams. Went through and provided code review using Gerrit. Used Jenkins CI pipeline.

## SKILLS

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| **Tools** | C++, C, Rust, SYCL, OpenCL, CUDA, Python, Haskell, JavaScript, Bash, Bluespec, (System)Verilog, Git, CMake, LLDB, Valgrind, Vivado, Quartus |
| **Languages** | English, Polish, German, Spanish (beginner) |

## PERSONAL PROJECTS

**Language Server for Bluespec System Verilog** github.com/robertszafa/bsv-lsp

· Implemented using Rust and asynchronous programming.

**Tree-sitter Parser for Bluespec System Verilog** github.com/robertszafa/tree-sitter-bsv

· Description of the Bluespec System Verilog language grammar using the tree-sitter JavaScript DSL to produce a very fast incremental parser that can be used in a language server.

· Reported upstream bugs in the Bluespec Language Reference document and proposed changes.

**MLIR compiler from C to Bluespec System Verilog** github.com/robertszafa/circt

· Key challenge of translating from a Sequential Control Flow model of computation used in C to a Guarded Atomic Actions model used in Bluespec, with the goal of parallelizing control flow.

· Modeling the Guarded Atomic Actions computational model as an MLIR dialect.

## ACADEMIC PUBLICATIONS

- (Short Paper) Robert Szafarczyk, Syed Waqar Nabi, and Wim Vanderbauwhede. "Reducing FPGA Memory Footprint of Stencil Codes through Automatic Extraction of Memory Patterns". In: *2022 32nd International Conference on Field-Programmable Logic and Applications (FPL)*. 2022, pp. 148–152. DOI: 10.1109/FPL57034.2022.00033 [pdf]

- (Extended Abstract) Robert Szafarczyk, Syed Waqar Nabi, and Wim Vanderbauwhede. "Dynamically Scheduled Memory Operations in Static High-Level Synthesis". In: *IEEE 31st Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM)*. 2023, pp. 220–220. DOI: 10.1109/FCCM57271.2023.00048 [pdf]

- (Best Paper Award) Robert Szafarczyk, Syed Waqar Nabi, and Wim Vanderbauwhede. "Compiler Discovered Dynamic Scheduling of Irregular Code in High-Level Synthesis". In: *2023 33rd International Conference on Field-Programmable Logic and Applications (FPL)*. 2023, pp. 1–9. DOI: 10.1109/FPL60245.2023.00009 [pdf]

- Robert Szafarczyk, Syed Waqar Nabi, and Wim Vanderbauwhede. "A High-Frequency Load-Store Queue with Speculative Allocations for High-Level Synthesis". In: *2023 International Conference on Field Programmable Technology (ICFPT)*. 2023, pp. 115–124. DOI: 10.1109/ICFPT59805.2023.00018 [pdf]

- Robert Szafarczyk, Syed Waqar Nabi, and Wim Vanderbauwhede. "Dynamic Loop Fusion in High-Level Synthesis". In: *Proceedings of the 2025 ACM/SIGDA International Symposium on Field Programmable Gate Arrays*. FPGA '25. Monterey, CA, USA: Association for Computing Machinery, 2025. DOI: 10.1145/3706628.3708871 [pdf]

- Robert Szafarczyk, Syed Waqar Nabi, and Wim Vanderbauwhede. "Compiler Support for Speculation in Decoupled Access/Execute Architectures". In: *Proceedings of the 34th ACM SIGPLAN International Conference on Compiler Construction*. CC '25. Las Vegas, United States, 2025. DOI: 10.1145/3708493.3712695 [pdf]