COMP 230: Computer Architecture and Organization Fall 2017 EXAM 2 (PRACTICE)

Instructions:

- This practice exam is meant to give you the flavor of questions that will be asked on the exam. Do not expect the real exam to be the same questions with only the numbers or MIPS instructions changed.
- Your real exam will be open book and notes. However, you are not allowed to use laptops, cell phones, calculators, or other electronics.
- If you do not show your work, do not expect partial credit for incorrect answers.
- If you believe a problem is incorrectly or incompletely specified, make a reasonable assumption and solve the problem. The assumption should not result in a trivial solution.
- In all cases, clearly state any assumptions you make in your answers.

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Question	Points Possible	Grade
1	10	
2	20	
3	20	
4	20	
5	30	
Total	100	

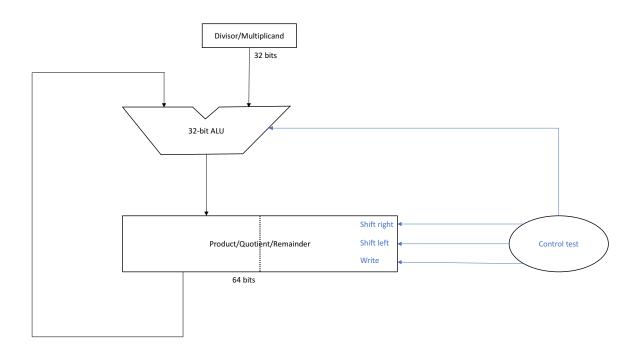


Figure 1: Hardware components for multiplication and division.

1. (a) Complete the following table to divide 12 (represented using 8 bits) by 5 (represented using 4 bits). Using the hardware in Figure 1.

Iteration	Step	8 Bits
0	initial	
1	subtract?	
	shift	
2	subtract?	
	shift	
3	subtract?	
	shift	
4	subtract?	
<u> </u>	shift	

(b) If our MIPS machine operates on 4-bit words (so that we only have 4-bits to represent our integers), after a divide instruction, what instruction puts the quotient into \$t0?

2.	Add 1.75 and 0.390625 using binary floating-point addition, assuming one round bit, one guard bit, one sticky bit, and using 5 fraction bits (5 bits of precision). Show your work. Also, what would the result be without a sticky bit?
3.	Write MIPS assembly code for a procedure divides that takes in two integers a and b as parameters. If a is divisible by b divides should return 1; otherwise 0.
	divisible by a divides should return 1, otherwise o.

4. You have just written a new program for your company, which exhibits no pipeline stalls and has the following breakdown of executed instructions:

add	addi	not	beq	lw	sw
20%	20%	0%	25%	25%	10%

(a) In what fraction of all cycles is the data memory used?

(b) In what fraction of all cycles is the input of the sign-extend circuit needed? What is this circuit doing in cycles in which its input is not needed?

5. Consider the following sequence of instructions, executing using the pipeline shown in figure 2:

add \$s1, \$s2, \$s3 add \$s2, \$s1, \$s4 add \$s1, \$s1, \$s2

(a) Assuming no forwarding, what are the hazards?

(b) Assuming no forwarding, how many cycles does this sequence take to execute?

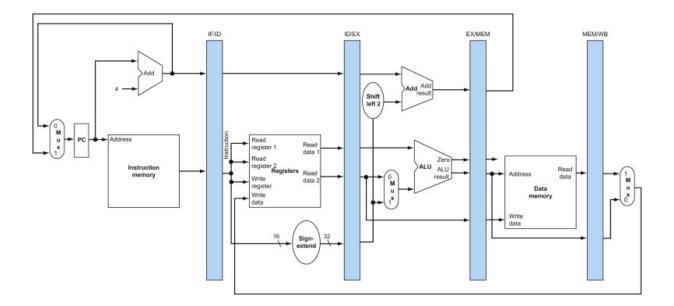


Figure 2: A simple MIPS pipeline.

(c) Assuming full forwarding, what hazards remain?

(d) Assuming full forwarding, how many cycles does this sequence take to execute?