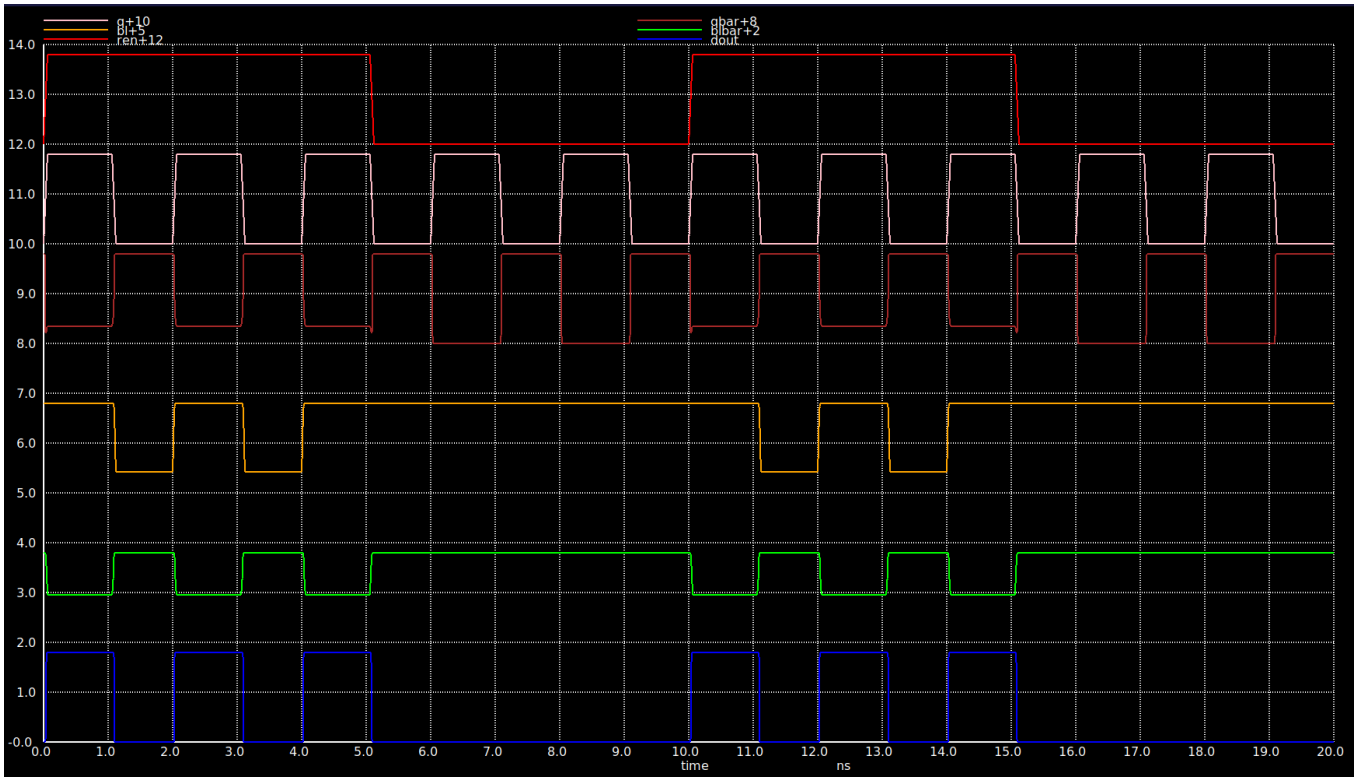
# Pre-layout

## Step 0. Baseline Analysis

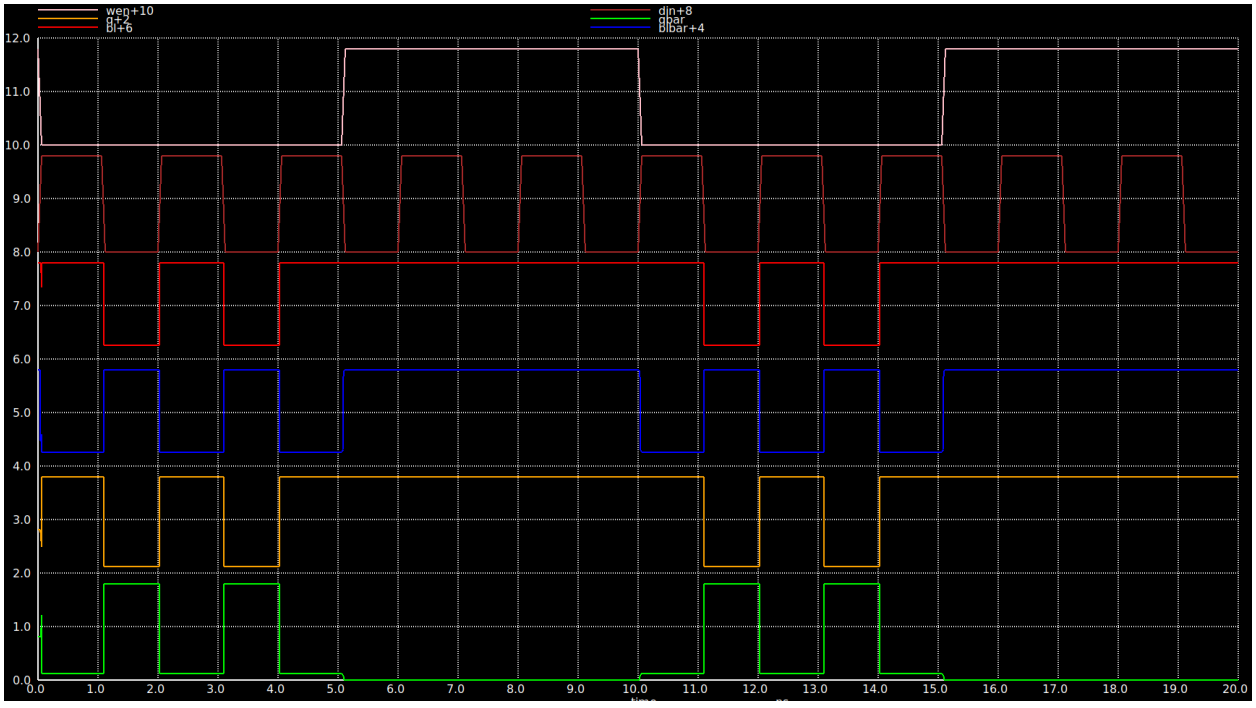
**Need PDK to get more precise simulation, and fine tune parameters, PDK was not working on my computer for some reason*
Wpd = 0.84, Wax = 0.42, Wpu = 0.42

### 1bit_sram_read.spice



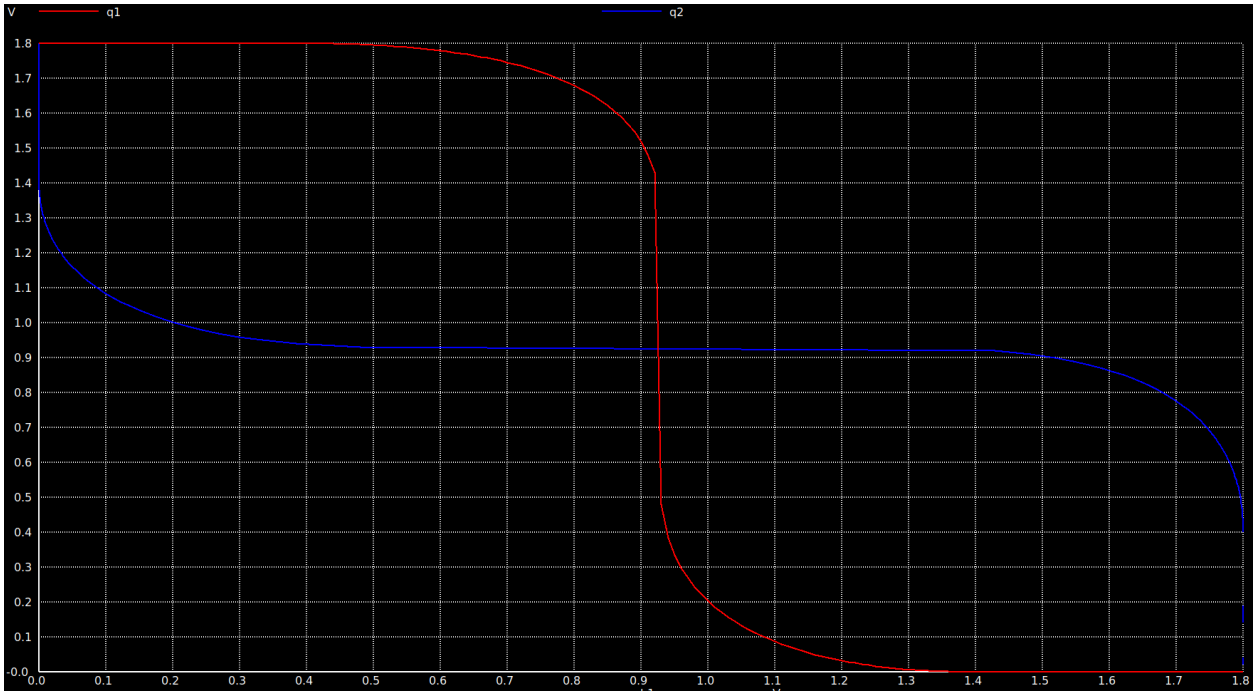
| Node | Voltage |
|---|---|
| vdd | 1.8 |
| q | 0 |
| qbar | 1.8 |
| wl | 0 |
| bl | 1.8 |
| blbar | 1.8 |
| dout1 | 1.80007 |
| 3 | 1.40063 |
| 2 | 1.39994 |
| ren | 0 |
| dout | 4.61713e-09 |
| dinb | 1.8 |
| din | 0 |
| dinbb | 4.61735e-09 |
| 4 | 0.9 |
| out1 | 1.16071e-09 |
| wen | 1.8 |
| 5 | 1.8 |
| out2 | 4.61735e-09 |
| vdin#branch | 0 |
| vwen#branch | 0 |
| vren#branch | 0 |
| vq#branch | 1.81e-12 |
| vwl#branch | 0 |
| vdd#branch | -2.22306e-11 |

## 1bit_sram_write.spice

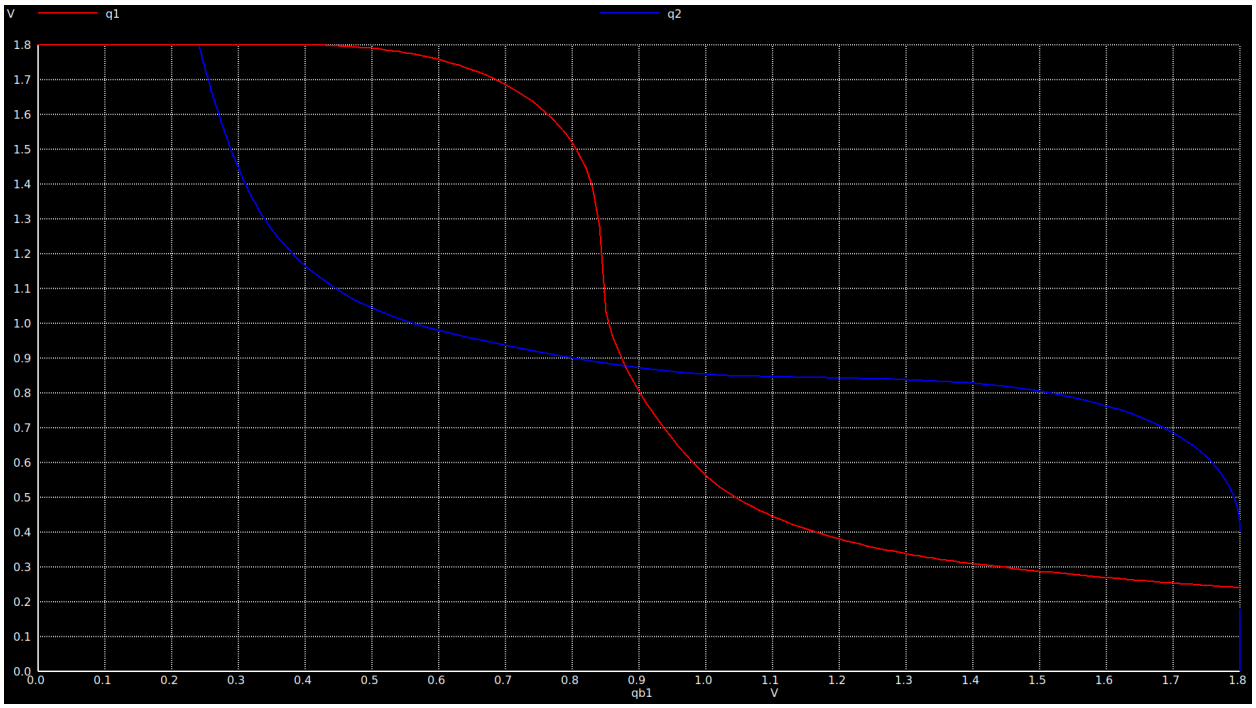


| Node | Voltage |
|---|---|
| vdd | 1.8 |
| q | 0.814419 |
| qbar | 0.814419 |
| wl | 0 |
| bl | 1.8 |
| blbar | 1.8 |
| dout1 | 1.39996 |
| 3 | 1.3999 |
| 2 | 1.68377 |
| ren | 0 |
| dout | 6.73212e-09 |
| dinb | 1.8 |
| din | 0 |
| dinbb | 4.61735e-09 |
| 4 | 0.9 |
| out1 | 1.16071e-09 |
| wen | 1.8 |
| 5 | 1.8 |
| out2 | 4.61735e-09 |
| vren#branch | 0 |
| vdin#branch | 0 |
| vwen#branch | 0 |
| vwl#branch | 0 |
| vdd#branch | -4.84798e-05 |

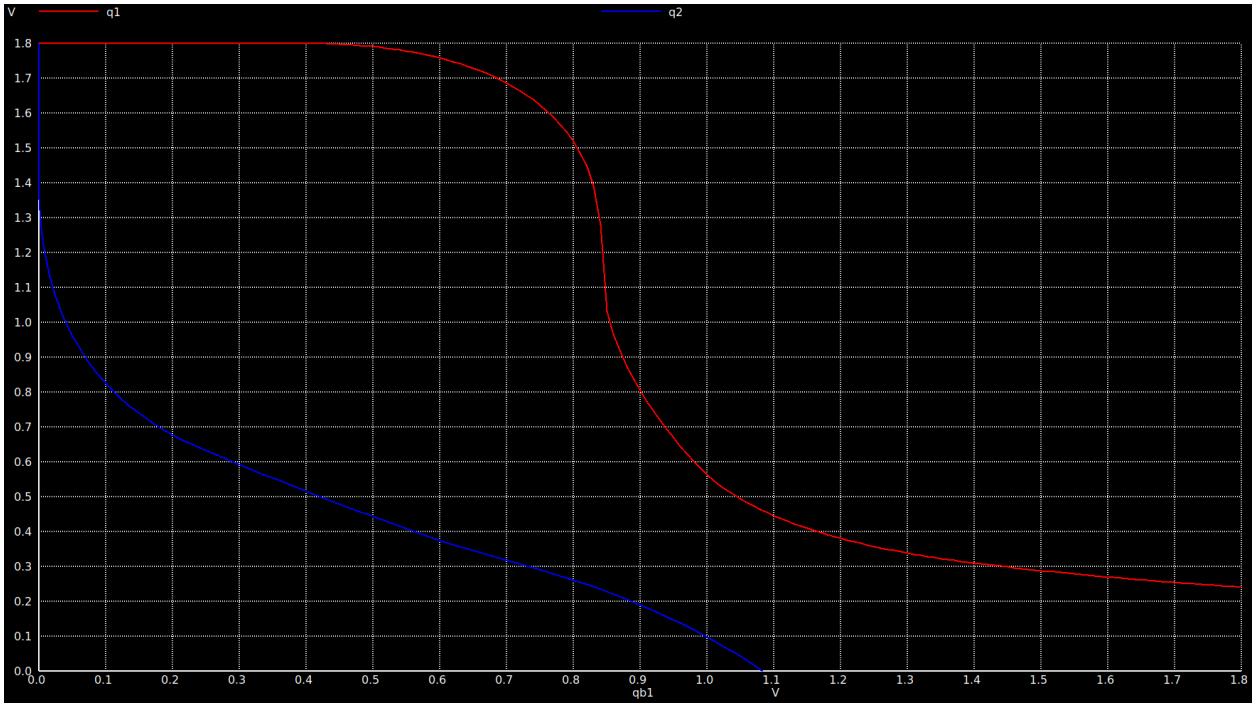
## Holdsnm.spice



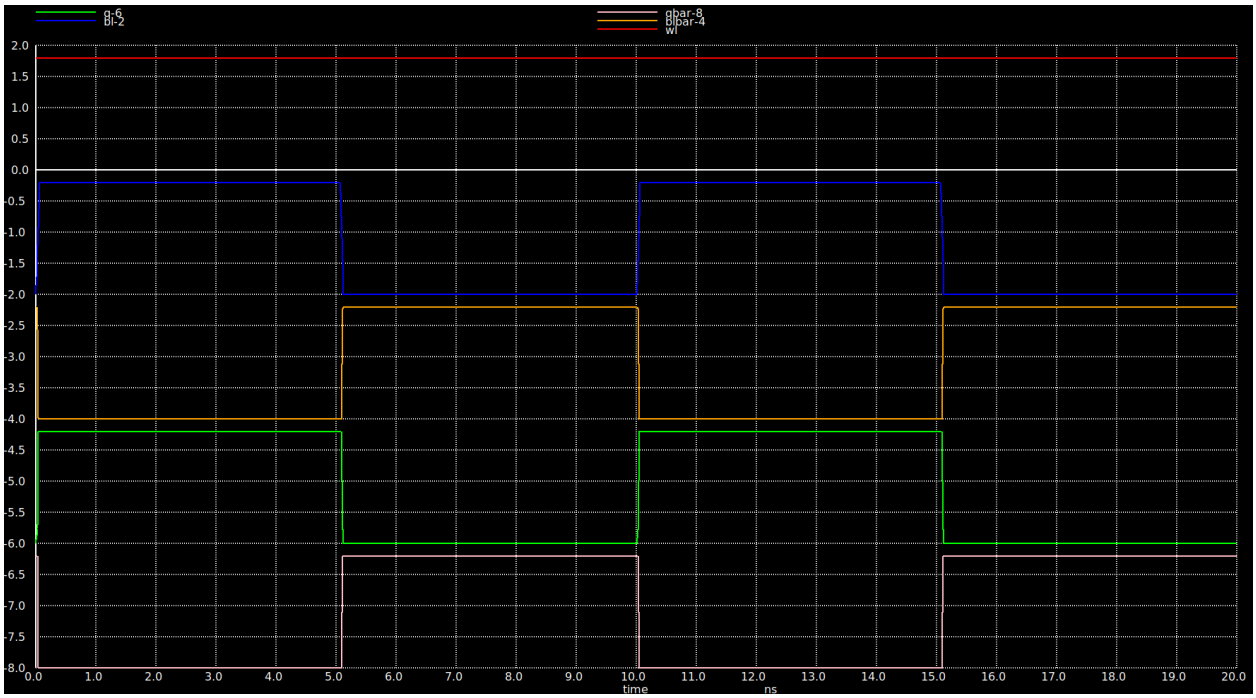
## Readsnm.spice




## Writesnm.spice



# 6T_sram_cell.spice

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Initial Transient Solution
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Node                                   Voltage
----                                   -------
vdd                                        1.8
q                                  2.30867e-09
qbar                                       1.8
bl                                           0
wl                                         1.8
blbar                                      1.8
v2#branch                                    0
v1#branch                           9.05e-13
vdd#branch                         -9.05e-12
```