ANY-1 Reference Guide

Table of Contents

Programming Model

Registers

Overview

The ANY-1 is a vector machine. The ISA is a 64-register machine with a unified register file for integer, floating-point, decimal-floating-point or posit arithmetic. There are many control and status (CSR) registers which hold an assortment of specific values relevant to processing.

General Purpose Registers (x0 to x63) / Scalar Registers

The register usage convention probably has more to do with software than hardware. Excepting a few special cases, the registers are general purpose in nature. Registers may hold integer, floating-point, decimal floating-point or posit values.

x0 always has the value zero. Register x63 is a read only alias of the instruction pointer register. Registers x61 and x62 are used for stack references and subject to stack bounds checking.

Register	Description / Suggested Usage	Saver
x0	always reads as zero (hardware)	
x2	constant building / temporary (cb)	
x3-x9	temporaries (t0-t6)	caller
x10-x19	register variables (s0-s9)	callee
x20-x27	function arguments (a0-a7) a7/g2	caller
x59	thread pointer (tp / g1)	
x60	global data pointer (g0)	callee
x61	base / frame pointer (fp)	callee
x62	current stack pointer (sp)	callee
x63	instruction pointer	

Control and Status Registers

Overview

There are numerous special purpose control and status registers in the design. Some registers are present to store variables for performance reasons that would otherwise be stored in main memory.

[U/S/H/M/D]_CAUSE (0x?006)

This register contains a code indicating the cause of an exception or interrupt. The break handler will examine this code to determine what to do. Only the low order 16 bits are implemented. The high order bits read as zero and are not updateable.

U_SEMA (CSR 0x000C) Semaphores

This register is available for user semaphores or flag use. Bits in this CSR may be set or cleared with one of the CSRxx instructions. This register has individual bit set / clear capability.

S_PTA (0x1003)

This register contains the base address of the highest-level page directory for memory management, the paging table depth and the size of the pages mapped. The base address must be page aligned (4kB).

63 12	11	10 8	7	6 0
Paging Directory Base Address$_{63..12}$	~	TD	S	~

TD	
0	1 level lookup
1	2 level lookup
2	3 level lookup
3	4 level lookup
4 to 7	reserved

S	
0	map 16kB pages
1	map 4MB pages

S_TID (CSR 0x1010)

This CSR register is reserved for use to contain the task id for the currently running task.

S_ASID – (CSR 0x101F)

This register contains the address space identifier (ASID) or memory map index (MMI). The ASID is used in this design to select (index into) a memory map in the paging tables.

S_KEYS – (CSR 0x1020 to 0x1022)

These registers contain a collection of keys associated with the process for the memory system. Each key is twenty bits in size. Each register contains three keys for a total of nine keys. All three registers are searched in parallel for keys matching the one associated with the memory page. Keyed memory enhances the security and reliability of the system.

63 60	59 40	39 20	19 0
~$_6$	key3	key2	key1

M_TVEC (0x3030 to 0x3033)

These registers are an alias for the D_TVEC registers 0x4030 to 0x4033 which allows access to the TVEC registers from machine mode. They contain the address of the exception handling routine for a given operating level. The lower bits of the exception address are determined from the operating level. TVEC[1] to TVEC[4] are used by the REX instruction.

D_TVEC (0x4030 to 0x4034)

These registers contain the address of the exception handling routine for a given operating level. TVEC[4] (0x4034) is used directly by hardware to form an address of the debug routine. The lower eight bits of TVEC[4] are not used. The lower bits of the exception address are determined from the operating level. TVEC[1] to TVEC[4] are used by the REX instruction.

Operating Levels

The core has five operating modes. The highest operating mode is operating mode four which is called the debug operating mode. Debug operating mode has complete access to the machine including special registers and features reserved for debug. Other operating levels may have more restricted access. When an interrupt occurs, the operating mode is set to the debug mode. The core vectors to an address depending on the current operating mode. When not operating at user mode addresses are not subjected to translation and the virtual address and physical address are the same.

Operating Mode	Moniker
0	user
1	supervisor
2	hypervisor
3	machine
4	debug

Switching Operating Modes

The operating mode is automatically switched to the debug mode when an interrupt occurs. The BRK instruction may be used to switch operating modes. The REX instruction may also be used by a handler to switch the operating mode to a lower mode. One of the exception return instructions (RTD, RTE) will switch the operating level back to what it was prior to the interrupt or exception.