# Register Set

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Regno | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |  |
| 000 |  | | | | | | | | Current Address 0 to 7, Channel 0 |
| 001 |  | | | | | | | | Current Address 8 to 15 |
| 002 |  | | | | | | | | Current Address 16 to 23 |
| 003 |  | | | | | | | | reserved |
| 004 |  | | | | | | | | Current Count 0 to 7 |
| 005 |  | | | | | | | | Current Count 8 to 15 |
| 006 |  | | | | | | | | Current Count 16 to 23 |
| 007 |  | | | | | | | | reserved |
| 008 |  | | | | | | | | Modulo Increment 0 to 7 |
| 009 |  | | | | | | | | Modulo Increment 8 to 15 |
| 00A |  | | | | | | | | Reserved |
| 00B |  | | | | | | | | Reserved |
| 00C |  | | | | | | | | Blit Width 0 to 7 |
| 00D |  | | | | | | | | Blit Width 8 to 15 |
| 00E |  | | | | | | | | Reserved |
| 00F |  | | | | | | | | reserved |
| 010 |  | | | | | | | | Base Address 0 to 7 |
| 011 |  | | | | | | | | Base Address 8 to 15 |
| 012 |  | | | | | | | | Base Address 16 to 23 |
| 013 |  | | | | | | | | reserved |
| 014 |  | | | | | | | | Base Count 0 to 7 |
| 015 |  | | | | | | | | Base Count 8 to 15 |
| 016 |  | | | | | | | | Base Count 16 to 23 |
| 017 |  | | | | | | | | reserved |
| 018 |  | Mode | | IDH | | AR | RWV | | Channel 0 Control |
| 019 |  |  |  |  | LNK | LNKCH | | | Channel 0 Linking |
| 01A | TG | |  | BSZ | | BUCKET | | | Channel 0 Bucket |
| 01B |  |  |  |  |  |  |  |  | reserved |
| … |  | | | | | | | |  |
| 020 | … | | | | | | | | Current Address 0 to 7, Channel 1 |
| … |  | | | | | | | |  |
| 100 | TC7 | TC6 | TC5 | TC4 | TC3 | TC2 | TC1 | TC0 | Channel Status – Term. Count (RO) |
| 101 | RQ7 | RQ6 | RQ5 | RQ4 | RQ3 | RQ2 | RQ1 | RQ0 | Channel Status – Request (RO) |
| 102 |  |  |  |  | SR | Channel Number | | | Software Request |
| 103 |  |  |  |  | SR | Channel Number | | | Request Mask |
| 104 | M7 | M6 | M5 | M4 | M3 | M2 | M1 | M0 | Mask Register |
| 105 |  |  | PLD | | | | | | Blit Pipeline Depth |
| 106 | Blit Op 2 | | | | Blit Op 1 | | | | Blit Operation |
| 108 | Destination Data | | | | | | | | Destination Data 0 to 7 |
| 109 | Destination Data | | | | | | | | Destination Data 8 to 15 |
| 10A | Destination Data | | | | | | | | Destination Data 16 to 23 |
| 10B | Destination Data | | | | | | | | Destination Data 24 to 31 |
| D030 | ~ | ~ | TREGNO | | | | | | Timing Register number |
| D031 | TDATA | | | | | | | | Timing Register data |
| D032 | ~ | 80 | ~ | ~ | ~ | ~ | ~ | RPG | Register paging |
| … |  |  |  |  |  |  |  |  |  |
| D03F |  |  |  |  |  |  |  |  | Not used |

TCx – terminal count is signalled when the channel current count register reaches zero

RMV – The bus cycle type to perform. This is one of verify(00), read(01), or write (10), the value 11 is reserved.

AR – Auto Reload. The channel current count and current address are automatically reloaded with the base count and base address once terminal count is reached.

IDH – Increment, Decrement, Hold or Refresh. This controls what happens to the current address after a DMA cycle. Hold keeps the address constant. Refresh increments address bits 0 to 11 and reflects the same bits on address bits 12 to 23. Hold (00), Increment (01), Decrement (10) and Refresh (11).

TG – Transfer granularity. Byte (00), 16-bit (01), 32-bit (10), reserved (11)