uart6551sbi

© 2022 Robert Finch

# Overview

A UART component (Universal Asynchronous Transmitter / Receiver) is used for the asynchronous transmission and reception of data. Asynchronous referring to the lack of a clock signal during transmission or reception.

uart6551sbi is a WDC6551 register compatible uart. The uart is a 8-bit peripheral device. The SBI version of the uart uses a simple synchronous bus interface like the 6502 bus.

Baud rate is controlled by clock divider which assumes a 50MHz baud reference clock input. If a different clock frequency is used, then the divider table will need to be updated. The baud rate may also be controlled via a clock divider register. This register is 24 bits so gives a minimum frequency of 2.98 Hz assuming a 50MHz clock. (50MHz / 2^24).

Note the use a reference clock separate from the bus clock. It is common in 65xx systems to create wait states by stretching the bus clock. This means the bus clock is not a suitable reference for other timing.

## Special Features

* WDC6551 register compatibility
* Independent bus and baud clocks

# Register Description

There are seventeen registers in the design. The function of the first four registers matches the 6551 function.

|  |  |  |
| --- | --- | --- |
| Reg | Moniker | Description |
| 00 | UART\_TRB | Transmit and receive buffer. Data written is transmitted, on a read data available is read. |
| 01 | UART\_STAT | Status Register. Returns status bits on a read, a write of any value will cause a reset of some of the command register bits |
| 02 | UART\_CMD | Command register |
| 03 | UART\_CTRL | Control register |

## UART\_TRB (reg 0)

Data written to the register is transmitted. A register read returns data received by the uart. When the fifo’s are enabled writing to this register writes to the transmit fifo. Reading this register reads the receive fifo.

## UART\_STAT (reg 1)

Uart status register. Writing any value to the status register resets some of the uart’s command bits.

|  |  |  |
| --- | --- | --- |
| Bit | Status |  |
| 0 | Parity Error | 1 = parity error occurred, 0 = no error |
| 1 | Framing Error | 1 = framing error |
| 2 | Overrun | 1 = overrun |
| 3 | Rx Full | 1 = receiver data available |
| 4 | Tx Empty | 1 = open slot in transmit fifo |
| 5 | DCD | 0 = data carrier present |
| 6 | DSR | 0 = data set ready |
| 7 | IRQ | 1 = irq occurred |

## UART\_LS (reg 11)

Uart line status register.

|  |  |  |
| --- | --- | --- |
|  | **Additional Line Status Byte** | |
| 0 | reserved |  |
| 1 | reserved |  |
| 2 | reserved |  |
| 3 | reserved |  |
| 4 | Break received | 1 if a break signal is received |
| 5 | Tx Full | 1 = transmit fifo full |
| 6 | reserved |  |
| 7 | G Rcv Err | 1 = global receiver error (set if any error status is set) |

## UART\_MS (reg 12)

Uart modem status

|  |  |  |
| --- | --- | --- |
|  | **Additional Modem Status Byte** | |
| 0 | CTS | 1 = CTS line changed state |
| 1 | DSR | 1 = DSR line changed state |
| 2 | RI | 1 = RI line changed state |
| 3 | DCD | 1 = DCD line changed state |
| 4 | CTS | CTS state |
| 5 | reserved |  |
| 6 | RI | RI state |
| 7 | reserved |  |

## UART\_IRQS (reg 13)

IRQ status register

|  |  |  |
| --- | --- | --- |
|  | **IRQ Status** | |
| 1,0 | zero | these two bits are zero |
| 2 to 4 | IRQENC | encoded irq value (0 to 7) |
| 5 to 6 | reserved |  |
| 7 | irq | IRQ is set |

## UART\_CMD (reg 2)

|  |  |  |
| --- | --- | --- |
| Bit |  |  |
| 0 | DTR | output 1 = low, 0 = high |
| 1 | RxIe | receiver interrupt enable 0 = enabled, 1 = disabled |
| 2,3 | RTS Control |  |
|  | 00 | output RTS high |
|  | 01 | output RTS low, enable transmit interrupt |
|  | 10 | output RTS low, |
|  | 11 | output RTS low, send a break signal |
| 4 | LLB | 1 = local loopback (receiver echo) |
| 5 to 7 | Parity Control |  |
|  | 000 | no parity |
|  | 001 | odd parity |
|  | 011 | even parity |
|  | 101 | transmit mark parity (parity error disabled) |
|  | 111 | transmit space parity (parity error disabled) |

## UART\_CMD2 (reg 9)

|  |  |  |
| --- | --- | --- |
| 0 | LSIe | line status change interrupt enable 1 = enabled |
| 1 | MSIe | modem status change interrupt enable 1 = enabled |
| 2 | RxToIe | receiver timeout interrupt enable 1 = enabled |
| 3 to 7 | reserved |  |

## UART\_CTRL (reg 3)

|  |  |  |
| --- | --- | --- |
| Bit |  |  |
| 0 to 3 | Baud Rate |  |
|  | |  |  | | --- | --- | | 0000 | Use 16x external clock | | 0001 | 50 | | 0010 | 75 | | 0011 | 109.92 | | 0100 | 134.58 | | 0101 | 150 | | 0110 | 300 | | 0111 | 600 | | 1000 | 1200 | | 1001 | 1800 | | 1010 | 2400 | | 1011 | 3600 | | 1100 | 4800 | | 1101 | 7200 | | 1110 | 9600 | | 1111 | 19200 | | This table is expanded using an extra control bit #27. |
| 4 | Rx clock source | 1 = external, 0 = baud rate generator |
| 5,6 | Word length   |  |  | | --- | --- | | 00 | 8 | | 01 | 7 | | 10 | 6 | | 11 | 5 | | code for word length in bits |
| 7 | Stop Bit   |  |  | | --- | --- | | 0 | 1 | | 1 | 1 if 8 bits and parity | | 1 | 1.5 if 5 bits and no parity | | 1 | 2 otherwise | |  |

## UART\_CTRL2 (reg 15)

Controls the fifos

|  |  |  |
| --- | --- | --- |
| 0 | Fifo enable | 1 = fifo’s enabled |
| 1 | Rx Fifo Clear | 1 = clear receiver fifo |
| 2 | Tx Fifo Clear | 1 = clear transmit fifo |
| 3 | reserved |  |
| 4,5 | Transmit Threshold   |  |  | | --- | --- | | 0 | 1 byte | | 1 | ¼ full | | 2 | ½ full | | 3 | ¾ full | | Threshold for DMA signal activation  If the transit fifo count is less than the threshold then a DMA transfer is triggered. |
| 6, 7 | Receive Threshold   |  |  | | --- | --- | | 0 | 1 byte | | 1 | ¼ full | | 2 | ½ full | | 3 | ¾ full | | Threshold for DMA signal activation. If the receive fifo count is greater than the threshold then a DMA transfer is triggered. |

## UART\_CTRL3 (reg 16)

|  |  |  |
| --- | --- | --- |
| 0 | hwfc | 1 = automatic hardware flow control |
| 1 | reserved |  |
| 2 | dmaEnable | 1 = dma enabled |
| 3 | Baud Rate bit 4   |  |  | | --- | --- | | 10000 | 38400 | | 10001 | 57600 | | 10010 | 115200 | | 10011 | 230600 | | 10100 | 460800 | | 10101 | 921600 | | 10110 | reserved | | 10111 | reserved | | 11xxx | reserved | | Extended baud rate selection bit, used in combination with bits 0 to 3. |
| 4,5 | reserved |  |
| 6 | selDV | 1 = use clock divider register, 0 = use baud table |
| 7 | reserved |  |

Selecting the clock divider register as the baud source allows any programmable baud rate.

## UART\_CLKD0 (reg 4)

Bits 0 to 7 of the divider value.

## UART\_CLKD1 (reg 5)

Bits 8 to 15 of the divider value.

## UART\_CLKD2 (reg 6)

Bits 16 to 23 of the divider value.

## OTHERS (reg 8, 10, 14)

Reserved

# Bus Interface

The synchronous bus interface transfers data according to the bus clock. Write data is latched on the negative edge of the bus clock. The address, control, and data outputs are latched on the positive edge of the bus clock. There is no bus acknowledge; transfers are assumed to complete within one clock cycle.

# Ports

|  |  |  |  |
| --- | --- | --- | --- |
| Signal | I/O | Wid | Purpose |
| rst\_i | I | 1 | reset |
| refclk\_i | I | 1 | Reference clock (50 MHz) |
| ph2\_i | I | 1 | bus clock input |
| cs\_i | I | 1 | circuit/core select |
| irq\_o | O | 1 | interrupt request |
|  | SYNCHRONOUS BUS SIGNALS | | |
| rw\_i | I | 1 | Read (1) / write (0) enable |
| adr\_i | I | 5 | address bits 0 to 4 (selects register) |
| dat\_i | I | 7 | data input bus |
| dat\_o | O | 7 | data output bus |
|  | Modem Controls | | |
| cts\_ni | I | 1 | clear to send input active low. |
| rts\_no | O | 1 | request to send output active low |
| dsr\_ni | I | 1 | data set ready active low |
| dcd\_ni | I | 1 | data carrier detect active low |
| dtr\_no | O | 1 | data terminal ready active low |
| ri\_ni | I | 1 | ring indicator active low |
|  |  |  |  |
| rxd\_i | I | 1 | serial data input (receive) |
| txd\_o | O | 1 | serial data output (transmit) |
| data\_present | O | 1 | data is present in the receiver |
| rxDRQ\_o | O | 1 | receiver DMA request |
| txDRQ\_o | O | 1 | transmitter DMA request |
| xclk\_i | I | 1 | external baud rate clock |
| RxC\_i | I | 1 | external receiver clock |