## Programming Model

|  |  |  |
| --- | --- | --- |
| 23 16 | 15 0 | |
|  | X – Index Register | |
|  | Y – Index Register | |
|  | U – User stack pointer | |
| 0000 | S – Hardware stack pointer | |
| PC | | |
|  | A | B |
|  | DPR | 0 |
| USPPG | | 0 |

A,B registers concatenate to form D register

There is an additional 16-bit register allowing the user stack to be relocated to any page of memory.

## Configurations

The rf6809 core may be configured to use 12-bit bytes which increases the address range to 36-bits.

## Instruction Prefixes

rf6809 makes use of instruction prefixes to extend the addressing modes available. There are two prefixes FAR, and OUTER, which indicate to use a far address or outer indexing.

### FAR

FAR when applied to extended addressing indicates to use a full 24-bit/triple byte address rather than a 16 bit one.

When the FAR prefix is applied to indirect addressing the prefix indicates that the indirect address is 24-bit. This allows the use of a 24-bit indirect address to reach anywhere in memory.

Opcode: 0x15

### OUTER

The OUTER prefix indicates that the index register is applied after retrieving an indirect address. Normally the index register is used in the calculation of the indirect address.

When configured for 12-bit bytes the OUTER prefix is not used as there are sufficient bits in the index post-byte to encode outer indexing mode.

Opcode: 0x1B

## Additional Instructions

JMP FAR – performs a jump using a 24-bit extended address.

Opcode: 0x8F

JSR FAR – performs a jump to subroutine using a 24-bit extended address. The full 24-bit program counter is stored on the stack.

Opcode: 0xCF

RTF – performs a far return from subroutine by loading a full 24-bit program counter from the stack.

Opcode: 0x38

Indirect addresses must reside within the first 64k bank of memory.

## Differences from the 6809

The program counter is a full 24-bit register. The JMP and JSR instructions modify only the low order 16 bits of the program counter. To modify the full 24-bits use the JMP FAR and JSR FAR instructions. A return from a far subroutine may be done using the RTF instruction.

During interrupt processing the entire 24-bit program counter is stacked. The RTI instruction also loads the entire 24-bit program counter.

### Control Registers

There are several control registers mapped into the address space.

|  |  |  |
| --- | --- | --- |
| Address | Access | Register Usage |
| FF..FE0 | RO | Core ID – used to identify core in multi-core application. Reflects the value of the coreid\_i input. |
| FF..FE1 | WO | Checkpoint register. If checkpointing is enabled this register must be written within one second, or an NMI will occur. |
| FF..FE4/5 | RO | high order bits of millisecond count |
| FF.FF6/7 | RO | low order bits of millisecond count |

The millisecond count register contains a count of the number of milliseconds since the last reset.

### Checkpoint Register

The core may be configured to include a checkpoint register and timer. When checkpointing is present an NMI will be generated is the checkpoint register is not written to within one second.

### Hardware:

This is a softcore implementation of a 6809 compatible processor. As such no attempt was made to duplicate the 6809’s bus cycle activity. Instructions may not execute in the same number of clock cycles as the 6809. Instructions in some circumstances execute in fewer clock cycles.