GFX\_TextController

## 

## Description

This is a text mode video display controller that supports color intended for use with a 64-bit bus. The controller uses several internal dual ported r/w memories to store text, text attributes and character bitmaps. The display memory is sixty-four bits wide. 512 different simultaneous characters may be displayed along with 21-bit background and foreground colors (RGB777 format). The use of internal dual ported memories means that the text controller does not consume any memory bandwidth from the processor.

The core is selected via a circuit select input.

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| --- | --- |
| **Address** | **Description** |
| $0000 to $1DEFF | text screen and attribute memory area, currently the controller only supports a 119.75kB memory |
| $1E000 to $1FFFF | character bitmap memory, currently the controller only supports a 8kx9 memory, which allows 1024 8x8 character bitmaps. |
| $1DF00 to $1DFFF | text controller register area |
|  |  |

Text and Attribute Memory Layout

|  |  |  |  |
| --- | --- | --- | --- |
| **63  58** | **57        37** | **36       16** | **9                0** |
| z-order | Fg Color | Bk Color | char code |

## Clocks

The text video display controller uses two clocks, a bus timing clock (clk\_i) and a video timing clock (dot\_clk\_i), which can be completely independent.

The core synchronizes the display relative to externally supplied horizontal and vertical synchronization signals.

## Register Description

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| --- | --- | --- | --- | --- |
| **Reg. No.** | **31                                                 0** | **R/W** | **Function** | **Description** |
| 0 | dddddddd -------- nnnnnnnn | RW | number of columns | nnn = number of columns  ddd = character output delay (default 3). |
| 1 | -------- nnnnnnnn | RW | number of row |  |
| 2 | ---- nnnnnnnnnnnn | W | window left | Text window position- pixels before the display starts, referenced to the hsync signal |
| 3 | ---- nnnnnnnnnnnn | W | window top | Text window position - scan lines down from the top of the screen referenced to the vsync signal |
| 4 | -------- --- nnnnn | W | max scanline | maximum scan line used to display chars  default 7. |
| 5 | -------- hhhh wwww | W | pixel size | pixel size in video clocks and scan lines  default is 1 (2 video clocks per pixel) and 1 (two video scan lines per pixel). |
| 6 | -------- -------r | W | reset state | This bit when set to 1 places the controller in a special reset mode. Default is 1. |
| 7 | nnnnnnn nnnnnnnn nnnnnnn | W | Transparent Color | color value that corresponds to a transparent background color |
| 8 | -------T TBB sssss | W | cursor start | sssss=scan line cursor display starts on   |  |  | | --- | --- | | **TT** | **= Cursor Type** | | 00 | Box | | 01 | Line | | 10 | Underscore | | 11 | Asterisk |  |  |  | | --- | --- | | **BB** | **= Cursor Blink Rate** | | 00 | no blink | | 01 | no display | | 10 | 1/16 frame rate (4 times per second) | | 11 | 1/32 frame rate (2 times per second) | |
| 9 | -------- --- eeeee | W | cursor end | scan line cursor display ends on |
| 10 | aaaaaaaa aaaaaaaa | W | display offset | starting address of the text screen in the display memory, defaults to zero |
| 11 | aaaaaaaa aaaaaaaa | W | cursor position | location of the cursor in the display memory |
| 12 | aaaaaaaa aaaaaaaa | R | light pen position | address of the light pen |
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## Graphics

The core may be used as a low-resolution graphics controller via the programmable character set. The characters can be programmed for block graphics. For instance, each character could be a two by two grid of pixels. Sixteen different characters would be required to represent all the different combinations. It is also possible to program characters to a three by three grid of pixels using all 512 programmable characters to represent every possible combination of on/off pixels. The default resolution is 56x29 or (392x232 pixels). This would allow approximately a 168x87 graphics display.

Graphics and text may be intermixed by allocating part of the programmable character set for a graphic arrray. For instance using 256 programmable characters a 128x128 bitmapped display can be created.

## Special Reset Mode

In special reset mode the core display memory is continuously updated according to the address on the address bus. This mode allows an echo of the system startup data to the display. This mode is disabled by writing a zero bit to register 6.

## Core Parameters

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| --- | --- | --- |
| **Name** | **Default Value** | **Description** |
| COLS | 84 | default number of columns of text |
| ROWS | 31 | default number of rows of text |
|  |  |  |

## Module Interface Description

rtfTextController

module rtfTextController(rst\_i, clk\_i, cs\_i, cyc\_i, stb\_i, ack\_o, we\_i, adr\_i, dat\_i, dat\_o, vclk, hsync, vsync, blank, border, rgbIn, rgbOut);

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| --- | --- |
| **System** | **Description** |
| rst\_i | This signal is normally connected to the system reset signal. It resets the text controller interface forcing it to the reset state. |
| clk\_i | This is usually connected to the system clock and is used as a base timing clock for I/O operations. |
| Slave Port | |
| cs\_i | circuit select input - selects the core for a read or write operation. |
| cyc\_i | indicates that a valid bus cycle is taking place. The core will not respond to the bus unless this signal is active. |
| stb\_i | This strobe signal also indicates that a valid bus cycle is taking place |
| ack\_o | This signal indicates that the core has processed the bus transaction (it is the logical and of cyc\_i and stb\_i). |
| we\_i | This signal is used to signify a write operation to the text controller. |
| adr\_i | This sixteen bit address bus is used to address one of text controllers's registers or internal memory. (Registers are described below). Registers respond to the address range $DFxx |
| dat\_i | This is the 32 bit data input bus to the text controller. |
| dat\_o | This is the 32 bit data output bus from the text controller. |
| Video Ports | |
| vclk | This input is the video clock input. Pixel timing is derived from it. |
| hsync | Horizontal sync. This input signal signals the start/end of a video scanline (end-of-line) |
| vsync | Vertical sync. This input signal indicates the end of the video frame. |
| blank | This input signal indicates that the display should be blanked. It is active during the video blanking period. |
| border | This input signal indicates that a border area is active. |
| rgbIn | This 24 bit input bus can be connected to an external RGB input. (The text controller may display on top of the external input). |
| rgbOut | This output signal bus contains the 24 bit RGB display data. |
| **Parameters** |  |
| ROWS | Use this parameter to specify the default number of text rows. |
| COLS | Use this parameter to specify the default number of text columns. |

# WISHBONE Compatibility Datasheet

The text controller core may be directly interfaced to a WISHBONE compatible bus.

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| --- | --- | --- |
| WISHBONE Datasheet  WISHBONE SoC Architecture Specification, Revision B.3 | | |
|  |  | |
| Description: | Specifications: | |
| General Description: | GFX\_TextController - Text mode video display controller | |
| Supported Cycles: | SLAVE, READ / WRITE  SLAVE, BLOCK READ / WRITE  SLAVE, RMW | |
| Data port, size:  Data port, granularity:  Data port, maximum operand size:  Data transfer ordering:  Data transfer sequencing | 64 bit  64 bit  64 bit  Little Endian  any (undefined) | |
| Clock frequency constraints: |  | |
| Supported signal list and cross reference to equivalent WISHBONE signals | Signal Name:  ack\_o  adr\_i(16:0)  clk\_i  dat\_i(63:0)  dat\_o(63:0)  cyc\_i  stb\_i  we\_i | WISHBONE Equiv.  ACK\_O  ADR\_I()  CLK\_I  DAT\_I()  DAT\_O()  CYC\_I  STB\_I  WE\_I |
| Special Requirements: | external sync generator | |