rfTextController

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## 

## Description

This is a text mode video display controller that supports color intended for use with a 64 or 32-bit bus. The controller uses several internal dual ported r/w memories to store text, text attributes and character bitmaps. The display memory is sixty-four bits wide. 512 different simultaneous characters may be displayed along with 21-bit background and foreground colors (RGB777 format). The use of internal dual ported memories means that the text controller does not consume any memory bandwidth from the processor.

The controller is programmable using only seven registers. Default values are established that should provide a reasonable display for 800x600 VGA mode.

The core respects byte lane selects and partial updates of registers are possible. This makes it possible for the core to have an optional 32-bit bus slave interface.

The core is selected via a circuit select input.

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| --- | --- |
| **Address** | **Description** |
| $0000 to $1DEFF | text screen and attribute memory area, currently the controller only supports a 119.75kB memory |
| $1E000 to $1FFFF | character bitmap memory, currently the controller only supports a 8kx9 memory, which allows 1024 8x8 character bitmaps. |
| $1DF00 to $1DFFF | text controller register area |
|  |  |

Text and Attribute Memory Layout

|  |  |  |  |
| --- | --- | --- | --- |
| **63  58** | **57        37** | **36       16** | **9                0** |
| z-order | Fg Color | Bk Color | char code |

## Clocks

The text video display controller uses two clocks, a bus timing clock (clk\_i) and a video timing clock (dot\_clk\_i), which can be completely independent.

The core synchronizes the display relative to externally supplied horizontal and vertical synchronization signals.

## Register Description

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Reg No. | Bit | R/W |  | Default Value |  |
| 00 | 7 – 0 | RW | Number of character columns | 64 |  |
| 15 - 8 | RW | Number of character row | 32 |  |
| 19 - 16 | RW | Character output delay | 7 |  |
| 31 – 20 | - | These bits are reserved |  |  |
| 43 – 32 | RW | Window left | 3956 |  |
| 47-44 | - | These bits are reserved |  |  |
| 59-48 | RW | Window top | 4058 |  |
| 63 – 60 | - | These bits are reserved |  |  |
| 08 | 4 – 0 | RW | Maximum scanline for character -1 | 7 |  |
| 7 - 5 | - | Reserved |  |  |
| 11 – 8 | RW | Pixel size width -1 (dot clocks) | 0 |  |
| 15 – 12 | RW | Pixel size height -1 (scan lines) | 0 |  |
| 24 | RW | Reset state (auto resets to zero) | 0 |  |
| 32 | RW | Controller enable | 1 |  |
| 40 | RW | Multi-color mode enable | 0 |  |
| 52 – 48 | RW | Y scroll | 0 |  |
| 60 – 56 | RW | X scroll | 0 |  |
| Other | - | reserved |  |  |
| 10 | 30 – 0 | RW | Color for transparent color ZRGB 4-9-9-9 | 511 |  |
| 62 – 32 | RW | Border color ZRGB 4-9-9-9 | FFBF2020h |  |
| 18 | 30 – 0 | RW | Tile color 1 (multi-color mode) | 0 |  |
| 62 - 32 | RW | Tile color 2 (multi-color mode) | 0 |  |
| 20 | 4 – 0 | RW | Cursor end | 31 |  |
| 7 – 5 | RW | Blink Control  |  |  | | --- | --- | | 00 | No blink | | 01 | No display | | 10 | 1/16 field rate | | 11 | 1/32 field rate | | 7 |  |
| 12 - 8 | RW | Cursor start | 0 |  |
| 15 - 14 | RW | Cursor image type | 0 |  |
| 47 - 32 | RW | Cursor location in memory | 3 |  |
| Other | - | reserved |  |  |
| 28 | 15 – 0 | RW | start address – index into display memory | 0 |  |
| Other | - | reserved |  |  |
| 30 | 15 – 0 | RW | Font address in char bitmap memory | 0 |  |
| Other | - | reserved |  |  |

## Graphics

The core may be used as a low-resolution graphics controller via the programmable character set. The characters can be programmed for block graphics. For instance, each character could be a two by two grid of pixels. Sixteen different characters would be required to represent all the different combinations. It is also possible to program characters to a three by three grid of pixels using all 512 programmable characters to represent every possible combination of on/off pixels. The default resolution is 64x32 or (448x256 pixels).

Graphics and text may be intermixed by allocating part of the programmable character set for a graphic arrray. For instance using 256 programmable characters a 128x128 bitmapped display can be created.

## Power On Screen Randomizer

The controller features an automatic screen randomizer that causes random characters to be displayed when the controller is reset. Video display memory is loaded with random values. This is a visual aid that the controller is working properly.

## Display Input / Output Bus

The controller inputs 40-bit ZRGB data and outputs 40-bit ZRGB video data. ZRGB is RGB data with plane number indicator bits tacked on. Four bits are reserved for the plane number and 12 bits are reserved for each RGB color component.

## Core Parameters

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| --- | --- | --- |
| **Name** | **Default Value** | **Description** |
| COLS | 64 | default number of columns of text |
| ROWS | 32 | default number of rows of text |
| BUSWID | 64 | Slave bus width may be 64 or 32 |

## Module Interface Description

rfTextController

module rfTextController(rst\_i, clk\_i, cs\_i, cyc\_i, stb\_i, ack\_o, wr\_i, sel\_i, adr\_i, dat\_i, dat\_o, dot\_clk\_i, hsync\_i, vsync\_i, blank\_i, border\_i, zrgb\_i, zrgb\_o, xonoff\_i);

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| --- | --- |
| **System** | **Description** |
| rst\_i | This signal is normally connected to the system reset signal. It resets the text controller interface forcing it to the reset state. |
| clk\_i | This is usually connected to the system clock and is used as a base timing clock for I/O operations. |
| Slave Port | |
| cs\_i | circuit select input - selects the core for a read or write operation. |
| cyc\_i | indicates that a valid bus cycle is taking place. The core will not respond to the bus unless this signal is active. |
| stb\_i | This strobe signal also indicates that a valid bus cycle is taking place |
| ack\_o | This signal indicates that the core has processed the bus transaction (it is the logical and of cyc\_i and stb\_i). |
| wr\_i | This signal is used to signify a write operation to the text controller. |
| sel\_i | These are byte lane selects Either 8 for 64 bit interface or 4 for 32-bit interface. |
| adr\_i | This seventeen bit address bus is used to address one of text controllers's registers or internal memory. (Registers are described above). Registers respond to the address range $1DFxx |
| dat\_i | This is the 64 or 32 bit data input bus to the text controller. |
| dat\_o | This is the 64 or 32 bit data output bus from the text controller. |
| Video Ports | |
| vclk | This input is the video clock input. Pixel timing is derived from it. |
| hsync | Horizontal sync. This input signal signals the start/end of a video scanline (end-of-line) |
| vsync | Vertical sync. This input signal indicates the end of the video frame. |
| blank | This input signal indicates that the display should be blanked. It is active during the video blanking period. |
| border | This input signal indicates that a border area is active. |
| zrgb\_i | This 40-bit input bus can be connected to an external RGB input. (The text controller may display on top of the external input). |
| zrgb\_o | This output signal bus contains the 40-bit RGB display data. |
| **Parameters** |  |
| ROWS | Use this parameter to specify the default number of text rows. |
| COLS | Use this parameter to specify the default number of text columns. |
| BUSWID | Specify the slave bus width using this parameter |

# WISHBONE Compatibility Datasheet

The text controller core may be directly interfaced to a WISHBONE compatible bus.

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| --- | --- | --- |
| WISHBONE Datasheet  WISHBONE SoC Architecture Specification, Revision B.3 | | |
|  |  | |
| Description: | Specifications: | |
| General Description: | rfTextController - Text mode video display controller | |
| Supported Cycles: | SLAVE, READ / WRITE  SLAVE, BLOCK READ / WRITE  SLAVE, RMW | |
| Data port, size:  Data port, granularity:  Data port, maximum operand size:  Data transfer ordering:  Data transfer sequencing | 64 or 32 bit (configurable)  8 bit byte lane selects  64 or 32 bit  Little Endian  any (undefined) | |
| Clock frequency constraints: | None, uses separate independent slave bus and video clocks. | |
| Supported signal list and cross reference to equivalent WISHBONE signals | Signal Name:  ack\_o  sel\_i(7:0)  adr\_i(16:0)  clk\_i  dat\_i(63:0)  dat\_o(63:0)  cyc\_i  stb\_i  wr\_i  rst\_i | WISHBONE Equiv.  ACK\_O  SEL\_I()  ADR\_I()  CLK\_I  DAT\_I()  DAT\_O()  CYC\_I  STB\_I  WE\_I  RST\_I |
| Special Requirements: | external sync generator | |