## WISHBONE Compatibility Datasheet

The rtfBitmapController5 core may be directly interfaced to a WISHBONE compatible bus.

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| WISHBONE Datasheet  WISHBONE SoC Architecture Specification, Revision B.3 | | |
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| Description: | Specifications: | |
| General Description: | Frame Buffer Display / Bitmap controller | |
| Supported Cycles: | SLAVE, READ / WRITE  SLAVE, BLOCK READ / WRITE  SLAVE, RMW | |
| Data port, size:  Data port, granularity:  Data port, maximum operand size:  Data transfer ordering:  Data transfer sequencing | 64 bit (128/64 or 32 for master)  64 bit (some registers will respect greater granularity)  64 bit  Little Endian  any (undefined) | |
| Clock frequency constraints: |  | |
| Supported signal list and cross reference to equivalent WISHBONE signals  (Slave) | Signal Name:  rst\_i  S\_ack\_o  S\_adr\_i(11:0)  S\_clk\_i  S\_dat\_i(63:0)  S\_dat\_o(63:0)  S\_cyc\_i  S\_stb\_i  S\_we\_i  S\_sel\_i(7:0) | WISHBONE Equiv.  RST\_I  ACK\_O  ADR\_I()  CLK\_I  DAT\_I()  DAT\_O()  CYC\_I  STB\_I  WE\_I  SEL\_I |
| Data port, size:  Data port, granularity:  Data port, maximum operand size:  Data transfer ordering:  Data transfer sequencing | Configurable (128/64 or 32 for master)  128/64/ or 32 bit  128/64 or 32 bit  Little Endian  any (undefined) | |
| MASTER | Signal Name:  rst\_i  m\_ack\_i  m\_adr\_o(31:0)  m\_clk\_i  m\_dat\_i(63:0)  m\_dat\_o(63:0)  m\_cyc\_o  m\_stb\_o  m\_we\_o  m\_sel\_o(7:0) | WISHBONE Equiv.  RST\_I  ACK\_I  ADR\_O  CLK\_I  DAT\_I  DAT\_O  CYC\_O  STB\_O  WE\_O  SEL\_O |
| Special Requirements: |  | |