**WISHBONE Compatibility Datasheet**

The rtfSpriteController2 core may be directly interfaced to a WISHBONE compatible bus.

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| WISHBONE Datasheet  WISHBONE SoC Architecture Specification, Revision B.3 | | |
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| Description: | Specifications: | |
| General Description: | Sprite / Hardware Cursor Controller | |
| Supported Cycles: | SLAVE, READ / WRITE  SLAVE, BLOCK READ / WRITE  SLAVE, RMW  MASTER, READ | |
| **SLAVE**  Data port, size:  Data port, granularity:  Data port, maximum operand size:  Data transfer ordering:  Data transfer sequencing | 64 bit  64 bit (varies depending on register)  64 bit  Little Endian  any (undefined) | |
| **MASTER**  Data port, size:  Data port, granularity:  Data port, maximum operand size:  Data transfer ordering:  Data transfer sequencing | 64 bit  64 bit  64 bit  Little Endian  any (undefined) | |
| Clock frequency constraints: | m\_clk\_i should be the same or faster than clk\_i | |
| **SLAVE**  Supported signal list and cross reference to equivalent WISHBONE signals | Signal Name:  rst\_i  ack\_o  adr\_i(31:0)  clk\_i  dat\_i(63:0)  dat\_o(63:0)  cyc\_i  stb\_i  we\_i  ack\_i  clk\_i  sel\_i(7:0) | WISHBONE Equiv.  RST\_I  ACK\_O  ADR\_I()  CLK\_I  DAT\_I()  DAT\_O()  CYC\_I  STB\_I  WE\_I   ACK\_I  CLK\_I  SEL\_I |
| **MASTER**  Supported signal list and cross reference to equivalent WISHBONE signals | Signal Name:  rst\_i  m\_ack\_i  m\_adr\_o(31:0)  m\_clk\_i  m\_dat\_i(63:0)  m\_cyc\_o  m\_stb\_o  m\_ack\_i | WISHBONE Equiv.  RST\_I  ACK\_I  ADR\_O()  CLK\_I  DAT\_I()  CYC\_O  STB\_O   ACK\_I |
| Special Requirements: |  | |