Register-Register Encoding (R2)

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 47 42 | 41 36 | 35 29 | 28 22 | 21 15 | 14 8 | 7 6 | 5 0 |
| Func6 | ~6 | Mask7 | Rb7 | Ra7 | Rt7 | Fmt2 | 46 |

Register-Immediate Encoding (RI)

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 47 37 | 36 | 35 29 | 28 22 | 21 15 | 14 8 | 7 6 | 5 0 |
| Imm17..7 | S | Mask7 | Imm6..0 | Ra7 | Rt7 | Fmt2 | Opcode6 |

Register-Immediate High Encoding (RIH)

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 4743 | 44 37 | 36 | 35 29 | 28 22 | 21 15 | 14 8 | 7 6 | 5 0 |
| ~3 | Imm31..24 | S | Mask6 | Imm23..17 | Ra7 | Rt7 | Fmt2 | Opcode6 |

|  |  |  |  |
| --- | --- | --- | --- |
| Format2 | Rb6 | Ra6 | Rt6 |
| 00 | Scalar | Scalar | Scalar |
| 01 | Scalar | Vector | Vector |
| 10 | Vector | Vector | Vector |
| 11 | reserved |  |  |

|  |  |  |  |
| --- | --- | --- | --- |
| S | Immediate Swap | | |
| 0 | Immed. | Ra | Rt |
| 1 | Rb | Immed. | Rt |

|  |  |
| --- | --- |
| Register Spec Field | |
| 6 | 5 0 |
| Invert | Regno |

The invert bit inverts or negates a register depending on the instruction.

Instructions are a fixed 48 bits in size.

The masking register spec is present in all instructions. This makes it possible to use a two-bit format field in the instruction.

Branch Instruction Format

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 47 37 | 36 32 | 31 29 | 28 22 | 21 15 | 14 8 | 7 6 | 5 0 |
| Disp17..7 | ~5 | Cond3 | Disp6..0 | Rb7 | Ra7 | Fmt2 | Opcode6 |

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 47 37 | 36 | 3532 | 31 29 | 28 22 | 21 15 | 14 8 | 7 6 | 5 0 |
| Disp17..7 | S | Im4 | Cond3 | Disp6..0 | Imm6..0 | Ra7 | Fmt2 | Opcode6 |

bra / bsr format

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 47 37 | 36 | 35 29 | 28 22 | 21 15 | 14 8 | 7 6 | 5 0 |
| Disp17..7 | ~ | Disp24..18 | Disp6..0 | Disp31..25 | Rt7 | ~2 | 576 |

jal / ret format

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 47 37 | 36 | 35 29 | 28 22 | 21 15 | 14 8 | 7 6 | 5 0 |
| Imm17..7 | ~ | Imm24..18 | Imm6..0 | Ra7 | Rt7 | Op2 | 586 |

|  |  |  |
| --- | --- | --- |
| Fmt2 | Operands |  |
| 0 | Register – Register |  |
| 1 | Register - Immediate |  |
| 2,3 | reserved |  |

|  |  |  |
| --- | --- | --- |
| Cond | Mnemonic | Comment |
| 0 | beq |  |
| 1 | bne |  |
| 2 | bgt / blt | Swap operands to switch between bgt and blt |
| 3 | bge / ble |  |
| 4 | bgtu /bltu |  |
| 5 | bgeu / bleu |  |
| 6 | bbc / bbs | Invert register to check for bits set |
| 7 | reserved |  |

|  |  |  |
| --- | --- | --- |
| Op2 | Mnemonic | Operation |
| 0 | JAL | Jump and link |
| 1 | RTD | Return and deallocate |
| 2 | RTE | Return from exception |
| 3 | JALI | Jump and link indirect |

|  |  |  |
| --- | --- | --- |
| Opcode6/Func6 | Mnemonic | Description |
| 00 | or / nor /orc / norc | Bitwise or |
| 01 | and / nand / andc / nandc | Bitwise and |
| 02 | syscall | System call |
| 03 | Xor / xnor / xorc / xnorc | Bitwise exclusive or |
| 05 | add / sub |  |
| 06 |  |  |
| 07 | mul / nmul |  |
| 08 | mulhu |  |
| 09 | asr | Arithmetic shift right |
| 10 | lsr | Logical shift right |
| 11 | asl | Arithmetic shift left |
| 12 | clz / clo |  |
| 13 | shuffle |  |
| 14 | ctz / cto |  |
| 16 | ceq / cne |  |
| 17 |  |  |
| 18 | cgt / cle |  |
| 19 | cge / clt |  |
| 20 |  |  |
| 21 |  |  |
| 22 | cgtu / cleu |  |
| 23 | cgeu / cltu |  |
| 24 |  |  |
| 25 |  |  |
| 26 | getlane |  |
| 27 | ftoi | Float to integer |
| 28 | reciprocal |  |
| 29 | sextb | Sign extend byte |
| 30 | sextw | Sign extend wyde |
| 31 | mulh |  |
| 32 | Fadd fsub |  |
| 33 |  |  |
| 34 | fmul |  |
| 35 |  |  |
| 42 | itof | Integer to float |
| 43 |  |  |
| 44 | fcgt |  |
| 45 | fcge |  |
| 46 | fclt |  |
| 47 | fcle |  |
| 48 | fceq |  |
| 49 | fcne |  |
| 52 | orh | Or high order bits |
| 53 | andh | Bitwise and high order bits |
| 55 | xorh | Exclusive or high order bits |
| 56 | addh | Add high order bits |
| 57 | bra / bsr | Branch, Branch to subroutine |
| 58 | jal | Jump and link |
| 62 | break |  |
|  |  |  |