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Reimagining Heterogeneous Computing: a Functional Instruction Set Architecture (F-ISA) Computing Model

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Heterogeneous Computing is an architectural approach where there are multiple cores which may or may not share the same design and ISA. This idea of heterogeneous computing is beginning to emerge in cloud and mobile technology, to combat the power and memory wall, but the paper suggests that Heterogeneous Computing can only be the solution if there is a radical shift in the instruction set architectures employed. The proposed idea is to store the instructions (referred to from here as "functions") which the core will call alongside the data, which may be stored in various memory spaces. A matrix and its functions could be stored in one memory structure, and a list and it's functions in another dissimilar memory structure. This has obvious costs and complexity when compared to a system with axiomatic numeric types and generic adder circuits, for example. The proposed improvement is to add abstractions to the ISA of such a system. Functions which are present in the hardware, such as an adder, would unfold to become that build-in instruction; functions which are not present would be represented symbolically and would unfold until those instructions were pointed at, which would be present in the memory space associated with the data. This article simply introduces the idea as a possible way forward for Heterogeneous Computing architectures, but with suggestions that such a change would herald an era of improved performance over traditional approaches in terms of power usage and continued scalability in cloud computing. The hope is that this heterogeneous approach would make better use of cores and reduce phenomena related to power consumption in our current homogeneous chip design (i.e. Dark silicon).

Reference:

Daniel Nemirovsky et. al., "Reimagining Heterogeneous Computing: a Functional Instruction Set Architecture (F-ISA) Computing Model", *IEEE Micro*, vol. PP, is. 99, Nov. 2015.