CE312_TP2_Chognot_Lafage

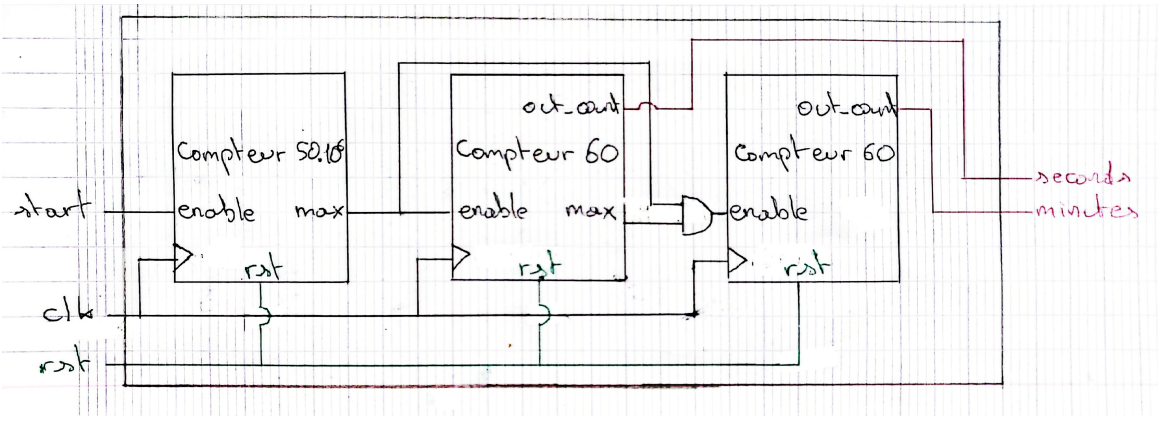
Authors : Gabin CHOGNOT, Robin LAFAGE

▼ Architecture of the chronometer

The clock counter is a counter modulo 50 000 000 as the system clock is at $50MHz$, the other two are the counters of the seconds and the minutes, and are counters modulo 60.

The *max* of the clock counter is the *enable* of the second counter, as a second is only counted each time 50 000 000 are counted. And the *enable* of the third counter is the result of a *and gate* between the *max* of the two other counters, as you only add a minute when you have 59 seconds and 50 000 000 clock count (the end of the last second).

We do not represent the *out_count* of the first counter, and the *max* of the third one, as they are not useful here.



Schematic of the architecture of the chronometer

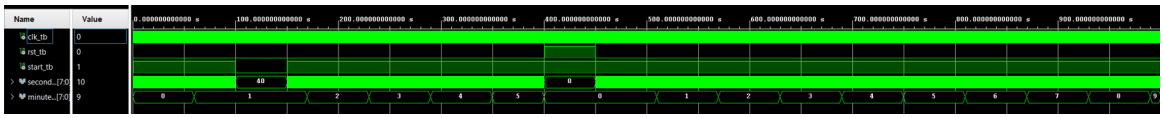
We expect 44 flip-flops, as we need 26 flip-flop to represent the 50 000 000 counter ($2^{26} = 67108864$), 8 flip-flop per counter of the minutes and the seconds, so 16 flip-flops, and 2 flip-flops for the 2 *max.* So 26+8+8+2=44 flip-flops.

We indeed have this result with the synthesis of the chronometer.

▼ Codes and simulation

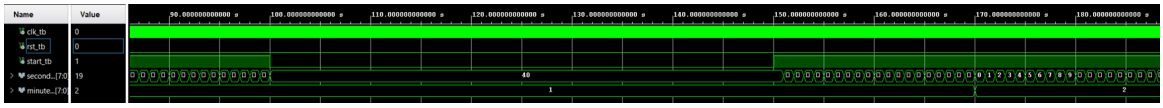
→ The code chronometer.vhd and the test_bench.vhd are in annexes.

If we run the simulation, we have the following output :

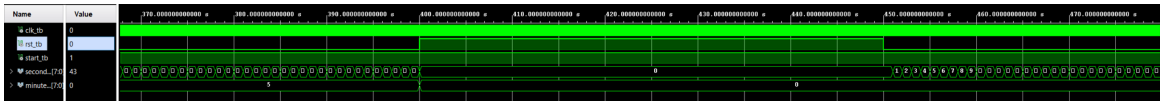


Global view of the behaviour of the chronometer.

We see that the program indeed counts the minutes, stop to count when *start=0*, and reset when *reset=1*. In details :

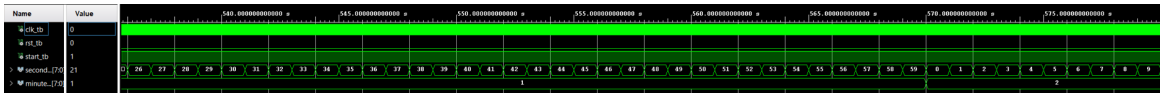


Zoom on the behaviour of the chronometer when *start=0.*



Zoom on the behaviour of the chronometer when reset=*1.*

If we zoom in, we see that the seconds does count from 0 to 59, then a minute is increased by one :



Zoom on the behaviour of the second count, and the increasing by one of a minute.