

POKHARA UNIVERSITY

Level: Bachelor
Programme: BE
Course: Logic Circuits

Semester: Fall

Year : 2020
Full Marks: 100
Pass Marks: 45
Time : 3 hrs.

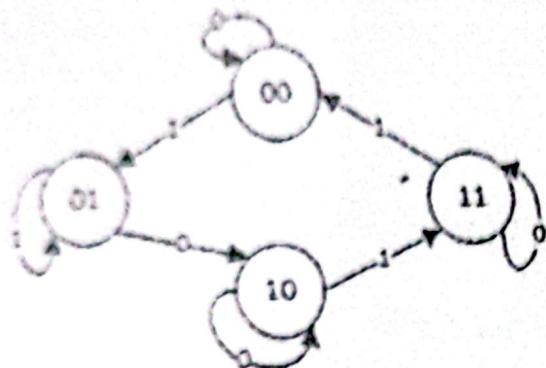
Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

- i) Define digital system. Why do you prefer Digital systems against its analog counterpart? Explain. 5
- ii) Perform the following subtraction using (r-1)'s complement:
i. $(111001)_2 - (11011)_2$
ii. $(2321)_{10} - (8301)_{10}$
- iii) What is weighted and non-weighted code? Why Gray code is called reflected code? 5
- a) Discuss the significance of NAND & NOR gate in Logic circuit. Prove that NAND and NOR gates are the Universal gate. 7
- b) For the given logic expression:
 $F(A,B,C,D) = A'B + BD + A'D' + B'D'$
i) Make a truthtable
ii) Simplify it using K map
iii) Realize the simplified expression using NOR gate (2 inputs) only. 8
-) Use K-map scheme to obtain the minimized SOP expression for the given function $f(A, B, C, D) = \sum m(1, 5, 8, 12) + d(3, 7, 10, 11, 14, 15)$ and implement the result using NOR gates only. 8
-) What are parity bits? Design 3-bit parity generator and 4-bit parity checker circuit for even parity. 7
-) Design a combinational circuit using PLD device as ROM which is used to find square of 3 bit numbers. 8
-) Design and implement full adder circuit using decoder. 7
-) What are the significance of a flip-flop? Explain J-K flip-flop along with its logic diagram, truth table and excitation table. 7

- b) Design synchronous sequential circuit for the given state diagram using T flip-flop.



6. a) Design and implement Mod-5 counter using JK flip flop.
 b) Design an arithmetic circuit implementing given functions. Where A and B are 4-bit binary input lines.

S_1	S_0	C_{in}	Output (F)
0	0	0	A
0	0	1	$A+1$
0	1	0	$A+B$
0	1	1	$A+B+1$
1	0	0	$A+\bar{B}$
1	0	1	$A-B$
1	1	0	$A-1$
1	1	1	\bar{A}

7. Write short notes on: (Any two)

- a) Johnson Counter
 b) Tristate Logic
 c) 4-Bit Nibble Adder

POKHARA UNIVERSITY

Level: Bachelor

Semester - Spring

Year 2020

Program: BE

Full Marks: 70

Course: Logic Circuits

Pass Marks: 31.5

Time: 2 hrs

Candidates are required to answer in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

Section - A: (5×10=50)

- Q. N. 1** Which system do you prefer, analog or digital? Justify with a real world example. 5+5
Do the following as indicated(@@@ is the last two digit of your symbol number):
I. $(@@@5 \text{ DD})_{16} = (\dots)_3$
II. $(F@@@2)_{16} = (\dots)_7$

OR

5+5

Simplify the given function F and Don't care condition D in SOP and POS form and draw the logic diagram using

- I. NAND gate only
II. Nor gate only

$$F = \sum(1,4,5,6,12,14,15), D = \sum(11,13)$$

- Q. N. 2** Explain with suitable example how to overcome Half Adder (HA) drawbacks using Full Adder (FA). Is it possible to add & subtract n-bit data using full adder?

- Q. N. 3** What are the major difference between ROM and PLA? Implement the given function using multiplexer (suppose your own data and symbols if necessary)
 $F = (\text{set of digits of your symbol number})$

[For example, if your symbol number is 15070195 then $F = (0,1,5,7,9)$ i.e you should omit the repeated digits of your symbol number.]

- Q. N. 4** Differentiate between combinational circuit and sequential circuit. What is the problem found in RS flip-flop? Explain how it is solved in JK flip-flop.

- Q. N. 5** What are shift registers? Explain the operation of SISO and PISO shift register. Take data 1101

Section - B: (1×20=20)

- Q. N. 6** If you were assign a job for design a simple processor can be used in educational purposes. It consists two units only. They are arithmetic unit and logic unit. Starting with basic function design a complete circuit diagram for

- a) Arithmetic Circuits
b) Logic Circuits

POKHARA UNIVERSITY

Level: Bachelor

Semester - Spring

Year 2020

Program: BE

Full Marks: 70

Course: Logic Circuits

Pass Marks: 35

Time: 2 hrs

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Attempt all the questions.

Section - A: (5×10=50)

- Q. N. 1 Which system do you prefer, analog or digital? Justify with a real world example. 5+5
Do the following as indicated(@@@ is the last two digit of your symbol number)

- I. $(@@@5.DD)_{16} = (\dots)_5$
II. $(F@@@2)_{16} = (\dots)_7$

OR

5+5

Simplify the given function F and Don't care condition D in SOP and POS form
and draw the logic diagram using

- I. NAND gate only
II. Nor gate only
 $F = \sum(1,4,5,6,12,14,15), D = \sum(11,13)$

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- Q. N. 3 What are the major difference between ROM and PLA? Implement the given function using multiplexer (suppose your own data and symbols if necessary).

$F = (\text{set of digits of your symbol number})$

[For example, if your symbol number is 15070195 then $F = (0,1,5,7,9)$ i.e you should omit the repeated digits of your symbol number.]

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Take data 1101

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- Q. N. 6 If you were assign a job for design a simple processor can be used in educational purposes. It consists two units only. They are arithmetic unit and logic unit. Starting with basic function design a complete circuit diagram for

- a) Arithmetic Circuits
b) Logic Circuits

POKHARA UNIVERSITY

Level: Bachelor

Semester: Fall

Year : 2021

Programme: BE

Full Marks: 100

Course: Logic Circuits

Pass Marks: 45

Time : 3 hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

-) Explain briefly about 7
 - (i) instruction code,
 - (ii) Hexadecimal code, and
 - (iii) Alphanumeric code.
-) Perform the conversions as indicated (any two). 4
 - i. $(556)_4 = (?)_{\text{Excess-3}}$
 - ii. $(786)_{10} = (?)_{\text{BCD}}$
 - iii. $(437.126)_8 = (?)_2$
-) Using (r-1)'s complement perform subtraction: $(1010100)_2 - (1000100)_2$. 4
-) Convert the following to the other canonical form. 8
 - i. $F(x,y,z) = \Sigma(1,5,7)$
 - ii. $F(A, B, C, D) = \Sigma(1, 2, 7, 11, 12, 14)$
 - iii. $F(x,y,z) = \Pi(0, 4, 6, 7)$
 - iv. $F(A, B, C, D) = \Pi(0, 1, 2, 3, 4, 6, 12)$

Design a logic circuit to implement the Boolean function. 7

$$F(A,B,C,D) = \Sigma(1,3,4,5,7,9,13,14,15)$$

$$D(A,B,C,D) = \sum(0,2,8)$$

- i. Sum of product
- ii. Implement with NAND-NAND gate only.

Design a combinational circuit with three inputs and one output. 8

The output is 1 when binary value of the inputs is less than or equal to 3. The output is 0 otherwise

The output is 1 when the binary value of the inputs is an odd number.

POKHARA UNIVERSITY

Level: Bachelor

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Full Marks: 100

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Pass Marks: 45

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Attempt all the questions.

Explain briefly about 7

- i) instruction code,
- ii) Hexadecimal code, and
- iii) Alphanumeric code.

Perform the conversions as indicated (any two). 4

- i. $(556)_4 = (?)_{\text{Excess-3}}$
- ii. $(786)_{10} = (?)_{\text{BCD}}$
- iii. $(437.126)_8 = (?)_2$

Using (r-1)'s complement perform subtraction: $(1010100)_2 - 1000100)_2$. 4

Convert the following to the other canonical form. 8

$$F(x,y,z) = \Sigma(1,5,7)$$

$$F(A, B, C, D) = \Sigma(1, 2, 7, 11, 12, 14)$$

$$F(x,y,z) = \Pi(0, 4, 6, 7)$$

$$F(A, B, C, D) = \Pi(0, 1, 2, 3, 4, 6, 12)$$

Design a logic circuit to implement the Boolean function. 7

$$(A,B,C,D) = \Sigma(1,3,4,5,7,9,13,14,15)$$

$$(A,B,C,D) = \Sigma(0,2,8)$$

- i. Sum of product
- ii. Implement with NAND-NAND gate only.

Design a combinational circuit with three inputs and one output. 8

The output is 1 when binary value of the inputs is less than or equal to 3. The output is 0 otherwise

The output is 1 when the binary value of the inputs is an odd number.

- iii. The output is 1 when the binary value of the inputs is an even number.

OR

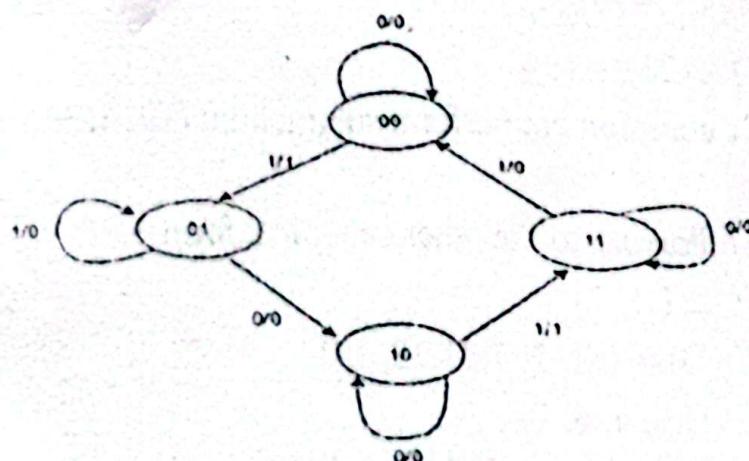
Design a combinational logic circuit with 3 inputs that provide 1 output when exactly two variables are 1.

- b) Construct 8×1 Mux using 4×1 MUX & explain with truth table.
 4. a) Implement the following three Boolean function with a PLA
 $F_1 = \sum(0,1,3) F_2 = \sum(1,3,4,7) F_3 = \sum(0,2,5,6)$

OR

Design a BCD to excess -3 code converter and implement using suitable PLA.

- b) Explain operation of JK Flip-flop with its logic diagram, truth table, excitation table. Why JK flip-flop is preferred over RS flip-flop?
 5. a) Realize the following state diagram into a circuit using T flip-flop. How can you replace T flip-flops of your final circuit with JK flipflops?



- b) Design a circuit for synchronous MOD - 7 counter.
 6. a) What are shift registers? Explain Parallel in Parallel out (PIPO) and Serial in Parallel out (SIPO) shift register with diagrams.
 b) Design an ALU which performs eight arithmetic and four logical operations.
 7. Write short notes on: (Any two)
 a) Johnson (Switch tail ring) Counter
 b) State reduction.
 c) Grey code as reflected code.

POKHARA UNIVERSITY

Level: Bachelor	Semester: Spring	Year : 2021
Programme: BE		Full Marks: 100
Course: Logic Circuits		Pass Marks: 45

Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

"Logical computation is either based on digital system or analog system", today which one is better and why. 5

Perform the conversion as indicated (any two). 5

i. $(73)_8 = (\quad)_{\text{Excess-3}}$

ii. $(196)_{10} = (\quad)_{2421}$

iii. $(CAB)_{16} = (\quad)_2$

Use 2's complement to subtract the following: 5

i. $(10101)_2 - (10111)_2$

ii. $(457)_{10} - (876)_{10}$

iii. $(378)_{BCD} - (256)_{BCD}$

Simplify the following Boolean functions to a minimum number of literals. 8

a. $(x' + y)(x + y')$

b. $x'y'z + x'y + xyz'$

c. $(x + y)'(x' + y')$

d. $x(wz' + wz) + xy$

A Boolean function is given by $F(A,B,C,D) = \sum(1,2,7,9,10,13,14)$ and don't care condition $d(A,B,C,D) = \sum(0,3,6,11)$. Implement it using NAND gate only. 7

Design a combinational circuit that converts a decimal digit from BCD to Excess 3 code. 8

Derive a PLA program table and circuit to implement the functions
 $F_1(A,B,C) = \sum(1,3,5,7)$ 7

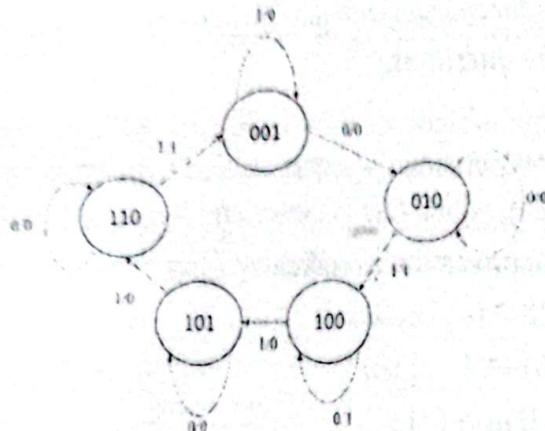
$$F_2(A,B,C) = \sum(0,2,4,6)$$

4. a) Implement the Boolean function $F(A,B,C, D) = \sum(0,1,3,4,7,11, 15)$ using: (i) 8x1 MUX, (ii) 16x1 MUX
 b) Implement the full adder circuit using 3x8 decoder.

OR

What is register? Explain the different type of shift register in brief.

5. a) Design a sequential circuit corresponding to the given state diagram.



- b) Explain operation of RS Flip-flop with its logic diagram, truth table, excitation table.

OR

Design a MOD-8 asynchronous up counter by using J-K Flip Flop.

6. a) Differentiate between synchronous and Ripple Counter. Design a 2-bit synchronous UP counter by using J.K flip-flop.
 b) Design a binary adder/subtractor circuit with one selection variable S and two inputs A and B. For S = 0, the circuit need to perform addition i.e. (A+B) and for S = 1, the circuit must perform subtraction i.e. (A - B) by taking 2's complement of B.

7. Write short notes on: (Any two)

- a) Read only memory (ROM)
- b) Output hazard races
- c) Ring counter

POKHARA UNIVERSITY

Level: Bachelor

Semester: Fall

Year : 2022

Programme: BE

Full Marks: 100

Course: Logic Circuits

Pass Marks: 45

Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

- a) Define Signal. Differentiate between analog and digital signals. 5
- b) If $A = (11011011)_2$ and $B = (1001101)_2$ then perform $A-B$ and $B-A$ using 2's complement method. 5
- c) Perform the following conversion as indicated 5
 - i. $(346)_8 = (\quad)_{\text{excess-3}}$
 - ii. $(BDA.DE7)_{16} = (\quad)_8$
 - iii. $(101111)_{\text{gray}} = (\quad)_{10}$
- a) Why are NAND and NOR gates called universal gates ? Realize XOR gate using NAND gate. 8
- b) Define literal. Prove the De-Morgan's first and second theorem. 7
- a) Discuss the role of K-map in logic circuit. Minimize the expression mentioned below using K-Map Design a Logic circuit for minimal expression using 8
 - i. Basic gate.
 - ii. NAND gate.

$$F(A,B,C,D,E) = \Sigma(0,1,6,7,8,9,21,22,23,29,31)$$

- b) Design 3 bit even parity generator and parity checker with circuit diagram. Assume the input message bits be x, y and z . 7
- a) A combinational circuit is defined by the function, 8

$$F_1(A, B, C) = \sum(3, 5, 6, 7)$$

$$F_2(A, B, C) = \sum(0, 2, 4, 7) \text{ & } F_3(A, B, C) = \sum(1, 2, 4, 6)$$
 implement by using PLA with program table.
- b) Differentiate between Flip-flop and Latch. Explain the operation of clocked J-K flip-flop with the help of its logic diagram, characteristic table and characteristic equation. 7

5. a) What is shift register? Differentiate between serial in serial out register and serial in Parallel out register with associated diagrams.
b) Design a 3-bit Asynchronous up counter using J-K flip flop.
6. a) Differentiate between synchronous and asynchronous counters
Design and implement MOD 6 synchronous counter using J-K flip flop.
b) Design Arithmetic Logic Unit (ALU) that performs eight Arithmetic operations and four different logical operations.
7. Write short notes on: (Any two)
 - a) Self Complementing Code
 - b) Ring counter
 - c) Processor Unit

POKHARA UNIVERSITY

Level: Bachelor

Semester: Spring

Year : 2015

Programme: BE

Full Marks: 100

Course: Logic Circuit

Pass Marks: 45

Time : 3 hrs.

Candidates are required to give their answers in their own words as far as practicable.

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Attempt all the questions.

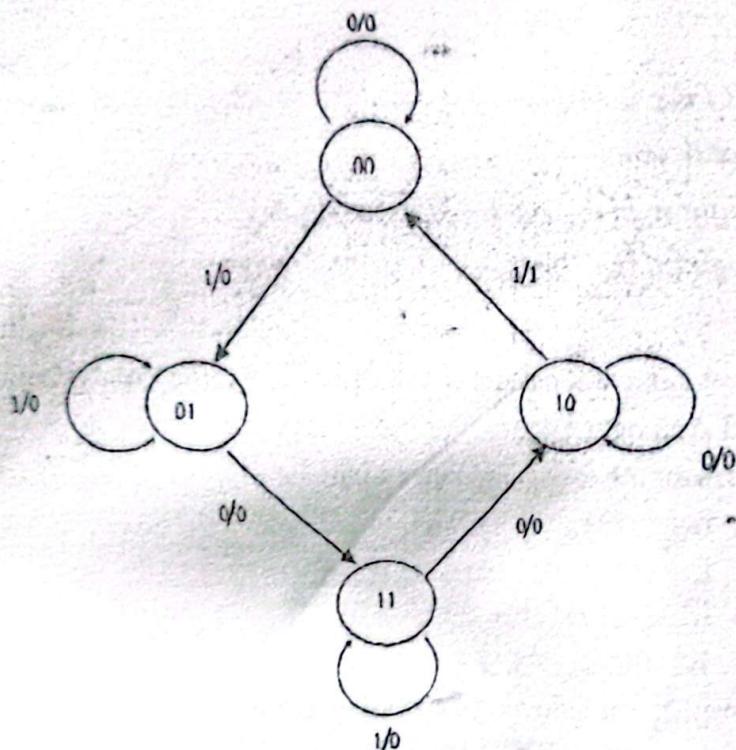
- . a) How can we represent the information? Differentiate between Digital and Analogue system. 7
- . b) Perform the following conversion. 8
 - i. $(573)_{10} = (\)_{\text{excess-3}}$
 - ii. $(842)_{10} = (\)_{2421}$
 - iii. $(1010111)_{\text{GRAY}} = (\)_2$
 - iv. $(FAB)_{16} = (\)_8$
- . a) Simplify the following expression using Boolean algebra 5
 - i. $(AB' + AB'C') + A(B' + AB')$
 - ii. $[(BC' + A'D)(AB' + C'D)]$
- . b) Simplify the Boolean function F and don't care conditions din(1) SOP (2) POS and (3) draw NAND-NAND equivalent logic. Given: 5
 - i. $F = A'B'D' + A'CD + A'BC$
 - ii. $d = A'BC'D + ACD + AB'D'$
- . c) A Boolean function is given by $F(A,B,C,D) = \sum(3,4,6,8,10,12,14)$ and don't care condition $d(A,B,C,D) = \sum(0,2,8)$. Simplify it using K-Map and implement using NAND gate only. 5
- . a) Design a combinational circuit that converts a decimal digit from the 2421 code to 84-2-1 code to binary. 8
- . b) Design a circuit for 4 bit full Subtract adder. 7
- . a) Design a comparator circuit that compared two 4 bit numbers. The two numbers being A and B. It is required to obtain three possible outcomes. i.e., $A > B$, $A < B$ and $A = B$. 8

b) Implement the following with appropriate MUX:

i. $F(A,B,C) = \sum (1,3,5,6)$

ii. $F(A,B,C,D) = \sum (0,1,3,4,8,9,15)$

5. a) Design a sequential circuit corresponding to the given state diagram using J-K flip flop.



b) Design a counter with the following binary sequence, 0, 1, 3, 2, 6, 4, 5, 7 and repeat. Use T flip flop.

6. a) Design an adder/subtractor circuit with one selection variable S and two inputs A and B. When $S=0$ the circuit performs $A+B$ when $S=1$ the circuit performs $A-B$ by taking the 2's compliment of B.
b) Design a 4-bit arithmetic circuit which performs eight different arithmetic operations.

c) Write short notes on: (Any two)

- a) Magnitude comparator
b) Universality of NAND and NOR gates
c) Output Hazard Races

POKHARA UNIVERSITY

Level: Bachelor
 Programme: BE
 Course: Logic Circuits

Semester: Fall

Year : 2016
 Full Marks: 100
 Pass Marks: 45
 Time : 3hrs.

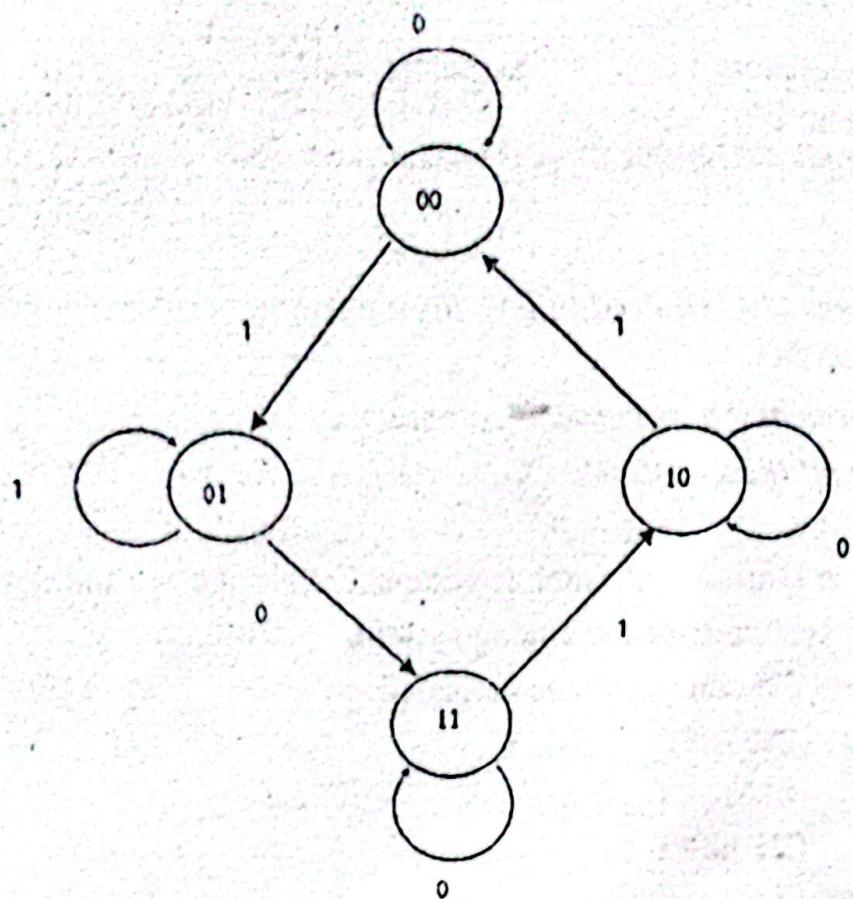
Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

- | | |
|--|---|
| a) What is Digital and Analog systems? Also list out the advantages of digital system over the analog system. | 7 |
| b) Perform the conversion as indicated | 8 |
| i. $(243)_6 = ()_{\text{Excess-3}}$ | |
| ii. $(816)_{10} = ()_{2421}$ | |
| iii. $(BE)_{16} = ()_2$ | |
| iv. $(777)_x = (212)_8$ | |
| a) Implement XNOR gate using only NAND gates and XOR gate using NOR gate only. | 7 |
| b) Define Literal & term. Find Canonical SOP for this expression $F=ac+ab+bc$. | 8 |
| a) Design a combinational circuit that converts a decimal digit from the 2421 code to BCD. | 8 |
| b) A Boolean function is given: $F(w,x,y,z)=\Sigma(1,4,5,6,12,14,15)$ and don't care condition $d(w,x,y,z)=\Sigma(1011)$. Simplify it using K-map with logic gate implementation. | 7 |
| a) Design a comparator circuit that compared two 4 bit numbers. The two numbers being A and B. It is required to obtain three possible outcomes. i.e . $A>B$, $A<B$ and $A= B$. | 8 |
| b) Realize the following state diagram into a circuit using T- flip-flop. | 7 |

नेपाली विद्यालय एवं प्रौद्योगिकी संकाय
 काठमाडौं, नेपाल ९८४९५६५५५२
 NCIT College



5. a) What are major 5 differences between synchronous and asynchronous counters? Design a 4-bit up-down binary counter.
- b) What is counter? Differentiate between serial in serial out register and parallel in serial out register with associated diagrams.
6. Design an arithmetic circuit with two selection variables, s_1 and s_0 , that generates the following arithmetic operations. Draw the logic diagram of one typical stage.

s_1	s_0	$C_{in} = 0$	$C_{in} = 1$
0	0	$F = A+B$	$F = A+B+1$
0	1	$F = A$	$F = A+1$
1	0	$F = B'$	$F = B'+1$
1	1	$F = A+B'$	$F = A+B'+1$

7. Write short notes on: (Any two)

- a) Shift register
 b) D-flip flop
 c) PLA

POKHARA UNIVERSITY

Level: Bachelor
Programme: BE
Course: Logic Circuits

Semester: Spring

Year : 2016
Full Marks: 100
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Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

- a) Define Analog and Digital System. Why digital systems are preferred over Analog system. 5
- b) Convert the following numbers from the given base to the other bases 1+2+2 as indicated
 - i. $(11001.11)_2 = (\)_8$
 - ii. $(5FE.DD)_{16} = (\)_{10}$
 - iii. $(777)_8 = (\)_{16}$
- c) Perform the subtraction with the following Binary number using 1's Complement
 - i. $1010100 - 1000100$
 - ii. $1000100 - 1010100$
- a) State and Prove De-Morgan's Theorem. Briefly explain the factors to be considered while constructing the Logic Gates. 8
- b) What is don't care condition? Simplify given function using K-map and implement it in a circuit.

 $F(W,X,Y,Z) = \Sigma(1,4,5,6,12,14,15)$ and don't care condition
 $D(W,X,Y,Z) = \Sigma(11,13)$. 7
- a) Design a combinational circuit that accepts a 4 bit number as input and generates the output binary number equal to the 2's complement of input number. 8

OR

Design a circuit for 3-bit parity generation and 4-bit parity checker using even parity.

- b) Explain in detail about synchronous Up/Down counter. 7
- a) Define the term LSI and MSI. Design 3:8 decoder with its logic circuit 7

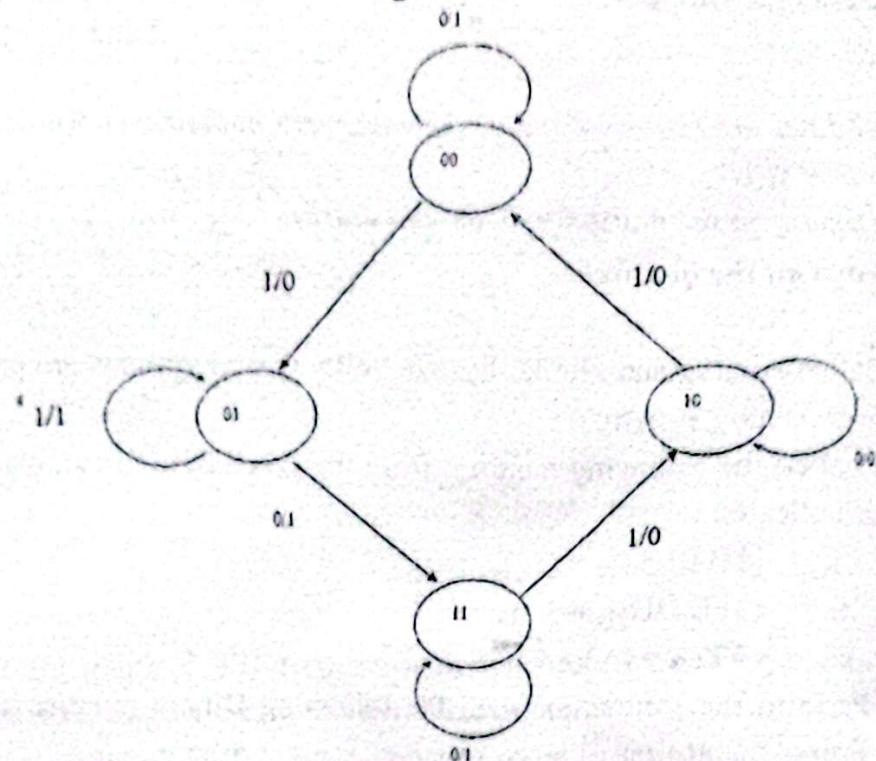
and block diagram.

- b) Implement the following :

i. $F(A,B,C) = \sum(1,3,5,6)$ (using MUX)

ii. $F1 = \sum(0,2,5)$ $F2 = \sum(3,4,7)$ $F3 = \sum(6,7)$ (using ROM)

5. a) Realize the following state diagram into a circuit using S-R flip-flop



a)

b)

c)

a)

b)

- b) Explain operation of J-K Flip-flop with its logic diagram and truth table.
6. a) Design Arithmetic Logic Unit (ALU) that performs 8 Arithmetic operation and 4 different logical operations.
b) Design a MOD 11 asynchronous counter using J k flip flop and showing with its working, counting sequence and timing diagram.

OR

What is shift register? Explain the SISO shift register with circuit diagram.

a)

7. Write short notes on: (Any two)

- a) Parity method for error detection
b) SOP and POS
c) PLA
d) Nibble Adder

POKHARA UNIVERSITY

Level: Bachelor
Programme: BE
Course: Logic Circuits

Semester: Fall

Year : 2017
Full Marks: 100
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Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

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Attempt all the questions.

- a) 'Gray code is also known as reflected code'. Justify your answer with appropriate illustration. 5
- b) Determine the value of base x if $(211)_x = (152)_8$. 5
- c) Realize all the basic gates using NAND gate only. 5
- a) Use K-map to simplify the given Boolean function in SOP form and implement the simplified function using NAND gate only. 7
- $F(A, B, C, D) = \sum(5, 7, 9, 12, 13, 14, 15,)$ and don't care, $d(A, B, C, D) = \sum(3, 6, 8)$
- b) Design a circuit of a 3-bit parity generator and the circuit of a 4-bit parity checker for odd parity. 4+4

OR

Design a combinational circuit that has four inputs and two outputs one of the outputs is high when majority of inputs are high. The second output is high only when all inputs are of same type. 8

- a) With the help of an example, show how you can construct a higher order MUX using two or more number of lower order MUXs. 8
- b) Implement a full adder circuit with the help of two half adder circuit along with the truth table. 7
- a) Explain the operation of clocked R-S flip-flop with the help of its logic diagram, characteristic table and characteristic equation. Differentiate RS and JK flip flop. 8
- b) Design a synchronous 4 bit binary up counter using T flip flop which counts all possible odd numbers. 7

OR

What is a modulo-7 counter? Design such a counter using JK flip-flop. 2+5

5. a) What do you mean by ALU? Design an arithmetic circuit to implement the following function table. A and B are 4 bit binary numbers.

S1	S0	Cin	F
0	0	0	A
0	0	1	A+1
0	1	0	A+B
0	1	1	A+B+1
1	0	0	A+B'
1	0	1	A-B
1	1	0	A-1
1	1	1	A

- b) What is a shift register? Draw the block diagram for shifting the content of register A to register B. Describe the operation.
6. Compare and contrast *any three* of the following:
- Synchronous and asynchronous logic.
 - Decoder and encoder
 - XOR and XNOR gates
 - Analog versus Digital System
7. Write short notes on: (Any two)
- Accumulator
 - Don't care conditions
 - Parity method for error detection

4.

5.

POKHARA UNIVERSITY

Level: Bachelor
Programme: BE
Course: Logic Circuits

Semester: Spring

Year : 2017
Full Marks: 100
Pass Marks: 45
Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

- . a) Explain the digital Number system. Differentiate between analog and digital system. 5
- . b) Perform the following subtraction using 2"s Compliment method 5
 - i. $(1000100)_2 - (1010100)$
 - ii. $(11010)_2 - (10000)_2$
- . c) What are the different types of Binary Codes? Explain each in brief. 5
- . a) How can you find the r's complement using (r-1)'s complement? 3
Explain with example.
- . b) "Excess 3 code is self complementary code" verify the statements 4
- . c) What are the universal gates? Why they are called so? Construct 3+5
NAND gate using NOR gate and NOR gate using NAND gate.
- . a) Use K-map to simplify the given Boolean function and once by 8
considering the don't care condition and once by ignoring the don't
care condition and realize it using the basic gates
 $F(A,B,C,D) = \sum(1,4,8,12,13,15)$ and don't care, $d(A,B,C,D) =$
 $\sum(3,14)$.
- . b) Design a combinational circuit that has four inputs and two outputs 7
one of the outputs is high when majority of inputs are high. The
second output is high only when all inputs are of same type.
- . a) Design a combinational circuit using PLD device as PLA($4*8*4$) 7
which is used to implement the full adder functions in which sum
represented as Si and carry represented as Ci+1.
- . b) How the drawback of RS flip-flop is overcome in J-K flip-flop? 8
Explain the J-K flip-flop in detail.
- . a) Define counter. Design a BCD counter that counts the binary 7

- sequence from 0000 to 1001 and returns to 0000 to repeat the sequence using T-flip-flops.
- b) Explain the operation of RS flip-flop with the help of characteristics table. How it can be converted into T-flip-flop?
6. a) Design a synchronous binary 3-bit up counter using R-S flip-flop.
b) Draw arithmetic circuit logic diagram. Design arithmetic circuit with function table that perform eight major functions.
7. Write short notes on: (Any two)
a) Venn diagram
b) Master Slave Flip Flop
c) Edge Triggered flip-flop



POKHARA UNIVERSITY

Level: Bachelor

Semester: Fall

Year : 2018

Programme: BE

Full Marks: 100

Course: Logic Circuits

Pass Marks: 45

Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

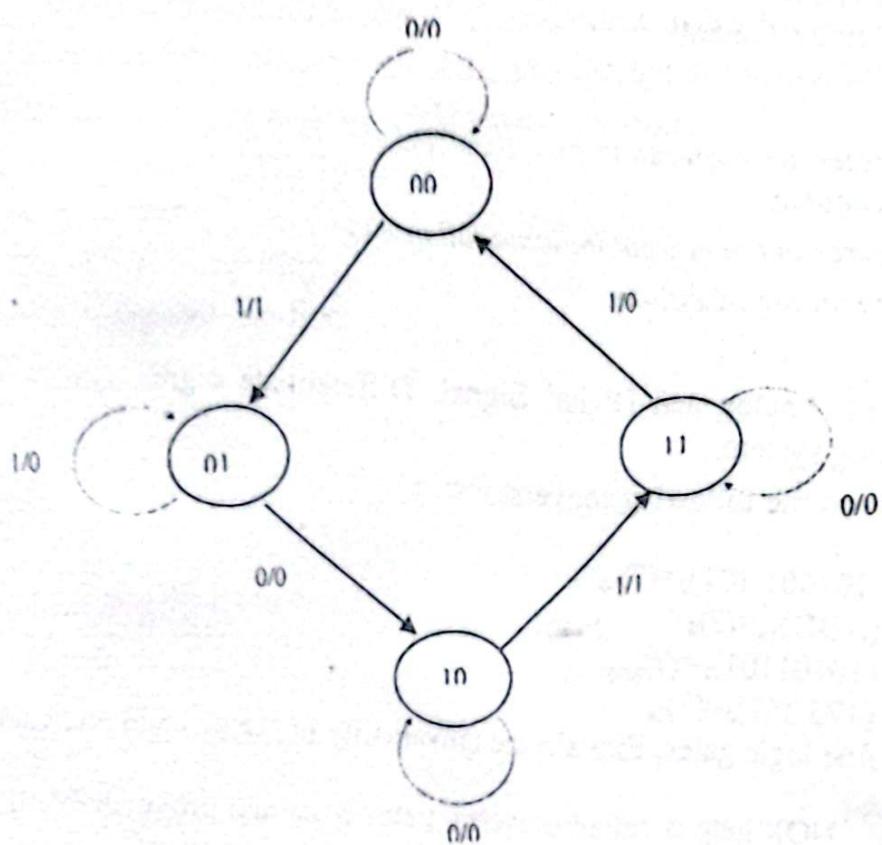
-) Define Analog and Digital Signal. Differentiate digital system and Analog system. 4
-) Convert the following conversions: 8
 - i. $(101001.101)_2 = (?)_{10}$
 - ii. $(ABD)_{16} = (?)_8$
 - iii. $(10101101)_2 = (?)_{\text{gray}}$
 - iv. $(175.351)_8 = (?)_{16}$
-) Define logic gates. Explain the universality of NAND and NOR gates. 3
- i) Why NOR gate is called universal gate? State and prove De-Morgan's theorem. 8
- ii) Use K-map to simply the given Boolean function with don't care condition and realize it using basic gates only: $F = \sum(1, 4, 8, 12, 13, 15)$ and $d = \sum(3, 7, 11, 14)$. 7
- a) Design a combinational logic circuit that has four input and two outputs. One of the outputs is high when majority of inputs are high. The second output is high only when all inputs are of same type. 8
- b) Design a circuit for 3-bit parity generation and 4-bit parity checker using odd parity. 7
- a) A combinational circuit is defined by the function, 8

$$F_1(A, B, C) = \sum(3, 5, 6, 7)$$

$$F_2(A, B, C) = \sum(0, 2, 4, 7), \text{ implement by using PLA.}$$
- b) What is magnitude comparator? Design a two bit magnitude 7
 - 1

comparator whose outputs are $A > B$, $A < B$ and $A = B$.

5. a) Design a sequential circuit corresponding to the given state diagram using S-R FlipFlop for the following state diagram.



- b) With necessary logic diagram, truth table, excitation table, explain the operation of J-K flip flop.

6. a) What is shift register? Explain serial in parallel out and parallel in parallel out shift registers.

- b) Design a 4-bit arithmetic circuits which performs eight different arithmetic operations.

7. Write short notes on: (Any two)

a) Counters

b) Master -slave Flip Flop

c) Nibble Adder

POKHARA UNIVERSITY

Level: Bachelor

Semester: Spring

Year : 2018

Programme: BE

Full Marks: 100

Course: Logic Circuit

Pass Marks: 45

Time : 3 hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

How does the logic system express data during computation? 5
Differentiate between Digital and Analog system.

Perform the conversion as indicated (any two). 5

i. $(235)_6 = (\quad)_{base-10}$

ii. $(369)_{10} = (\quad)_{oct}$

iii. $(BCA)_8 = (\quad)_2$

Use 2's complement to subtract the following: 5

i. $(1010)_2 - (10100)_2$

ii. $(957)_{10} - (376)_{10}$

iii. $(378)_{oct} - (256)_{oct}$

Why NAND and NOR are called Universal Gates? Construct $F = AB + CD$ using universal gates. 7

Define K-Map. Simplify the expression mentioned below using K-Map. 8

$$F(A, B, C, D) = \sum(1, 3, 7, 10, 13, 15)$$

$$d(A, B, C, D) = \sum(0, 2, 8)$$

Where d denotes don't care. Also implement the simplified function using NOR gates only.

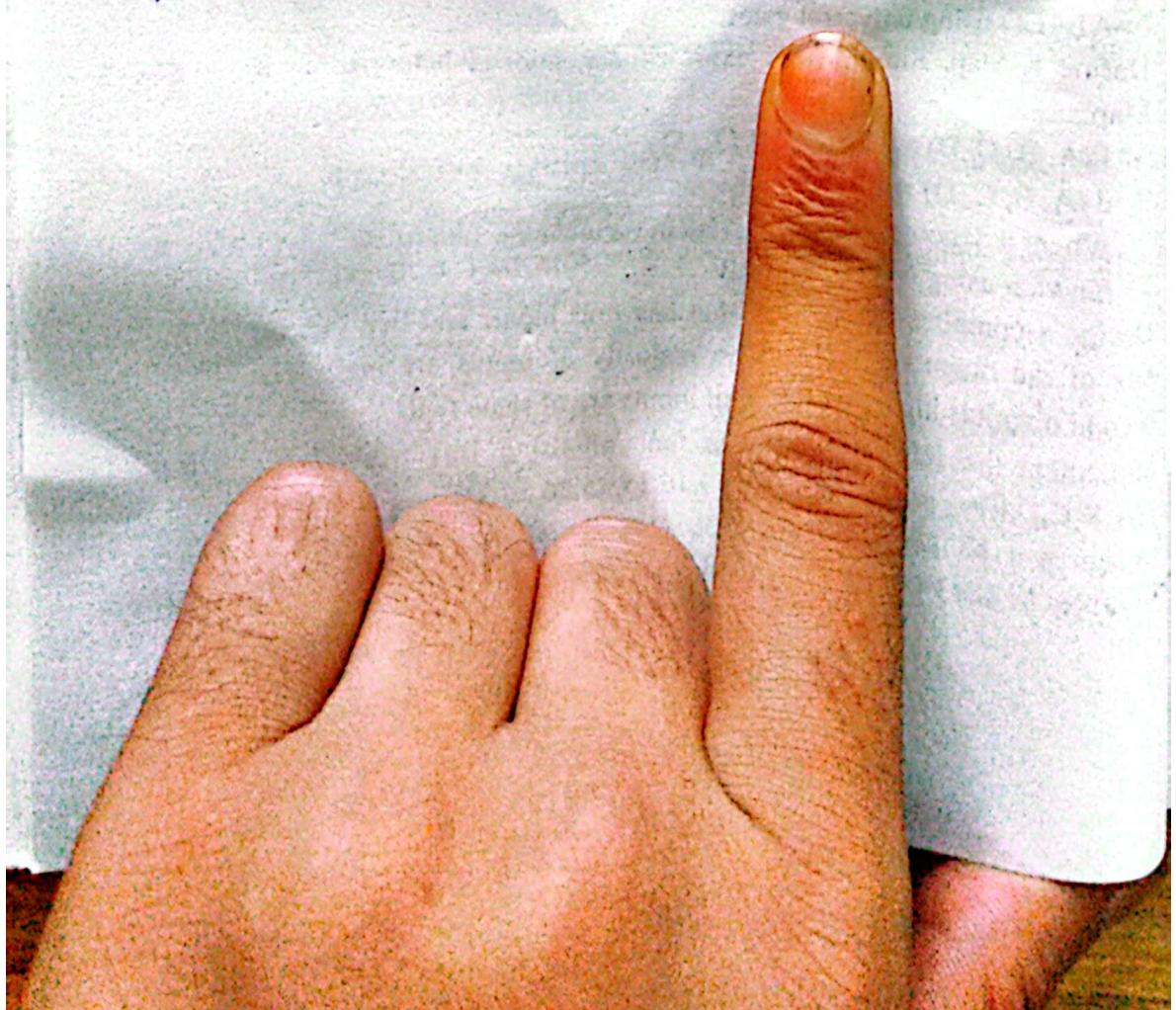
Design a combinational circuit that has four inputs and two outputs one of the outputs is high when majority of inputs are high .The second output is high only when all inputs are of same type. 7

Implement the following Boolean function using 16:1 Multiplexer 8

$$F(A, B, C, D, E) = \sum m(2, 4, 5, 7, 10, 14, 15, 16, 17, 25, 26, 30, 31)$$

Design a 4 bit parallel adder subtractor circuit with one selection variables M and two inputs A and B. For M = 0, the circuit required to

- perform addition i.e. $(A+B)$ and for $M = 1$, the circuit must perform subtraction $(A - B)$ by taking 2'S complement of B.
- b) Explain negative edge triggered S-R flip-flop with necessary logic diagram, characteristic table, characteristic equation and waveform.
5. a) Design a synchronous Mod-6 counter using clocked D Flip Flop
b) Define shift register. Draw diagram for parallel in serial out shift register and discuss its operation with necessary explanation.
6. a) Explain the process how does binary value of 4 flags in status register change with necessary diagram.
b) Design a 3-bit Synchronous DOWN Counter using T flip-flop.
7. Write short notes on: (Any two)
a) State Reduction and State Assignment
b) Random Access Memory
c) Self-complementing code



POKHARA UNIVERSITY

Level: Bachelor
Programme: BE
Course: Logic Circuit

Semester: Fall

Year : 2019
Full Marks: 100
Pass Marks: 45
Time : 3 hrs.

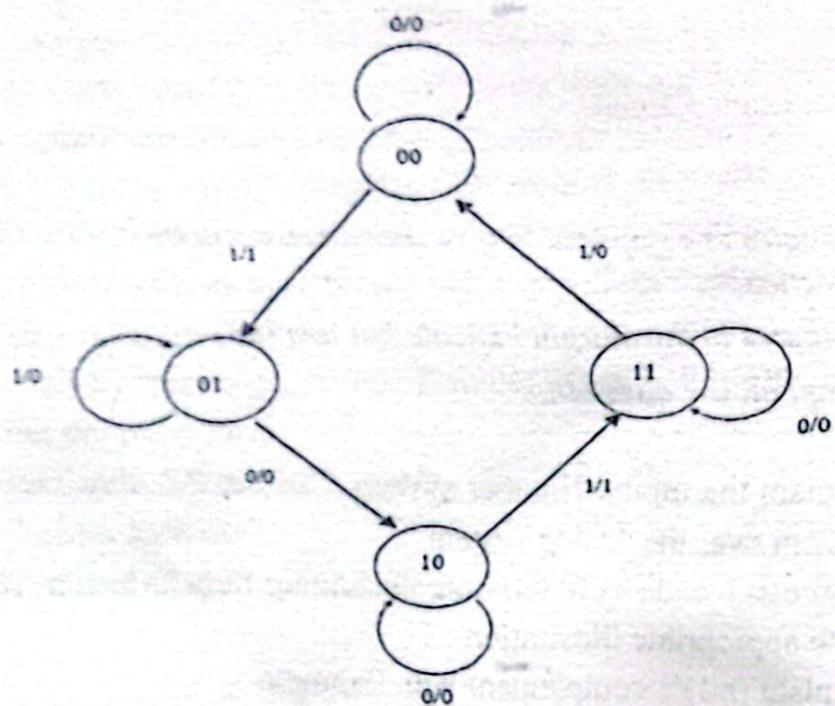
Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

- a) Explain the digital Number system. List out the advantages of digital system over the analog system. 6
- b) "Excess-3 code is a self-complementing code". Justify your answer with appropriate illustration. 5
- c) Explain $(r-1)$'s complement with Example 4
- a) Perform the conversion as indicated 8
 - i. $(123)_4 = ()_{BCD}$
 - ii. $(4FC)_{16} = ()_8$
 - iii. $(1011011)_{gray} = ()_2$
 - iv. $(45)_{10} - (99)_{10}$, using r's complement.
- b) State and Prove De-Morgan's Theorem. Explain the universal property of the NOR gate. 7
- a) Simplify the following Boolean expression using K- map and implement using NGR gates only. 7
$$F(A,B,C,D) = \sum(0,2,4,6,12,15)$$
$$D(A,B,C,D) = \sum(8,10,14)$$
- b) Design a code conversion circuit to convert Binary Code into Gray Code. 8
- a) Define Multiplexer and De-Multiplexer. Construct 8×1 MUX using 4×1 MUX and explain with the truth table. 8
- b) Design a combinational circuit using PLD device as PLA ($4 \times 8 \times 4$) that is used to implement full adder function in which sum is represented as S_i and carry as C_i . 7
- a) Differentiate between Latches and Flip-flop. Draw JK flip-flop circuit to further convert it into T flip-flop with state table and state equation. 8

- b) Design a sequential circuit using JK Flip Flop for the following state diagram.



6. a) Design MOD-10 counter using T flipflop.
b) Design a 4-bit Arithmetic unit that performs Addition when mode control bit is 0 and Subtraction when mode control bit is 1.
7. Write short notes on: (Any two)
a) Master Slave Flip flop
b) Johnson Counter
c) Status Register

POKHARA UNIVERSITY

Level: Bachelor

Semester: Spring

Year : 2019

Programme: BE

Full Marks: 100

Course: Logic Circuits

Pass Marks: 45

Time : 3 hrs.

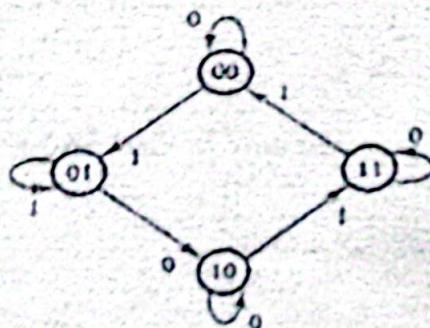
Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

- a) With characters differentiate between Digital and Analog system. 5
- b) Perform the conversion as indicated (any two). 5
 - i. $(543)_6 = (\)_{\text{Excess-3}}$
 - ii. $(708)_{10} = (\)_{2421}$
 - iii. $(BBA)_{16} = (\)_2$
- c) Use 2's complement to subtract the following: 5
 - i. $(1011)_2 - (10100)_2$
 - ii. $(952)_{10} - (873)_{10}$
 - iii. $(368)_{\text{BCD}} - (256)_{\text{BCD}}$
- a) Prove the following Boolean expression 5
 - i. $\overline{A}\overline{B} + BC + \overline{A}\overline{B}\overline{C} = \overline{A} + BC$
 - ii. $X\overline{Y} + Y\overline{Z} + Z\overline{X} = \overline{X}Y + \overline{Y}Z + \overline{Z}X$
- b) Simplify the Boolean function F and don't care conditions d in (1) SOP (2) POS and (3) draw NAND-NAND equivalent logic. Given:
 $F = B'CD' + A'CD + A'BC + A'B'C'D'$
 $d = A'BC'D + ACD + AB'D'$ 5
- c) A Boolean function is given by $F(A,B,C,D) = \sum(0,1,2,3,10,13,14)$ and don't care condition $d(A,B,C,D) = \sum(4,7,12)$. Simplify it using K-Map and implement using NAND gate only. 5
- a) Design a combinational circuit that converts decimal digits from 8-4-2-1 to Excess 3 8
- b) Design a combinational circuit using PLD device as PLA (4X8X4) that is used to implement full Subtract or function in which difference is represented as Di and borrow as Br. 7
- a) Illustrate the process how does binary value of 4 flags in status registers change with necessary diagram. 8
- b) Implement the following with appropriate MUX: 7

- i. $F(A,B,C) = \sum (1,4,5,6)$
ii. $F(A,B,C,D) = \sum (0,1,3,8,9,15)$
5. a) Realize the following state diagram into a circuit using SR flip-flop.



- Describe with diagram the working and characteristics of JK flipflop.
b) Explain operation of J-K Flip-flop with its logic diagram, truth table, excitation table
6. a) What are shift registers? Explain Parallel in serial out and Serial in Parallel out shift register with diagrams.
b) Design 3 bit up counter using T flip-flop
7. Write short notes on: (Any two)
a) Computational Logic Design Procedure
b) Johnson Counter
c) Self-complementing code

Level: Bachelor
 Programme: B E
 Course: Logic Circuits

Semester: Fall

Year : 2020
 Full Marks: 100
 Pass Marks: 45
 Time : 3 hrs.

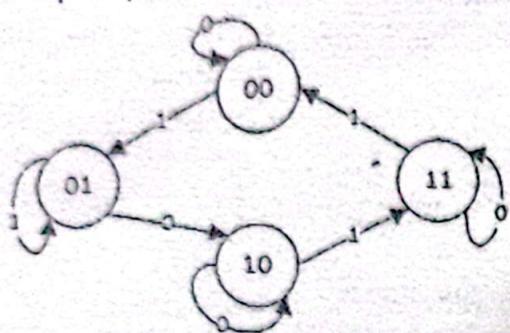
Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

- a) Define digital system. Why do you prefer Digital systems against its analog counterpart? Explain. 5
- b) Perform the following subtraction using $(r-1)$'s complement:
 - i. $(111001)_2 - (11011)_2$
 - ii. $(2321)_{10} - (8301)_{10}$
- c) What is weighted and non-weighted code? Why Gray code is called reflected code? 5
- a) Discuss the significance of NAND & NOR gate in Logic circuit. Prove that NAND and NOR gates are the Universal gate. 7
- b) For the given logic expression:
 $F(A,B,C,D) = A'B + BD + A'D' + B'D'$
 - i) Make a truthtable
 - ii) Simplify it using K map
 - iii) Realize the simplified expression using NOR gate (2 inputs) only.
- a) Use K-map scheme to obtain the minimized SOP expression for the given function $f(A, B, C, D) = \sum m(1, 5, 8, 12) + d(3, 7, 10, 11, 14, 15)$ and implement the result using NOR gates only. 8
- b) What are parity bits? Design 3-bit parity generator and 4-bit parity checker circuit for even parity. 7
- a) Design a combinational circuit using PLD device as ROM which is used to find square of 3 bit numbers. 8
- b) Design and implement full adder circuit using decoder. 7
- a) What are the significance of a flip-flop? Explain J-K flip-flop along with its logic diagram, truth table and excitation table. 7

- b) Design synchronous sequential circuit for the given state diagram using T flip-flop.



5. a) Design and implement Mod-5 counter using JK flip flop.
b) Design an arithmetic circuit implementing given functions. Where A and B are 4-bit binary input lines.

S ₁	S ₀	C _{in}	Output (F)
0	0	0	A
0	0	1	A+1
0	1	0	A+B
0	1	1	A+B+1
1	0	0	A+B̄
1	0	1	A-B
1	1	0	A-I
1	1	1	Ā

7. Write short notes on: (Any two)

- a) Johnson Counter
b) Tristate Logic
c) 4-Bit Nibble Adder