

# Icepi Zero Testing Guide

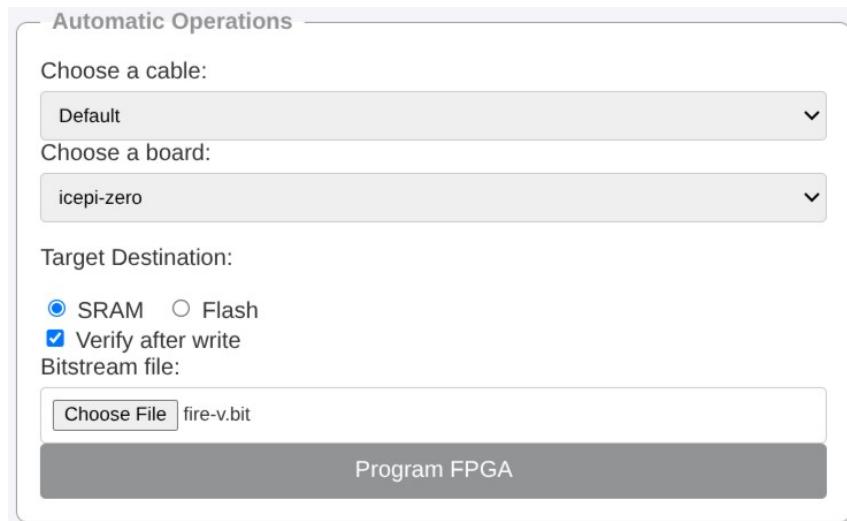
## Setup

Download the following bitstream file:

<https://github.com/cheyao/icepi-zero/raw/refs/main/documentation/fire-v.bit>

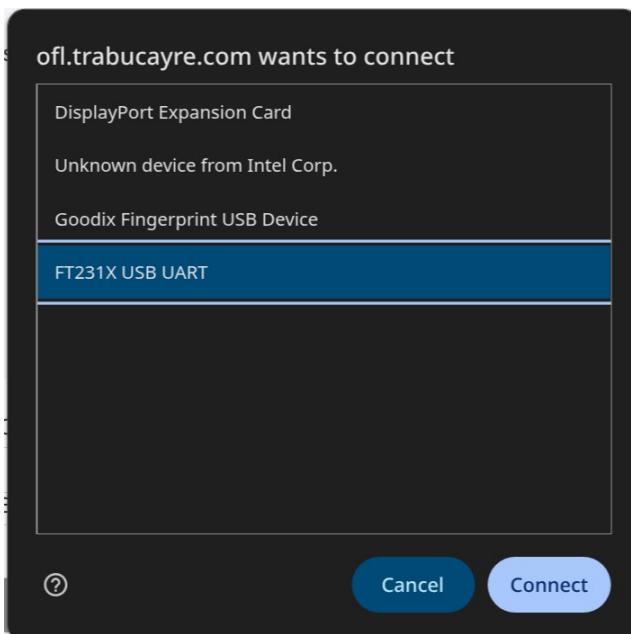
## Testing

1. Plug in a USB-C data cable to the left-most USB port on the PCB. (One next to the HDMI port, labeled Flash). Connect the other end to a PC/laptop. Also use a micro-HDMI to HDMI cable to connect the HDMI port to a monitor.
2. Open <https://ofl.trabucayre.com/> in Google Chrome (Firefox does **NOT** work)
3. On the bottom left, in the “Automatic Operations” section, select the following options:



(Click “Choose File” and select the fire-v.bit file downloaded during setup)

4. Click on “Program FPGA” and select “FT231X USB UART” in the popup menu and click connect:



6. Wait for a few seconds, “Done” should be written in “openFPGALoader Logs”:

**openFPGALoader WEB interface**

**Important Notes:**

- For Linux users, the ‘ftdi\_sio’ driver must be unloaded: ‘sudo modprobe -r ftdi\_sio’
- Google Chrome must be used, as USB access is not supported by Firefox.

This page offers two ways to program an FPGA directly from a web browser:

- \*\*Manual Mode\*\*: Requires openFPGALoader’s arguments entered exactly as you would on a terminal.
- \*\*Automatic Mode\*\*: A guided process where you can select:
  - The target board and/or cable from a list.
  - The bitstream destination (SRAM or Flash). A verification step can be optionally performed after writing to Flash.
  - The bitstream file to be programmed.

[openFPGALoader repository](#)  
[openFPGALoader documentation](#)  
[openFPGALoader\\_webUSB Repository sources](#)

**Manual Operations**

Command line args:  
e.g., -c f22232 -b ulks3

Bitstream file:  
Choose File No file chosen

Program FPGA

**openFPGALoader Command Line: openFPGALoader -b icepi-zero fire-v.bit**

Operation Status

```
SpiOverJtag Bridge: Not required.
Fetch SpiOverJtag Bridge: Not required
Fetch fire-v.bit Bitstream: Done
Execute openFPGALoader: Done
```

**Automatic Operations**

Choose a cable:  
Default

Choose a board:  
icepi-zero

Target Destination:  
 SRAM  Flash  
 Verify after write

Bitstream file:  
Choose File fire-v.bit

Program FPGA

**openFPGALoader Logs**

```
Jtag frequency : requested 6000000Hz -> real 3000000Hz
ret 0
Open file: DONE
b2b0ffff
Parse file: DONE
Enable configuration: DONE
SRAM erase: DONE
Loading: [=====] 22.64%
Loading: [=====] 44.51%
Loading: [=====] 65.23%
Loading: [=====] 86.34%
Loading: [=====] 100.00%
Done
Disable configuration: DONE
Execution completed in 4925ms
```

USB Status: Connected

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7. If the PCB works, you should see LEDs blinking and the following HDMI output on the monitor:

