**Q1 – II.A (True/False)** The execution phase comes after the decode phase.

**Q2 – II.A (Fill-in-the-Blank)** The instruction execution cycle usually has **three** main stages: Fetch, \_\_\_\_\_\_\_\_, and Execute.

**Q3 – II.B (MCQ)** Which mode offers full access to memory and hardware?  
 A. User Mode  
 B. Supervisor Mode   
 C. Real Mode  
 D. Safe Mode

**Q4 – II.B (Fill-in-the-Blank)** Protected mode supports multitasking and \_\_\_\_\_\_\_\_ protection.

**Q5 – II.C (True/False)** Registers are slower than main memory.

**Q6 – II.C (MCQ)** Which register is used to store function return addresses?  
 A. EAX  
 B. ESP  
 C. EBP  
 D. EIP

**Q7 – II.D (True/False)** The FPU can only add and subtract.

**Q8 – II.D (Fill-in-the-Blank)** The FPU follows the IEEE \_\_\_\_\_\_\_\_ standard for floating point.

**Q9 – II.A (MCQ)** What happens during the "Decode" step?  
 A. Result is stored  
 B. Instruction is run  
 C. Instruction is interpreted   
 D. Data is fetched

**Q10 – II.B (True/False)** Real mode has no memory protection.

**Q11 – General Topic II (Fill-in-the-Blank)** Registers like **EAX** are part of the \_\_\_\_\_\_\_\_ architecture.

**Q12 – General Topic II (MCQ)** Which flag indicates a negative result?  
 A. CF  
 B. ZF  
 C. SF   
 D. OF

**Q13 – II.D (MCQ)** Which operation is **not** typically handled by the FPU?  
 A. Square root  
 B. Multiplication  
 C. Bit shifting   
 D. Division

**Q14 – II.C (True/False)** The Carry Flag (CF) is used when addition exceeds register capacity.