reg\_rt\_src

Inst[3:0]

Inst[11:8]

reg\_rt

StackReg

DataReg

Inst[7:4] – reg\_rs

sign\_ext\_sel

reg\_rd\_wb

reg\_rd\_data

Inst[15:12] – cntrl opcode

sign\_ext

Reg\_16bit\_file

CONTROL

Control Outputs

Other 3 Pipe to Pipe

update\_rdy

RegWrite

arith\_imm\_out

sign\_ext\_out

load\_save\_imm\_out

Read\_Bus\_2

Write\_Bus

Write\_Reg

Read\_Bus\_1

Read\_Reg\_2

Read\_Reg\_1

Inst[11:8] – branch cond

read\_data\_2

read\_data\_1