**Project Report**

**WISC-S15**

PHASE 1

ECE/CS 552

April 9, 2015

Submitted to: Parmesh Ramanathan

Graham Nygard

Robert Wagner

*INTRODUCTION*

Intro

**Special Features**

Spec feats

**Optimizations**

Optimizations

**Challenges**

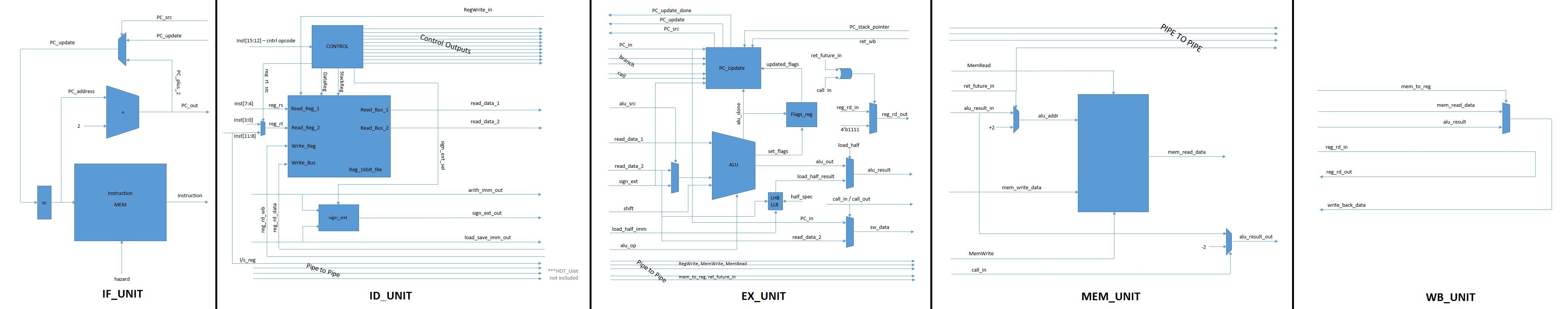
Challenges

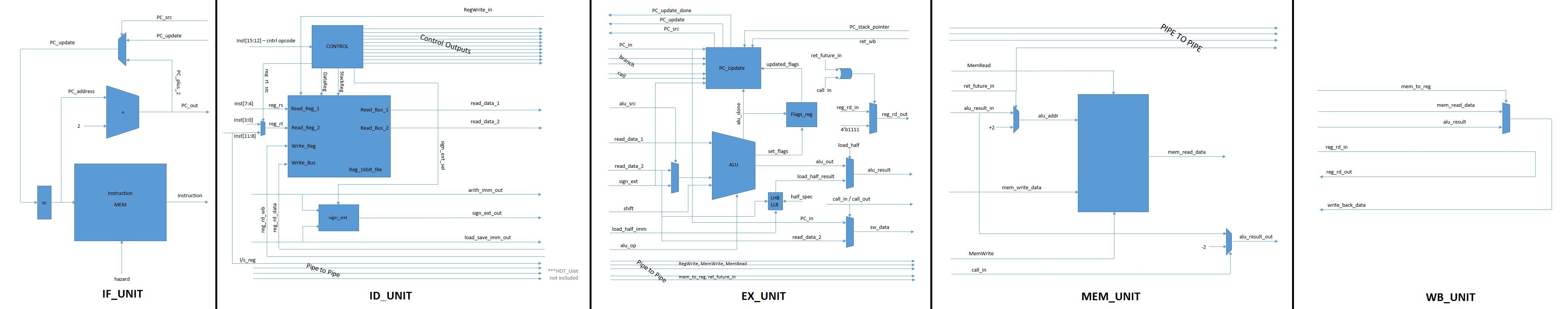
**Requirement Satisfaction**

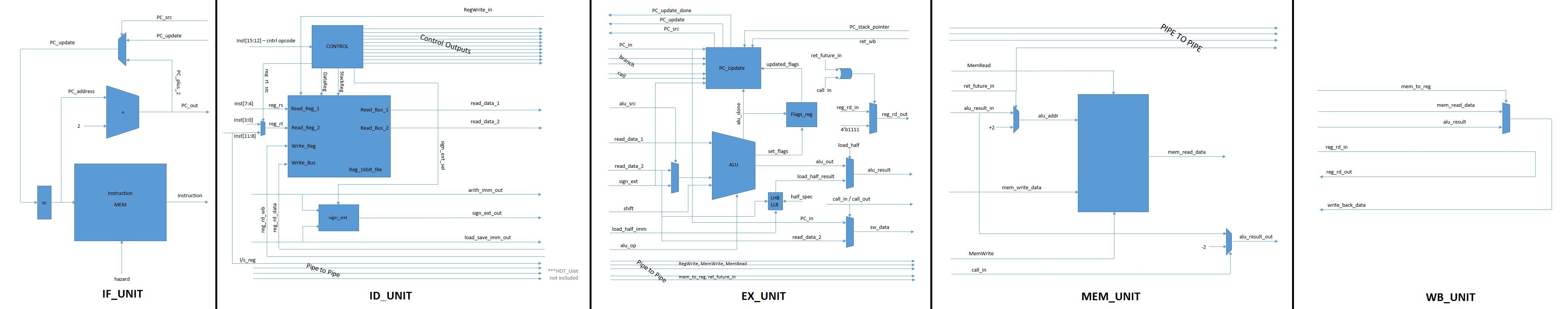
To our knowledge, *all*

*VERILOG CODE*

*ARCHITECTURE DIAGRAM*

For your convenience, we have included a five-stage diagram illustrating the five pipelined sections of our architecture. The pipeline registers and Hazard Detection Unit have been omitted due to spatial constraints and increased readability:





*AREA REPORT*

The Verilog code in the previous section was synthesized using the script provided; the following Area Report was generated:

*SIMULATION RESULTS*

The Verilog code in the previous section was synthesized using the script provided; the following Area Report was generated:

*SUMMARY*

Student Names: Graham Nygard, Robert (Bob) Wagner

Area of Design (except memory, cache):

|  |  |  |
| --- | --- | --- |
| Name of Module | Execution Time (pre-synthesis) | Execution Time (post-synthesis) |
|  |  |  |
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