**Project Report**

**WISC-S15**

PHASE 1

ECE/CS 552

April 9, 2015

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*INTRODUCTION*

WISC-S15 is a 16-bit computer with a load/store architecture, register file, three-bit FLAG register, and fourteen arithmetic, load/store, and control instructions. For this intermediate project milestone, our team focused on achieving support for all instructions specified by the given ISA specification. We prioritized the development of critical test benches (such as the ALU, control logic, top level, etc.) such that we could guarantee a functionally correct architecture. Our team plans to expand our test bench support framework over the remainder of the semester to increase depth and breadth coverage of our modules.

For this intermediate milestone in the completion of this project, we are assuming that the instruction cache is a large as the main memory with one clock cycle access delay. Furthermore, we also assume that all accesses to the instruction cache will result in hits. The second and final phase of this project will modify these memory architectures to a direct-mapped instruction cache.

**Special Features**

Spec feats

**Optimizations**

Optimizations

**Challenges**

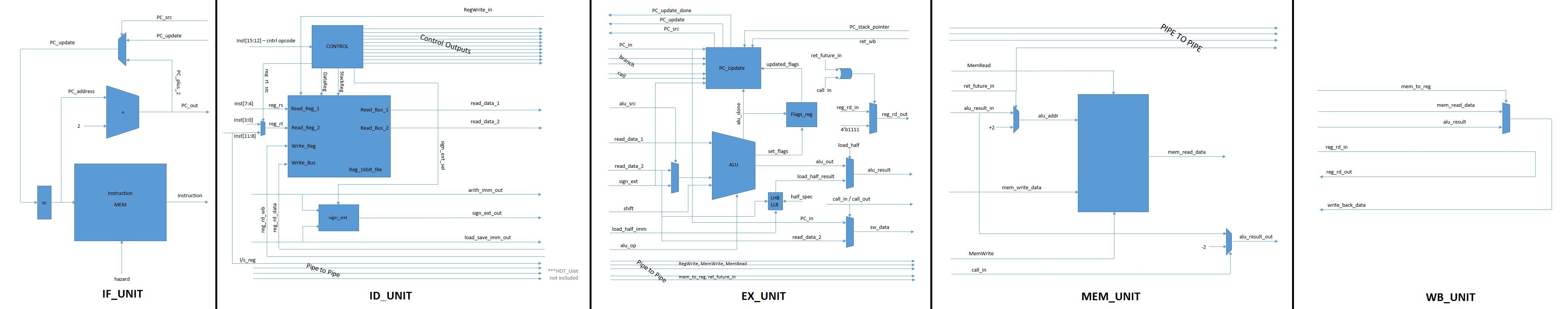
Challenges

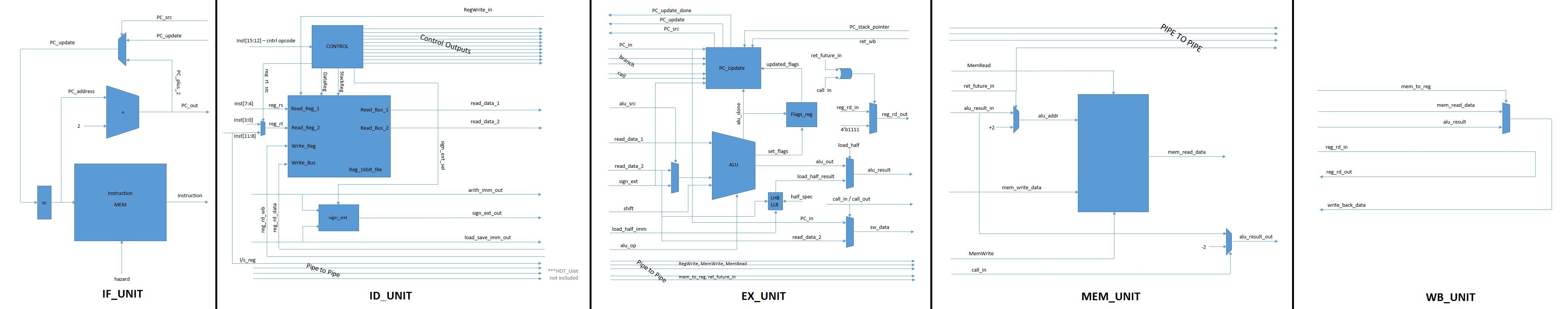
**Requirement Satisfaction**

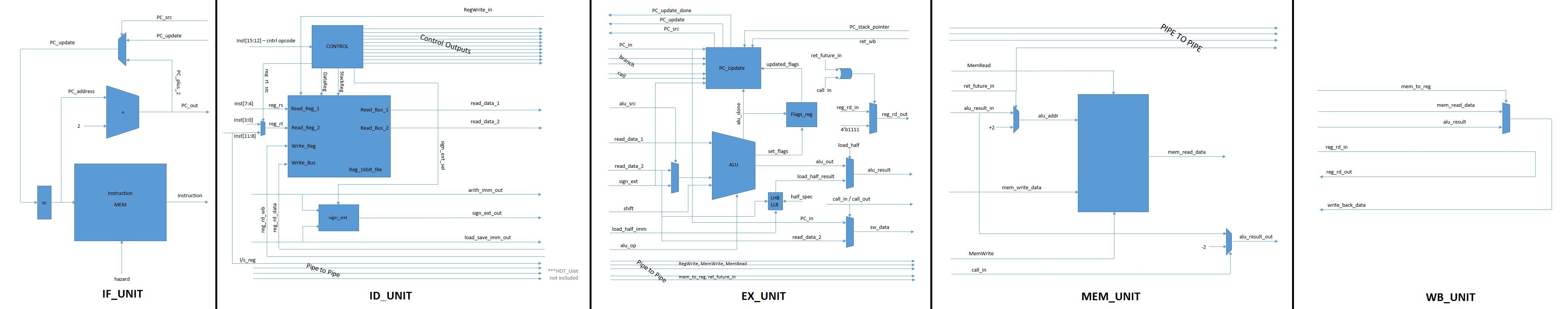
To our knowledge, *all*

*VERILOG CODE*

*ARCHITECTURE DIAGRAM*

For your convenience, we have included a five-stage diagram illustrating the five pipelined sections of our architecture. The pipeline registers and Hazard Detection Unit have been omitted due to spatial constraints and increased readability:





*AREA REPORT*

The Verilog code in the previous section was synthesized using the script provided; the following Area Report was generated:

*SIMULATION RESULTS*

The Verilog code in the previous section was synthesized using the script provided; the following Area Report was generated:

*SUMMARY*

Student Names: Graham Nygard, Robert (Bob) Wagner

Area of Design (except memory, cache):

|  |  |  |
| --- | --- | --- |
| Name of Module | Execution Time (pre-synthesis) | Execution Time (post-synthesis) |
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